Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Rev 0; 1/09

MAXIM

Low-Power, Dual-Core Microcontroller

General Description

The MAXQ3108 is a low-power microcontroller that features two high-performance MAXQ20 cores: a dedicated core (DSPCore) for intensive data processing and a user core (UserCore) for supervisory functions. The two cores can operate at different clock speeds, allowing lower system power consumption for even processing intensive applications. The UserCore can be configured to run at the lowest clock rate possible for monitoring the peripherals for communication activities, while the DSPCore runs at the highest speed. Each core has access to an independent math accelerator (a multiply/accumulate unit). The UserCore supports SPI™, I^2C, two UART channels with one channel supporting IR carrier modulation, a trimmable real-time clock (RTC), battery-backed RTC registers, and data memory. The DSPCore is fully user programmable and configurable. With the standard 32,768Hz crystal, the DSPCore operates at 10.027MHz, while the UserCore runs at 5.014MHz.

Applications

Electricity Meters

Industrial Control

Battery-Powered and Portable Devices

Smart Transmitters

Medical Instrumentation

Features

- **High-Performance, Low-Power, Dual 16-Bit RISC Cores**
- **Approaches 1MIPS per MHz**
- **System Clock**
  - 10.027MHz (DSPCore)
  - 5.014MHz (UserCore)
- **33 Instructions**
- **Approximately 100ns Execution Time at 10.027MHz**
- **Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement**
- **16-Bit Instruction Word, 16-Bit Data Bus**
- **16 x 16-Bit General-Purpose Working Registers for Each Core**
- **16-Level Hardware Stack for Each Core**
- **Hardware Support for Software Stack**
- **Memory Features**
  - UserCore
    - 64KB Flash Program Memory
    - 16B Battery-Backed (V_{BAT}) Data SRAM
    - 4KB Utility ROM
    - 2KB Data SRAM; 10KB Total Data SRAM (If DSPCore Inactive)
  - DSPCore
    - 8KB User-Loadable SRAM Code Memory
    - 1KB Data SRAM
- **Peripherals**
  - FLL (10MHz Output with 32kHz Input)
  - SPI Master, I^2C Master
  - Two UART Channels (One Supports IR Carrier Modulation)
  - Math Accelerator for Each Core
  - Three Manchester Decoder and Cubic Sinc Filter Channels for Interfacing to DS8102 Delta-Sigma Modulators
  - Two 16-Bit Programmable Timer/Counters
  - RTC with Alarms and Digital Trim, Dedicated Battery-Backup Pin (V_{BAT})
  - Two Programmable Pulse Generators
  - Independent Watchdog Timer for Each Core
  - External Interrupts
  - JTAG Interface
- **Operating Modes**
  - Stop Mode: 0.1µA typ
  - Active Current at 10MHz and V_{DD} = 2.0V: 1.0mA typ

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXQ3108-FFN+	-40°C to +85°C	28 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration appears at end of data sheet.

SPI is a trademark of Motorola, Inc.

MAXQ is a registered trademark of Maxim Integrated Products, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

Low-Power, Dual-Core Microcontroller

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF TABLES

Low-Power, Dual-Core Microcontroller

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin except V_{DD} with Respect to V_{SS} .....-0.3V to V_{DD}
Voltage Range on V_{DD} with Respect to V_{SS} .....-0.3V to +3.6V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = V_{RST} to 3.6V, T_A = -40°C to +85°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		V_{RST}		3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD}	1.875		1.975	V
1.8V Internal Regulator	V_{REG18}		1.71	1.8	1.89	V
1.8V Power-Fail Reset Voltage	V_{REGRST}	Monitors REGOUT	1.62		1.71	V
Battery Supply Voltage	V_{BAT}		1.8		3.6	V
Battery Current (Note 3)	I_{BAT1}	V_{DD} = 0, V_{BAT} = 3.6V, 32kHz oscillator and RTC enabled		0.8		µA
		V_{DD} = 0, V_{BAT} = 2V, 32kHz oscillator and RTC enabled		0.6		
Active Current with 32.768kHz Crystal Connected to CX1, CX2; FLL Selected (10MHz Output); ENDSP = 0; All Decimators and Sinc Filters Off (Note 4)	I_{DD_FLL1}	/1 mode, V_{DD} = 2.0V		1.3	2.2	mA
	I_{DD_FLL2}	/1 mode, V_{DD} = 3.6V		1.5	2.5	
	I_{DD_FLL9}	PMM2 (32kHz), V_{DD} = 2.0V		0.5	0.8	
	I_{DD_FLL10}	PMM2 (32kHz), V_{DD} = 3.6V		0.6	1.0	
Active Current with 32.768kHz Crystal Connected to CX1, CX2; FLL Selected (10MHz Output); UserCore = /256 PMM; DSPCore = /1 ; ENDSP = 1; Manchester Decoders On; Decimators On	I_{DD_FLL14}	V_{DD} = 2.0V		1.0	1.7	mA
	I_{DD_FLL15}	V_{DD} = 3.6V		1.8	3.0	
Stop-Mode Current (Note 5)	I_{STOP_1}	BOD = 1, REGEN = 0, SVMSTOP = 0, RTC off (lowest current stop mode)		0.1	2.4	µA
	I_{STOP_2}	BOD = 0, REGEN = 0, SVMSTOP = 0, RTC off (adds brownout-reset detection)		30	125	
Input Low (CX1)	V_{IL1}		V_{SS}		0.20 x V_{DD}	V
Input Low (All Other Pins)	V_{IL2}		V_{SS}		0.30 x V_{DD}	V
Input High (CX1)	V_{IH1}		0.75 x V_{DD}		V_{DD}	V
Input High (All Other Pins)	V_{IH2}		0.70 x V_{DD}		V_{DD}	V
Input Hysteresis (Schmitt)	V_{IHYS}		0.18			V
Output Low (All Port Pins)	V_{OL}	I_{OL} = 4mA (Note 6)	V_{SS}		0.4	V
Output High (All Port Pins)	V_{OH}	I_{OH} = -4mA (Note 6)	V_{DD} - 0.4			V

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = -40°C to +85°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input/Output Pin Capacitance	C_{IO}	Guaranteed by design			15	pF
Input Low Current All Pins	I_{IL}	V_{IN} = 0.4V			-30	µA
Input-Leakage Current	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor (All Inputs)	R_{PU}			60		kΩ
CLOCK SOURCE						
FLL Output Frequency	f_{FLL}	CX1 = 32.768kHz	9.5	10.0	10.5	MHz
FLL Output Accuracy	Δf_{FLL}	CX1 = 32.768kHz		1.5	±5	%
FLASH MEMORY						
System Clock During Flash Programming/Erase			2			MHz
Flash Erase Time		Mass erase	22.8	24	25.2	ms
		Page erase	22.8	24	25.2	
Flash Programming Time Per Word		(Note 7)	59.5		66.5	µs
Write/Erase Cycles				1000		Cycles
Data Retention		T_A = +25°C	100			Years
SUPPLY VOLTAGE MONITOR						
Set Point	SV_{TR}		2.0		3.5	V
Increment Resolution				0.1		V
Default Set Point				2.7		V
Current Consumption	I_{SVM}				10	µA
Start Time	t_{SVMST}				200	µs
Setup Time (Change Set Point)	t_{SVM_SU1}	Changing from one set point to another set point			2	µs
Setup Time (Stop Mode Exit)	t_{SVM_SU2}	Exit from stop mode			8	µs
REAL-TIME CLOCK						
RTC Input Frequency	f_{32KIN}	32kHz watch crystal		32,768		Hz
RTC Operating Current	I_{RTC}	V_{DD} = 2.0V		0.6		µA
		V_{DD} = 3.6V		0.8		

Note 1: Results based on simulation data. Characterization data will be available at a later date. All voltages are referenced to ground. Specifications to T_A = -40°C are guaranteed by design and are not production tested.

Note 2: Typical values are not guaranteed. These values are measured at room temperature, V_{DD} = 3.3V.

Note 3: This current is from V_{BAT} only if (V_{DD} < V_{BAT} and V_{DD} < V_{RST}) or (STOP = 1, REGEN = 0, BOD = 1). Otherwise, this current is from V_{DD}.

Note 4: Measured on the V_{DD} pin and the device not in reset. All inputs are connected to V_{SS} or V_{DD}. Outputs do not source/sink any current. Timer enabled, RTC enabled, part executing JUMP $ from flash.

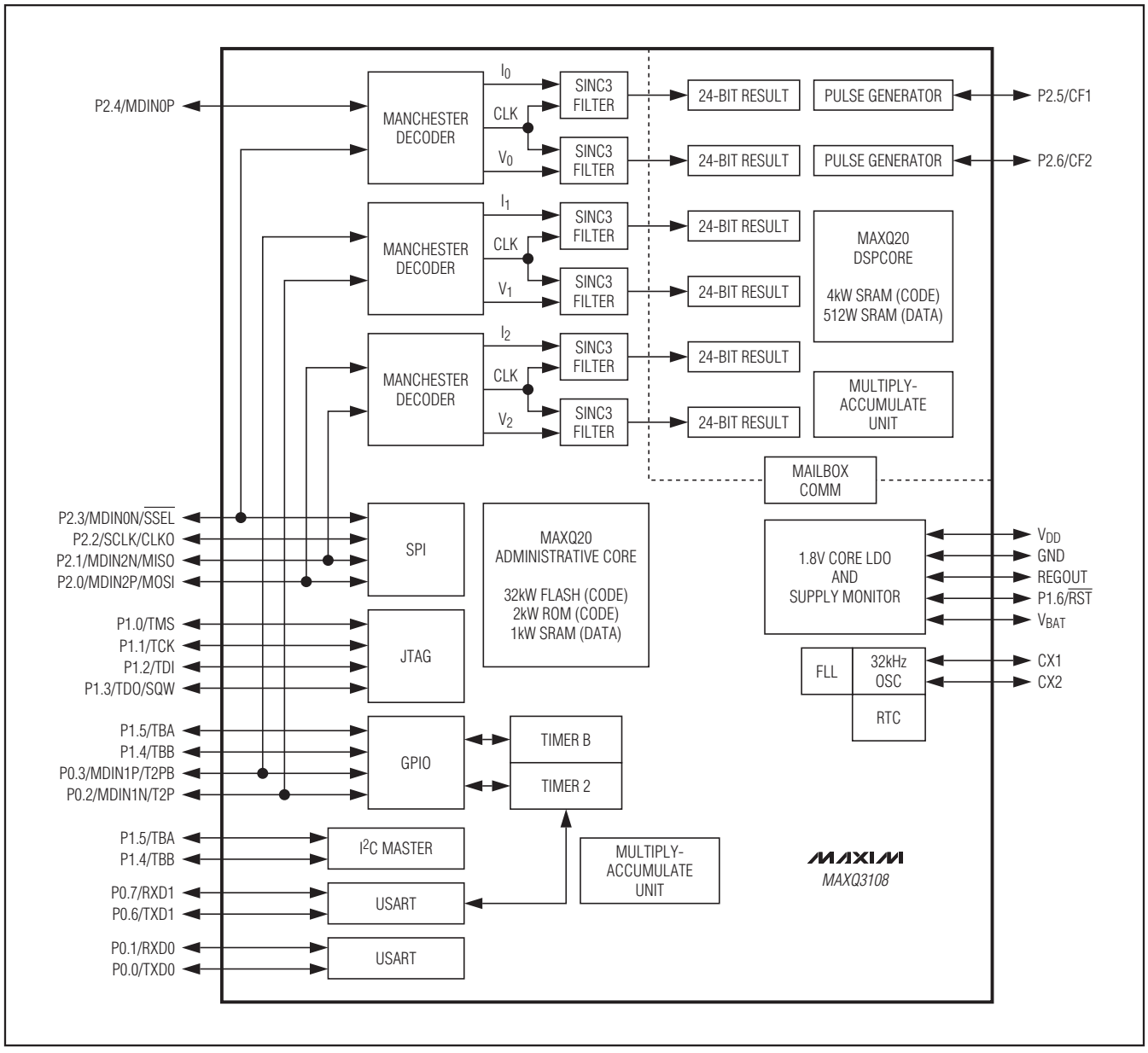
Note 5: If the RTC is on for parameters ISTOP_2, ISTOP_3, and ISTOP_4, a current equal to I_{BAT1} is added to I_{DD}.

Note 6: The maximum total current, $I_{OH(MAX)}$ and $I_{OL(MAX)}$, for all outputs combined should not exceed 35mA to satisfy the maximum specified voltage drop.

Note 7: The timing listed above is clocked by 63 cycles of the internal 1MHz ±5% clock. There will be ROM code overhead, which is a function of system clock. For data sheet purposes, a better way is to specify the limits that include ROM code execution with specified system clock speed.

Low-Power, Dual-Core Microcontroller

Block Diagram



Pin Description

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td colspan="3">POWER PINS</td></tr>
<tr><td>21</td><td>V_{DD}</td><td>Supply Voltage. Must be bypassed with a 4.7µF capacitor with ESR < 5Ω and a 0.1µF ceramic capacitor.</td></tr>
<tr><td>17</td><td>GND</td><td>Ground</td></tr>
<tr><td>20</td><td>REGOUT</td><td>Regulator Output. 1.8V output. Must be connected to a 1µF low-ESR (< 1Ω) external ceramic chip capacitor.</td></tr>
<tr><td>19</td><td>V_{BAT}</td><td>Battery Input for Backing Up the RTC</td></tr>
<tr><td colspan="3">CLOCK PINS</td></tr>
<tr><td>15, 16</td><td>CX1, CX2</td><td>RTC Crystal Inputs. The RTC requires a 32.768kHz crystal to be connected in order to supply the time base for the RTC. The 6pF load capacitors are included in the circuitry.</td></tr>
<tr><td colspan="3">I/O PINS</td></tr>
<tr><td rowspan="10">2–7, 23, 22</td><td rowspan="10">P0.0–P0.7</td><td>Port 0. Port 0 functions as both an 8-bit I/O port and as a special function interface to the I^2C master and serial UARTs 0 and 1. All pins support external interrupt functionality. The default reset condition of the pins is weakly pulled up (input). To drive output, either the port direction register must be programmed to enable output or the alternate function module must be configured to drive the pins. This port is accessible to the UserCore only.</td></tr>
<tr><td>
<table>
<tr><th>PIN</th><th>PORT</th><th>ALTERNATE FUNCTION</th></tr>
<tr><td>2</td><td>P0.0</td><td>TXD0/INT0</td></tr>
<tr><td>3</td><td>P0.1</td><td>RXD0/INT1</td></tr>
<tr><td>4</td><td>P0.2</td><td>MDIN1N/T2P/INT2</td></tr>
<tr><td>5</td><td>P0.3</td><td>MDIN1P/T2PB/INT3</td></tr>
<tr><td>6</td><td>P0.4</td><td>SDA/INT4</td></tr>
<tr><td>7</td><td>P0.5</td><td>SCL/INT5</td></tr>
<tr><td>23</td><td>P0.6</td><td>TXD1/INT6</td></tr>
<tr><td>22</td><td>P0.7</td><td>RXD1/INT7</td></tr>
</table>
</td></tr>
<tr><td rowspan="10">10, 11, 12, 13, 14, 18, 24</td><td rowspan="10">P1.0–P1.6</td><td>Port 1. Port 1 functions as both a 6-bit I/O port and as a special function interface to the JTAG compatible test access port (TAP), the RTC square-wave output, and as the input/output to and from timer B. All pins support external interrupt functionality. The default reset condition of pins P1.0–P1.3 is the JTAG functions. To use the 4-bit port as standard GPIO, the TAP must be disabled by user code. This port is accessible to the UserCore only.

Active-Low Reset ($\overline{RST}$). The $\overline{RST}$ pin recognizes external active-low reset inputs and employs an internal pullup resistor to allow for a combination of wired-OR external reset sources. An RC is not required for power-up, as this function is provided internally. The $\overline{RST}$ pin function is enabled on power-on reset. It is critical that this pin not be held low externally after a power-on reset or the device cannot exit the reset state.</td></tr>
<tr><td>
<table>
<tr><th>PIN</th><th>PORT</th><th>ALTERNATE FUNCTION</th></tr>
<tr><td>10</td><td>P1.0</td><td>TMS/INT8</td></tr>
<tr><td>11</td><td>P1.1</td><td>TCK/INT9</td></tr>
<tr><td>12</td><td>P1.2</td><td>TDI/INT10</td></tr>
<tr><td>13</td><td>P1.3</td><td>TDO/SQW/INT11</td></tr>
<tr><td>14</td><td>P1.4</td><td>TBB</td></tr>
<tr><td>18</td><td>P1.5</td><td>TBA</td></tr>
<tr><td>24</td><td>P1.6</td><td>$\overline{RST}$</td></tr>
</table>
</td></tr>
</table>

Low-Power, Dual-Core Microcontroller

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th colspan="3">FUNCTION</th></tr>
<tr><td rowspan="9">1, 28, 27, 26, 25, 8, 9</td><td rowspan="9">P2.0–P2.6</td><td colspan="3">Port 2. Port 2 functions as both a 7-bit I/O port and as a special function interface to the CF pulse generator outputs, clock output, and the Manchester ENDEC or SPI. The default reset condition of the pins is weakly pulled up (input), with exception of P2.5 and P2.6, which are always outputs and default to strong high. To drive output, either the port direction register must be programmed to enable output, or the alternate function module must be configured to drive the pins. P2.5 and P2.6 are accessible to the DSPCore only.</td></tr>
<tr><td>PIN</td><td>PORT</td><td>ALTERNATE FUNCTION</td></tr>
<tr><td>1</td><td>P2.0</td><td>MDIN2P/MOSI</td></tr>
<tr><td>28</td><td>P2.1</td><td>MDIN2N/MISO</td></tr>
<tr><td>27</td><td>P2.2</td><td>SCLK/CLKO</td></tr>
<tr><td>26</td><td>P2.3</td><td>MDIN0N/$\overline{\text{SSEL}}$</td></tr>
<tr><td>25</td><td>P2.4</td><td>MDIN0P</td></tr>
<tr><td>8</td><td>P2.5</td><td>CF1</td></tr>
<tr><td>9</td><td>P2.6</td><td>CF2</td></tr>
</table>

Detailed Description

The MAXQ3108 microcontroller is an integrated, low-cost solution to simplify the design of electricity metering and industrial control products. Standard features include two highly optimized, single-cycle, MAXQ 16-bit RISC microcontroller cores; 64KB of flash memory, 11KB RAM, and independent hardware stacks; general-purpose registers; and data pointers for each core. Application-specific peripherals include hardware SPI and I^2C masters, real-time clock, programmable pulse generators, dual UARTs (one of which that supports IR carrier frequency modulation), and math accelerators.

At the heart of the MAXQ3108 are two MAXQ20 16-bit RISC microcontrollers. The dual-core approach allows one core (DSPCore) to be entirely dedicated to collection and processing of AFE samples for the metering function, while the second core handles any communication and user-specific administrative functions. The MAXQ3108 DSPCore operates at 10.027MHz with the default crystal and almost all instructions execute in a single clock cycle (100ns), while the UserCore runs at half that frequency (5.014MHz).

The dual-core strategy promotes flexibility by allowing the update of metering routines and parameters separately in DSPCore code and data memory. Furthermore, an independent DSPCore solely responsible for accurate metering introduces a measure of safety and reliability since all administrative/communication functions and interruptions are handled by the UserCore. Both cores feature standard MAXQ power-saving system clock-divide modes and independently implement low-power stop (UserCore) and idle (DSPCore) modes. The DSPCore implements an idle mode that allows CPU execution to be halted while awaiting an ADC sample. The UserCore implements an ultra-low-power stop mode that automatically disables the DSPCore and results in a quiescent current consumption of less than 1.5µA. The combination of high performance and core-specific low-power mode implementation provides increased power efficiency and capability over competitive microcontrollers.

Microprocessor

The MAXQ20 is a low-power implementation of the new 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate 16-bit program and data address buses, but also provides pseudo-Von Neumann support through utility ROM functions. A fixed 16-bit instruction is standard, but data can be arranged in 8 or 16 bits. The MAXQ20 core is implemented as a nonpipelined processor with single clock-cycle instruction execution. The data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled to the arithmetic logic unit (ALU). Program flow is supported by a dedicated 16-level-deep hardware stack.

Execution of instructions is triggered by data transfer between functional register modules, or between a functional register module and memory. Since data

movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides maximum flexibility and reusability, which are important for a microprocessor used in embedded applications.

The MAXQ instruction set is designed to be highly orthogonal. All arithmetical and logical operations can use any register along with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data pointer registers with auto increment/decrement support.

Memory

The MAXQ3108 supports a pseudo-Von Neumann memory structure that can merge program and data into a linear memory map. This is accomplished by mapping the data memory into the program space or mapping the program memory segment into the data space. Memory access is under the control of the memory management unit (MMU). During flash programming, the MMU maps the flash memory into data space, and the built-in firmware provides necessary controls to the embedded flash memory for all read/erase/write operations when the ROM loader is invoked. Additionally, when the DSPCore is disabled, all its code SRAM (8KB) is mapped into the data SRAM space of the UserCore. This allows streamlined reconfiguration of the DSP code memory or a larger data SRAM for applications not employing DSPCore operation.

The MAXQ3108 incorporates the following:

- 4KB utility ROM
- 64KB program flash
- 2KB SRAM data memory
- 8KB program SRAM (DSPCore)
- 1KB SRAM data memory (DSPCore)

The MMU operates automatically and maps data memory as a function of the contents of the instruction pointer; that is, the execution location controls the structure of the data memory map. The only constraint is that no memory region is available as data when code is being fetched from that region. For example, when executing from flash, flash cannot be read as data. But changing the execution location to the utility ROM through a subroutine call allows the flash memory to be read as data.

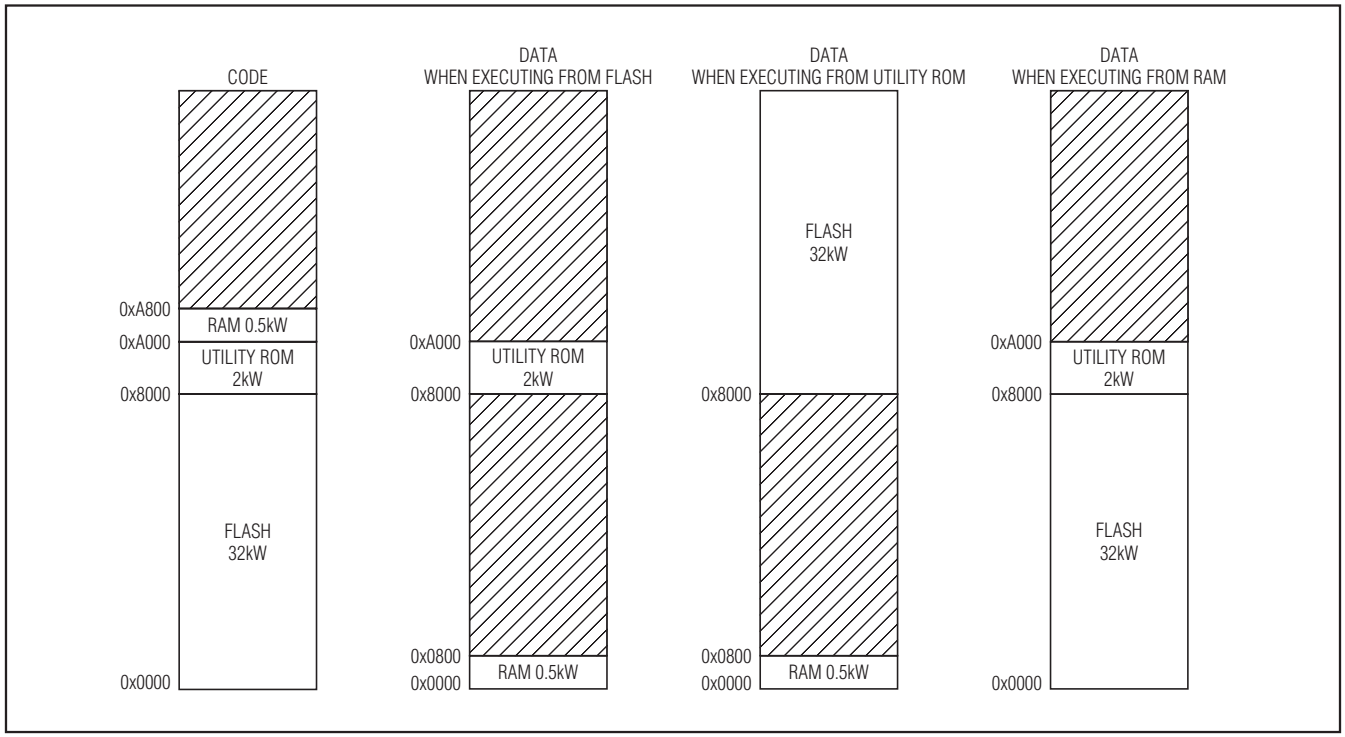


Figure 1. Memory Map

Low-Power, Dual-Core Microcontroller

DSP Program RAM

A 4K Word (8KB) section of memory is available to the DSPCore as code memory. When the DSPCore is disabled (as it is immediately following a reset event) that block of memory appears in the UserCore data memory map at location 0x1000. Thus, a typical startup sequence to operate both cores might include:

1) Low-level initialization of the UserCore.
2) Copy DSP code from program flash to DSPCore code RAM at 0x1000.
3) Enable DSPCore.
4) Poll mailbox registers to verify that DSPCore is correctly running.

For more information, see the *Dual-Core Interfaces* section.

Registers

The MAXQ family of microcontrollers uses a bank of registers to access memory and peripherals and to perform basic CPU activities. These registers are organized into as many as 16 register modules, each of which can have as many as 32 registers, giving a system maximum of 512 registers. The registers are divided into two sections: system registers (modules 7 to 15) and peripheral registers (modules 0 to 5).

Since the MAXQ3108 contains two MAXQ core processors, each has a set of system registers and a set of peripheral registers.

System Registers

The MAXQ3108 UserCore implements the standard set of system registers as described in the *MAXQ Family User's Guide*. The exceptions are listed below:

- In the IMR register, bit IM5 is not implemented since there is no module 5 implemented in the MAXQ3108.
- In the SC register, bits CDA1 and UPM are not implemented since the size of the memory in the device does not require their implementation.
- In the IIR register, bit II5 is not implemented since there is no module 5 implemented in the MAXQ3108.
- In the CKCN register, bits XT/$\overline{RC}$, RGSL, and RGMD are not implemented. Instead, bits 5 and 6 are FLLMD and FLLSL, respectively. These bits support the frequency-locked loop (FLL) that forms a core part of the MAXQ3108 clocking scheme. More information is given in the *Clock* section.

The MAXQ3108 DSPCore system register complement is identical to that found in the UserCore, with these exceptions:

- In the IMR register, only IM0 is implemented.
- The system control (SC) register is not implemented.
- In the IIR register, only the II0 bit is implemented.
- The WDCN register is not implemented because there is no watchdog timer in the DSPCore. Watchdog functionality can be implemented in the UserCore by determining if the DSPCore is responding to messages.
- In the CKCN register, the STOP, RGSL, and SWB bits are not implemented because the corresponding functions do not exist in the DSPCore. The FLLMD and FLLSL bits are not implemented because a common clock block is shared with the UserCore, and the control bits here would be redundant.

Peripheral Registers—UserCore

The MAXQ3108 UserCore exposes its peripheral complement in five modules numbered 0 to 4. Table 1 describes the functions associated with the peripheral registers, and Table 2 shows the default values of these registers.

Table 1. UserCore Peripheral Registers

REGISTER	MOD:REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD0	0:0	ADC0 Output Register															
AD1	0:1	ADC1 Output Register															
AD2	0:2	ADC2 Output Register															
AD3	0:3	ADC3 Output Register															
AD4	0:4	ADC4 Output Register															
AD5	0:5	ADC5 Output Register															
SRSP0	0:6											RSPSDV	REQE	RSPST			
SRSP1	0:7	Slave Response Register 1															
AD0LSB	0:8									ADC0 Output Register LSB							

Table 1. UserCore Peripheral Registers (continued)

REGISTER	MOD:REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD1LSB	0:9									ADC1 Output Register LSB							
AD2LSB	0:10									ADC2 Output Register LSB							
AD3LSB	0:11									ADC3 Output Register LSB							
AD4LSB	0:12									ADC4 Output Register LSB							
AD5LSB	0:13									ADC5 Output Register LSB							
MREQ0	0:14											REQCDV	RSPIE	REQCM			
MREQ1	0:15	Master Request Register 1															
MREQ2	0:16	Master Request Register 2															
ADCN	0:17	IFCSEL	IF54E	IF32E	IF10E	MDCKS	MD2E	MD1E	MD0E	OSR		ABF5	ABF4	ABF3	ABF2	ABF1	ABF0
ADCC	0:18	ADC Clock Correction Register															
MSTC	0:19											CCSL			MD2SNC	MD1SNC	MD0SNC
PO0	1:0									Port 0 Output Register							
PO1	1:1										Port 1 Output Register						
PI0	1:2									Port 0 Input Register							
PI1	1:3										Port 1 Input Register						
EIF0	1:4									Port 0 Interrupt Flag Register							
EIE0	1:5									Port 0 Interrupt Enable Register							
EIF1	1:6													Port 1 Interrupt Flag Register			
EIE1	1:7													Port 1 Interrupt Enable Register			
PD0	1:8									Port 0 Direction Register							
PD1	1:9										Port 1 Direction Register						
EIES0	1:10									Port 0 External Interrupt Edge Select							
EIES1	1:11													Port 1 External Interrupt Edge Select			
SVM	1:12					SVTH							SVMSTOP	SVMI	SVMIE	SVMRDY	SVMEN
FCNTL	1:13									FBUSY					FC		
FDATA	1:14	Flash Data Register															
PWCN	1:15						ENDSP			BOD	REGEN	RSTD			ECLKO	FLOCK	FLLEN
BB0	1:16	Battery-Backed General-Purpose Storage 0															
BB1	1:17	Battery-Backed General-Purpose Storage 1															
BB2	1:18	Battery-Backed General-Purpose Storage 2															
BB3	1:19	Battery-Backed General-Purpose Storage 3															
BB4	1:20	Battery-Backed General-Purpose Storage 4															
BB5	1:21	Battery-Backed General-Purpose Storage 5															
BB6	1:22	Battery-Backed General-Purpose Storage 6															
BB7	1:23	Battery-Backed General-Purpose Storage 7															
RTRM	1:24									TSGN	TRM						
RCNT	1:25	WE	X32D	32KRDY	32KBYP	32KMD		FT	SQE	ALSF	ALDF	RDYE	RDY	BUSY	ASE	ADE	RTCE
RTSS	1:26									RTC Subsecond Counter							
RTSH	1:27	RTC Seconds Register MSW															
RTSL	1:28	RTC Seconds Register LSW															
RSSA	1:29									RTC Subsecond Alarm							
RASH	1:30													RTC Seconds Alarm MSW			
RASL	1:31	RTS Seconds Alarm LSW															
T2CNA	2:0									ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
T2H	2:1									Timer 2 MSB							

Low-Power, Dual-Core Microcontroller

Table 1. UserCore Peripheral Registers (continued)

REGISTER	MOD: REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T2RH	2:2									Timer 2 MSB Reload Value							
T2CH	2:3									Timer 2 MSB Capture/Compare Value							
PO2	2:4										Port 2 Output Register						
PI2	2:5										Port 2 Input Register						
SCON0	2:6									SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF0	2:7									Serial Data Buffer 0							
SMD0	2:8									EPWM	OFS				ESI	SMOD	FEDE
PR0	2:9	Phase Register 0															
PD2	2:10										Port 2 Direction Register						
T2CNB	2:11									ET2L	T2OE1	T2POL1		TF2	TF2L	TCC2	T2CL
T2V	2:12	Timer 2 Value Register															
T2R	2:13	Timer 2 Reload Register															
T2C	2:14	Timer 2 Capture/Compare Register															
T2CFG	2:15									T2CI	T2DIV			T2MD	CCF		C/$\overline{T2}$
MCNT	3:0									OF	MCW	CLD	SQU	OPCS	MSUB	MMAC	SUS
MA	3:1	Multiplier Operand “A” Register															
MB	3:2	Multiplier Operand “B” Register															
MC2	3:3	Multiplier Accumulator Register 2 (MSB, bits 47-32)															
MC1	3:4	Multiplier Accumulator Register 1 (bits 31-16)															
MC0	3:5	Multiplier Accumulator Register 0 (LSB, bits 15-0)															
SPIB	3:7	SPI Data Buffer															
MC1R	3:8	Multiplier Read Register 1 (MSB, bits 31-16)															
MC0R	3:9	Multiplier Read Register 0 (LSB, bits 15-0)															
SPICN	3:13									STBY	SPIC	ROVR	WCOL	MODF	MODFE	MSTM	SPIEN
SPICF	3:14									ESPII					CHR	CKPHA	CKPOL
SPICK	3:15									SPI Clock Register							
I2CBUF	4:0							I2C Data Buffer Register									
I2CST	4:1	I2CBUS	I2CBUSY			I2CSPI	I2CSCL	I2CROI	I2CGCI	I2CNACKI	I2CALI	I2CAMI	I2CTOI	I2CSTRI	I2CRXI	I2CTXI	I2CSRI
I2CIE	4:2					I2CSPIE		I2CROIE	I2CGCIE	I2CNACKIE	I2CALIE	I2CAMIE	I2CTOIE	I2CSTRIE	I2CRXIE	I2CTXIE	I2CSRIE
TB0R	4:4	Timer B Capture/Reload Value															
TB0C	4:5	Timer B Compare Value															
SCON1	4:6									SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF1	4:7									Serial Data Buffer 1							
SMD1	4:8														ESI	SMOD	FEDE
PR1	4:9	Phase Register 1															
TB0CN	4:10	C/$\overline{TB}$			TBCS	TBCR	TBPS			TFB	EXFB	TBOE	DCEN	EXENB	TRB	ETB	CP/$\overline{RLB}$
TB0V	4:11	Timer B Value Register															
I2CCN	4:12	I2CRST						I2CSTREN	I2CGCEN	I2CSTOP	I2CSTART	I2CACK	I2CSTRS		I2CMODE	I2CMST	I2CEN
I2CCK	4:13	I2C Clock High Period								I2C Clock Low Period							
I2CTO	4:14									I2C Timeout Period							
I2CSLA	4:15							I2C Slave Address									

Table 2. UserCore Peripheral Register Default Values

REGISTER	MOD:REG	BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD0	0:0	0xFFFF															
AD1	0:1	0xFFFF															
AD2	0:2	0xFFFF															
AD3	0:3	0xFFFF															
AD4	0:4	0xFFFF															
AD5	0:5	0xFFFF															
SRSP0	0:6											0	0	0x0			
SRSP1	0:7	0x0000															
AD0LSB	0:8									0xFF							
AD1LSB	0:9									0xFF							
AD2LSB	0:10									0xFF							
AD3LSB	0:11									0xFF							
AD4LSB	0:12									0xFF							
AD5LSB	0:13									0xFF							
MREQ0	0:14											0	0	0x0			
MREQ1	0:15	0x0000															
MREQ2	0:16	0x0000															
ADCN	0:17	0	0	0	0	0	0	0	0	0x0		0	0	0	0	0	0
ADCC	0:18	0x0000															
MSTC	0:19											0x3			0	0	0
PO0	1:0									0xFF							
PO1	1:1										0x7F						
PI0	1:2									0xXX							
PI1	1:3										0xXX						
EIF0	1:4									0x00							
EIE0	1:5									0x00							
EIF1	1:6													0x0			
EIE1	1:7													0x0			
PD0	1:8									0x00							
PD1	1:9										0x00						
EIES0	1:10									0x00							
EIES1	1:11													0x0			
SVM	1:12					0x7							0	0	0	0	0
FCNTL	1:13									1					0x0		
FDATA	1:14	0x0000															
PWCN	1:15						0			0	0	0			0	0	0
BB0	1:16	0xXXXX															
BB1	1:17	0xXXXX															
BB2	1:18	0xXXXX															
BB3	1:19	0xXXXX															
BB4	1:20	0xXXXX															
BB5	1:21	0xXXXX															
BB6	1:22	0xXXXX															
BB7	1:23	0xXXXX															
RTRM	1:24									X	X						

Table 2. UserCore Peripheral Register Default Values (continued)

REGISTER	MOD:REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCNT	1:25	0	X	X	X	0xX		0	0	0	0	0	0	1	0	0	X
RTSS	1:26									0xXX							
RTSH	1:27	0xXXXX															
RTSL	1:28	0xXXXX															
RSSA	1:29									0xXXXX							
RASH	1:30													0xX			
RASL	1:31	0xXXXX															
T2CNA	2:0									0	0	0	0	0	0	0	0
T2H	2:1									0x00							
T2RH	2:2									0x00							
T2CH	2:3									0x00							
PO2	2:4										1Fh						
PI2	2:5										0xXX						
SCON0	2:6									0	0	0	0	0	0	0	0
SBUF0	2:7									0x00							
SMD0	2:8									0	0				0	0	0
PR0	2:9	0x0000															
PD2	2:10										0x00						
T2CNB	2:11									0	0	0		0	0	0	0
T2V	2:12	0x0000															
T2R	2:13	0x0000															
T2C	2:14	0x0000															
T2CFG	2:15									0	0x0			0	0x0		0
MCNT	3:0									0	0	0	0	0	0	0	0
MA	3:1	0x0000															
MB	3:2	0x0000															
MC2	3:3	0x0000															
MC1	3:4	0x0000															
MC0	3:5	0x0000															
SPIB	3:7	0x0000															
MC1R	3:8	0x0000															
MC0R	3:9	0x0000															
SPICN	3:13									0	0	0	0	0	0	0	0
SPICF	3:14									0					0	0	0
SPICK	3:15									0x00							
I2CBUF	4:0							0x0000									
I2CST	4:1	0	0			0	0	0	0	0	0	0	0	0	0	0	0
I2CIE	4:2					0		0	0	0	0	0	0	0	0	0	0
TB0R	4:4	0x0000															
TB0C	4:5	0x0000															
SCON1	4:6									0	0	0	0	0	0	0	0
SBUF1	4:7									0x0000							
SMD1	4:8														0	0	0
PR1	4:9	0x0000															
TB0CN	4:10	0			0	0	0x0			0	0	0	0	0	0	0	0

Table 2. UserCore Peripheral Register Default Values (continued)

REGISTER	MOD:REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TB0V	4:11	0x0000															
I2CCN	4:12	0						0	0	0	0	0	0		0	0	0
I2CCK	4:13	0x02								0x04							
I2CTO	4:14									0x00							
I2CSLA	4:15							0x000									

Peripheral Registers—DSPCore

The MAXQ3108 DSPCore exposes its peripheral complement in modules numbered 0 and 1. Table 3 describes the functions associated with the peripheral registers, and Table 4 shows the default values of these registers.

Table 3. DSPCore Peripheral Registers

REGISTER	MOD:REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD0	0:0	ADC0 Output Register															
AD1	0:1	ADC1 Output Register															
AD2	0:2	ADC2 Output Register															
AD3	0:3	ADC3 Output Register															
AD4	0:4	ADC4 Output Register															
AD5	0:5	ADC5 Output Register															
SRSP0	0:6											RSPSDV	REQE	RSPST			
SRSP1	0:7	Slave Response Register 1															
AD0LSB	0:8									ADC0 Output Register LSB							
AD1LSB	0:9									ADC1 Output Register LSB							
AD2LSB	0:10									ADC2 Output Register LSB							
AD3LSB	0:11									ADC3 Output Register LSB							
AD4LSB	0:12									ADC4 Output Register LSB							
AD5LSB	0:13									ADC5 Output Register LSB							
MREQ0	0:14											REQCDV	RSPIE	REQCM			
MREQ1	0:15	Master Request Register 1															
MREQ2	0:16	Master Request Register 2															
ADCN	0:17	IFCSEL	IF45E	IF23E	IF10E	MDCKS	MD2E	MD1E	MD0E	OSRI		ABF5	ABF4	ABF3	ABF2	ABF1	ABF0
ADCC	0:18	ADC Clock Correction Register															
MSTC	0:19											CCSL			MD2SNC	MD1SNC	MD0SNC
MCNT	1:0									OF	MCW	CLD	SQU	OPCS	MSUB	MMAC	SUS
MA	1:1	Multiplier Operand “A” Register															
MB	1:2	Multiplier Operand “B” Register															
MC2	1:3	Multiplier Accumulator Register 2 (MSB, bits 47-32)															
MC1	1:4	Multiplier Accumulator Register 1 (bits 31-16)															
MC0	1:5	Multiplier Accumulator Register 0 (LSB, bits 15-0)															

Low-Power, Dual-Core Microcontroller

Table 3. DSPCore Peripheral Registers (continued)

REGISTER	MOD: REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO2	1:7	Port 2 Output Register															
MC1R	1:8	Multiplier Read Register 1 (MSB, bits 31-16)															
MC0R	1:9	Multiplier Read Register 0 (LSB, bits 15-0)															
CF1D	1:12	CF1 Delay Register															
CF2D	1:13	CF2 Delay Register															

Table 4. DSPCore Peripheral Register Default Values

REGISTER	MOD: REG	BIT															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD0	0:0	0xFFFF															
AD1	0:1	0xFFFF															
AD2	0:2	0xFFFF															
AD3	0:3	0xFFFF															
AD4	0:4	0xFFFF															
AD5	0:5	0xFFFF															
SRSP0	0:6											0	0	0x0			
SRSP1	0:7	0x0000															
AD0LSB	0:8									0xFF							
AD1LSB	0:9									0xFF							
AD2LSB	0:10									0xFF							
AD3LSB	0:11									0xFF							
AD4LSB	0:12									0xFF							
AD5LSB	0:13									0xFF							
MREQ0	0:14											0	0	0x0			
MREQ1	0:15	0x0000															
MREQ2	0:16	0x0000															
ADCN	0:17	0	0	0	0	0	0	0	0	0x0		0	0	0	0	0	0
ADCC	0:18	0x0000															
MSTC	0:19											0x3			0	0	0
MCNT	1:0									0	0	0	0	0	0	0	0
MA	1:1	0x0000															
MB	1:2	0x0000															
MC2	1:3	0x0000															
MC1	1:4	0x0000															
MC0	1:5	0x0000															
PO2	1:7	0x0000															
MC1R	1:8	0x0000															
MC0R	1:9	0x0000															
CF1D	1:12	0x0000															
CF2D	1:13	0x0000															

Special Function Register Bit Descriptions

REGISTER	DESCRIPTION
AD0 (00h, 00h) *Initialization:* *Read/Write Access:*	**Analog-to-Digital Converter 0 Output Register** This register is reset to 0xFFFF on all forms of reset. Unrestricted read access.
AD0.[15:0]:	**Analog-to-Digital Converter 0 Output Register.** This register contains the most significant 16 bits of the current ADC0 data sample that was acquired from the respective sinc3 filter. Reading from the ADC0 register(s) results in the ABF0 flag being cleared by hardware (when set), unless the read operation is performed simultaneously with a write. Reading a disabled ADC returns the data last acquired if the associated buffer full flag is set and returns FFFFh if the flag is clear.
AD1 (01h, 00h)	**Analog-to-Digital Converter 1 Output Register**
AD2 (02h, 00h)	**Analog-to-Digital Converter 2 Output Register**
AD3 (03h, 00h)	**Analog-to-Digital Converter 3 Output Register**
AD4 (04h, 00h)	**Analog-to-Digital Converter 4 Output Register**
AD5 (05h, 00h)	**Analog-to-Digital Converter 5 Output Register**

SRSP0 (06h, 00h) *Initialization:* *Read/Write Access:*	**Slave Response Register 0** This register is reset to 00h on all forms of reset. Unrestricted read access only to the UserCore (except RSPSDV; see the bit description). Unrestricted read/write access to the DSPCore (except RSPSDV and RSPST[3:0]; see the bit descriptions).
SRSP0.[3:0]: RSPST[3:0]	**Response Status Bits 3:0.** These bits can be used to report acknowledgement and status of the current command being processed by the slave and to report slave system conditions (e.g., watchdog timeout) that are not related to a master command. To notify the master that status is ready to be read, the RSP0DV bit should be set to 1 either by software (in the case of command status) or, in some cases, by hardware (as for the watchdog). In cases where slave hardware sets the status bits, these bits are not writable by slave software until the status condition has been cleared. When the DSPCore watchdog timer reaches FFFFh, a system interrupt from the DSPCore is signaled by the setting of the SRSP0.5 status flag along with the SRSP0.[3:0] status code of 0000b. This hardware condition for the SRSP0 register persists (preventing software writes of these bits by the DSPCore) until a reset of the DSPCore is executed (UserCore may disable the DSPCore through ENDSP = 0 to force the reset).
SRSP0.4: REQE	**Request Registers Interrupt Enable.** Setting this bit to 1 enables an interrupt for the master request-command data valid (interrupt) flag (REQCDV). The master request-command data valid flag is reported in MREQ0.5 (and the associated command code is contained in MREQ0.[3:0]). Clearing this bit to 0 disables the interrupt associated with the master request-command data valid flag.
SRSP0.5: RSPSDV	**Response Status Data Valid Flag.** This flag can only be set by the slave (DSPCore) or slave hardware once a valid status or system interrupt condition is supplied in the RSPST[3:0] field of the SRSP0 register to notify the master that valid status is ready for reading. Status information or data could also be contained in SRSP1, so the slave should only set this flag when all data has been loaded (included any that is loaded to SRSP1). This flag can only be cleared by the master (UserCore) software unless the status condition that caused hardware to set the flag persists (e.g., slave watchdog counter timeout). If made available by the slaveCPU, more information can be ascertained about the status by additional master request read commands.
SRSP0.[7:6]: Reserved	**Reserved.** Reads return 0.

Low-Power, Dual-Core Microcontroller

Special Function Register Bit Descriptions (continued)

SRSP1 (07h, 00h) *Initialization:* *Read/Write Access:*	**Slave Response Register 1** This register is reset to 0000h on all forms of reset. Unrestricted read access only to the UserCore. Unrestricted read/write access to the DSPCore.
SRSP1.[15:0]:	**Slave Response Register 1 Bits 15:0.** These bits are used to supply output data to the master. To notify the master that data is ready to be read, the RSPCDV bit should be set to 1 by software. The slave should not write further data to SRSP1 until the valid condition (RSPSDV = 1) is cleared by the master software.

AD0LSB (08h, 00h) *Initialization:* *Read/Write Access:*	**Analog-to-Digital Converter 0 Least Significant Byte Output Register** This register is reset to FFh on all forms of reset. Unrestricted read access.		
AD0LSB.[7:0]:	**Analog-to-Digital Converter 0 Least Significant Byte Output Register.** This register always provides read access to the least significant byte of the most current ADC0 data sample acquired from the respective sinc3 filter. See the below table for the least significant byte available OSR options. Reading from the AD0 register results in the ABF0 flag being cleared by hardware (when set) unless the read operation is performed simultaneously with a write. What this means is that when OSR > 32, AD0LSB should be read first if the clearing of ABF0 is intended to indicate that the full result (AD0LSB and AD0) was read. Reading a disabled ADC returns the data last acquired if the associated buffer full flag is set and returns FFFFh if the flag is clear.		
	OSR	**ADC DATA OUTPUT WIDTH**	**AD0LSB FORMAT**
	32	16	00000000b
	64	19	d2–d0, 00000b
	128	22	d5–d0, 00b
	256	24	d7–d0
AD1LSB (09h, 00h)	**Analog-to-Digital Converter 1 Least Significant Byte Output Register**		
AD2LSB (0Ah, 00h)	**Analog-to-Digital Converter 2 Least Significant Byte Output Register**		
AD3LSB (0Bh, 00h)	**Analog-to-Digital Converter 3 Least Significant Byte Output Register**		
AD4LSB (0Ch, 00h)	**Analog-to-Digital Converter 4 Least Significant Byte Output Register**		
AD5LSB (0Dh, 00h)	**Analog-to-Digital Converter 5 Least Significant Byte Output Register**		

MREQ0 (0Eh, 00h) *Initialization:* *Read/Write Access:*	**Master Request Register 0** This register is reset to 00h on all forms of reset. Unrestricted read/write access to the UserCore (except REQCDV; see the bit description). Unrestricted read access only to the DSPCore (except REQCDV; see the bit description).
MREQ0.[3:0]: REQCM[3:0]	**Request Command Bits 3:0.** These bits are written by the master to supply a command request to the slave. To notify the slave that a command is ready to be read, the REQ0DV bit should be set to 1.
MREQ0.4: RSPIE	**Response Registers Interrupt Enable.** Setting this bit to 1 enables an interrupt for the slave response status data valid flag (which is associated with Response Registers 0 and 1). The status data valid (interrupt) flag is reported in SRSP0.5. Clearing this bit to 0 disables the interrupt associated with the response status data valid flag.
MREQ0.5: REQCDV	**Request Command Data Valid Flag.** This flag can only be set by the master (UserCore). This flag should be set once a valid command is supplied in the REQCM[3:0] field of the MREQ0 and/or data supplied in the MREQ1, MREQ2 registers to notify the slave that these registers are ready for reading. This flag can only be cleared by slave (DSPCore) software.
MREQ0.[7:6]: Reserved	**Reserved.** Reads return 0.

Special Function Register Bit Descriptions (continued)

MREQ1 (0Fh, 00h) *Initialization:* *Read/Write Access:*	**Master Request Register 1** This register is reset to 0000h on all forms of reset. Unrestricted read/write access only to the UserCore. Unrestricted read access only to the DSPCore.
MREQ1.[15:0]:	**Master Request Register 1 Bits 15:0.** These bits are used to supply follow-on address and data information for commands issued by the master. To notify the slave that data is ready to be read, the REQCDV bit should be set to 1. The master should poll the REQCDV bit to know when the slave has read MREQ1 and when it is safe to write further data to MREQ1.

MREQ2 (10h, 00h) *Initialization:* *Read/Write Access:*	**Master Request Register 2** This register is reset to 0000h on all forms of reset. Unrestricted read/write access only to the UserCore. Unrestricted read access only to the DSPCore.
MREQ2.[15:0]:	**Master Request Register 2 Bits 15:0.** These bits are used to supply follow-on address and data information for commands issued by the master. To notify the slave that data is ready to be read, the REQCDV bit should be set to 1. The master should poll the REQCDV bit to know when the slave has read MREQ2 and when it is safe to write further data to MREQ2.

ADCN (11h, 00h) *Initialization:* *Read/Write Access:*	**Analog-to-Digital Converter Control Register** This register is cleared to 0000h on all forms of reset. UserCore: Unrestricted read/write access except bits 0:5 are read only and 6:7 have hardware restricted write access. DSPCore: Read-only.
ADCN.0: ABF0	**ADC0 Buffer Full Flag.** This bit is set by hardware to indicate that a sample is available from ADC0. An interrupt request is generated to a CPU if IF01E = 1 and interrupts are not otherwise masked globally or modularly. This bit is cleared by hardware by a CPU read (either the UserCore or the DSPCore) of the AD0 output register. The ABF0 and ABF1 flags are set in the same clock cycle.
ADCN.1: ABF1	**ADC1 Buffer Full Flag.** This bit is set by hardware to indicate that a sample is available from ADC1. An interrupt request is generated to a CPU if IF01E = 1 and interrupts are not otherwise masked globally or modularly. This bit is cleared by hardware by a CPU read (either the UserCore or the DSPCore) of the AD1 output register. The ABF0 and ABF1 flags are set in the same clock cycle.
ADCN.2: ABF2	**ADC2 Buffer Full Flag.** This bit is set by hardware to indicate that a sample is available from ADC2. An interrupt request is generated to a CPU if IF23E = 1 and interrupts are not otherwise masked globally or modularly. This bit is cleared by hardware by a CPU read (either the UserCore or the DSPCore) of the AD2 output register. The ABF2 and ABF3 flags are set in the same clock cycle.
ADCN.3: ABF3	**ADC3 Buffer Full Flag.** This bit is set by hardware to indicate that a sample is available from ADC3. An interrupt request is generated to a CPU if IF23E = 1 and interrupts are not otherwise masked globally or modularly. This bit is cleared by hardware by a CPU read (either the UserCore or the DSPCore) of the AD3 output register. The ABF2 and ABF3 flags are set in the same clock cycle.
ADCN.4: ABF4	**ADC4 Buffer Full Flag.** This bit is set by hardware to indicate that a sample is available from ADC4. An interrupt request is generated to a CPU if IF45E = 1 and interrupts are not otherwise masked globally or modularly. This bit is cleared by hardware by a CPU read (either the UserCore or the DSPCore) of the AD4 output register. The ABF4 and ABF5 flags are set in the same clock cycle.

Low-Power, Dual-Core Microcontroller

Special Function Register Bit Descriptions (continued)

ADCN.5: ABF5	**ADC5 Buffer Full Flag.** This bit is set by hardware to indicate that a sample is available from ADC5. An interrupt request is generated to a CPU if IF45E = 1 and interrupts are not otherwise masked globally or modularly. This bit is cleared by hardware by a CPU read (either the UserCore or the DSPCore) of the AD5 output register. The ABF4 and ABF5 flags are set in the same clock cycle.
ADCN.[7:6]: OSR[1:0]	**Oversampling Rate Bits 1:0.** These register bits control the oversampling rate applied by all of the cubic sinc digital filters (as given in the table below). These bits are writable only when all Manchester decoders are disabled.

OSR[1:0]	OVERSAMPLING RATE
00b	32
01b	64
10b	128
11b	256

ADCN.8: MD0E	**Manchester Decoder 0 Enable.** This bit controls whether Manchester decoder 0 and the two associated cubic sinc filters are enabled or disabled. When MD0E is configured to logic 1, Manchester decoder 0 and the associated cubic sinc filters are enabled. This is a special case where enabling the special function input (Manchester decoder input) forces a specific input mode (single-ended or differential) based upon the PO bit for the port pin corresponding to the Manchester decoder positive input (e.g., PO2.4 controls the single-ended or differential configuration for Manchester decoder 0 when MD0E = 1). When the PO bit = 0, single-ended mode is in effect. When PO bit = 1, differential mode is in effect. When MD0E is configured to logic 0, these hardware blocks are disabled. This bit is write accessible only to the UserCore.
ADCN.9: MD1E	**Manchester Decoder 1 Enable.** This bit controls whether Manchester decoder 1 and the two associated cubic sinc filters are enabled or disabled. When MD1E is configured to logic 1, Manchester decoder 1 and the associated cubic sinc filters are enabled. This is a special case where enabling the special function input (Manchester decoder input) forces a specific input mode (single-ended or differential) based upon the PO bit for the port pin corresponding to the Manchester decoder positive input (e.g., PO0.3 controls the single-ended or differential configuration for Manchester decoder 1 when MD1E = 1). When the PO bit = 0, single-ended mode is in effect. When PO bit = 1, differential mode is in effect. When MD1E is configured to logic 0, these hardware blocks are disabled. This bit is write accessible only to the UserCore.
ADCN.10: MD2E	**Manchester Decoder 2 Enable.** This bit controls whether Manchester decoder 2 and the two associated cubic sinc filters are enabled or disabled. When MD2E is configured to logic 1, Manchester decoder 2 and the associated cubic sinc filters are enabled. This is a special case where enabling the special function input (Manchester decoder input) forces a specific input mode (single-ended or differential) based upon the PO bit for the port pin corresponding to the Manchester decoder positive input (e.g., PO2.0 controls the single-ended or differential configuration for Manchester decoder 2 when MD2E = 1). When the PO bit = 0, single-ended mode is in effect. When PO bit = 1, differential mode is in effect. When MD2E is configured to logic 0, these hardware blocks are disabled. This bit is write accessible only to the UserCore.
ADCN.11: MDCKS	**Manchester Decoders Clock Speed Select.** This bit must be configured to tell the Manchester decoders whether a fast or slow bit-stream sampling clock is used. When configured to 0, the decoders expect that the sampling clock is faster than the clock source being used by the AD02 modulator(s). When configured to 1, the decoders expect that the sampling clock is slower that than being used by the AD02.
ADCN.12: IF10E	**ADC Interrupt Flags 1 and 0 Enable.** This bit serves as the local interrupt enable for the ADC cubic sinc filter output buffers 1 and 0.

Special Function Register Bit Descriptions (continued)

ADCN.13: IF32E	**ADC Interrupt Flags 3 and 2 Enable.** This bit serves as the local interrupt enable for the ADC cubic sinc filter output buffers 3 and 2.
ADCN.14: IF54E	**ADC Interrupt Flags 5 and 4 Enable.** This bit serves as the local interrupt enable for the ADC cubic sinc filter output buffers 5 and 4.
ADCN.15: IFCSEL	**ADC Interrupt Flag Core Select.** This bit controls the routing and the ability to clear the ADC interrupt flags. When this bit is configured to 0, the ADC interrupt capability and the ability to clear the associated flags belongs to the UserCore. When this bit is configured to 1, only the DSPCore can be interrupted and has the ability to clear the interrupt flags. This bit is write accessible only to the UserCore.

ADCC (12h, 00h)	**Analog-to-Digital Clock Correction Register**
Initialization:	This register is reset to 0000h.
Read/Write Access:	Unrestricted read access.
ADCC.[15:0]:	**ADC Clock Correction Value 15:0.** This value reflects the count (measurement) of decoder sync bits during the predefined duration of 32kHz x 2^9 clocks for the decoder selected by CCSL[1:0]. The clock correction facility is enabled on any write to the CCSL[1:0] bits (other than the 11b disable request). The ADCC register reads 0000h to indicate a busy (measuring) condition until the measurement completes, at which point, the ADCC register is updated.

MSTC (13h, 00h)	**Manchester Decoder Status Register**
Initialization:	This register is reset to 30h.
Read/Write Access:	Unrestricted read access. Unrestricted write access to bits 5:4 (see description).
MSTC.0: MD0SNC	**Manchester Decoder 0 Synchronization Status Bit.** This bit reflects the synchronization status of Manchester decoder 0. When the decoder has achieved synchronization, this bit is set to 1. When the decoder cannot or has not yet detected the required alternating synchronization bit in the Manchester bit stream, this bit is cleared to 0. Once synchronized, loss of synchronization is signaled (i.e., bit is cleared) once three sync bit errors are detected in 10 frames. If fewer than three errors are detected in 10 frames, the synchronization bit error counter restarts on the next sync bit error.
MSTC.1: MD1SNC	**Manchester Decoder 1 Synchronization Status Bit.** This bit reflects the synchronization status of Manchester decoder 1. When the decoder has achieved synchronization, this bit is set to 1. When the decoder cannot or has not yet detected the required alternating synchronization bit in the Manchester bit stream, this bit is cleared to 0. Once synchronized, loss of synchronization is signaled (i.e., bit is cleared) once three sync bit errors are detected in 10 frames. If fewer than three errors are detected in 10 frames, the synchronization bit error counter restarts on the next sync bit error.
MSTC.2: MD2SNC	**Manchester Decoder 2 Synchronization Status Bit.** This bit reflects the synchronization status of Manchester decoder 2. When the decoder has achieved synchronization, this bit is set to 1. When the decoder cannot or has not yet detected the required alternating synchronization bit in the Manchester bit stream, this bit is cleared to 0.
MSTC.3: Reserved	**Reserved.** Reads return 0.

Special Function Register Bit Descriptions (continued)

<table>
<tr><td>MSTC.[5:4]: CCSL[1:0]</td><td>Clock Correction Hardware Selection Bits 1:0. These bits are used to enable and assign the clock measurement hardware to one of the three Manchester decoders. When these bits are 11b, the clock measurement utility is disabled. Writing these bits to any other state enables one clock measurement interval. When the clock measurement interval is enabled, the ADCC output register is cleared to 0000h to indicate a busy (measuring) condition. No hardware protection is in place to prevent attempts to measure a disabled decoder, which would result in seeing a persistent busy (ADCC = 0000h) condition. The table below summarizes the measurement options.

Separate physical implementations of these two control bits exist for the UserCore and the DSPCore. The ENDSP bit controls which bits are used to control the clock correction measurement hardware. When ENDSP = 0, the UserCore CCSL[1:0] bits control the hardware. When ENDSP = 1, the DSPCore CCSL[1:0] bits control the hardware. The bits not being used by the hardware are still write accessible but have no effect on the hardware. Once a clock measurement is requested, a second request should not be issued from the other core. There is no need for hardware protection against this possibility; the ADCC register can be polled to ascertain the busy status.
<table>
<tr><th>CCSL[1:0]</th><th>CLOCK MEASUREMENT (SYNC BIT FREQUENCY)</th></tr>
<tr><td>00b</td><td>Decoder 0</td></tr>
<tr><td>01b</td><td>Decoder 1</td></tr>
<tr><td>10b</td><td>Decoder 2</td></tr>
<tr><td>11b</td><td>Disabled</td></tr>
</table>
</td></tr>
<tr><td>MSTC.[7:6]: Reserved</td><td>Reserved. Reads return 0.</td></tr>
</table>

PO0 (00h, 01h) *Initialization:* *Read/Write Access:*	**Port 0 Output Register (8-Bit Register)** This register is set to 0FFh on all forms of reset. Unrestricted read/write.
PO0.[7:0]:	**Port 0 Output Register Bits 7:0.** The PO0 register stores output data for port 0 when it is defined as an output port and controls whether the internal weak p-channel pullup transistor is enabled/disabled if a port pin is defined as an input. The contents of this register can be modified by a write access. Reading from the register returns the contents of the register. Changing the direction of port 0 does not change the data contents of the register.

PO1 (01h, 01h) *Initialization:* *Read/Write Access:*	**Port 1 Output Register (8-Bit Register)** This register is set to 07Fh on all forms of reset. Unrestricted read/write.
PO1.[6:0]:	**Port 1 Output Register Bits 6:0.** The PO1 register stores output data for port 1 when it is defined as an output port and controls whether the internal weak p-channel pullup transistor is enabled/disabled if a port pin is defined as an input. The contents of this register can be modified by a write access. Reading from the register returns the contents of the register. Changing the direction of port 1 does not change the data contents of the register. Special note about P1.6: The $\overline{RST}$ input function remains enabled on P1.6 unless it is explicitly disabled (RSTD = 1). This means that the ports control bits (PD, PO) can be used to generate a reset (e.g., by driving the pin low).
PO1.7: Reserved	**Reserved.** Reads return 0.

Special Function Register Bit Descriptions (continued)

PI0 (02h, 01h)	**Port 0 Input Register**
Initialization:	The reset value for this register is dependent on the logical states of the pins.
Read/Write Access:	Unrestricted read-only.
PI0.[7:0]:	**Port 0 Input Register Bits 7:0.** The PI0 register always reflects the logic state of its pins when read. Note that each port pin has a weak pullup circuit when functioning as an input and the p-channel pullup transistor is controlled by its respective PO bits. If the PO bit is set to 1, the weak pullup is on, if the PO bit is cleared to 0, the weak pullup is off and forces the port pin into three-state.

PI1 (03h, 01h)	**Port 1 Input Register**
Initialization:	The reset value for this register is 0ssssssb, where “s” depends on the logical state of the pin.
Read/Write Access:	Unrestricted read.
PI1.[6:0]:	**Port 1 Input Register Bits 6:0.** The PI1 register always reflects the logic state of its pins when read. Note that each port pin has a weak pullup circuit when functioning as an input and the p-channel pullup transistor is controlled by its respective PO bits. If the PO bit is set to 1, the weak pullup is on, if the PO bit is cleared to 0, the weak pullup is off and forces the port pin into three-state.
PI1.7: Reserved	**Reserved.** Read returns 0.

EIF0 (04h, 01h)	**External Interrupt Flag 0 Register**
Initialization:	EIF0 is cleared to 00h on all forms of reset.
Read/Write Access:	Unrestricted read/write.
EIF0.[7:0]: IE[7:0]	**Interrupt Edge Detect Bits 7:0.** These bits are set when a negative edge (ITx = 1) or a positive edge (ITx = 0) is detected on the interrupt x pin. Setting any of the bits to 1 generates an interrupt to the CPU if the corresponding interrupt is enabled. This bit remains set until cleared by software or a reset. It must be cleared by software before exiting the interrupt source routine or another interrupt is generated as long as the bit remains set.

EIE0 (05h, 01h)	**External Interrupt Enable 0 Register**
Initialization:	EIE0 is cleared to 00h on all forms of reset.
Read/Write Access:	Unrestricted read/write.
EIE0.[7:0]: EX[7:0]	**Enable External Interrupt Bits 7:0.** Setting any of these bits to 1 enables the corresponding external interrupt. Clearing any of the bits to 0 disables the corresponding interrupt function.

EIF1 (06h, 01h)	**External Interrupt Flag 1 Register**
Initialization:	EIF1 is cleared to 00h on all forms of reset.
Read/Write Access:	Unrestricted read/write.
EIF1.[3:0]: IE[11:8]	**Interrupt Edge Detect Bits 11:8.** These bits are set when a negative edge (ITx = 1) or a positive edge (ITx = 0) is detected on the interrupt x pin. Setting any of the bits to 1 generates an interrupt to the CPU if the corresponding interrupt is enabled. This bit remains set until cleared by software or a reset. It must be cleared by software before exiting the interrupt source routine or another interrupt is generated as long as the bit remains set.
EIF1.[7:4]: Reserved	**Reserved.** Reads return 0.

Low-Power, Dual-Core Microcontroller

Special Function Register Bit Descriptions (continued)

EIE1 (07h, 01h)	**External Interrupt Enable 1 Register**
Initialization:	EIE1 is cleared to 00h on all forms of reset.
Read/Write Access:	Unrestricted read/write.
EIE1.[3:0]: EX[11:8]	**Enable External Interrupt Bits 11:8.** Setting any of these bits to 1 enables the corresponding external interrupt. Clearing any of the bits to 0 disables the corresponding interrupt function.
EIE1.[7:4]: Reserved	**Reserved.** Reads return 0.

PD0 (08h, 01h)	**Port 0 Direction Register**
Initialization:	This register is cleared to 00h on all forms of reset.
Read/Write Access:	Unrestricted read/write.
PD0.[7:0]:	**Port 0 Direction Register Bits 7:0.** PD0 is used to determine the direction of the Port 0 function. The port pins are independently controlled by their direction bits. When a bit is set to 1, its corresponding pin is used as an output; data in the PO register is driven on the pin. When a bit is cleared to 0, its corresponding pin is used as an input, and allows an external signal to drive the pin. Note that each port pin has a weak pullup circuit when functioning as an input and the p-channel pullup transistor is controlled by its respective PO bits. If the PO bit is set to 1, the weak pullup is on; if the PO bit is cleared to 0, the weak pullup is off and forces the port pin into three-state.

PD1 (09h, 01h)	**Port 1 Direction Register**
Initialization:	This register is cleared to 00h on all forms of reset.
Read/Write Access:	Unrestricted read/write.
PD1.[6:0]:	**Port 1 Direction Register Bits 6:0.** PD1 is used to determine the direction of the port 1 function. The port pins are independently controlled by their direction bit. When a bit is set to 1, its corresponding pin is used as an output; data in the PO register is driven on the pin. When a bit is cleared to 0, its corresponding pin is used as an input, and allows an external signal to drive the pin. Note that each port pin has a weak pullup circuit when functioning as an input and the p-channel pullup transistor is controlled by its respective PO bits. If the PO bit is set to 1, the weak pullup is on; if the PO bit is cleared to 0, the weak pullup is off and forces the port pin into three-state. Special note about P1.6: The $\overline{RST}$ input function remains enabled on P1.6 unless it is explicitly disabled (RSTD = 1). This means that the ports control bits (PD, PO) can be used to generate a reset (e.g., by driving the pin low).
PD1.7: Reserved	**Reserved.** Reads return 0.

EIES0 (0Ah, 01h)	**External Interrupt Edge Select 0 Register**
Initialization:	EIES0 is cleared to 00h on all forms of reset.
Read/Write Access:	Unrestricted read/write.
EIES0.[7:0]: IT[7:0]	**Edge Select for External Interrupt Bits 7:0** ITx = 0: External interrupt x is positive-edge triggered. ITx = 1: External interrupt x is negative-edge triggered.

Special Function Register Bit Descriptions (continued)

EIES1 (0Bh, 01h) *Initialization:* *Read/Write Access:*	**External Interrupt Edge Select 1 Register** EIES1 is cleared to 00h on all forms of reset. Unrestricted read/write.
EIES1.[3:0]: IT[11:8]	**External Interrupt Edge Select Bits 11:8** ITx = 0: External interrupt x is positive-edge triggered. ITx = 1: External interrupt x is negative-edge triggered.
EIES1.[7:4]: Reserved	**Reserved.** Reads return 0.

SVM (0Ch, 01h) *Initialization:* *Read/Write Access:*	**Supply Voltage Monitor Register (16-Bit Register)** This register is set to 0700h on all forms of reset. Unrestricted read/write except SVMRDY and SVMTH. The supply voltage monitor ready (SVMRDY) bit is set and cleared by hardware only. SVMTH can only be written to when the supply voltage monitor is disabled (SVMEN = 0).
SVM.0: SVMEN	**Supply Voltage Monitor Enable.** Setting this bit to 1 enables the monitoring of supply voltage according to SVMTH settings. Clearing this bit to 0 disables the supply voltage monitoring circuitry.
SVM.1: SVMRDY	**Supply Voltage Monitor Ready.** This bit is set to 1 to indicate that the supply voltage monitor is ready for use. This bit is cleared to 0 when SVMEN = 0 or on entrance to stop mode if SVMSTOP = 0.
SVM.2: SVMIE	**Supply Voltage Monitor Interrupt Enable.** Setting this bit to 1 generates an interrupt to the CPU when SVMI is set to 1. Clearing this bit to 0 disables the interrupt from generating.
SVM.3: SVMI	**Supply Voltage Monitor Interrupt.** This bit is set to 1 when the supply voltage falls below the set point defined by SVTH. Clearing this bit to 0 clears the interrupt. However, if the supply voltage is still below the set point, this flag is set again. Setting this bit to 1 causes an interrupt to the CPU when SVMIE = 1.
SVM.4: SVMSTOP	**Supply Voltage Monitor Stop Mode Enable.** Setting this bit to 1 enables the supply voltage monitor circuit to operate during stop mode if SVMEN = 1. Clearing this bit to 0 disables the supply voltage monitor when stop mode is enabled.
SVM.[7:5]: Reserved	**Reserved.** Reads return 0.
SVM.[11:8]: SVTH[3:0]	**Supply Voltage Threshold Bits [3:0].** These bits are used to select a user-defined supply voltage threshold under which an interrupt is generated to the CPU if enabled. The level can be adjusted from 2.0V to 3.5V in a 0.1V increment. The supply voltage monitor is enabled by setting SVMEN = 1. The default value is 07h (2.7V). Supply Voltage Monitor Threshold = 2.0V + SVMTH[3:0] x 0.1V Note that the SVTH bits can only be modified when SVMEN = 0. Writing to these bits is ignored if SVMEN = 1.
SVM.[15:12]: Reserved	**Reserved.** Reads return 0.