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MAXQ612/MAXQ622

16-Bit Microcontrollers with Infrared Module and Optional USB

General Description

The MAXQ612/MAXQ622 are low-power, 16-bit MAXQ® microcontrollers designed for low-power applications including universal remote controls, consumer electronics, and white goods. Both devices use a low-power, high-throughput, 16-bit RISC microcontroller. Serial peripherals include two universal synchronous/asynchronous receiver-transmitters (USARTs), two SPI™ master/slave communications ports, and an inter-integrated circuit (I^2C) bus. The devices also incorporate an IR module with carrier frequency generation and flexible port I/O capable of multiplexed keypad control. The MAXQ622 adds a universal serial bus (USB) with integrated physical interface (PHY).

The MAXQ612/MAXQ622 include 128KB of flash memory and 6KB of data SRAM. Intellectual property (IP) protection is provided by a secure memory management unit (MMU) that supports multiple application privilege levels and protects code against copying and reverse engineering. Privilege levels enable vendors to provide libraries and applications to execute on the MAXQ612/MAXQ622, while limiting access to only data and code allowed by their privilege level.

For the ultimate in low-power battery-operated performance, the devices include an ultra-low-power stop mode (0.3µA typical). In this mode, the minimum amount of circuitry is powered. Wake-up sources include external interrupts, the power-fail interrupt, and a timer interrupt. The microcontroller runs from a wide operating voltage of 1.70V to 3.6V, and can also be powered from the USB.

Applications

Remote Controls

Battery-Powered Portable Equipment

Consumer Electronics

Home Appliances

White Goods

***Ordering Information/Selector Guide* appears at end of data sheet.**

MAXQ is a registered trademark of Maxim Integrated Products, Inc. SPI is a trademark of Motorola, Inc.

Features

- **High-Performance, Low-Power, 16-Bit RISC Core**
- **DC to 12MHz Operation Across Entire Operating Range**
- **1.70V to 3.6V Operating Voltage**
- **Can Be Powered from Battery (V_{DD}) or USB (V_{DDB})**
- **33 Total Instructions for Simplified Programming**
- **Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement**
- **Dedicated Pointer for Direct Read from Code Space**
- **16-Bit Instruction Word, 16-Bit Data Bus**
- **16 x 16-Bit General-Purpose Working Registers**
- **Secure MMU for Application Partitioning and IP Protection**
- **Memory Features**
  - **128KB Flash Memory**
    - **512-Byte Sectors**
    - **20,000 Erase/Write Cycles per Sector**
  - **6KB Data SRAM**
- **USB Features (MAXQ622 Only)**
  - **USB 2.0 Full-Speed Compatible**
  - **Hardware Receive and Transmit Buffers for High Throughput**
  - **Integrated Full-Speed Transceiver**
  - **On-Chip Termination and Pullup Resistors**
- **Additional Peripherals**
  - **Power-Fail Warning**
  - **Power-On Reset (POR)/Brownout Reset**
  - **Automatic IR Carrier Frequency Generation and Modulation**
  - **Two 16-Bit Programmable Timers/Counters with Prescaler and Capture/Compare**
  - **Two SPI Communication Ports**
  - **Two USART Communication Ports**
  - **I^2C Port**
  - **Programmable Watchdog Timer**
  - **8kHz Nanopower Ring Oscillator Wake-Up Timer**
  - **Up to 56 General-Purpose I/O**
- **Low Power Consumption**
  - **0.3µA (typ), 3µA (max) in Stop Mode**
    T_A = +25°C, Power-Fail Monitor Disabled
  - **4.8mA (typ) at 12MHz, 520µA (typ) at 1MHz in Active Mode**

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maximintegrated.com/errata.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5117; Rev 2; 5/11

16-Bit Microcontrollers with Infrared Module and Optional USB

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Voltage Range on Any Lead with
Respect to GND Except V_{BUS}..... -0.3V to (V_{DD} + 0.5V)
Voltage Range on V_{BUS} with Respect to GND....-0.3V to +6.0V
Continuous Output Current
Any Single I/O Pin.....25mA
All I/O Pins Combined.....25mA
Voltage Range on DP, DM with
Respect to GND.....-0.3V to (V_{BUS} + 0.3V)
Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			V_{RST}		3.6	V
1.8V Internal Regulator	V_{REG18}			1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply	V_{PFW}	Monitors V_{DD} (Notes 2, 3, 4)		1.75	1.8	1.85	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD} (Note 5)		1.64	1.67	1.70	V
POR Voltage	V_{POR}	Monitors V_{DD}		1.0		1.42	V
RAM Data-Retention Voltage	V_{DRV}	(Note 6)		1.0			V
Active Current	I_{DD_1}	Sysclk = 12MHz			4.8	5.5	mA
	I_{DD_2}	Sysclk = 1MHz (Note 6)			0.52	0.8	
Stop-Mode Current	I_{S1}	Power-Fail Off (Note 7)	T_A = +25°C		0.3	3	µA
			T_A = +70°C		2.8	13	
	I_{S2}	Power-Fail On	T_A = +25°C		24	30	
			T_A = +70°C		30	40	
Current Consumption During Power Fail	I_{PFR}	(Notes 6, 8, 9)		[(3 x I_{S2}) + ((PCI - 3) x (I_{S1} + I_{NANO}))]/ PCI			µA
Current Consumption During POR	I_{POR}	(Note 10)			100		nA
Stop-Mode Resume Time	t_{ON}				375 + 8192 t_{HFXIN}		µs
Power-Fail Monitor Startup Time	t_{PFM_ON}	(Note 6)				150	µs
Power-Fail Warning Detection Time	t_{PFW}	(Notes 6, 11)		10			µs
Input Low Voltage for IRTX, IRRX, $\overline{RESET}$, and All Port Pins	V_{IL}			V_{GND}		0.3 x V_{DD}	V
Input High Voltage for IRTX, IRRX, $\overline{RESET}$, and All Port Pins	V_{IH}			0.7 x V_{DD}		V_{DD}	V

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Low Voltage for HFXIN	V_{IL_HFXIN}	External driven clock and not feedback connected crystal oscillator	V_{GND}		0.3 x V_{DD}	V
Input High Voltage for HFXIN	V_{IH_HFXIN}	External driven clock and not feedback connected crystal oscillator	0.7 x V_{DD}		V_{DD}	V
IRRX Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
Output Low Voltage for IRTX	V_{OL_IRTX}	V_{DD} = 3.6V, I_{OL} = 25mA (Note 6)			1.0	V
		V_{DD} = 2.35V, I_{OL} = 10mA (Note 6)			1.0	
		V_{DD} = 1.85V, I_{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{RESET}$ and All Port Pins (Note 12)	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA (Note 6)		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA (Note 6)		0.4	0.5	
		V_{DD} = 1.85V, I_{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V_{OH}	I_{OH} = -2mA	V_{DDIO} - 0.5		V_{DDIO}	V
Input/Output Pin Capacitance for All Port Pins Except DP, DM	C_{IO}	(Note 6)			15	pF
Input Leakage Current	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{RESET}$, IRTX, IRRX, P0 to P6	R_{PU}	V_{DD} = 3V, V_{OL} = V_{DD}/2 (Note 6)	16	25	39	kΩ
		V_{DD} = 2V, V_{OL} = V_{DD}/2	17	27	41	
		V_{DD} = 3.0V, V_{OL} = 0.4V (Note 6)	16	28	39	
		V_{DD} = 2.0V, V_{OL} = 0.4V (Note 6)	17	30	41	
GPIO Supply Output High Voltage	V_{DDIOH}	V_{DDIOH} current is the sum of V_{DDIO} current and I_{OH} of all GPIO, I_{OH} = 10mA	V_{DD} - 0.4		V_{DD}	V
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f_{HFXIN}	(Note 13)	1		12	MHz
Crystal/Resonator Period	t_{HFXIN}			1/f_{HFXIN}		ns
Crystal/Resonator Warmup Time	t_{XTAL_RDY}	From initial oscillation		8192 x t_{HFXIN}		ms
Oscillator Feedback Resistor	R_{OSCF}	(Note 6)	0.5	1.0	1.5	MΩ
Crystal ESR		(Note 6)			60	Ω
EXTERNAL CLOCK INPUT						
External Clock Frequency	f_{XCLK}	(Note 13)	DC		12	MHz
External Clock Period	t_{XCLK}			1/f_{XCLK}		ns
External Clock Duty Cycle	t_{XCLK_DUTY}		45		55	%
System Clock Frequency	f_{CK}			f_{HFXIN}		MHz
		HFXOUT = GND		f_{XCLK}		

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Period	t_{CK}			$1/f_{CK}$		ns
NANOPOWER RING						
Nanopower Ring Frequency	f_{NANO}	T_A = +25°C	3	13	20	kHz
		T_A = +25°C, V_{DD} = POR voltage (Note 6)	1.7	2.4		
Nanopower Ring Duty Cycle	t_{NANO}	(Note 6)	40		60	%
Nanopower Ring Current	I_{NANO}	Typical at V_{DD} = 1.64V, T_A = +25°C (Note 6)		40	400	nA
WAKE-UP TIMER						
Wake-Up Timer Interval	t_{WAKEUP}		$1/f_{NANO}$		$65,535/f_{NANO}$	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	$f_{FPSYSCLK}$		1			MHz
Flash Erase Time	t_{ME}	Mass erase	20		40	ms
	t_{ERASE}	Page erase	20		40	
Flash Programming Time per Word	t_{PROG}	(Note 14)	20		100	µs
Write/Erase Cycles			20,000			Cycles
Data Retention		T_A = +25°C	100			Years
USB						
USB Supply Voltage	V_{BUS}	(Note 15)	4.5	5.0	5.5	V
V_{BUS} Supply Current (Note 16)	I_{VBUS}	Transmitting on DP and DM at 12Mbps, C_L = 50pF on DP and DM to GND, FRCVDD = 0			13.5	mA
		Transmitting on DP and DM at 12Mbps, C_L = 50pF on DP and DM to GND, FRCVDD = 1			3.5	mA
V_{BUS} Supply Current During Idle (Note 16)	I_{VBUSID}	DP = high, DM = low, FRCVDD = 0 (Note 6)			6	mA
		DP = high, DM = low, FRCVDD = 1			0.2	mA
V_{BUS} Suspend Supply Current	$I_{VBUSSUS}$				500	µA
Single-Ended Input High Voltage DP, DM	V_{IHD}		2.0			V
Single-Ended Input Low Voltage DP, DM	V_{ILD}				0.8	V
Output Low Voltage DP, DM	V_{OLD}	R_L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V_{OHD}	R_L = 15kΩ from DP and DM to GND	2.8			V
Differential Input Sensitivity DP, DM	V_{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Receiver Threshold	V_{SE}		0.8		2.0	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	C_L = 50pF (Note 6)	1.3		2.0	V
DP, DM Off-State Input Impedance	R_{LZ}		300			kΩ
Driver Output Impedance	R_{DRV}	Steady-state drive	28		44	Ω
DP Pullup Resistor	R_{PU}	Idle	0.9		1.575	kΩ
		Receiving	1.425		3.090	
USB TIMING						
DP, DM Rise Time (Transmit)	t_R	C_L = 50pF	4		20	ns
DP, DM Fall Time (Transmit)	t_F	C_L = 50pF	4		20	ns
Rise/Fall Time Matching (Transmit)	t_R/t_F	C_L = 50pF (Note 6)	90		110	%
IR						
Carrier Frequency	f_{IR}				$f_{CK}/2$	Hz
SPI (Note 6)						
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{CK}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{CK}/4$	MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, pullup = 560Ω	8		24	ns
SCLK_ Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MOSI_ Output Hold Time After SCLK_ Sample Edge	t_{MOH}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MOSI_ Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MISO_ Input Valid to SCLK_ Sample Edge Rise/Fall Setup	t_{MIS}		25			ns
MISO_ Input to SCLK_ Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK_ Inactive to MOSI_ Inactive	t_{MLH}		$t_{MCK}/2$ - t_{SPI_RF}			ns
SCLK_ Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
$\overline{SSEL}$_ Active to First Shift Edge	t_{SSE}		t_{SPI_RF}			ns

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI_ Input to SCLK_ Sample Edge Rise/Fall Setup	t_{SIS}		t_{SPI_RF}			ns
MOSI_ Input from SCLK_ Sample Edge Transition Hold	t_{SIH}		t_{SPI_RF}			ns
MISO_ Output Valid After SCLK_ Shift Edge Transition	t_{SOV}				50	ns
$\overline{SSEL}$_ Inactive	t_{SSH}		t_{CK} + t_{SPI_RF}			ns
SCLK_ Inactive to $\overline{SSEL}$_ Rising	t_{SD}		t_{SPI_RF}			ns
MISO_ Output Disabled After $\overline{SSEL}$_ Edge Rise	t_{SLH}				$2t_{CK}$ + $2t_{SPI\_RF}$	ns

I²C ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V, T_A = 0°C to +70°C.) (Note 1, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Input Low Voltage	V_{IL_I2C}	(Note 18)	-0.5	0.3 x V_{DD}	-0.5	0.3 x V_{DD}	V
Input High Voltage	V_{IH_I2C}	(Note 18)	0.7 x V_{DD}		0.7 x V_{DD}	V_{DD} + 0.5V	V
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	V_{DD} > 2V			0.05 x V_{DD}		V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DD} > 2V, 3mA sink current	0	0.4	0	0.4	V
Output Fall Time from V_{IH_MIN} to V_{IL_MAX} with Bus Capacitance from 10pF to 400pF	t_{OF_I2C}	(Notes 19, 20)		250	20 + 0.1C_B	250	ns
Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter	t_{SP_I2C}				0	50	ns
Input Current on I/O	I_{IN_I2C}	Input voltage from 0.1 x V_{DD} to 0.9 x V_{DD}	-10	+10	-10	+10	µA
I/O Capacitance	C_{IO_I2C}			10		10	pF

I²C BUS CONTROLLER TIMING

(Notes 6, 21) (Figure 2)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
I²C Bus Operating Frequency	f_{I2C}	0	100	0	400	kHz
System Frequency	f_{SYS}	0.90		3.60		MHz
I²C Bit Rate	f_{I2C}		$f_{SYS}/8$		$f_{SYS}/8$	Hz
Hold Time After (Repeated) START	$t_{HD:STA}$	4.0		0.6		µs
Clock Low Period	t_{LOW_I2C}	4.7		1.3		µs
Clock High Period	t_{HIGH_I2C}	4.0		0.6		µs
Setup Time for Repeated START	$t_{SU:STA}$	4.7		0.6		µs
Hold Time for Data (Notes 22, 23)	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Setup Time for Data (Note 24)	$t_{SU:DAT}$	250		100		ns
SDA/SCL Fall Time (Note 20)	t_{F_I2C}		300	$20 + 0.1C_B$	300	ns
SDA/SCL Rise Time (Note 20)	t_{R_I2C}		1000	$20 + 0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$	4.0		0.6		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nL_I2C}	$0.1 \times V_{DD}$		$0.1 \times V_{DD}$		V
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nH_I2C}	$0.2 \times V_{DD}$		$0.2 \times V_{DD}$		V

Note 1: Specifications to 0°C are guaranteed by design and are not production tested.

Note 2: V_{PFW} can be programmed to the following nominal voltage trip points: 1.8V, 1.9V, 2.55V, and 2.75V ±3%. The values listed in the *Recommended Operating Conditions* table are for the default configuration of 1.8V nominal.

Note 3: It is not recommended to write to flash when the supply voltage drops below the power-fail warning levels, as there is uncertainty in the duration of continuous power supply. The user application should check the status of the power-fail warning flag before writing to flash to ensure complete write operations.

Note 4: The power-fail warning monitor and the power-fail reset monitor are designed to track each other with a minimum delta between the two of 0.11V.

Note 5: The power-fail reset and POR detectors are designed to operate in tandem to ensure that one or both of these signals is active at all times when $V_{DD} < V_{RST}$, ensuring the device maintains the reset state until minimum operating voltage is achieved.

Note 6: Guaranteed by design and not production tested.

Note 7: I_{S1} is measured with the USB data RAM powered down.

Note 8: The power-check interval (PCI) can be set to always on, or to 1024, 2048, or 4096 nanopower ring clock cycles.

Note 9: Measured on the V_{DD} pin and the device not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current. The device is executing code from flash memory.

Note 10: Current consumption during POR when powering up while V_{DD} is less than the POR release voltage.

Note 11: The minimum amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected.

Note 12: The maximum total current, $I_{OH(MAX)}$ and $I_{OL(MAX)}$, for all listed outputs combined should not exceed 25mA to satisfy the maximum specified voltage drop. This does not include the IRTX output.

Note 13: External clock frequency must be 12MHz to support USB functionality. Full-speed USB(12Mbps)-required bit-rate accuracy is ±2500ppm or ±0.25%. This is inclusive of all potential error sources: frequency tolerance, temperature, aging, crystal capacitive loading, board layout, etc.

Note 14: Programming time does not include overhead associated with utility ROM interface.

Note 15: For USB operation, both V_{DD} and V_{BUS} must be connected.

Note 16: FRCVDD is the force V_{DD} power-supply bit (PWCN.10). When FRCVDD = 1, V_{DDB} power switching is disabled, and V_{DD} is always used as the core 3V power supply.

Note 17: The ESD protection scheme is in production on existing parts. The 1µF capacitor on V_{BUS} is intended to protect that pin from ESD damage (rather than DP or DM) since it is externally exposed. The ESD test uses 150pF charged to 15kV applied to the 1µF capacitor creating a delta V of approximately 2.25V and limiting the voltage on V_{BUS}.

Note 18: Devices that use nonstandard supply voltages that do not conform to the intended I^2C bus system levels must relate their input levels to the voltage to which the pullup resistors R_P are connected.

Note 19: The maximum fall time, t_{F_I2C} of 300ns for the SDA and SCL bus lines is longer than the specificed maximum t_{OF_I2C} of 250ns for the output stages. This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in *I^2C Bus Controller Timing* without exceeding the maximum specified fall time.

Note 20: C_B = Capacitance of one bus line in pF.

Note 21: All values referred to $V_{IH\_I2C(MIN)}$ and $V_{IL\_I2C\ (MAX)}$.

Note 22: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\_I2C(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 23: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW_I2C}) of the SCL signal.

Note 24: A fast-mode I^2C bus device can be used in a standard-mode I^2C bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\_I2C(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ (according to the standard-mode I^2C specification) before the SCL line is released.

Note 25: AC electrical specifications are guaranteed by design and are not production tested.

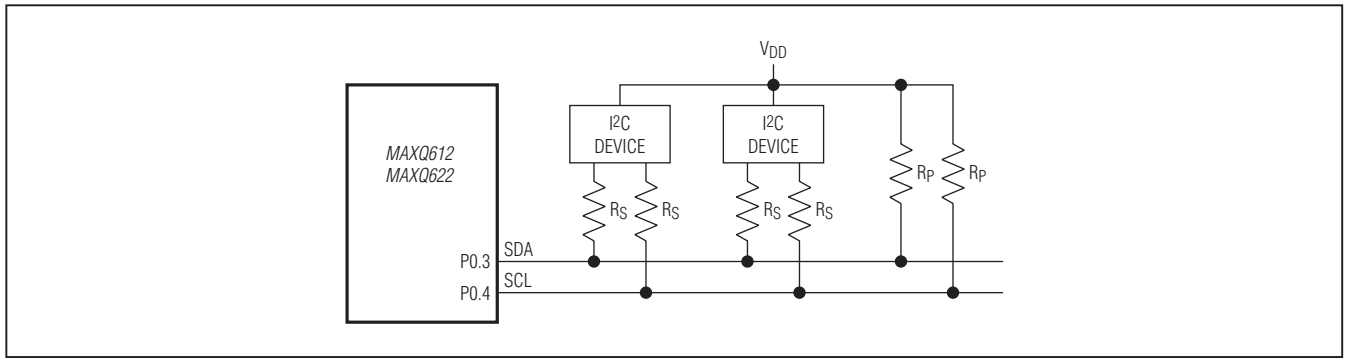


Figure 1. Series Resistors (R_S) for Protecting Against High-Voltage Spikes

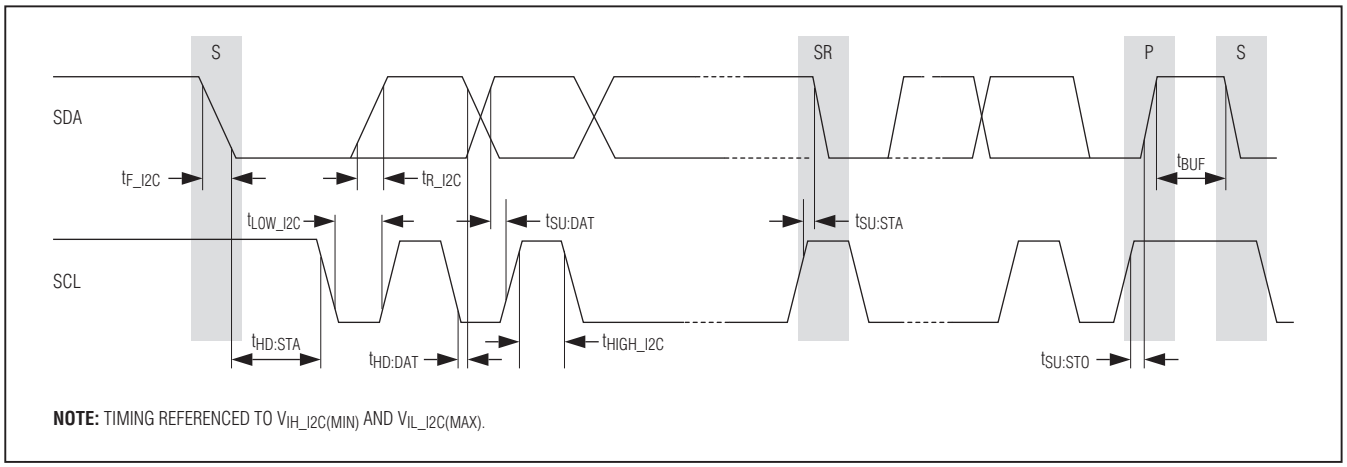
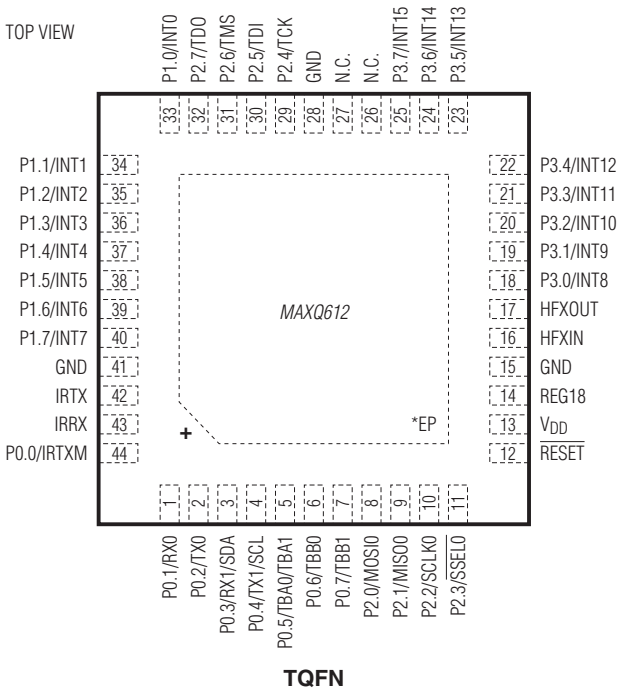


Figure 2. I^2C Bus Controller Timing Diagram

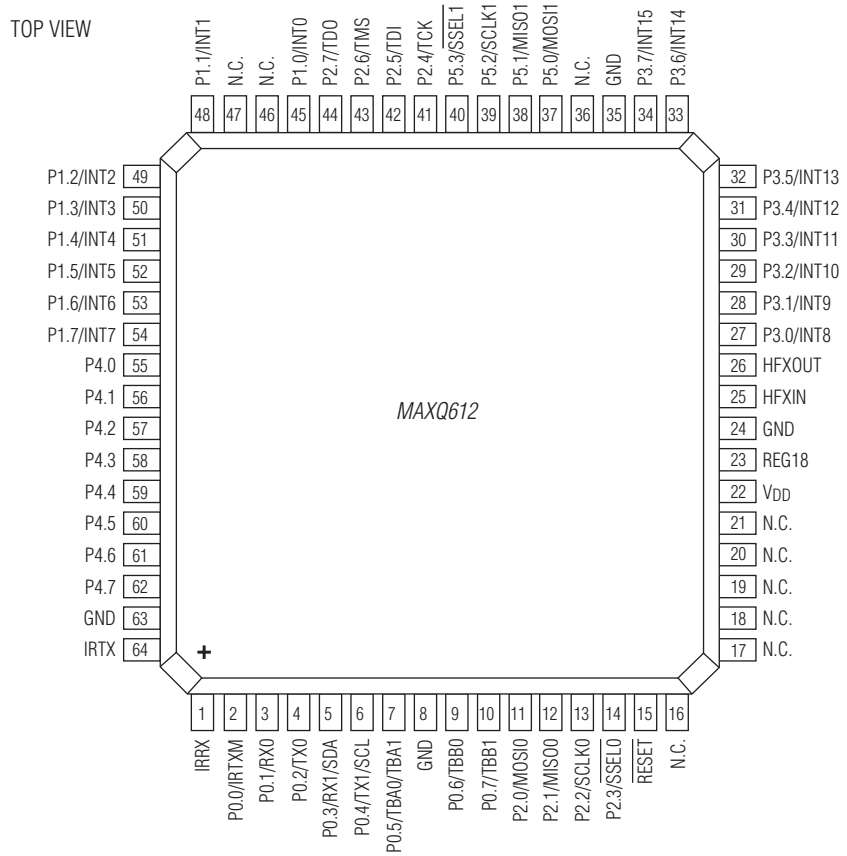
Pin Configurations



TQFN

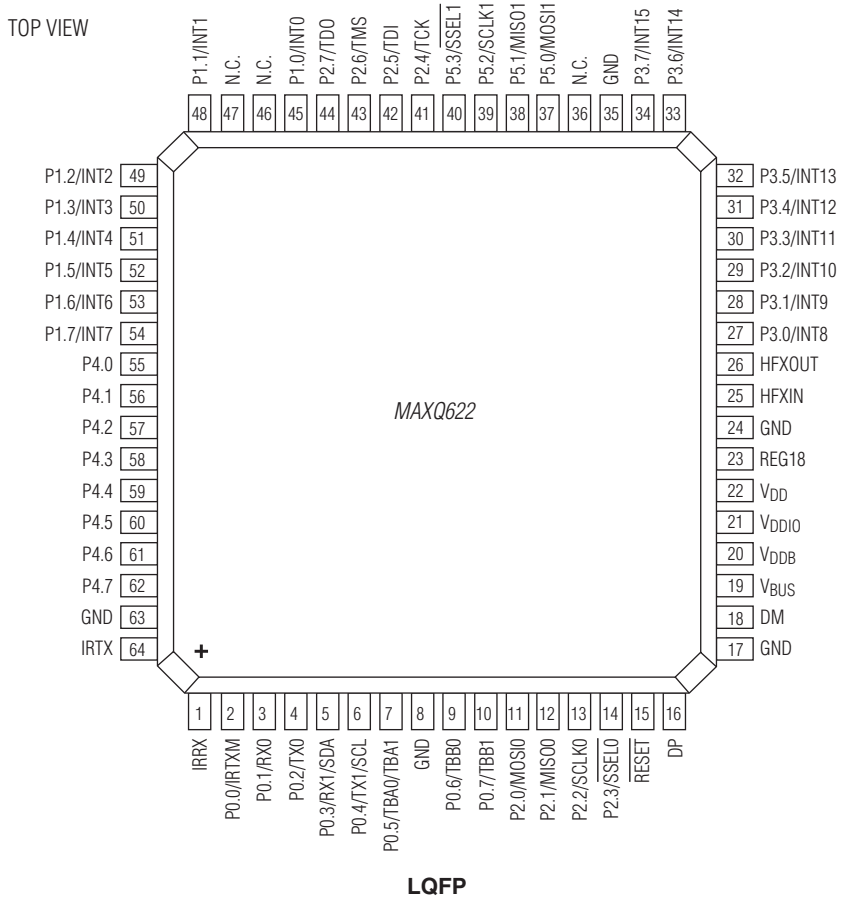
*EXPOSED PAD.

Pin Configurations (continued)



LQFP

Pin Configurations (continued)



LQFP

Pin Descriptions—TQFN, LQFP

PIN			NAME	FUNCTION
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP		
POWER PINS				
13	22	22	V_{DD}	Supply Voltage
15, 28, 41	8, 24, 35, 63	8, 17, 24, 35, 63	GND	Ground
14	23	23	REG18	Regulator Capacitor. This pin must be connected to ground through a 1.0µF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.

Pin Descriptions—TQFN, LQFP (continued)

PIN			NAME	FUNCTION
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP		
RESET PINS				
12	15	15	$\overline{\text{RESET}}$	Digital, Active-Low, Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS				
16	25	25	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is shorted to ground during POR.
17	26	26	HFXOUT	
USB FUNCTION PINS				
—	—	19	V_{BUS}	USB V_{BUS} Supply Voltage. Connect V_{BUS} to a positive 5.0V power supply. Bypass V_{BUS} to ground with a 1.0µF ceramic capacitor as close to the V_{BUS} pin as possible.
—	—	16	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	18	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	20	V_{DDB}	USB Transceiver Supply Voltage. This is the power output of the internal voltage regulator that is used for the USB transceiver (3.3V) block. This pin is bypassed to ground with a 1.0µF capacitor as close as possible to the package. No external circuitry should be powered from this pin.
—	—	21	V_{DDIO}	Switched 3V Power Supply. This is the power output after selection between V_{BUS} and V_{DD}. Must be connected to an external ceramic chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.
IR FUNCTION PINS				
42	64	64	IRTX	IR Transmit Output. Active-low IR transmit pin capable of sinking 25mA. This pin defaults to three-state input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the three-state input condition.
43	1	1	IRRX	IR Receive Input

Pin Descriptions—TQFN, LQFP (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th></tr>
<tr><td colspan="6">GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS</td></tr>
<tr><td rowspan="9">44, 1–7</td><td rowspan="9">2–7, 9, 10</td><td rowspan="9">2–7, 9, 10</td><td rowspan="9">P0.0–P0.7; IRTXM, RX0, TX0, RX1, TX1, SDA, SCL, TBA0, TBA1, TBB0, TBB1</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software.
MAXQ612 TQFN-EP | MAXQ612 LQFP | MAXQ622 LQFP | PORT | SPECIAL FUNCTION</td></tr>
<tr><td>44 | 2 | 2 | P0.0 | IRTXM</td></tr>
<tr><td>1 | 3 | 3 | P0.1 | RX0</td></tr>
<tr><td>2 | 4 | 4 | P0.2 | TX0</td></tr>
<tr><td>3 | 5 | 5 | P0.3 | RX1/SDA</td></tr>
<tr><td>4 | 6 | 6 | P0.4 | TX1/SCL</td></tr>
<tr><td>5 | 7 | 7 | P0.5 | TBA0/TBA1</td></tr>
<tr><td>6 | 9 | 9 | P0.6 | TBB0</td></tr>
<tr><td>7 | 10 | 10 | P0.7 | TBB1</td></tr>
<tr><td rowspan="9">33–40</td><td rowspan="9">45, 48–54</td><td rowspan="9">45, 48–54</td><td rowspan="9">P1.0–P1.7; INT0–INT7</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.
MAXQ612 TQFN-EP | MAXQ612 LQFP | MAXQ622 LQFP | PORT | SPECIAL FUNCTION</td></tr>
<tr><td>33 | 45 | 45 | P1.0 | INT0</td></tr>
<tr><td>34 | 48 | 48 | P1.1 | INT1</td></tr>
<tr><td>35 | 49 | 49 | P1.2 | INT2</td></tr>
<tr><td>36 | 50 | 50 | P1.3 | INT3</td></tr>
<tr><td>37 | 51 | 51 | P1.4 | INT4</td></tr>
<tr><td>38 | 52 | 52 | P1.5 | INT5</td></tr>
<tr><td>39 | 53 | 53 | P1.6 | INT6</td></tr>
<tr><td>40 | 54 | 54 | P1.7 | INT7</td></tr>
</table>

Pin Descriptions—TQFN, LQFP (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th></tr>
<tr><td rowspan="11">8–11, 29–32</td><td rowspan="11">11–14, 41–44</td><td rowspan="11">11–14, 41–44</td><td rowspan="11">P2.0–P2.7; MOSI0, MISO0, SCLK0, $\overline{SSEL0}$, TCK, TDI, TMS, TDO</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. P2.0 to P2.3 default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin. The JTAG pins (P2.4 to P2.7) default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register.
P2.7 functions as the JTAG test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP's shift_IR or shift_DR states.</td></tr>
<tr><td><table>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>8</td><td>11</td><td>11</td><td>P2.0</td><td>MOSI0</td></tr>
<tr><td>9</td><td>12</td><td>12</td><td>P2.1</td><td>MISO0</td></tr>
<tr><td>10</td><td>13</td><td>13</td><td>P2.2</td><td>SCLK0</td></tr>
<tr><td>11</td><td>14</td><td>14</td><td>P2.3</td><td>$\overline{SSEL0}$</td></tr>
<tr><td>29</td><td>41</td><td>41</td><td>P2.4</td><td>TCK</td></tr>
<tr><td>30</td><td>42</td><td>42</td><td>P2.5</td><td>TDI</td></tr>
<tr><td>31</td><td>43</td><td>43</td><td>P2.6</td><td>TMS</td></tr>
<tr><td>32</td><td>44</td><td>44</td><td>P2.7</td><td>TDO</td></tr>
</table></td></tr>
<tr><td rowspan="11">18–25</td><td rowspan="11">27–34</td><td rowspan="11">27–34</td><td rowspan="11">P3.0–P3.7; INT8–INT15</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.</td></tr>
<tr><td><table>
<tr><th>MAXQ612 TQFN</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>18</td><td>27</td><td>27</td><td>P3.0</td><td>INT8</td></tr>
<tr><td>19</td><td>28</td><td>28</td><td>P3.1</td><td>INT9</td></tr>
<tr><td>20</td><td>29</td><td>29</td><td>P3.2</td><td>INT10</td></tr>
<tr><td>21</td><td>30</td><td>30</td><td>P3.3</td><td>INT11</td></tr>
<tr><td>22</td><td>31</td><td>31</td><td>P3.4</td><td>INT12</td></tr>
<tr><td>23</td><td>32</td><td>32</td><td>P3.5</td><td>INT13</td></tr>
<tr><td>24</td><td>33</td><td>33</td><td>P3.6</td><td>INT14</td></tr>
<tr><td>25</td><td>34</td><td>34</td><td>P3.7</td><td>INT15</td></tr>
</table></td></tr>
</table>

Pin Descriptions—TQFN, LQFP (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th></tr>
<tr><td rowspan="10">—</td><td rowspan="10">55-62</td><td rowspan="10">55–62</td><td rowspan="10">P4.0–P4.7</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.</td></tr>
<tr><td><table>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>—</td><td>55</td><td>55</td><td>P4.0</td><td>—</td></tr>
<tr><td>—</td><td>56</td><td>56</td><td>P4.1</td><td>—</td></tr>
<tr><td>—</td><td>57</td><td>57</td><td>P4.2</td><td>—</td></tr>
<tr><td>—</td><td>58</td><td>58</td><td>P4.3</td><td>—</td></tr>
<tr><td>—</td><td>59</td><td>59</td><td>P4.4</td><td>—</td></tr>
<tr><td>—</td><td>60</td><td>60</td><td>P4.5</td><td>—</td></tr>
<tr><td>—</td><td>61</td><td>61</td><td>P4.6</td><td>—</td></tr>
<tr><td>—</td><td>62</td><td>62</td><td>P4.7</td><td>—</td></tr>
</table></td></tr>
<tr><td rowspan="6">—</td><td rowspan="6">37–40</td><td rowspan="6">37–40</td><td rowspan="6">P5.0–P5.3; MOSI1, MISO1, SCLK1, $\overline{\text{SSEL1}}$</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.</td></tr>
<tr><td><table>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>—</td><td>37</td><td>37</td><td>P5.0</td><td>MOSI1</td></tr>
<tr><td>—</td><td>38</td><td>38</td><td>P5.1</td><td>MISO1</td></tr>
<tr><td>—</td><td>39</td><td>39</td><td>P5.2</td><td>SCLK1</td></tr>
<tr><td>—</td><td>40</td><td>40</td><td>P5.3</td><td>$\overline{\text{SSEL1}}$</td></tr>
</table></td></tr>
<tr><td colspan="5">NO CONNECTION PINS</td></tr>
<tr><td>26, 27</td><td>16–21, 36, 46, 47</td><td>36, 46, 47</td><td>N.C.</td><td>No Connection. Reserved for future use. Leave these pins unconnected.</td></tr>
<tr><td colspan="5">EXPOSED PAD</td></tr>
<tr><td>—</td><td>—</td><td>—</td><td>EP</td><td>Exposed Pad (TQFN Only). Connect EP to the ground plane.</td></tr>
</table>

Pin Descriptions—Bare Die

PIN		NAME	FUNCTION
MAXQ612	MAXQ622		
POWER PINS			
28	28	V_{DD}	Supply Voltage
8, 30, 45, 73	8, 23, 30, 45, 73	GND	Ground
29	29	REG18	Regulator Capacitor. This pin must be connected to ground through a 1.0µF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.
RESET PINS			
21	21	$\overline{RESET}$	Digital, Active-Low, Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS			
31	31	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is shorted to ground during POR.
32	32	HFXOUT	
USB FUNCTION PINS			
—	25	V_{BUS}	USB V_{BUS} Supply Voltage. Connect V_{BUS} to a positive 5.0V power supply. Bypass V_{BUS} to ground with a 1.0µF ceramic capacitor as close to the V_{BUS} pin as possible.
—	22	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	24	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	26	V_{DDB}	USB Transceiver Supply Voltage. This is the power output of the internal voltage regulator that is used for the USB transceiver (3.3V) block. This pin is bypassed to ground with a 1.0µF capacitor as close as possible to the package. No external circuitry should be powered from this pin.
—	27	V_{DDIO}	Switched 3V Power Supply. This is the power output after selection between V_{BUS} and V_{DD}. Must be connected to an external ceramic chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.

Pin Descriptions—Bare Die (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612</th><th>MAXQ622</th></tr>
<tr><td colspan="4">IR FUNCTION PINS</td></tr>
<tr><td>74</td><td>74</td><td>IRTX</td><td>IR Transmit Output. Active-low IR transmit pin capable of sinking 25mA. This pin defaults to three-state input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the three-state input condition.</td></tr>
<tr><td>75</td><td>75</td><td>IRRX</td><td>IR Receive Input</td></tr>
<tr><td colspan="4">GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS</td></tr>
<tr><td rowspan="10">1, 2, 3, 5, 6, 7, 9, 10</td><td rowspan="10">1, 2, 3, 5, 6, 7, 9, 10</td><td rowspan="10">P0.0–P0.7; IRTXM, RX0, TX0, RX1, TX1, SDA, SCL, TBA0, TBA1, TBB0, TBB1</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software.</td></tr>
<tr><td>
<table>
<tr><th>MAXQ612</th><th>MAXQ622</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>1</td><td>1</td><td>P0.0</td><td>IRTXM</td></tr>
<tr><td>2</td><td>2</td><td>P0.1</td><td>RX0</td></tr>
<tr><td>3</td><td>3</td><td>P0.2</td><td>TX0</td></tr>
<tr><td>5</td><td>5</td><td>P0.3</td><td>RX1/SDA</td></tr>
<tr><td>6</td><td>6</td><td>P0.4</td><td>TX1/SCL</td></tr>
<tr><td>7</td><td>7</td><td>P0.5</td><td>TBA0/TBA1</td></tr>
<tr><td>9</td><td>9</td><td>P0.6</td><td>TBB0</td></tr>
<tr><td>10</td><td>10</td><td>P0.7</td><td>TBB1</td></tr>
</table>
</td></tr>
<tr><td rowspan="10">55, 56, 58–63</td><td rowspan="10">55, 56, 58–63</td><td rowspan="10">P1.0–P1.7; INT0–INT7</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.</td></tr>
<tr><td>
<table>
<tr><th>MAXQ612</th><th>MAXQ622</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>55</td><td>55</td><td>P1.0</td><td>INT0</td></tr>
<tr><td>56</td><td>56</td><td>P1.1</td><td>INT1</td></tr>
<tr><td>58</td><td>58</td><td>P1.2</td><td>INT2</td></tr>
<tr><td>59</td><td>59</td><td>P1.3</td><td>INT3</td></tr>
<tr><td>60</td><td>60</td><td>P1.4</td><td>INT4</td></tr>
<tr><td>61</td><td>61</td><td>P1.5</td><td>INT5</td></tr>
<tr><td>62</td><td>62</td><td>P1.6</td><td>INT6</td></tr>
<tr><td>63</td><td>63</td><td>P1.7</td><td>INT7</td></tr>
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</td></tr>
</table>

Pin Descriptions—Bare Die (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th colspan="4">FUNCTION</th></tr>
<tr><th>MAXQ612</th><th>MAXQ622</th></tr>
<tr><td rowspan="11">16, 18, 19, 20, 50, 51, 53, 54</td><td rowspan="11">16, 18, 19, 20, 50, 51, 53, 54</td><td rowspan="11">P2.0–P2.7; MOSI0, MISO0, SCLK0, $\overline{SSEL0}$, TCK, TDI, TMS, TDO</td><td colspan="4">General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. P2.0 to P2.3 default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.
The JTAG pins (P2.4 to P2.7) default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register.
P2.7 functions as the JTAG test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP's shift_IR or shift_DR states.</td></tr>
<tr><td>MAXQ612</td><td>MAXQ622</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>16</td><td>16</td><td>P2.0</td><td>MOSI0</td></tr>
<tr><td>18</td><td>18</td><td>P2.1</td><td>MISO0</td></tr>
<tr><td>19</td><td>19</td><td>P2.2</td><td>SCLK0</td></tr>
<tr><td>20</td><td>20</td><td>P2.3</td><td>$\overline{SSEL0}$</td></tr>
<tr><td>50</td><td>50</td><td>P2.4</td><td>TCK</td></tr>
<tr><td>51</td><td>51</td><td>P2.5</td><td>TDI</td></tr>
<tr><td>53</td><td>53</td><td>P2.6</td><td>TMS</td></tr>
<tr><td>54</td><td>54</td><td>P2.7</td><td>TDO</td></tr>
<tr><td rowspan="11">33–37, 39, 40, 42</td><td rowspan="11">33–40</td><td rowspan="11">P3.0–P3.7; INT8–INT15</td><td colspan="4">General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.</td></tr>
<tr><td>MAXQ612</td><td>MAXQ622</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>33</td><td>33</td><td>P3.0</td><td>INT8</td></tr>
<tr><td>34</td><td>34</td><td>P3.1</td><td>INT9</td></tr>
<tr><td>35</td><td>35</td><td>P3.2</td><td>INT10</td></tr>
<tr><td>36</td><td>36</td><td>P3.3</td><td>INT11</td></tr>
<tr><td>37</td><td>37</td><td>P3.4</td><td>INT12</td></tr>
<tr><td>39</td><td>38</td><td>P3.5</td><td>INT13</td></tr>
<tr><td>40</td><td>39</td><td>P3.6</td><td>INT14</td></tr>
<tr><td>42</td><td>40</td><td>P3.7</td><td>INT15</td></tr>
<tr><td rowspan="11">65–72</td><td rowspan="11">65–72</td><td rowspan="11">P4.0–P4.7</td><td colspan="4">General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.</td></tr>
<tr><td>MAXQ612</td><td>MAXQ622</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>65</td><td>65</td><td>P4.0</td><td>—</td></tr>
<tr><td>66</td><td>66</td><td>P4.1</td><td>—</td></tr>
<tr><td>67</td><td>67</td><td>P4.2</td><td>—</td></tr>
<tr><td>68</td><td>68</td><td>P4.3</td><td>—</td></tr>
<tr><td>69</td><td>69</td><td>P4.4</td><td>—</td></tr>
<tr><td>70</td><td>70</td><td>P4.5</td><td>—</td></tr>
<tr><td>71</td><td>71</td><td>P4.6</td><td>—</td></tr>
<tr><td>72</td><td>72</td><td>P4.7</td><td>—</td></tr>
</table>

Pin Descriptions—Bare Die (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th colspan="4">FUNCTION</th></tr>
<tr><th>MAXQ612</th><th>MAXQ622</th></tr>
<tr><td rowspan="6">46–49</td><td rowspan="6">46–49</td><td rowspan="6">P5.0–P5.3; MOSI1, MISO1, SCLK1, $\overline{\text{SSEL1}}$</td><td colspan="4">General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.</td></tr>
<tr><td>MAXQ612</td><td>MAXQ622</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>46</td><td>46</td><td>P5.0</td><td>MOSI1</td></tr>
<tr><td>47</td><td>47</td><td>P5.1</td><td>MISO1</td></tr>
<tr><td>48</td><td>48</td><td>P5.2</td><td>SCLK1</td></tr>
<tr><td>49</td><td>49</td><td>P5.3</td><td>$\overline{\text{SSEL1}}$</td></tr>
<tr><td rowspan="9">12–15, 38, 41, 43, 44</td><td rowspan="9">12–15, 41–44</td><td rowspan="9">P6.0–P6.7</td><td colspan="4">General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.</td></tr>
<tr><td>MAXQ612</td><td>MAXQ622</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>12</td><td>12</td><td>P6.0</td><td>—</td></tr>
<tr><td>13</td><td>13</td><td>P6.1</td><td>—</td></tr>
<tr><td>14</td><td>14</td><td>P6.2</td><td>—</td></tr>
<tr><td>15</td><td>15</td><td>P6.3</td><td>—</td></tr>
<tr><td>38</td><td>41</td><td>P6.4</td><td>—</td></tr>
<tr><td>41</td><td>42</td><td>P6.5</td><td>—</td></tr>
<tr><td>43</td><td>43</td><td>P6.6</td><td>—</td></tr>
<tr><td>44</td><td>44</td><td>P6.7</td><td>—</td></tr>
<tr><td colspan="6">NO CONNECTION PINS</td></tr>
<tr><td>4, 11, 17, 22–27, 52, 57, 64</td><td>4, 11, 17, 52, 57, 64</td><td>N.C.</td><td colspan="4">No Connection. Reserved for future use. Leave these pins unconnected.</td></tr>
</table>

Detailed Description

The MAXQ612/MAXQ622 provide integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 128KB of flash memory; 6KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Lower active-mode current combined with the even lower MAXQ612/MAXQ622 stop-mode current results in increased battery life. IR application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation. A high-current, 25mA, IR drive pin and output pins capable of sinking up to 5mA support IR applications. It also includes a USB slave interface compatible with existing host HID device drivers, I^2C, dual SPI, dual USARTs, up to 56 general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify.

Operating from DC to 12MHz, almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true-code operation. When active device operation is not required, an ultra-low-power stop mode can be invoked from software, resulting in quiescent current consumption of less than 300nA typical and 3µA maximum. The combination of high-performance instructions and ultra-low

stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The MAXQ612/MAXQ622 are based on Maxim's MAXQ20 core, which is a low-power implementation of the new 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate internal 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core is a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). Program flow is supported by a configurable soft stack.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

Memory

The microcontroller incorporates several memory types:

- 128KB program flash memory
- 6KB SRAM data memory
- 6KB utility ROM
- Soft stack

Memory Protection

The optional memory-protection feature separates code memory into three areas: system, user loader, and user application. Code in the system area can be kept confidential. Code in the user areas can be prevented from reading and writing system code. The user loader can also be protected from user application code.

Memory protection is implemented using privilege levels for code. Each area has an associated privilege level. RAM/ROM are assigned privilege levels as well. Refer to the *MAXQ622 User's Guide* for a more thorough explanation of the topic.

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and can also be used for general-purpose data storage. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store values in the stack explicitly by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (BF0h). The CALL, PUSH, and interrupt-vectoring operations decrement SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then increment SP.

Utility ROM

The utility ROM is a 6KB block of internal ROM memory that defaults to a starting address of 8000h. The utility

Table 1. Memory Areas and Associated Maximum Privilege Levels

AREA	PAGE ADDRESS	MAXIMUM PRIVILEGE LEVEL
System	0 to ULDR-1	High
User Loader	ULDR to UAPP-1	Medium
User Application	UAPP to top	Low
Utility ROM	N/A	High
Other (RAM)	N/A	Low

ROM consists of subroutines that can be called from application software. These include the following:

- In-system programming (bootstrap loader) using JTAG interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash memory programming and fast table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of system code, or to one of the special routines mentioned. Routines within the utility ROM are user accessible and can be called as subroutines by the application software. More information on the utility ROM functions is contained in the *MAXQ622 User's Guide*.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh.

Three password locks protect three different program memory segments. When the PWL is set to one (power-on reset default) and the contents of the memory at addresses 0010h to 001Fh are any value other than FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to zero, these utilities are fully accessible without password. The PWLS bit uses a password that is at ULDR + 0010 to ULDR + 001F, and the PWLL uses a password at UAPP + 0010 to UAPP + 001F. The password is automatically set to all ones following a mass erase.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed infrared (IR) communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

Table 2. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (µs)
00	Sysclk/2^{15}	2.7ms	42.7
01	Sysclk/2^{18}	21.9ms	42.7
10	Sysclk/2^{21}	174.7ms	42.7
11	Sysclk/2^{24}	1.4s	42.7

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[1:0]}$
- Carrier Frequency ($f_{CARRIER}$) = f_{IRCLK}/(IRCAH + IRCAL + 2)
- Carrier High Time = IRCAH + 1
- Carrier Low Time = IRCAL + 1
- Carrier Duty Cycle = (IRCAH + 1)/(IRCAH + IRCAL + 2)

During transmission, the IRCA register is latched for each IRV downcount interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV downcount interval so that duty-cycle variation and frequency shifting is possible from one interval to the next. The starting/idle state and the carrier polarity of the IRTX pin can be configured when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reload its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

1) Reloads IRV with IRMT.
2) Samples IRCA, IRDATA, and IRTXPOL.
3) Generates IRTX accordingly.
4) Sets IRIF to 1.
5) Generates an interrupt to the CPU if enabled (IRIE = 1).

IR Transmit—Independent External Carrier and Modulator Outputs

The normal transmit mode modulates the carrier based upon the IRDATA bit. However, the user has the option to input the modulator (envelope) on an external pin if desired. The IRDATA bit is output directly to the IRTXM pin (if IRTXPOL = 0) on each IRV downcount interval boundary just as if it were being used to internally modulate the carrier frequency. If IRTXPOL = 1, the inverse of the IRDATA bit is output to the IRTXM pin on the IRV interval downcount boundaries. When the envelope mode is enabled, it is possible to output either the modulated (IRENV[1:0] = 01b) or unmodulated (INENV[1:0] = 10b) carrier to the IRTX pin.

IR Receive

When configured in receive mode (IRMODE = 0), the IR hardware supports the IRRX capture function. The IRRXSEL[1:0] bits define which edge(s) of the IRRX pin should trigger the IR timer capture function. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) allows clocking of the IRV register directly with the IRCLK for finer resolution. When IRCFME = 0, the IRCA defined carrier is counted by IRV. When IRCFME = 1, the IRCLK clocks the IRV register.

On the next qualified event, it does the following:

1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, IRDATA = 0. If a rising edge occurs, IRDATA = 1.

2) Transfers its current IRV value to the IRMT.

3) Resets IRV content to 0000h (if IRXRL = 1).

4) Continues counting again until the next qualified event.

If the IR timer value rolls over from 0FFFFh to 0000h before a qualified event happens, the IR timer overflow (IROV) flag is set to 1 and an interrupt is generated, if enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode or clearing IREN = 0.

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place. When RXBCNT = 1, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register only counts qualified edges. The IRIF interrupt flag now sets if two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit defines whether the IRV register is reloaded with 0000h on detection of a qualified edge (per the IRXSEL[1:0] bits).

16-Bit Timers/Counters

The microcontroller provides two general-purpose timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2n divider (for n = 0, 2, 4, 6, 8, 10)

General-Purpose I/O

The microcontroller provides port pins for general-purpose I/O that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, all port pins become three-state with both weak pullups and input buffers disabled, unless otherwise noted.

From a software perspective, each port appears as a group of peripheral registers with unique addresses. Special function pins can also be used as general-purpose I/O pins when the special functions are disabled. For a detailed description of the special functions available for each pin, refer to the IC-specific user's guide, e.g., the *MAXQ622 User's Guide* describes all special functions available on the MAXQ612/MAXQ622.

Serial Peripherals

The microcontroller supports two independent USARTs, two SPI master/slave communications ports, and an I^2C bus.

USART

The USART units are implemented with the following characteristics:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt for receive and transmit
- Independent baud-rate generator

Table 3. USART Mode Details

MODE	TYPE	START BITS	DATA BITS	STOP BITS
Mode 0	Synchronous	N/A	8	N/A
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1