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MB39A123

6 ch DC/DC Converter IC with Synchronous Rectification Datasheet

Description

MB39A123 is a 6-channel DC/DC converter IC using pulse width modulation (PWM) , and it is suitable for up conversion, down conversion, and up/down conversion. MB39A123 is built in 6 channels into LQFP-48P package and this IC can control and soft-start at each channel. MB39A123 is suitable for power supply of high performance potable instruments such as a digital still camera (DSC).

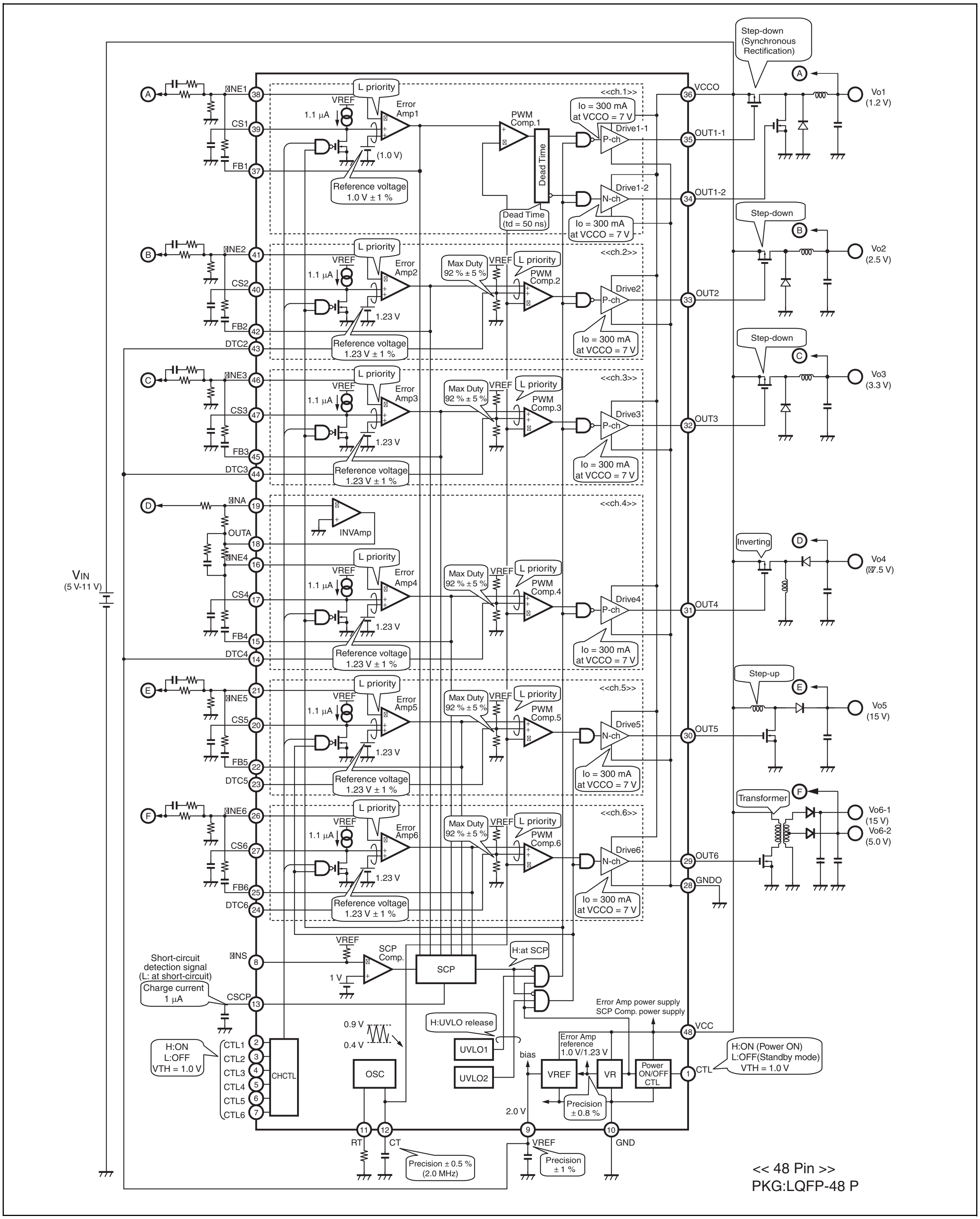
Features

- Supports for step-down with synchronous rectification (ch.1)
- Supports for step-down and up/down Zeta conversion (ch.2 to ch.4)
- Supports for step-up and up/down Sepic conversion (ch.5, ch.6)
- Negative voltage output (Inverting amplifier) (ch.4)
- Low voltage start-up (ch.5, ch.6) : 1.7 V
- Power supply voltage range : 2.5 V to 11 V
- Reference voltage : 2.0 V ± 1%
- Error amplifier reference voltage : 1.0 V ± 1% (ch.1) , 1.23 V ± 1% (ch.2 to ch.6)
- Oscillation frequency range : 200 kHz to 2.0 MHz
- Standby current : 0 µA (Typ)
- Built-in soft-start circuit independent of loads
- Built-in totem-pole type output for MOS FET
- Short-circuit detection capability by external signal (−INS terminal)
- Package : LQFP-48 pin

Applications

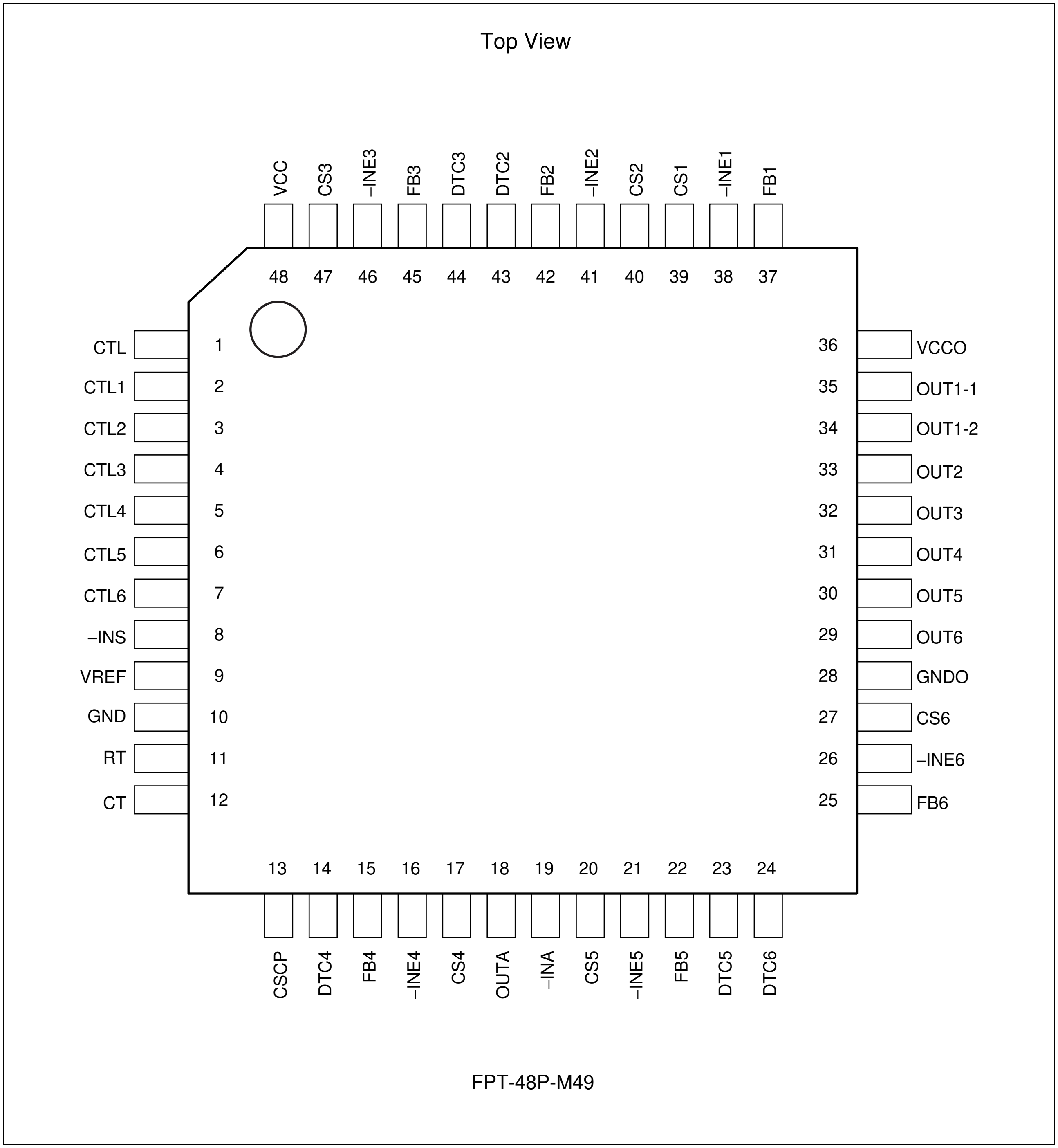
- Digital still camera (DSC)
- Digital video camera (DVC)
- Surveillance camera etc.

Block Diagram



Contents

Pin Assignments



Pin Descriptions

Block Name	Pin No.	Pin Name	I/O	Description
ch.1	37	FB1	O	ch.1: Error amplifier output terminal
	38	−INE1	I	ch.1: Error amplifier inverted input terminal
	39	CS1	–	ch.1: Soft-start setting capacitor connection terminal
	35	OUT1-1	O	ch.1: P-ch drive output terminal (External main side FET gate driving)
	34	OUT1-2	O	ch.1: N-ch drive output terminal (External synchronous rectification side FET gate driving)
ch.2	43	DTC2	I	ch.2: Dead time control terminal
	42	FB2	O	ch.2: Error amplifier output terminal
	41	−INE2	I	ch.2: Error amplifier inverted input terminal
	40	CS2	–	ch.2: Soft-start setting capacitor connection terminal
	33	OUT2	O	ch.2: P-ch drive output terminal
ch.3	44	DTC3	I	ch.3: Dead time control terminal
	45	FB3	O	ch.3: Error amplifier output terminal
	46	−INE3	I	ch.3: Error amplifier inverted input terminal
	47	CS3	–	ch.3: Soft-start setting capacitor connection terminal
	32	OUT3	O	ch.3: P-ch drive output terminal
ch.4	14	DTC4	I	ch.4: Dead time control terminal
	15	FB4	O	ch.4: Error amplifier output terminal
	16	−INE4	I	ch.4: Error amplifier inverted input terminal
	17	CS4	–	ch.4: Soft-start setting capacitor connection terminal
	31	OUT4	O	ch.4: P-ch drive output terminal
	19	−INA	I	Inverting amplifier input terminal
	18	OUTA	O	Inverting amplifier output terminal
ch.5	23	DTC5	I	ch.5: Dead time control terminal
	22	FB5	O	ch.5: Error amplifier output terminal
	21	−INE5	I	ch.5: Error amplifier inverted input terminal
	20	CS5	–	ch.5: Soft-start setting capacitor connection terminal
	30	OUT5	O	ch.5: N-ch drive output terminal
ch.6	24	DTC6	I	ch.6: Dead time control terminal
	25	FB6	O	ch.6: Error amplifier output terminal
	26	−INE6	I	ch.6: Error amplifier inverted input terminal
	27	CS6	–	ch.6: Soft-start setting capacitor connection terminal
	29	OUT6	O	ch.6: N-ch drive output terminal
OSC	12	CT	–	Triangular wave frequency setting capacitor connection terminal
	11	RT	–	Triangular wave frequency setting resistor connection terminal

Block Name	Pin No.	Pin Name	I/O	Description
Control	1	CTL	I	Power supply control terminal
	2	CTL1	I	ch.1 control terminal
	3	CTL2	I	ch.2 control terminal
	4	CTL3	I	ch.3 control terminal
	5	CTL4	I	ch.4 control terminal
	6	CTL5	I	ch.5 control terminal
	7	CTL6	I	ch.6 control terminal
	13	CSCP	–	Short-circuit detection circuit capacitor connection terminal
	8	−INS	I	Short-circuit detection comparator inverted input terminal
Power	36	VCCO	–	Drive output block power supply terminal
	48	VCC	–	Power supply terminal
	9	VREF	O	Reference voltage output terminal
	28	GNDO	–	Drive output block ground terminal
	10	GND	–	Ground terminal

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC, VCCO terminals	–	12	V
Output current	I_O	OUT1-1, OUT1-2, OUT2 to OUT6 terminals	–	20	mA
Peak output current	I_{OP}	OUT1-1, OUT1-2, OUT2 to OUT6 terminals Duty $\leq$ 5%	–	400	mA
Power dissipation	P_D	Ta $\leq$ +25°C (LQFP-48P)	–	2000[1]	mW
Storage temperature	T_{STG}	–	−55	+125	°C

Warning: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Note
1. When mounted on a 117 mm × 84 mm × 0.8 mm FR-4 boards.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Start power supply voltage	V_{CC}	ch.5, ch.6, VCC, VCCO terminals	1.7	–	11	V
Power supply voltage	V_{CC}	VCC, VCCO terminals	2.5	4	11	V
Reference voltage output current	I_{REF}	VREF terminal	−1	–	0	mA
Input voltage	V_{INE}	−INE1 to −INE6 terminals	0	–	$V_{CC} - 0.9$	V
		−INA terminal	− 0.2	–	$V_{CC} - 1.8$	V
		−INS terminal	0	–	V_{REF}	V
	V_{DTC}	DTC2 to DTC6 terminals	0	–	V_{REF}	V
Control input voltage	V_{CTL}	CTL, CTL1 to CTL6 terminals	0	–	11	V
Output current	I_O	OUT1-1, OUT1-2, OUT2 to OUT6 terminals	−15	–	+15	mA
Total gate charge of external FET	Qg	OUT1-1, OUT1-2, OUT2 to OUT6 terminals connection FET fosc = 2 MHz	–	2.6	7.5	nC
Oscillation frequency	f_{OSC}	–	0.2	1.0	2.0	MHz
Timing capacitor	C_T	–	27	100	680	pF
Timing resistor	R_T	–	3.0	6.8	39	kΩ
Soft-start capacitor	C_S	CS1 to CS6 terminals	–	0.1	1.0	µF
Short-circuit detection capacitor	C_{SCP}	–	–	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	–	–	0.1	1.0	µF
Operating ambient temperature	Ta	–	−30	+25	+85	°C

Warning: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Electrical Characteristics

(VCC = VCCO = 4 V, Ta = +25°C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [VREF]	Output voltage	V_{REF1}	9	VREF = 0 mA	1.98	2.00	2.02	V
		V_{REF2}	9	V_{CC} = 2.5 V to 11 V	1.975	2.000	2.025	V
		V_{REF3}	9	VREF = 0 mA to −1 mA	1.975	2.000	2.025	V
	Input stability	Line	9	V_{CC} = 2.5 V to 11 V[2]	–	2	–	mV
	Load stability	Load	9	VREF = 0 mA to −1 mA[2]	–	2	–	mV
	Temperature stability	$\Delta V_{REF}/V_{REF}$	9	Ta = 0°C to +85°C[2]	–	0.20	–	%
	Short-circuit output current	I_{OS}	9	VREF = 0 V[2]	–	−130	–	mA
Under voltage lockout protection circuit block (ch.1 to ch.4) [UVLO1]	Threshold voltage	V_{TH1}	35	V_{CC} =	1.7	1.8	1.9	V
	Hysteresis width	V_{H1}	35	–	0.05	0.1	0.2	V
	Reset voltage	V_{RST1}	35	V_{CC} =	1.55	1.7	1.85	V
Under voltage lockout protection circuit Block (ch.5, ch.6) [UVLO2]	Threshold voltage	V_{TH2}	30	V_{CC} =	1.35	1.5	1.65	V
	Hysteresis width	V_{H2}	30	–	0.02	0.05	0.1	V
	Reset voltage	V_{RST2}	30	V_{CC} =	1.27	1.45	1.63	V
Short-circuit detection Block [SCP]	Threshold voltage	V_{TH}	13	–	0.65	0.70	0.75	V
	Input source current	I_{CSCP}	13	–	−1.4	−1.0	−0.6	μA
Triangular Wave Oscillator Block [OSC]	Oscillation frequency	fosc1	29 to 35	C_T = 100 pF, R_T = 6.8 kΩ	0.95	1.0	1.05	MHz
		fosc2	29 to 35	C_T = 100 pF, R_T = 6.8 kΩ V_{CC} = 2.5 V to 11 V	0.945	1.0	1.055	MHz
	Frequency Input stability	$\Delta f_{OSC}/f_{OSC}$	29 to 35	C_T = 100 pF, R_T = 6.8 kΩ V_{CC} = 2.5 V to 11 V[2]	–	1.0	–	%
	Frequency temperature stability	$\Delta f_{OSC}/f_{OSC}$	29 to 35	C_T = 100 pF, R_T = 6.8 kΩ Ta = 0°C to +85°C[2]	–	1.0	–	%
Soft-Start Block (ch.1 to ch.6) [CS1 to CS6]	Charge current	I_{CS}	17,20,27, 39,40,47	CS1 to CS6 = 0 V	−1.45	−1.1	−0.75	μA

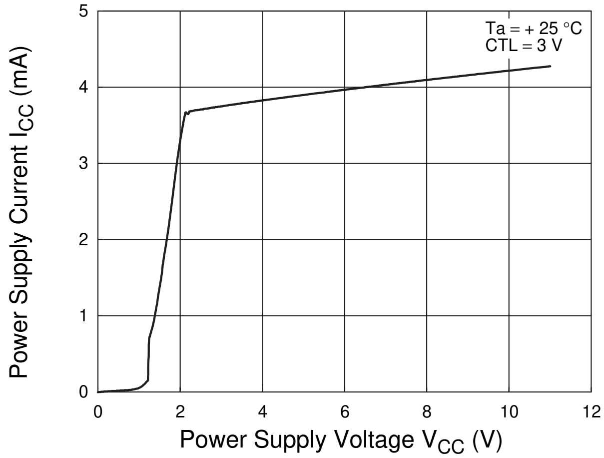
Note
2. Standard design values

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error Amp Block (ch.1) [Error Amp1]	Reference voltage	V_{TH1}	38	V_{CC} = 2.5 V to 11 V Ta = +25°C	0.990	1.000	1.010	V
		V_{TH2}	38	V_{CC} = 2.5 V to 11 V Ta = 0°C to +85°C[2]	0.988	1.000	1.012	V
	Temperature stability	$\Delta V_{TH}/V_{TH}$	38	Ta = 0°C to +85°C[2]	–	0.1	–	%
	Input bias current	I_B	38	–INE1 = 0 V	–120	–30	–	nA
	Voltage gain	A_V	37	DC[2]	–	100	–	dB
	Frequency bandwidth	BW	37	A_V = 0 dB[2]	–	1.4	–	MHz
	Output voltage	V_{OH}	37	–	1.7	1.9	–	V
		V_{OL}	37	–	–	40	200	mV
	Output source current	I_{SOURCE}	37	FB1 = 0.65 V	–	–2	–1	mA
	Output sink current	I_{SINK}	37	FB1 = 0.65 V	150	200	–	µA
Error Amp Block (ch.2 to ch.6) [Error Amp2 to Error Amp6]	Reference voltage	V_{TH3}	16, 21, 26, 41, 46	V_{CC} = 2.5 V to 11 V Ta = +25°C	1.217	1.230	1.243	V
		V_{TH4}	16, 21, 26, 41, 46	V_{CC} = 2.5 V to 11 V Ta = 0°C to +85°C[2]	1.215	1.230	1.245	V
	Temperature stability	$\Delta V_{TH}/V_{TH}$	16, 21, 26, 41, 46	Ta = 0°C to +85°C[2]	–	0.1	–	%
	Input bias current	I_B	16, 21, 26, 41, 46	–INE2 to –INE6 = 0 V	–120	–30	–	nA
	Voltage gain	A_V	15, 22, 25, 42, 45	DC[2]	–	100	–	dB
	Frequency bandwidth	BW	15, 22, 25, 42, 45	A_V = 0 dB[2]	–	1.4	–	MHz
	Output voltage	V_{OH}	15, 22, 25, 42, 45	–	1.7	1.9	–	V
		V_{OL}	15, 22, 25, 42, 45	–	–	40	200	mV
Error Amp Block (ch.2 to ch.6) [Error Amp2 to Error Amp6]	Output source current	I_{SOURCE}	15, 22, 25, 42, 45	FB2 to FB6 = 0.65 V	–	–2	–1	mA
	Output sink current	I_{SINK}	15, 22, 25, 42, 45	FB2 to FB6 = 0.65 V	150	200	–	µA
Inverting Amp Block (ch.4) [Inv Amp]	Input offset voltage	V_{IO}	18	OUTA = 1.23V	–10	0	+ 10	mV
	Input bias current	I_B	19	– INA = 0V	–120	–30	–	nA
	Voltage gain	A_V	18	DC[2]	–	100	–	dB
	Frequency bandwidth	BW	18	A_V = 0 dB[2]	–	1.0	–	MHz
	Output voltage	V_{OH}	18	–	1.7	1.9	–	V
		V_{OL}	18	–	–	40	200	mV
	Output source current	I_{SOURCE}	18	OUTA = 1.23V	–	–2	–1	mA
	Output sink current	I_{SINK}	18	OUTA = 1.23V	150	200	–	µA
PWM Comparator Block (ch.1) [PWM Comp.1]	Threshold voltage	V_{T0}	34, 35	Duty cycle = 0%	0.35	0.4	0.45	V
		V_{T100}	34, 35	Duty cycle = 100%	0.85	0.9	0.95	V

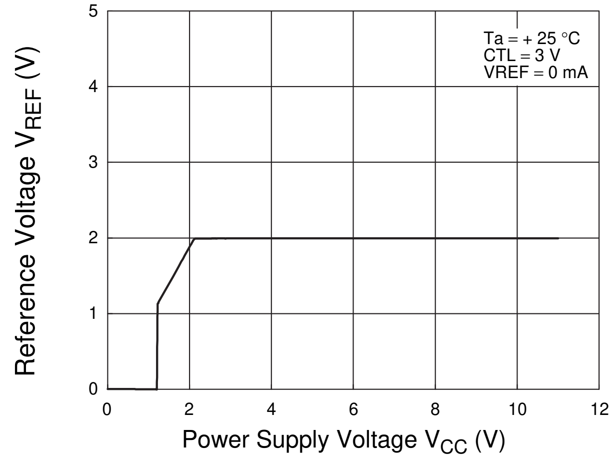
Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
PWM Comparator Block (ch.2 to ch.6) [PWM Comp.2 to PWM Comp.6]	Threshold voltage	V_{T0}	29 to 33	Duty cycle = 0%	0.35	0.4	0.45	V
		V_{T100}	29 to 33	Duty cycle = 100%	0.85	0.9	0.95	V
	Maximum duty cycle	Dtr	29 to 33	C_T = 100 pF, R_T = 6.8 kΩ	87	92	97	%
Output Block (ch.1 to ch.6) [Drive1 to Drive6]	Output source current	I_{SOURCE}	29 to 35	Duty ≤ 5% OUT = 0 V	–	–130	–75	mA
	Output sink current	I_{SINK}	29 to 35	Duty ≤ 5% OUT = 4 V	75	130	–	mA
	Output on resistor	R_{OH}	29 to 35	OUT = – 15 mA	–	18	27	Ω
		R_{OL}	29 to 35	OUT = 15 mA	–	18	27	Ω
	Dead time	t_{D1}	34, 35	OUT2 – OUT1 [2]	–	50	–	ns
		t_{D2}	34, 35	OUT1 – OUT2 [2]	–	50	–	ns
Short-Circuit Detection Comparator Block [SCP Comp.]	Threshold voltage	V_{TH}	35	–	0.97	1.00	1.03	V
	Input bias current	I_B	8	–INS = 0 V	–25	–20	–17	µA
Control Block (CTL, CTL1 to CTL6) [CTL, CHCTL]	Output on condition	V_{IH}	1 to 7	CTL, CTL1 to CTL6	1.5	–	11	V
	Output off condition	V_{IL}	1 to 7	CTL, CTL1 to CTL6	0	–	0.5	V
	Input current	I_{CTLH}	1 to 7	CTL, CTL1 to CTL6 = 3 V	5	30	60	µA
		I_{CTLL}	1 to 7	CTL, CTL1 to CTL6 = 0 V	–	–	1	µA
General	Standby current	I_{CCS}	48	CTL, CTL1 to CTL6 = 0 V	–	0	2	µA
		I_{CCSO}	36	CTL = 0 V	–	0	1	µA
	Power supply current	I_{CC}	48	CTL = 3 V	–	4.5	6.8	mA

Typical Characteristics

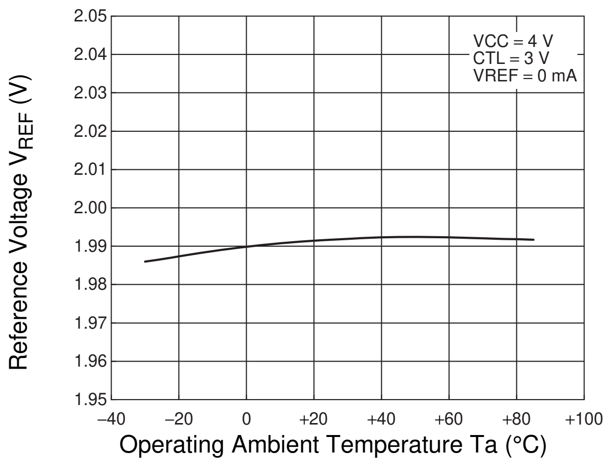
Power Supply Current vs. Power Supply Voltage



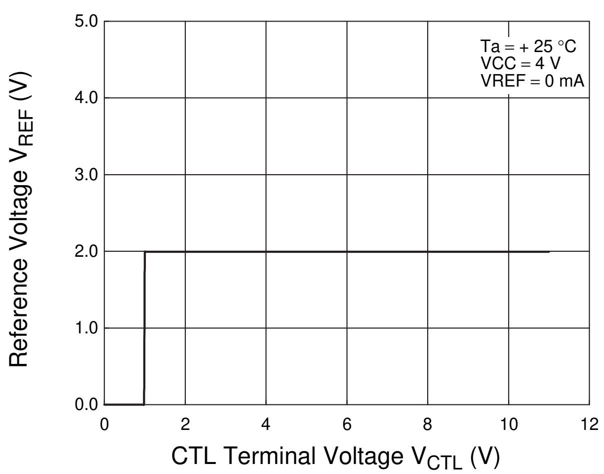
Reference Voltage vs. Power Supply Voltage



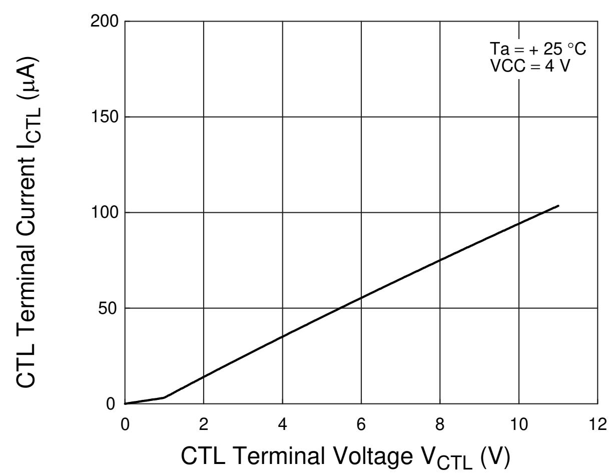
Reference Voltage vs. Operating Ambient Temperature



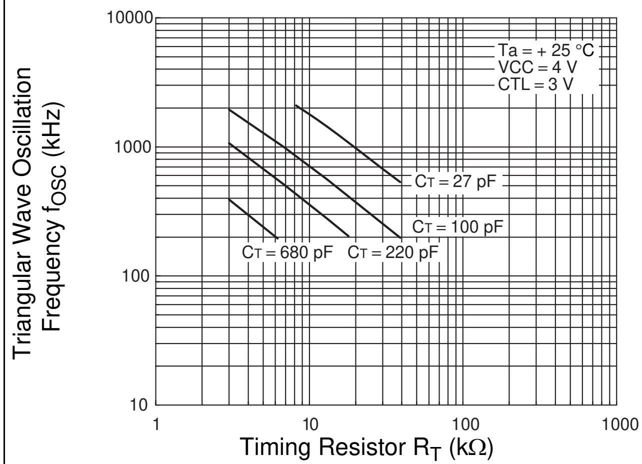
Reference Voltage vs. CTL Terminal Voltage



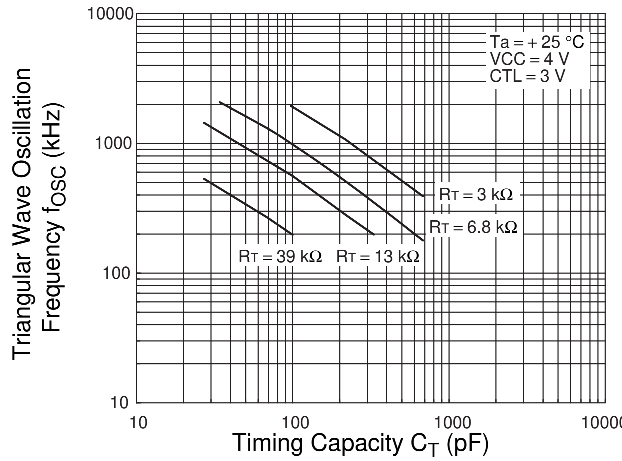
CTL Terminal Current vs. CTL Terminal Voltage



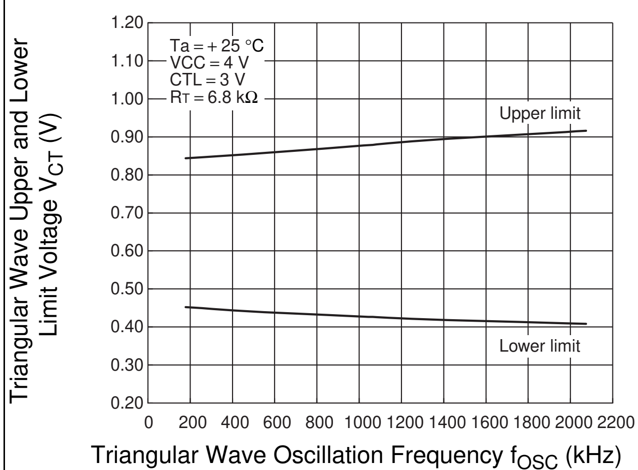
Triangular Wave Oscillation Frequency vs. Timing Resistor



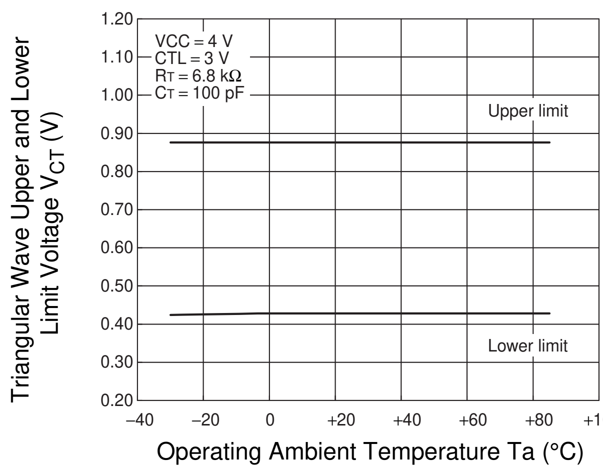
Triangular Wave Oscillation Frequency vs. Timing Capacity



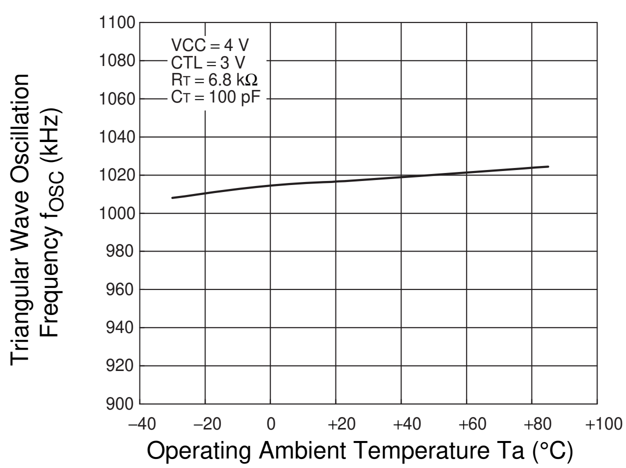
Triangular Wave Upper and Lower Limit Voltage vs. Triangular Wave Oscillation Frequency



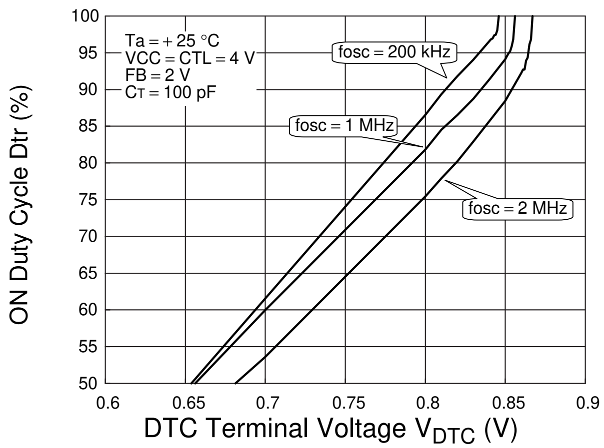
Triangular Wave Upper and Lower Limit Voltage vs. Operating Ambient Temperature



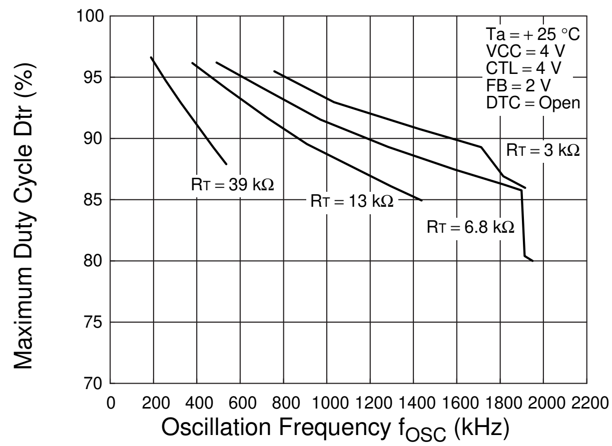
Triangular Wave Oscillation Frequency vs. Operating Ambient Temperature



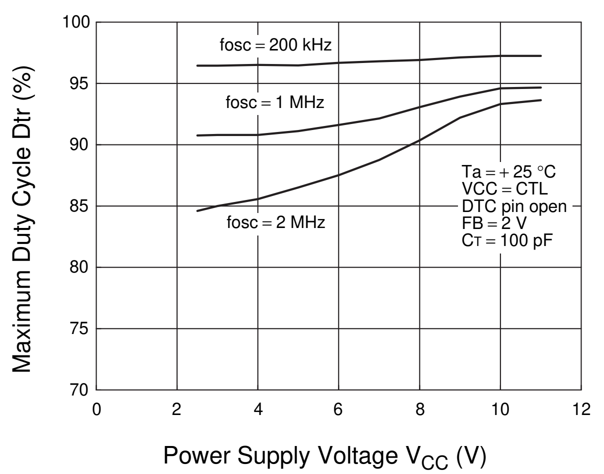
ON Duty Cycle vs. DTC Terminal Voltage



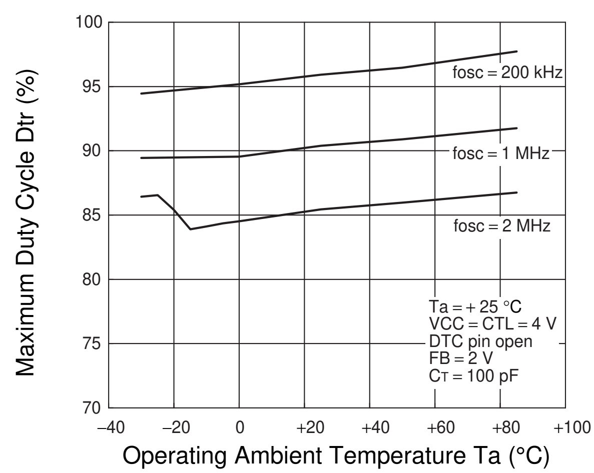
Maximum Duty Cycle vs. Oscillation Frequency



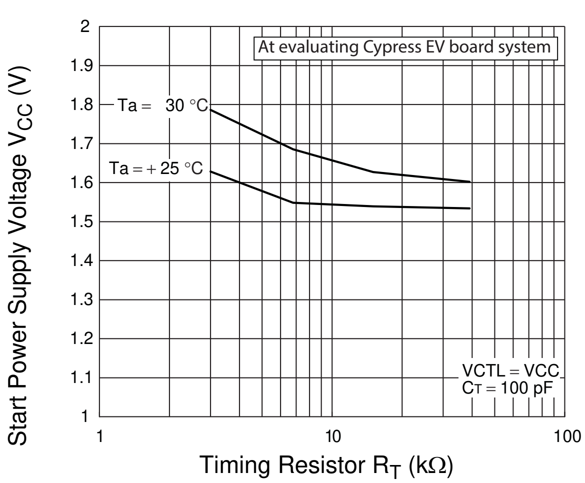
Maximum Duty Cycle vs. Power Supply Voltage



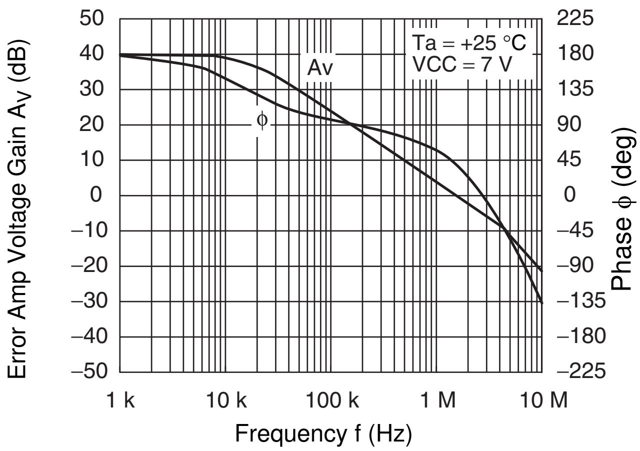
Maximum Duty Cycle vs. Operating Ambient Temperature

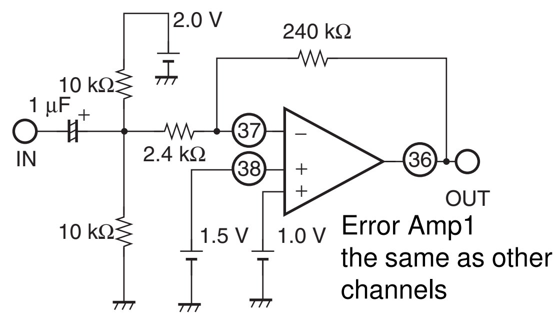


Start Power Supply Voltage vs. Timing Resistor

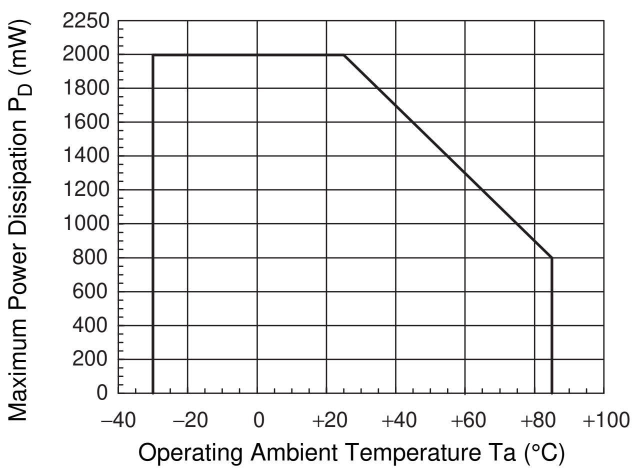


Error Amp Voltage Gain, Phase vs. Frequency





Maximum Power Dissipation vs.
Operating Ambient Temperature (for LQFP-48P)



Functional Description

DC/DC Converter Function

Reference voltage block (VREF)

The reference voltage circuit uses the voltage supplied from VCC terminal (pin 48) to generate a temperature compensated reference voltage (2.0 V Typ) used as the reference voltage for the internal circuits of the IC. It is also possible to supply the load current of up to 1 mA to external circuits as a reference voltage through the VREF terminal (pin 9) .

Triangular wave oscillator block (OSC)

The triangular wave oscillator block generates the triangular wave oscillation waveform width of 0.4 V lower limit and 0.5 V amplitude by the timing resistor (R_T) connected to the RT terminal (pin 11) , and the timing capacitor (C_T) connected to the CT terminal (pin 12) . The triangular wave is input to the PWM comparator circuits on the IC.

Error amplifier block (Error Amp1 to Error Amp6)

The error amplifier detects output voltage of the DC/DC converter and outputs PWM control signals. An arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverted input terminal of the error amplifier, enabling stable phase compensation for the system.

You can prevent surge currents when the IC is turned on by connecting soft-start capacitors to the CS1 terminal (pin 39) to CS6 terminal (pin 27) which are the noninverting input terminals of the error amplifier. The IC is started up at constant soft-start time intervals independent of the output load of the DC/DC converter.

PWM comparator block (PWM Comp.1 to PWM Comp.6)

The PWM comparator block is a voltage-pulse width converter that controls the output duty depending on the input/output voltage.

An output transistor is turned on, during intervals when the error amplifier output voltage and DTC voltage (ch.2 to ch.6) are higher than the triangular wave voltage.

Output block (Drive1 to Drive6)

The output circuit uses a totem-pole configuration and is capable of driving an external P-ch MOS FET (main side of ch.1, ch.2, ch.3 and ch.4) and N-ch MOS FET (synchronous rectification side of ch.1, ch.5 and ch.6).

Channel Control Function

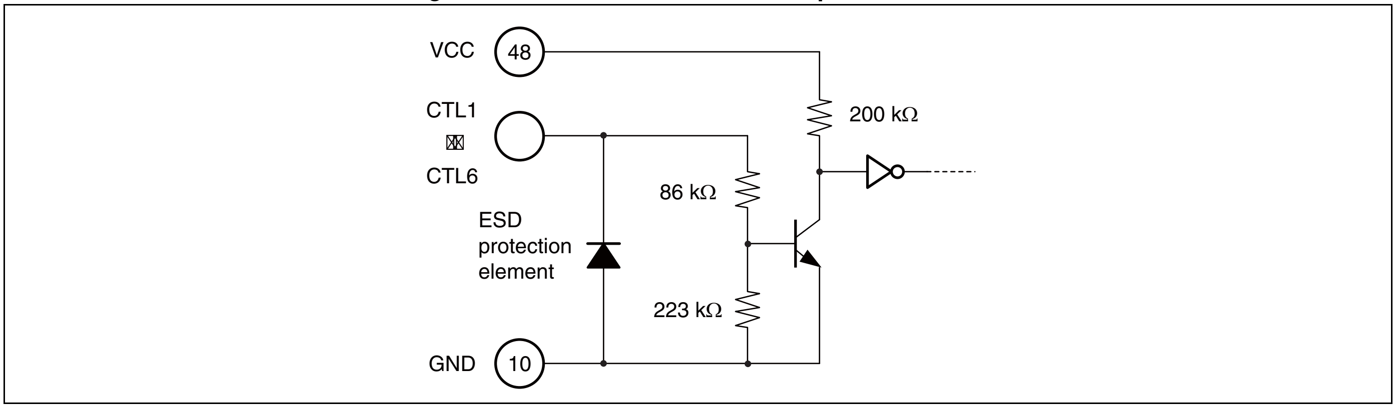
Use the CTL terminal (pin 1), CTL1 terminal (pin 2), CTL2 terminal (pin 3), CTL3 terminal (pin 4), CTL4 terminal (pin 5), CTL5 terminal (pin 6), and CTL6 terminal (pin 7) to set ON/OFF to the main and each channels.

Table 1. ON/OFF setting conditions for each channel

CTL	CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	Power	ch.1	ch.2	ch.3	ch.4	ch.5	ch.6
L	X	X	X	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF
H	H	L	L	L	L	L	ON	ON	OFF	OFF	OFF	OFF	OFF
H	L	H	L	L	L	L	ON	OFF	ON	OFF	OFF	OFF	OFF
H	L	L	H	L	L	L	ON	OFF	OFF	ON	OFF	OFF	OFF
H	L	L	L	H	L	L	ON	OFF	OFF	OFF	ON	OFF	OFF
H	L	L	L	L	H	L	ON	OFF	OFF	OFF	OFF	ON	OFF
H	L	L	L	L	L	H	ON	OFF	OFF	OFF	OFF	OFF	ON
H	H	H	H	H	H	H	ON	ON	ON	ON	ON	ON	ON

Note that current which is over standby current flows into VCC terminal when the CTL terminal is in “L” level and one of the terminals between CTL1 to CTL6 terminals is set to “H” level. (Refer to the following circuit)

Figure 1. CTL1 to CTL6 terminals equivalent circuit



Protection Function

Timer-latch short-circuit protection circuit (SCP, SCP Comp.)

The short-circuit detection comparator (SCP) detects the output voltage level of each channel. If the output voltage of any channel is lower than the short-circuit detection voltage, the timer circuit is actuated to start charging to the capacitor (Cscp) externally connected to the CSCP terminal (pin 13).

When the capacitor (Cscp) voltage becomes about 0.7 V, the output transistor is turned off and the dead time is set to 100%.

The short-circuit detection from external input is capable by using −INS terminal (pin 8) on short-circuit detection comparator (SCP Comp.) .

When the protection circuit is actuated, the power supply is rebooted or the CTL terminal (pin 1) is set to "L" level, resetting the latch as the voltage at the VREF terminal (pin 9) becomes 1.27 V (Min) or less (Refer to Setting the Time Constant for Timer-Latch Short-Circuit Protection Circuit on page 21) .

Under voltage lockout protection circuit block (UVLO)

The transient state or a momentary decrease in the power supply voltage, which occurs when the power supply is turned on, may cause the control IC to malfunction, resulting in the breakdown or degradation of the system. To prevent such malfunctions, under voltage lockout protection circuit detects a decrease in internal reference voltage level with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 13) at the "L" level.

The system returns to the normal state when the power supply voltage reaches the reference voltage of the under voltage lockout protection circuit.

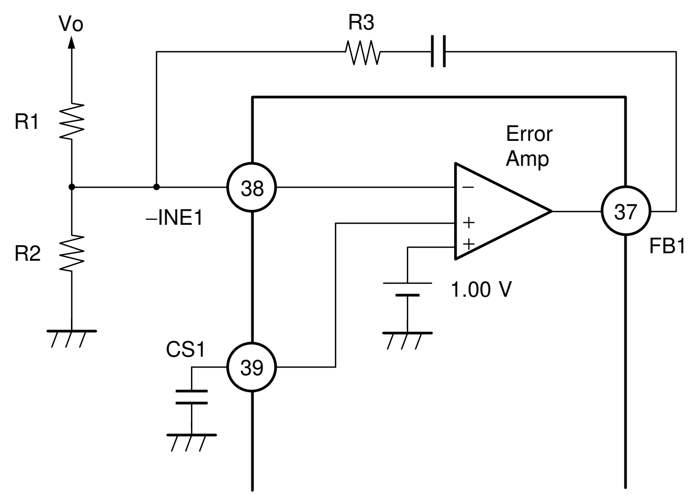
Protection circuit operating function table

The following table shows the output state that the protection circuit is operating.

Operation circuit	OUT1-1	OUT1-2	OUT2	OUT3	OUT4	OUT5	OUT6
Short-circuit protection circuit	H	L	H	H	H	L	L
Under voltage lockout protection circuit	H	L	H	H	H	L	L

Setting the Output Voltage

ch.1

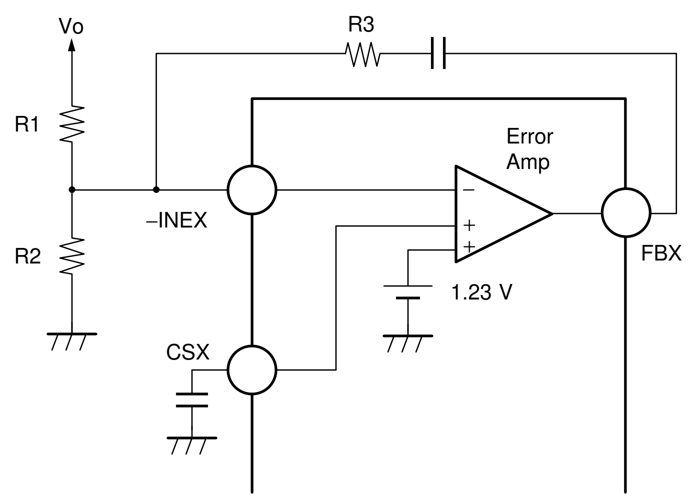


$$V_O = \frac{1.00\ V}{R2}\ (R1 + R2)$$

$$(R1 + R3) \geq \frac{V_O}{100\ \mu A}$$

Set R1 and R3 to prevent the error amp's response from decreasing by using above formula.

ch.2 to ch.6



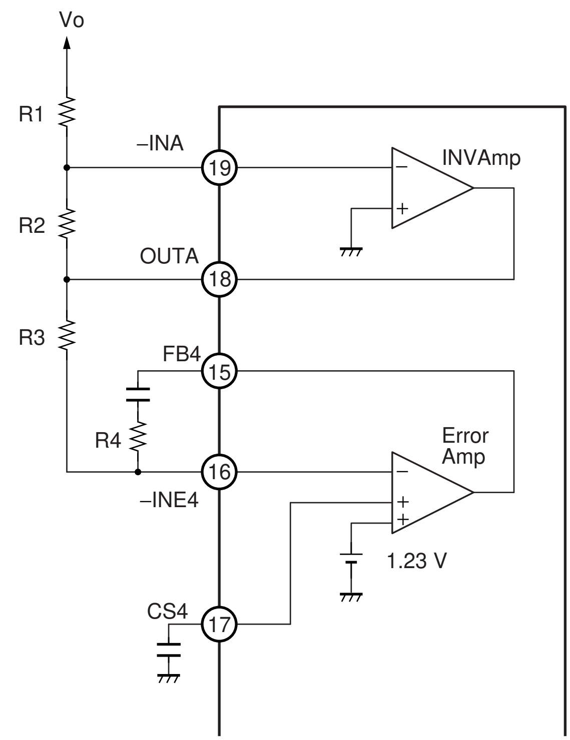
$$V_O = \frac{1.23\ V}{R2}\ (R1 + R2)$$

$$(R1 + R3) \geq \frac{V_O}{100\ \mu A}$$

X : Each channel number

Set R1 and R3 to prevent the error amp's response from decreasing by using above formula.

ch.4 (Negative voltage output)



$$V_O = \frac{-1.23\ V}{R2}\ R1$$

Setting the Triangular Wave Oscillation Frequency

The triangular wave oscillation frequency can be set by connecting a timing resistor (R_T) to the RT terminal (pin 11) and a timing capacitor (C_T) to the CT terminal (pin 12).

Triangular wave oscillation frequency : f_{OSC}

$$f_{OSC}\ (kHz) \doteqdot \frac{680000}{C_T\ (pF) \times R_T\ (k\Omega)}$$

Setting the Soft-Start Time

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} to C_{S6}) to the CS1 terminal (pin 39) to CS6 terminal (pin 27) respectively.

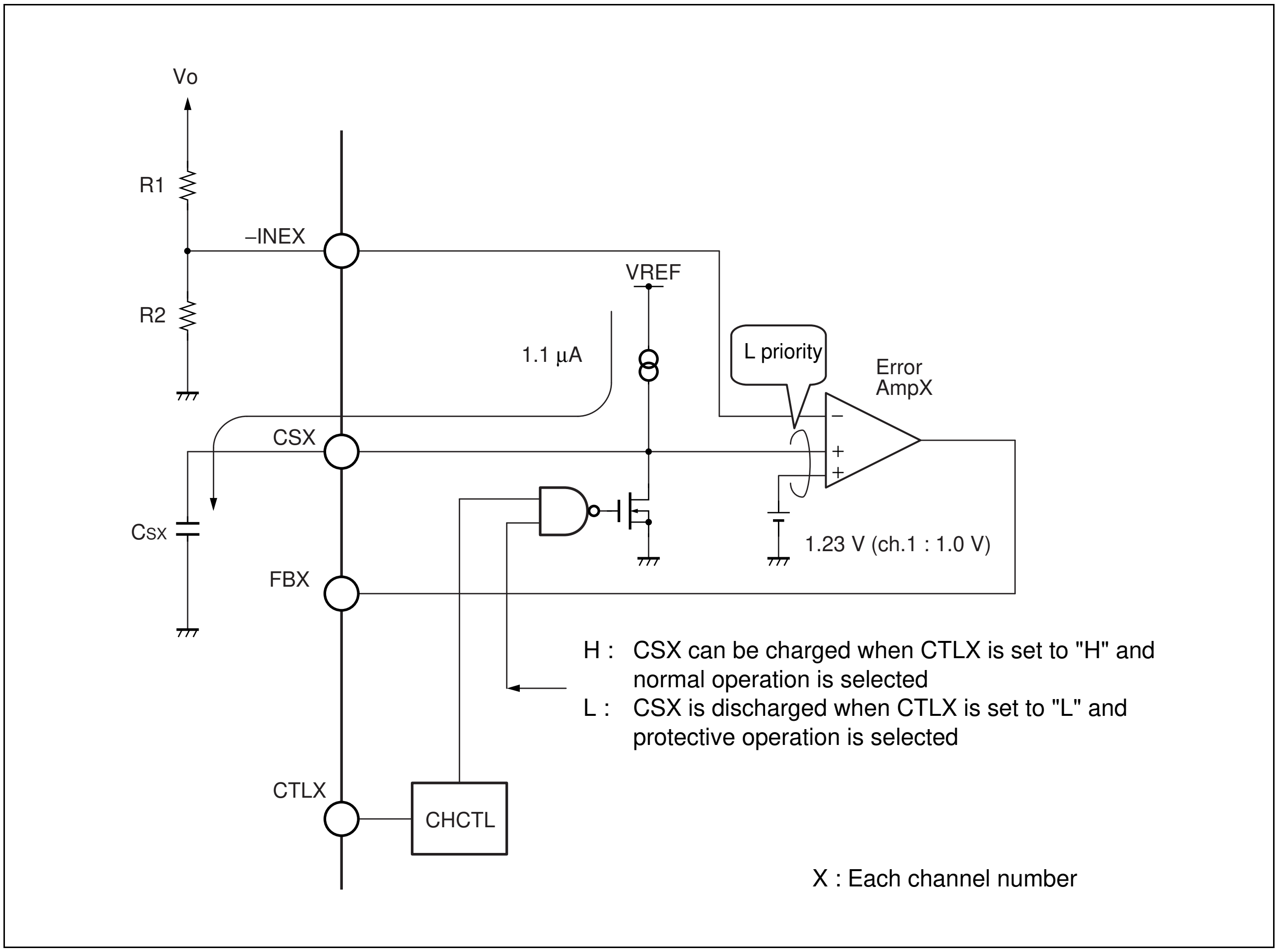
As illustrated below, when each CTLX is set to “H” from “L”, the soft-start capacitors (C_{S1} to C_{S6}) externally connected to the CS1 to CS6 terminals are charged at about 1.1 µA.

The error amplifier output (FB1 to FB6) is determined by comparison between the lower voltage of the two non-inverted input terminal voltage (1.23 V (ch.1 : 1.0 V) , CS terminal voltage) and the inverted input terminal voltage (−INE1 to −INE6) . The FB terminal voltage is decided for the soft-start period (CS terminal voltage < 1.23 V (ch.1 : 1.0 V)) by the comparison between −INE terminal voltage and CS terminal voltage. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor externally connected to the CS terminal is charged. The soft-start time is obtained from the following formula :

Soft-start time : ts (time until output voltage 100%)

ch.1 : ts (s) ≒ 0.91 × C_{S1} (µF)

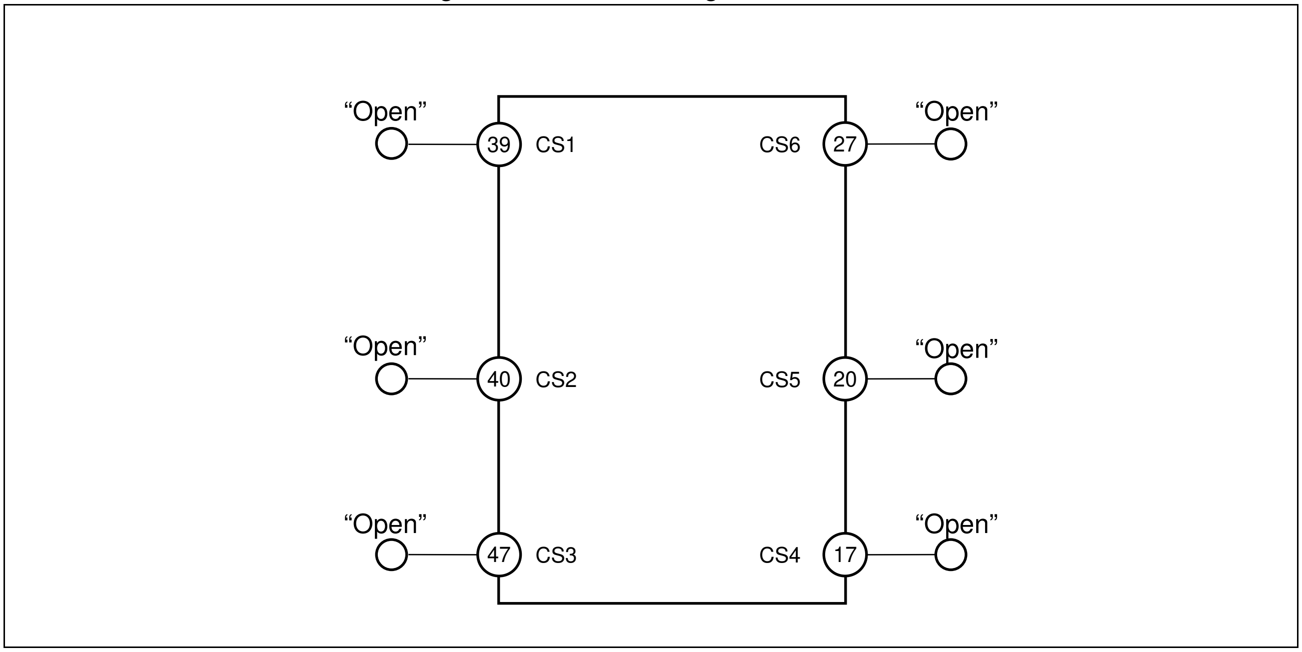
ch.2 to ch.6 : ts (s) ≒ 1.12 × C_{SX} (µF) X : Each channel number



Processing When Not Using CS Terminal

When soft-start function is not used, leave the CS1 terminal (pin 39), the CS2 terminal (pin 40), the CS3 terminal (pin 47), the CS4 terminal (pin 17), the CS5 terminal (pin 20) and the CS6 terminal (pin 27) open.

Figure 2. When not setting soft-start time



Setting the Time Constant for Timer-Latch Short-Circuit Protection Circuit

Each channel uses the short-circuit detection comparator (SCP) to always compare the error amplifier's output level to the reference voltage.

While DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at "L" level, and the CSCP terminal (pin 13) is held at "L" level.

If the load condition on a channel changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the output of the short-circuit detection comparator on that channel goes to "H" level.

This causes the external short-circuit protection capacitor C_{SCP} connected to the CSCP terminal (pin 13) to be charged at 1 μA.

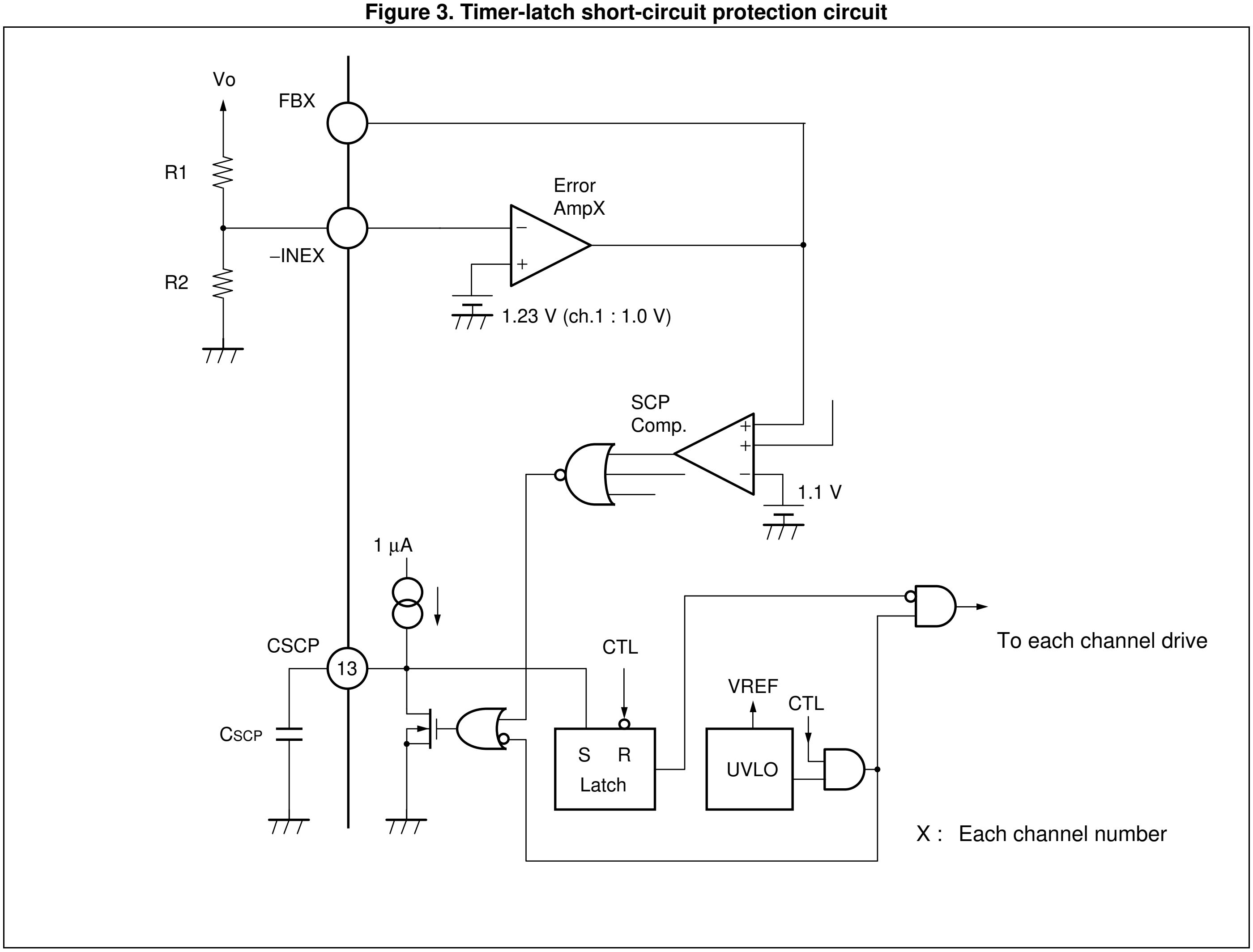
Short-circuit detection time : t_{CSCP}
....t_{CSCP} (s) $\risingdotseq$ 0.70 ∞ C_{SCP} (μF)

When the capacitor C_{SCP} is charged to the threshold voltage ($V_{TH} \risingdotseq 0.70$ V) , the latch is set to and the external FET is turned off (dead time is set to 100%) . At this time, the latch input is closed and CSCP terminal (pin 13) is held at "L" level.

The short-circuit detection from external input is capable by using −INS terminal (pin 8) . In this case, the short-circuit detection operates when the −INS terminal voltage becomes the level of the threshold voltage ($V_{TH} \risingdotseq$ IV) or less.

Note that the latch is reset as the voltage at the VREF terminal (pin 9) is decreased to 1.27 V (Min) or less by either recycling the power supply or setting the CTL terminal (pin 1) to "L" level.

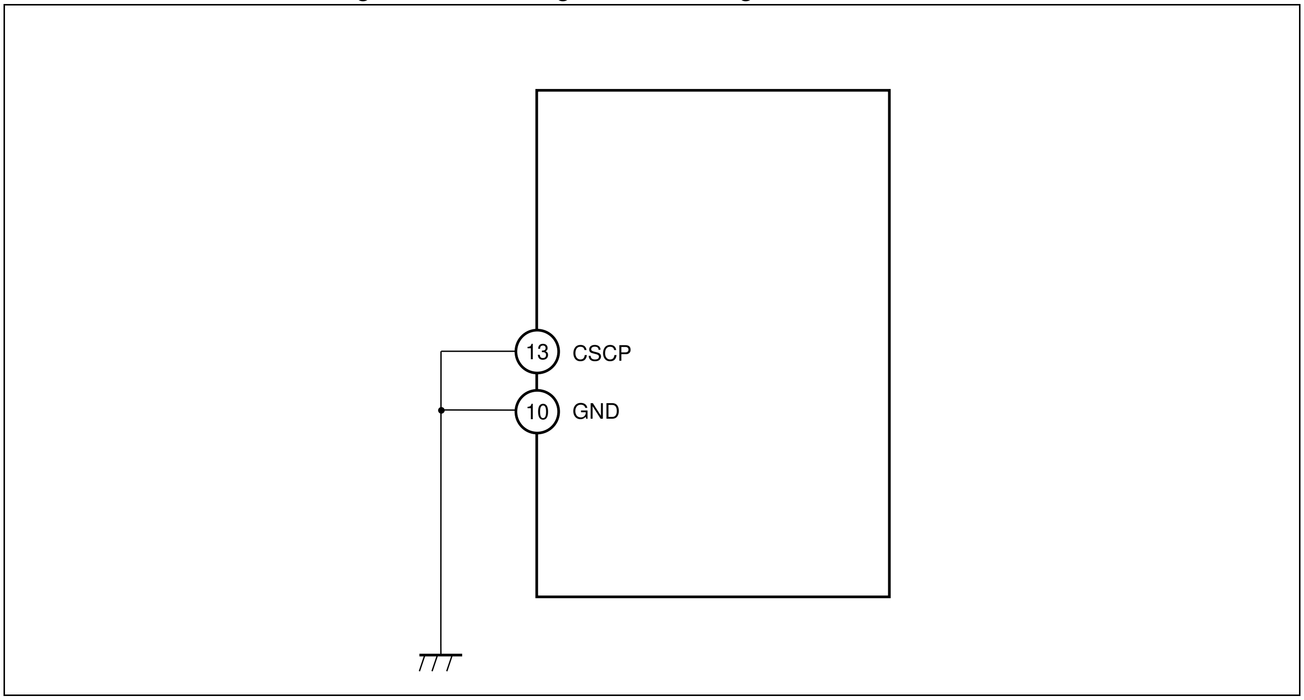
Figure 3. Timer-latch short-circuit protection circuit



Processing When Not Using CSCP Terminal

To disable the timer-latch short-circuit protection circuit, connect the CSCP terminal (pin 13) to GND in the shortest distance.

Figure 4. Processing when not using the CSCP terminal

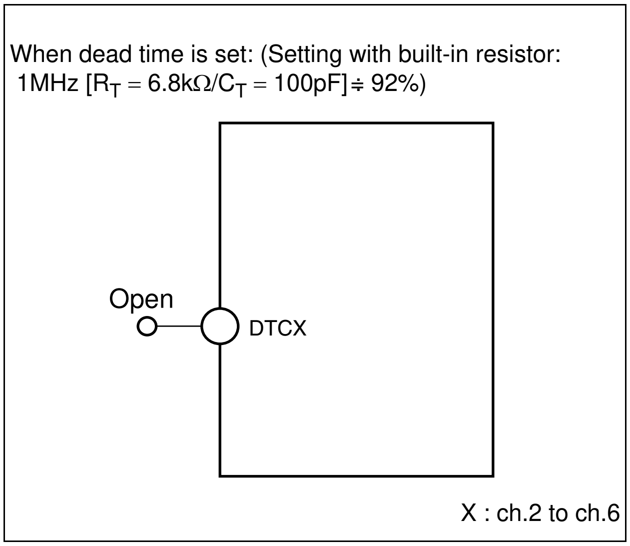


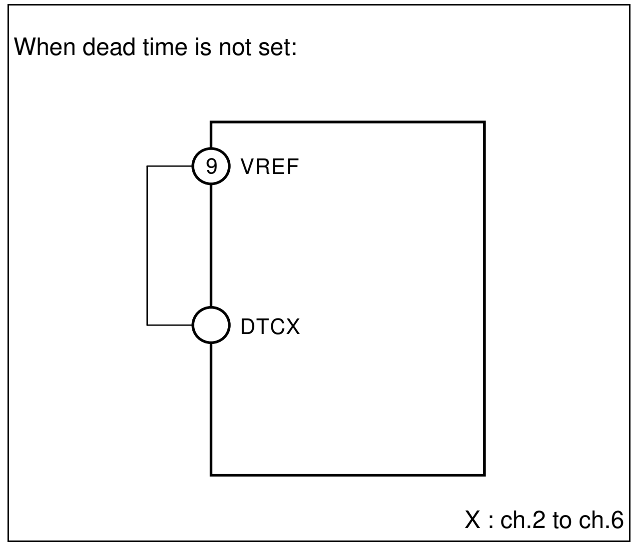
Setting the Dead Time (ch.2 to ch.6)

When the device is set for step-up or inverted output based on the step-up, step-up/down Zeta method, step up/down Sepic method, or flyback method, the FB terminal voltage may reach and exceed the triangular wave voltage due to load fluctuation. If this is the case, the output transistor is fixed to a full-ON state (ON duty = 100%). To prevent this, set the maximum duty of the output transistor.

When the DTC terminal is opened, the maximum duty is 92% (Typ) because of this IC built-in resistor which sets the DTC terminal voltage. This is based on the following setting: 1MHz ($R_T = 6.8k\Omega/C_T = 100pF$).

To disable the DTC terminal, connect it to the VREF terminal (pin 9) as illustrated below (when dead time is not set).





To change the maximum duty using external resistors, set the DTC terminal voltage by dividing resistance using the VREF voltage. Refer to Figure 6.

It is possible to set without regard for the built-in resistance value (including tolerance) when setting the external resistance value to 1/10 of the built-in resistance or less.

Note that the VREF load current must be set such that the total current for all the channels does not exceed 1 mA.

When the DTC terminal voltage is higher than the triangular wave voltage, the output transistor is turned on. The formula for calculating the maximum duty is as follows, assuming that the triangular wave amplitude and triangular wave lower limit voltage are about 0.5 V and 0.4 V, respectively.

$$\text{DUTY (ON) Max} \fallingdotseq \frac{\text{Vdt} - 0.4\text{ V}}{0.5\text{ V}} \times 100\ (\%)$$

$$\text{Vdt} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF (V)} \quad \left(\text{condition : Ra} < \frac{\text{R1}}{10},\ \text{Rb} < \frac{\text{R2}}{10}\right)$$

Note: DUTY obtained by the above-mentioned formula is a calculated value. For setting, refer to "ON Duty cycle vs. DTC terminal voltage".

The maximum duty varies depending on the oscillation frequency, regardless of settings in built-in or external resistors.

(This is due to the dependency of the peak value of a triangular wave on the oscillation frequency and R_T. Therefore, if R_T is greater, the maximum duty decreases, even when the same frequency is used.)

Furthermore, the maximum duty increases when the power supply voltage and the temperature are high. It is therefore recommended to set the duty, based on the Typical Characteristics on page 11 data, so that it does not exceed 95% under the worst conditions.

Figure 5. ON duty cycle vs. DTC terminal voltage

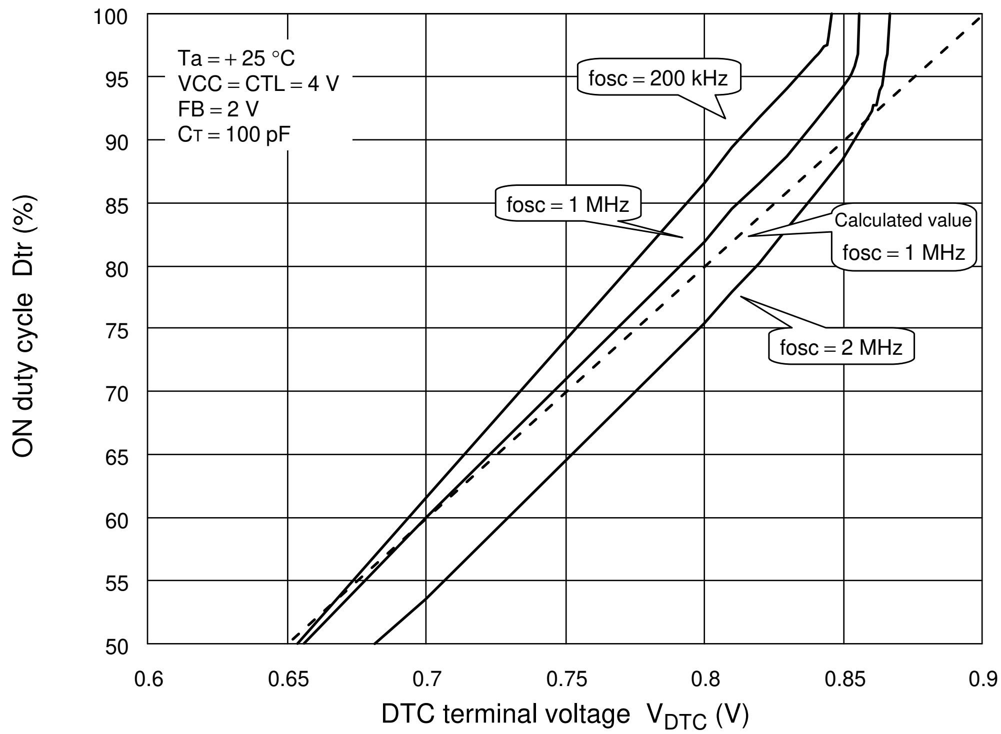
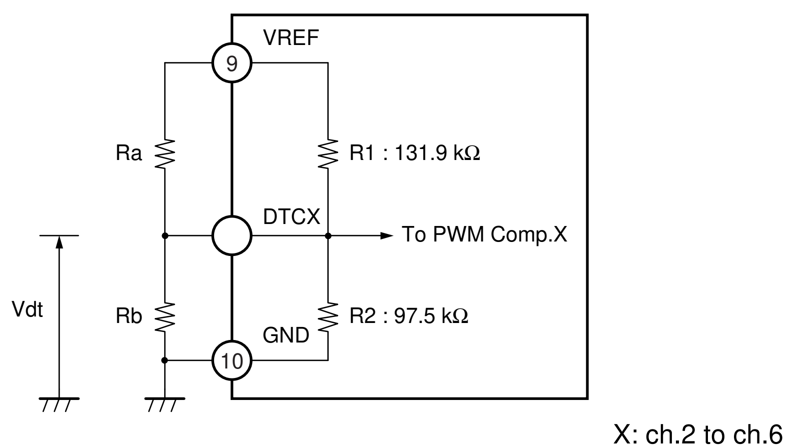


Figure 6. When dead time is set (Setting by external resistors)



Setting example (for an aim maximum ON duty of 80% (Vdt = 0.8 V) with Ra = 13.7 kΩ and Rb = 9.1 kΩ)

- Calculation using external resistors Ra and Rb only

$$Vdt = \frac{Rb}{Ra + Rb} \times VREF \doteqdot 0.80\ V$$

$$DUTY\ (ON)\ Max \doteqdot \frac{Vdt - 0.4\ V}{0.5\ V} \times 100\ (\%) \doteqdot 80\% \cdots\cdot\ (1)$$

- Calculation taking account of the built-in resistor (tolerance ± 20%) also

$$Vdt = \frac{(Rb,\ R2\ Combined\ resistance)}{(Ra,\ R1\ Combined\ resistance) + (Rb,\ R2\ Combined\ resistance)} \times VREF \doteqdot 0.80\ V \pm 0.13\%$$

$$DUTY\ (ON)\ Max \doteqdot \frac{Vdt - 0.4\ V}{0.5\ V} \times 100\ (\%) \doteqdot 80\% \pm 0.2\% \cdots\cdot\ (2)$$

Based on (1) and (2) above, selecting external resistances to 1/10th or less of the built-in resistance enables the built-in resistance to be ignored.

As for the duty dispersion, please expect ±5% at (fosc = 1 MHz) due to the dispersion of a triangular wave amplitude.

Processing When Not Using ch.4 INV AMP

Short-circuit the - INA terminal (pin 19) and OUTA terminal (pin 18) in the shortest distance when not using ch.4 INV Amp.

Figure 7. When not using ch.4 INV Amp