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MB39A130A

1ch DC/DC Buck Converter IC with Synchronous Rectification

Description

MB39A130A is a 1ch DC/DC Buck converter equipped with a bottom detection comparator and N-ch/N-ch synchronous rectification. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. MB39A130A realizes ultra-rapid response and high efficiency with built-in enhanced protection features.

Features

- Power conversion efficiency :96% (Max.)
- Adjustable frequency setting by an external resistor :100 kHz to 600 kHz
- High accuracy reference voltage : ±1.0%
- Output voltage setting range :0.7 V to 5 V or fixed to 1.2 V/2.5 V
- Adjustable output voltages setting by the external control
- Input voltage range (V_{IN}) :4.5 V to 25 V
- Inductor saturation detection function which can be set optional
- Built-in over voltage protection function
- Built-in under voltage protection function
- Built-in over current protection function
- Built-in Power-Good detection function
- Built-in over temperature protection function
- Built-in soft-start circuit without load dependence
- Built-in discharge control circuit
- Built-in synchronous rectification type output driver for N-ch MOS FET
- Standby current : 0 [µA] (Typ.)
- Small package : TSSOP-24 (4.4 × 6.5 [mm])

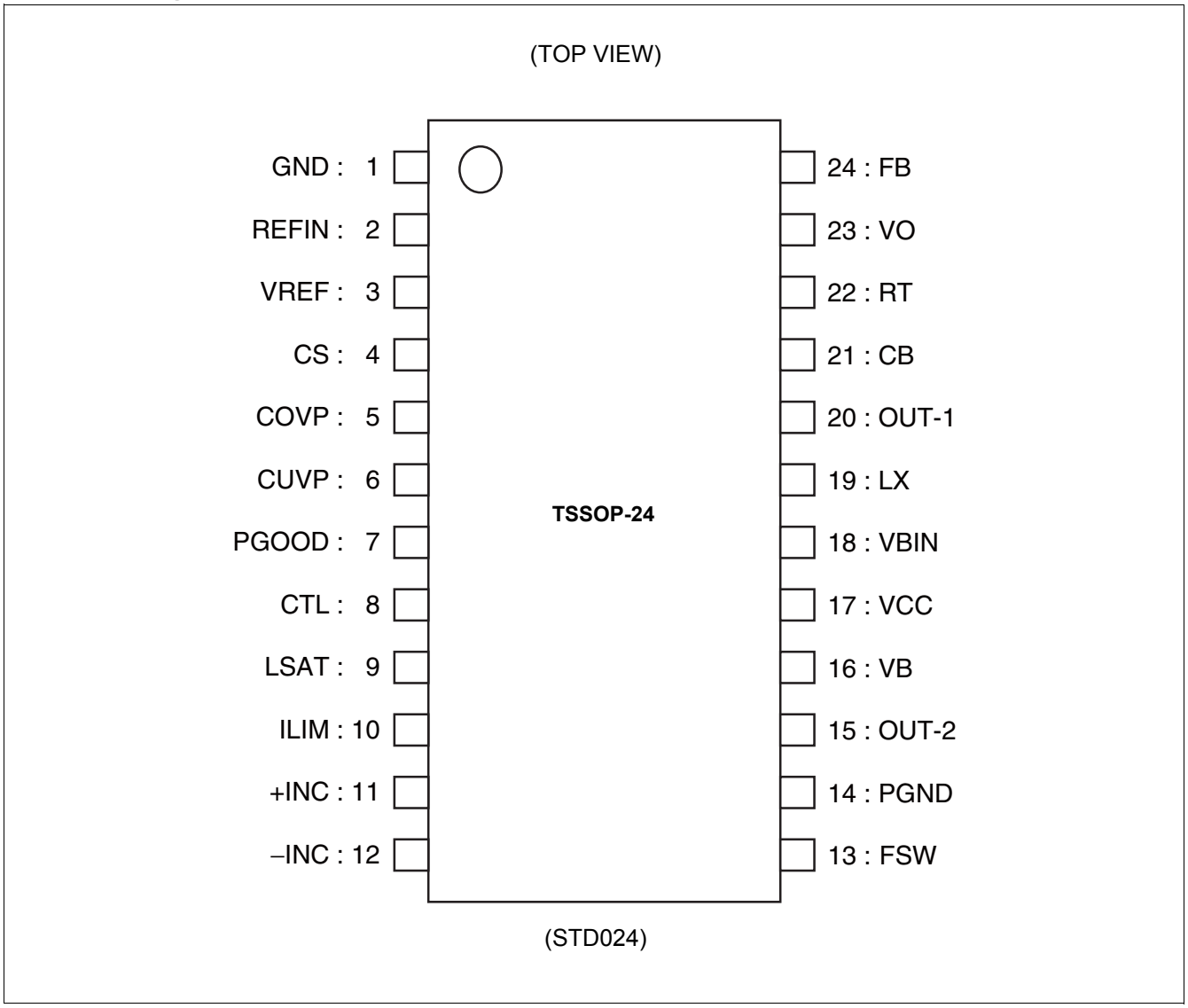
Applications

- Digital TV
- Photocopiers
- STB
- BD, DVD players/recorders
- Projectors

Various other advanced devices

Contents

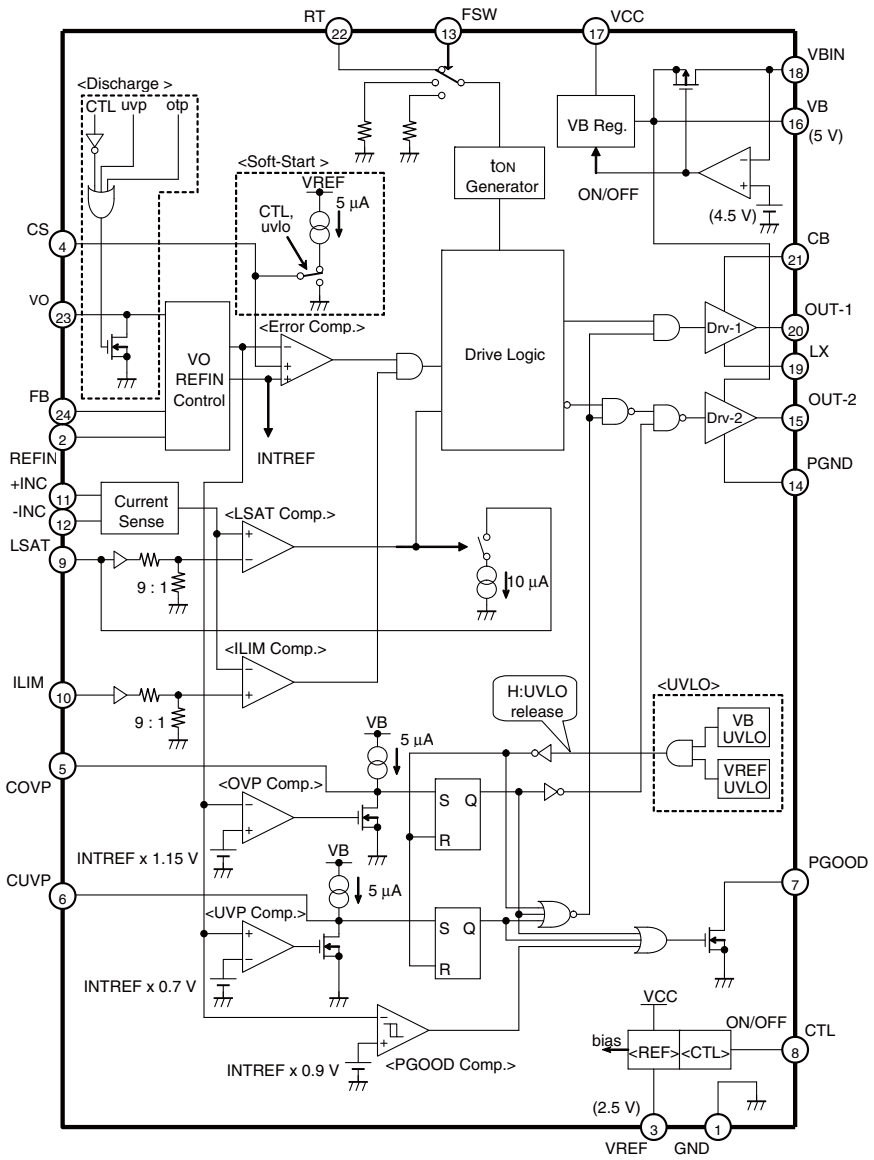
1. Pin Assignment



2. Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	GND	-	Ground pin.
2	REFIN	I	Reference voltage input pin for Error Comp.
3	VREF	O	Reference voltage output pin.
4	CS	I	Soft-start time setting capacitor connection pin.
5	COVP	-	Detection time setting capacitor connection pin for OVP function. The OVP function can be disabled by a short circuit with GND pin.
6	CUVP	-	Detection time setting capacitor connection pin for UVP function. The UVP function can be disabled by a short circuit with GND pin.
7	PGOOD	O	Power-Good detection circuit output pin. (Open-drain output)
8	CTL	I	Power supply control pin. IC changes to standby state when CTL is set to “L” level.
9	LSAT	I	Inductor oversaturation detection level setting voltage input pin.
10	ILIM	I	Over current detection level setting voltage input pin.
11	+INC	I	Current detection block (Current Sense) input pin.
12	-INC	I	Current detection block (Current Sense) input pin.
13	FSW	I	Preset value switching pin for operating frequency.
14	PGND	-	Ground pin for output circuit.
15	OUT-2	O	Output pin for external low-side FET gate drive.
16	VB	O	Bias output pin for output circuit.
17	VCC	-	Power supply pin.
18	VBIN	I	Bias voltage external input pin for output circuit and control circuit.
19	LX	-	Inductor and external high-side FET source and external low-side FET drain connection pin.
20	OUT-1	O	Output pin for external high-side FET gate drive.
21	CB	-	Connection pin for boot strap capacitor. It connects a capacitor between CB and LX pins.
22	RT	-	Connection pin for t_{ON} time setting resistor.
23	VO	I	Input pin for DC/DC output voltage.
24	FB	I	Feedback pin for DC/DC output voltage.

3. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	—	—	27	V
CB pin input voltage	V_{CB}	—	—	32	V
Voltage between CB and LX	V_{CBLX}	—	—	7	V
Bias external input voltage	V_{BIN}	—	—	7	V
Control input voltage	V_I	CTL pin	—	27	V
Input voltage	V_I	FB, VO, REFIN, FSW pins	—	VB + 0.3	V
	V_{+INC}	—	—	27	V
	V_{-INC}	—	—	27	V
	V_{ILIM}	—	—	VB + 0.3	V
	V_{LSAT}	—	—	VB + 0.3	V
PGOOD pin voltage	V_{PG}	—	—	7	V
Output current	I_{OUT}	DC	—	60	mA
Power dissipation	P_D	Ta ≤ + 25°C	—	1315	mW
Storage temperature	T_{STG}	—	-55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	—	4.5	—	25.0	V
CB pin input voltage	V_{CB}	—	—	—	30	V
Reference voltage output current	I_{REF}	—	-100	—	0	µA
Bias output current	I_{VB}	—	-1	—	—	mA
CTL pin input voltage	V_I	CTL pin	0	—	25	V
Input voltage	V_I	FB, VO, REFIN, FSW pins	0	—	VB	V
	V_{+INC}	—	-0.3	—	+ 2.9	V
	V_{-INC}	—	-0.3	—	+ 25	V
	V_{ILIM}	—	0	—	VB	V
	V_{LSAT}	—	0	—	VB	V
PGOOD pin output voltage	V_{PG}	—	0	—	5.5	V
PGOOD pin output current	I_{PG}	—	0	—	4	mA
Peak output current	I_{OUT}	Duty≤5% ($t = 1/f_{OSC} \times Duty$)	-1200	—	+ 1200	mA
Operation frequency range	f_{OSC}	—	100	450	780	kHz
Timing resistor	R_T	—	—	43	—	kΩ
Current detection resistor	R_S	—	—	10	—	mΩ
Soft start capacitor	C_S	—	—	0.018	—	µF
CB pin capacitor	C_{CB}	—	—	0.1	—	µF
Reference voltage output capacitor	C_{REF}	—	—	0.01	1.0	µF
Bias voltage output capacitor	C_{VB}	—	—	2.2	10	µF
Operating ambient temperature	Ta	—	-30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

6. Electrical Characteristics

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [REF]	Output voltage	V_{REF}	3	—	2.463	2.500	2.537	V
	Load stability	Load	3	VREF pin = 0 µA to -100 µA	—	1	10	mV
	Short-circuit output current	I_{OS}	3	VREF pin = 0 V	-20	-10	-5	mA
Bias Voltage Block [VB Reg.]	Output voltage	V_B	16	—	4.9	5.0	5.1	V
	Inside/Outside switching threshold	V_{TLH}	18	VBIN pin ↑	4.3	4.5	4.7	V
		V_{THL}	18	VBIN pin ↓	4.1	4.3	4.5	V
	Switch (SW) resistor	R_{SW}	18	VBIN pin = 5 V	—	4*1	—	Ω
Under voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	16	VB pin	3.8	4.0	4.2	V
		V_{THL}	16	VB pin	3.1	3.3	3.5	V
	Hysteresis width	V_H	16	VB pin	—	0.7*1	—	V
	Threshold voltage	V_{TLH}	3	VREF pin	1.8	2.0	2.2	V
		V_{THL}	3	VREF pin	1.6	1.8	2.0	V
	Hysteresis width	V_H	3	VREF pin	—	0.2*1	—	V
Soft-Start/Discharge Block [Soft-Start/ Discharge]	Charge current	I_{CS}	4	CTL pin = 5 V, CS pin = 0 V	-6.3	-4.5	-3.1	µA
	Electrical discharge resistance	R_D	23	CTL pin = 0 V, VO pin ≥ 0.3 V	—	16*1	—	Ω
	Discharge end voltage	V_O	23	CTL pin = 0 V	—	0.3*1	—	V
ON/OFF Time Generator Block [t_{ON} Generator]	ON time	t_{ON}	20	RT pin = 43 kΩ, FSW pin = GND, VCC pin = 15 V, VO pin = 1.5 V	246	280	314	ns
	ON time (Preset value 1)	t_{ON_2}	20	RT pin = GND, FSW pin = VREF pin, VCC pin = 15 V, VO pin = 1.5 V	272	390	508	ns
	ON time (Preset value 2)	t_{ON_3}	20	RT pin = GND, FSW pin = VB pin, VCC pin = 15 V, VO pin = 1.5 V	142	220	298	ns
	Minimum OFF time	t_{OFF}	20	—	360	480	600	ns
	R_T external condition	V_{FSW1}	13	FSW pin	0	—	1.5	V
	Preset value 1 condition	V_{FSW2}	13	FSW pin	1.5	VREF	VB-1.5	V
	Preset value 2 condition	V_{FSW}	13	FSW pin	VB-1.5	—	VB	V
	Input current	I_{FSWL}	13	FSW pin = 0 V	-10	-5	—	µA
		I_{FSWM}	13	FSW pin = VREF pin	-1	0	+1	µA
		I_{FSWH}	13	FSW pin = VB pin	—	5	10	µA

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Voltage Setting Block [VO REFIN Control, Error Comp.]	Output bottom detection voltage	V_{O1}	23	REFIN pin = GND pin, FB pin = VB pin	1.172	1.190	1.208	V
		V_{O2}	23	REFIN pin = VB pin, FB pin = VB pin	2.453	2.490	2.527	V
	Feedback voltage	V_{FB1}	24	REFIN pin = GND pin	0.693	0.700	0.707	V
		V_{FB1T}	24	REFIN pin = GND pin*3, Ta = -20°C to +70°C	0.689*2	0.700	0.711*2	V
		V_{FB2}	24	REFIN pin = VB pin	1.442	1.457	1.472	V
		V_{FB2T}	24	REFIN pin = VB pin*3, Ta = -20°C to +70°C	1.435*2	1.457	1.479*2	V
	REFIN input current	I_{REFIN}	2	REFIN pin = 0.6 V	-0.5	0	+0.5	µA
	FB input current	I_{FB}	24	FB pin = 0.7 V	-0.5	0	+0.5	µA
	VO input current	I_{VO}	23	VO pin = 2 V	—	17.0	24.3	µA
	Threshold voltage	V_{TH1}	24,2	REFIN, FB pins : Hi-side	2.4	2.5	—	V
		V_{TH2}	2	REFIN pin : Lo-side	—	0.3	0.4	V
Current Detection Block [Current Sense]	Input current	I_{INC}	11,12	+INC, -INC pins = 0	-1.0	-0.3	—	µA
Over Current Detection Block [ILIM Comp.]	Current limit setting value	V_{TH}	11,12	(+INC pin) - (-INC pin) ILIM pin = 5 V Internally fixed value	40	50	60	mV
		V_{TH2}	11,12	(+INC pin) - (-INC pin) ILIM pin = 1.0 V Externally fixed value	90	100	110	mV
	Input current	I_{ILIM}	10	ILIM pin = 0 V	-1	0	+1	µA
	Threshold voltage	V_{TH3}	10	ILIM pin	3.5	3.7	—	V
Inductor Saturation Detection Block [LSAT Comp.]	Oversaturation detection setting value	V_{TH}	11,12	(+INC pin) - (-INC pin) LSAT pin = 2.0 V	180	200	220	mV
	Input current	I_{LSAT}	9	LSAT pin = 0 V	-1	0	+1	µA
	LSAT pin sink current at detection of oversaturation	I_{LSAT2}	9	LSAT pin = 1 V	7.7	10.0	14.3	µA

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Over-voltage Protection Circuit Block [OVP Comp.]	Over-voltage detecting voltage	V_{OVP}	24	Error Comp. input	INTREF ×1.12	INTREF ×1.15	INTREF ×1.18	V
	Charge current	I_{COVP}	5	—	-7.7	-5.5	-4.1	µA
	Threshold voltage	V_{TH}	5	COVP pin	—	VB×0.5	—	V
	COVP pin on-resistance	R_{COVP}	5	—	—	1.1*1	—	kΩ
Under-voltage Protection Circuit Block [UVP Comp.]	Under-voltage detecting voltage	V_{UVP}	24	Error Comp. input	INTREF ×0.65	INTREF ×0.70	INTREF ×0.75	V
	Charge current	I_{CUVP}	6	—	-7.7	-5.5	-4.1	µA
	Threshold voltage	V_{TH}	6	CUVP pin	—	VB×0.5	—	V
	CUVP pin on-resistance	R_{CUVP}	6	—	—	1.1*1	—	kΩ
Power-Good Detection Circuit Block [PGOOD Comp.]	Threshold voltage	V_{THL}	24	Error Comp. input	INTREF ×0.87	INTREF ×0.90	INTREF ×0.93	V
	Hysteresis width	VH	24	Error Comp. input	—	INTREF×0.02*1	—	V
	Output leak current	I_{LEAK}	7	PGOOD pin = 5 V	—	0	1	µA
	“L” level output voltage	V_{OL}	7	PGOOD pin = 1 mA	—	0.1	0.4	V
Over-temperature Protection Circuit Block [OTP]	Protection temperature	T_{OTPH}	—	—	—	+150*1	—	°C
		T_{OTPL}	—	—	—	+125*1	—	°C

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Block [Drv-1, Drv-2]	High-side output on-resistance	R_{OH}	20	OUT–1 pin = – 100 mA	—	4	7	Ω
		R_{OL}	20	OUT–1 pin = 100 mA	—	1.0	3.5	Ω
	Low-side output on-resistance	R_{OH}	15	OUT–2 pin = –100 mA	—	4	7	Ω
		R_{OL}	15	OUT–2 pin = 100 mA	—	1.0	3.5	Ω
	Output source current	I_{SOURCE}	15,20	LX pin = 0 V, CB pin = 5 V, OUT–1, OUT–2 pins = 2.5 V, Duty ≤ 5%	—	–0.5*1	—	A
	Output sink current	I_{SINK1}	20	LX pin = 0 V, CB pin = 5 V, OUT-1 pin = 2.5 V, Duty ≤ 5%	—	0.9*1	—	A
		I_{SINK2}	15	OUT-2 pin = 2.5 V, Duty ≤ 5%	—	1.8*1	—	A
	Dead time	T_D	15,20	LX pin = 0 V, CB pin = 5 V	—	50*1	—	ns
Control Block [CTL]	ON condition	V_{ON}	8	—	2	—	25	V
	OFF condition	V_{OFF}	8	—	0	—	0.8	V
	Input current	I_{CTLH}	8	CTL pin = 5 V	—	25	40	µA
		I_{CTLL}	8	CTL pin = 0 V	—	0	1	µA
General	Standby current	I_{CCS}	17	CTL pin = 0 V	—	0	10	µA
	Power-supply current	I_{CC1}	17	CTL pin = 5 V, REFIN pin = GND pin, LX pin = 0 V, FB pin = 1.0 V	—	1.3	2.2	mA
		I_{CC2}	17	CTL pin = 5 V, LX pin = 0 V, FB pin = 1.0 V, VBIN pin = 5 V	—	130	220	µA

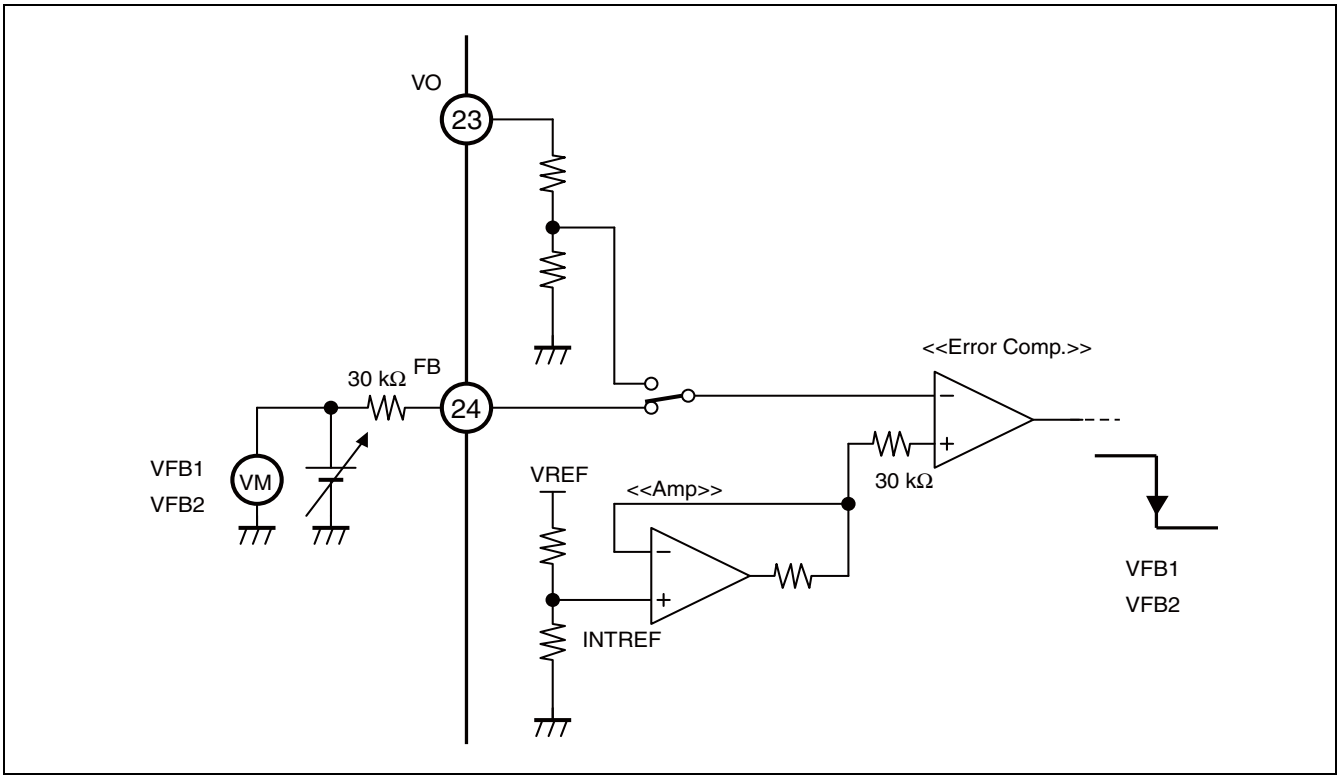
*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: This parameter is guaranteed by design, which is not supported by a final test.

*3: For the measurement circuit, see the “ Diagram of Feedback Voltage Measurement Circuit”.

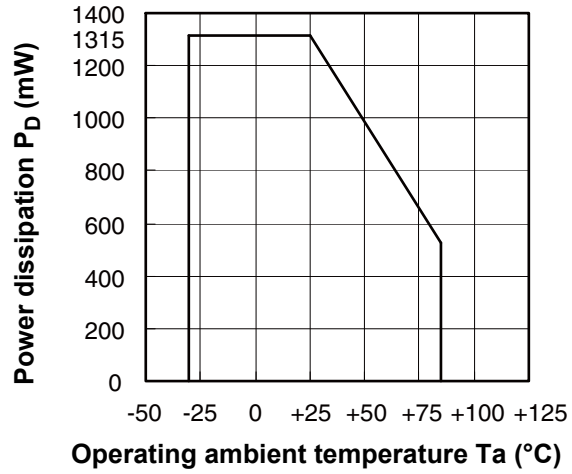
7. Diagram of Feedback Voltage Measurement Circuit

- VFB1,VFB2

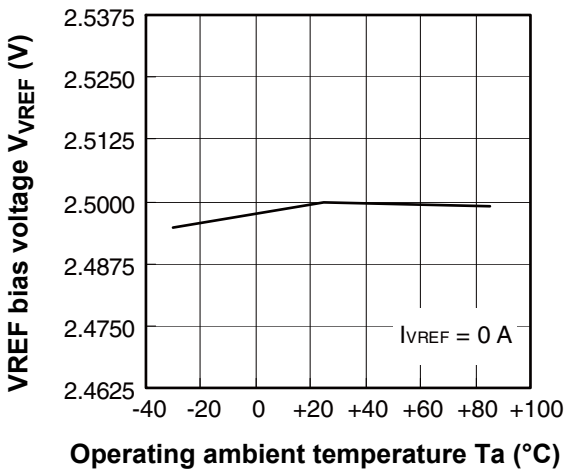


8. Typical Characteristics

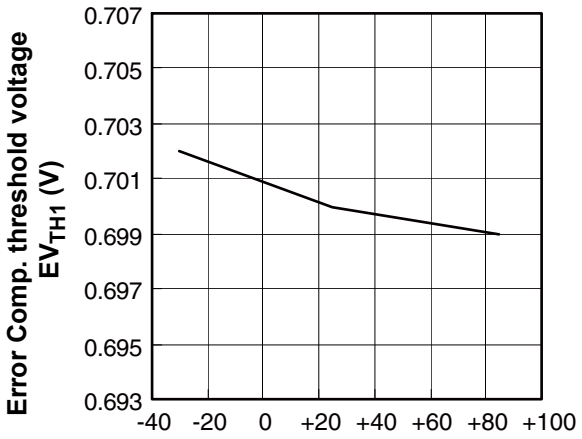
Power dissipation vs.
Operating ambient temperature



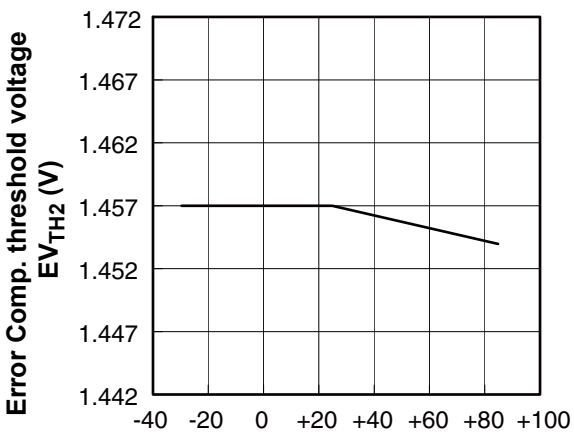
VREF bias voltage vs.
Operating ambient temperature



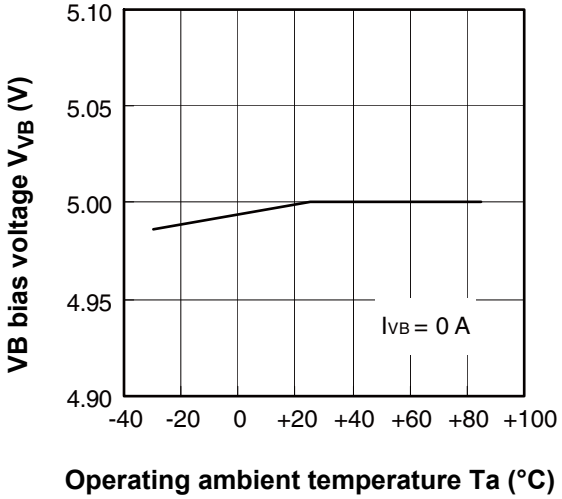
Error Comp. threshold voltage vs.
Operating ambient temperature



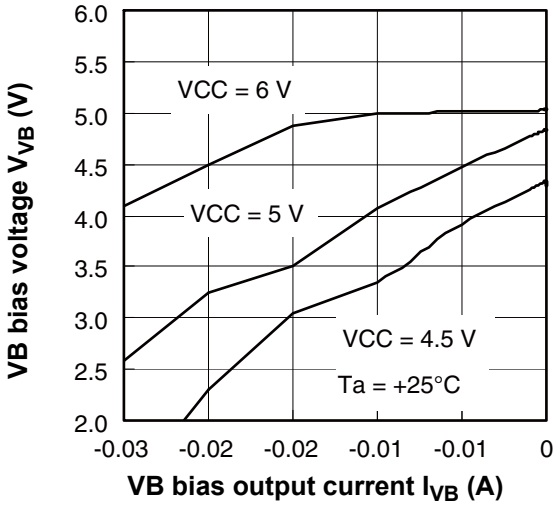
Error Comp. threshold voltage vs.
Operating ambient temperature



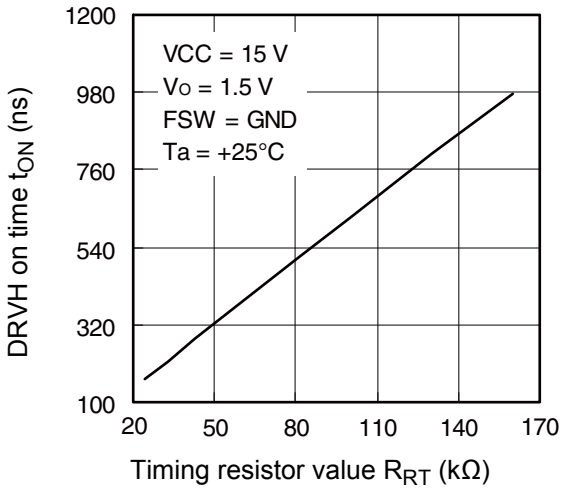
VB bias voltage vs. Operating ambient temperature



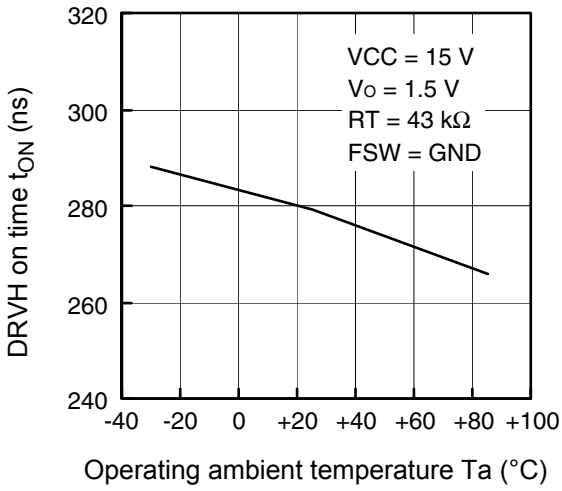
VB bias voltage vs. VB bias output current



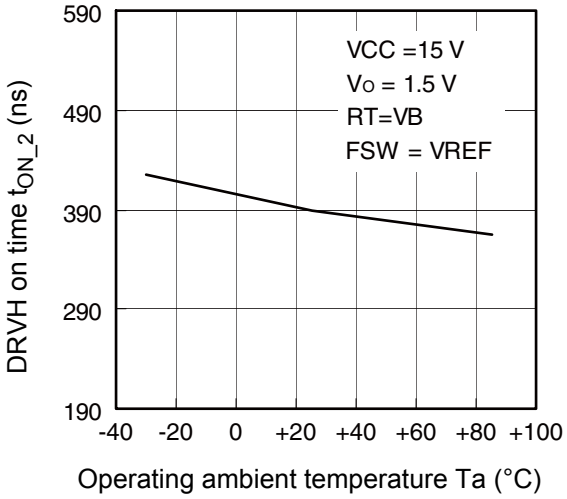
DRVH on time vs. Timing resistor value



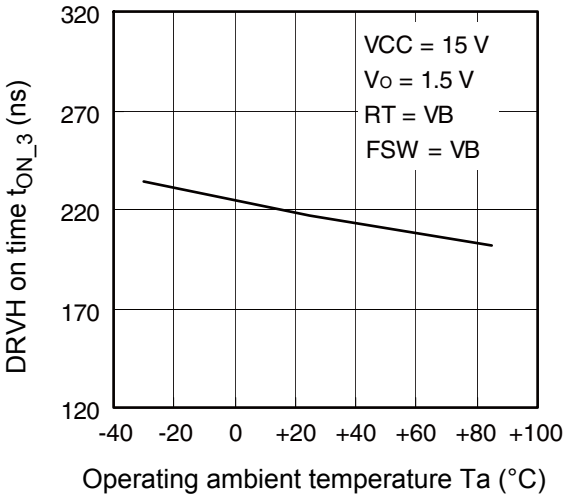
DRVH on time vs. Operating ambient temperature



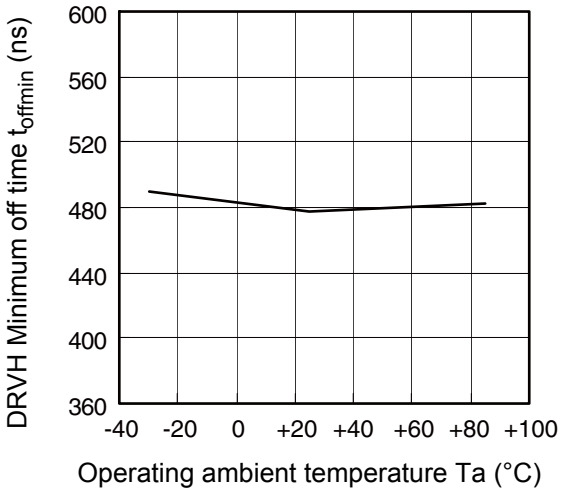
DRVH on time vs.
Operating ambient temperature



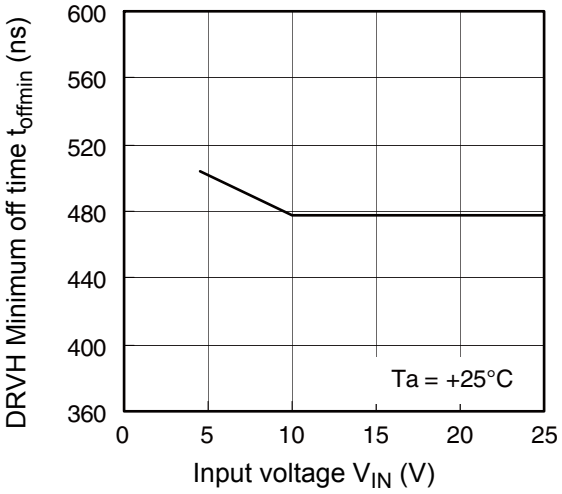
DRVH on time vs.
Operating ambient temperature

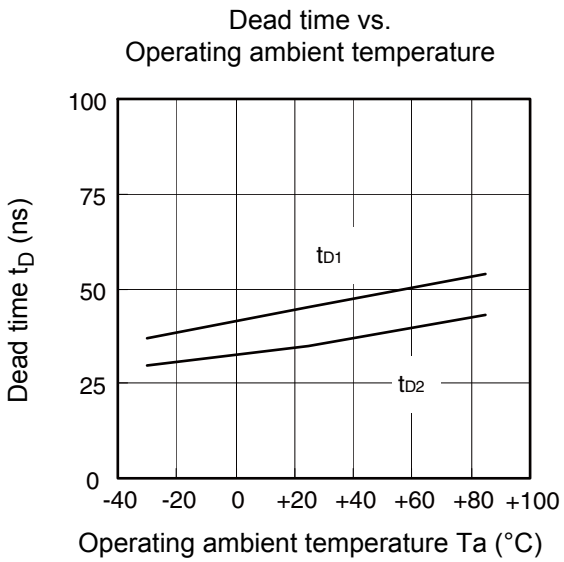


DRVH Minimum off time vs.
Operating ambient temperature



DRVH Minimum off time vs.
Input voltage




Dead time vs.
Operating ambient temperature
Dead time t_D (ns)
100
75
50
25
0
t_{D1}
t_{D2}
-40
-20
0
+20
+40
+60
+80
+100
Operating ambient temperature Ta (°C)

9. Function

Bottom detection comparator system

The bottom detection comparator system uses fixed ON time (t_{ON}) and the switching ripple voltage which superimposed the output voltage (V_O) , instead of a certain triangular waveform.

The t_{ON} time is uniquely defined by the power supply voltage (V_{IN}) and the output voltage (V_O) .

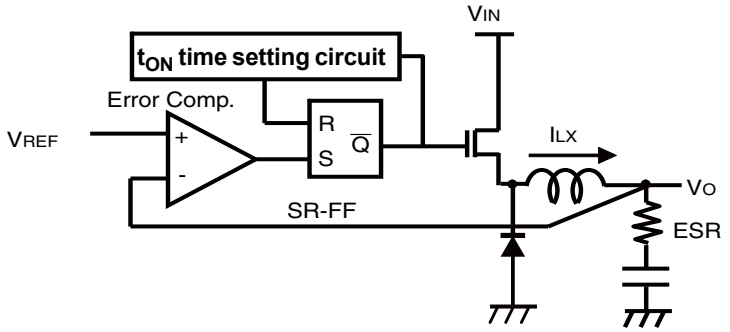
During the t_{ON} period, a current is supplied from the power supply voltage (V_{IN}) . This results in an increased inductor current (I_{LX}). And also an increased output voltage (V_O) due to the parasitic resistance (ESR) of the output capacitor.

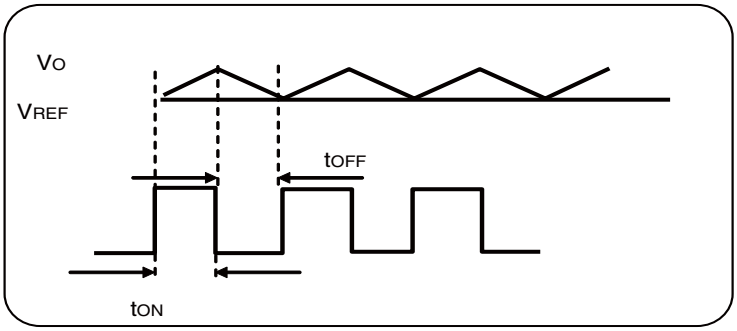
And when the t_{OFF} period arrives, the energy accumulated in the inductor is supplied to the load to decrease the inductor current (I_{LX}) gradually. Consequently, the output voltage (V_O) , which has been increasing due to the parasitic resistance (ESR) of the output capacitor, also decreases.

When the output voltage goes below a certain V_{REF} potential, SR-FF is set and the t_{ON} period comes back.

Switching is repeated as described above. Error Comp. is used to compare the reference voltage (VREF) with the output voltage (V_O) to control the off-duty condition in order to stabilize the output voltage.

Bottom Detection Comparator Model





9.1 Reference Voltage Block (REF)

The reference voltage block (REF) generates a temperature-compensated stable voltage (2.5 V Typ.) based on the voltage supplied from the VCC pin (Pin 17) . It is used as the reference power supply for the IC's internal circuit.

The reference voltage is output from the VREF pin (Pin 3), and up to 100 µA can be supplied to the outside as the maximum load current.

9.2 Under Voltage Lockout Protection Circuit Block (UVLO)

A bias voltage (V_B) , a transitional state at startup, or a sudden drop in an internal reference voltage (V_{REF}) leads to malfunction of the control IC, causing system destruction/deterioration. To prevent such malfunction, the under voltage lockout protection circuit detects a voltage drop at the VB pin (Pin 16) or the VREF pin (Pin 3) and fixes the OUT-1 pin (Pin 20) and the OUT-2 pin (Pin 15) to the "L" level. When voltages at the VB pin and the VREF pin exceed the threshold voltage of the under voltage lockout protection circuit, the system is restored.

Table of Protection Circuit (VB-UVLO, VREF-UVLO) Operation Functions

The logics of the following pins are fixed during UVLO operation (when VB and VREF voltages are below the UVLO threshold voltage) .

OUT-1	OUT-2	CS	OVP	UVP
L	L	L	Latch reset COVP = L	Latch reset CUVP = L

9.3 Soft-start Block (Soft-Start)

It prevents a rush current or an output voltage (V_O) overshooting at the output start.

It prevents a rush current at start-up by connecting a capacitor to the CS pin (Pin 4) .

When the CTL pin (Pin 8) is set to the "H" level, the capacitor connected to the CS pin starts charging and its lamp voltage is input to the error comparator (Error Comp.) . This allows for the setting of the soft-start time that does not depend on the output load of the DC/DC converter.

9.4 Discharge Block (Discharge)

It discharges electrical charges stored in a smoothing capacitor at output stop. When the CTL pin (Pin 8) is set to the "L" level, the OUT-1 pin (Pin 20) and the OUT-2 pin (Pin 15) are set to the "L" level and turn on the discharging FET (RON ≈ 16 Ω) which is connected between the VO pin (Pin 23) and GND. When the voltage at the VO pin falls below 0.3 V, the discharging FET is turned off and the IC changes to standby state. The discharge function also operates after the under-voltage protection circuit block (UVP Comp.) is latched or when the over-temperature protection circuit block is in operation.

9.5 ON/OFF Time Generator Block (t_{ON} Generator)

The ON time generator block (t_{ON} Generator, ON ONE-SHOT) has a built-in capacitor for timing setting. When the FSW pin (Pin 13) is connected to GND, ON time that is dependent on the input voltage is generated by connecting a timing setting resistor to the RT pin (Pin 22) .

$$t_{ON} = \frac{V_O}{V_{CC}} \times R_T \times 0.059 + 30$$

t_{ON} : ON time on high-side FET [ns]
R_T : Timing resistor value [Ω]
V_{CC} : Power supply voltage [V]
V_O : Output voltage [V]

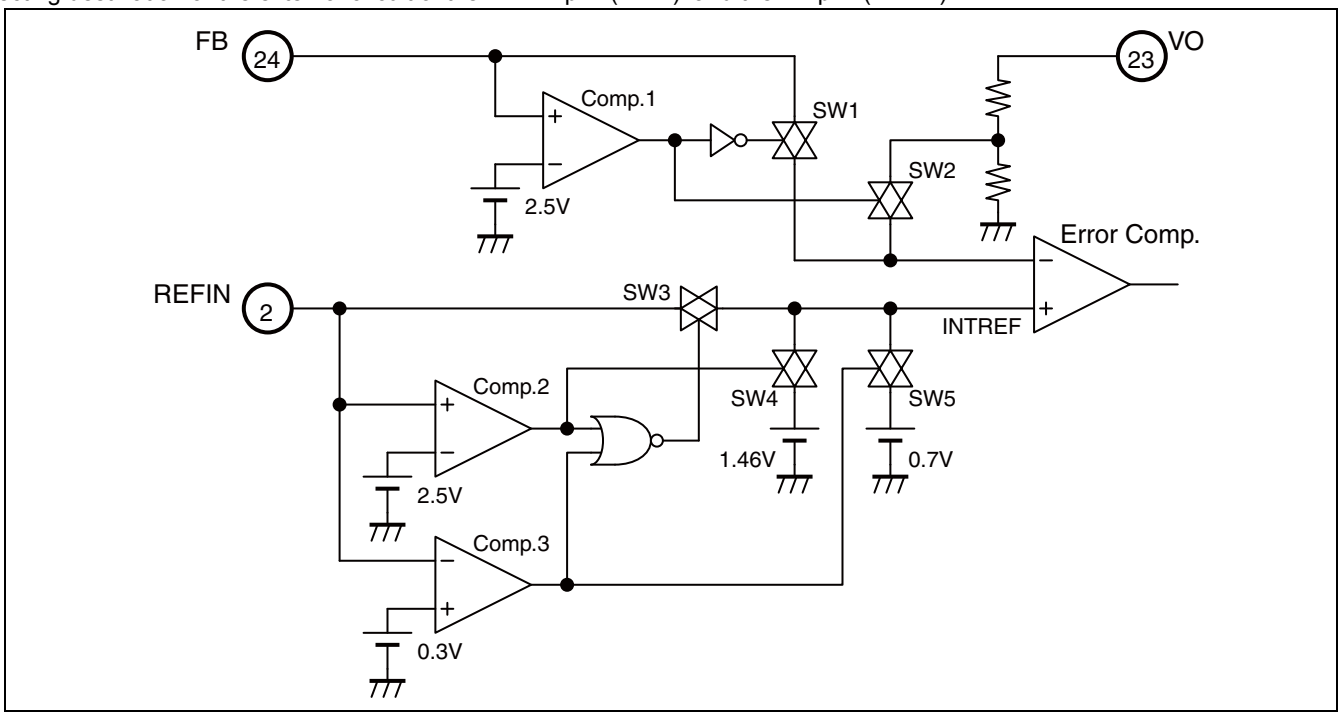
If the V_O1 and V_O2 voltages are 0.1 V or less at soft-start, it is fixed in a value at 0.1V in V_O1 and V_O2 in ON time.
In addition, the FSW pin can be used to switch the ON time setting between the setting by the resistor that is externally connected to the RT pin and the setting by the IC's internal resistor.
The OFF time generator block (OFF ONE-SHOT) generates 480[ns] (Typ.) as the minimum OFF time.

$$t_{OFF} = \left(\frac{V_{CC}}{V_O} - 1 \right) \times t_{ON}$$

t_{ON} : ON time on high-side FET [ns]
V_{CC} : Power supply voltage [V]
V_O : Output voltage [V]

9.6 Output Voltage Setting Block (VO REFIN Control, Error Comp.)

The output voltage setting block (VO REFIN Control, Error Comp.) supports the setting of various output voltages according to connecting destination or the external circuit of the REFIN pin (Pin 2) and the FB pin (Pin 24) .



Output Voltage Setting Table

REFIN	FB	SW state	INTREF (Internal Reference Voltage)	Remarks
GND	VB	SW2,5:ON, SW1,3,4:OFF	0.7 V (Typ.)	VO = 1.2 V set (internal setting)
VB	VB	SW2,4:ON, SW1,3,5:OFF	1.46 V (Typ.)	VO = 2.5 V set (internal setting)
GND	0.7 V	SW1,5:ON, SW2,3,4:OFF	0.7 V (Typ.)	Internal reference voltage fixed to 0.7 V, output voltage setting discretionary by external resistor value ratio between VO-FB and between FB-GND
VB	1.457 V	SW1,4:ON, SW2,3,5:OFF	1.457 V (Typ.)	Internal reference voltage fixed to 1.457 V, output voltage setting discretionary by external resistor value ratio between VO-FB and between FB-GND
0.5 V to 2.2 V	VB	SW2,3:ON, SW1,4,5:OFF	= REFIN pin voltage	The reference voltage can be discretionary set by the external resistor value ratio between VREF-REFIN and between REFIN-GND, and the built-in feedback resistor for the output setting is used.

Error Comp. detects the end timing of the OFF period by comparing the non-inverting input and inverting input. In other words, it detects that the output voltage has fallen below the output setting voltage, and puts the output in ON state. In this case, the delay time is 100 ns (Typ.) .

9.7 Current Detection Block (Current Sense)

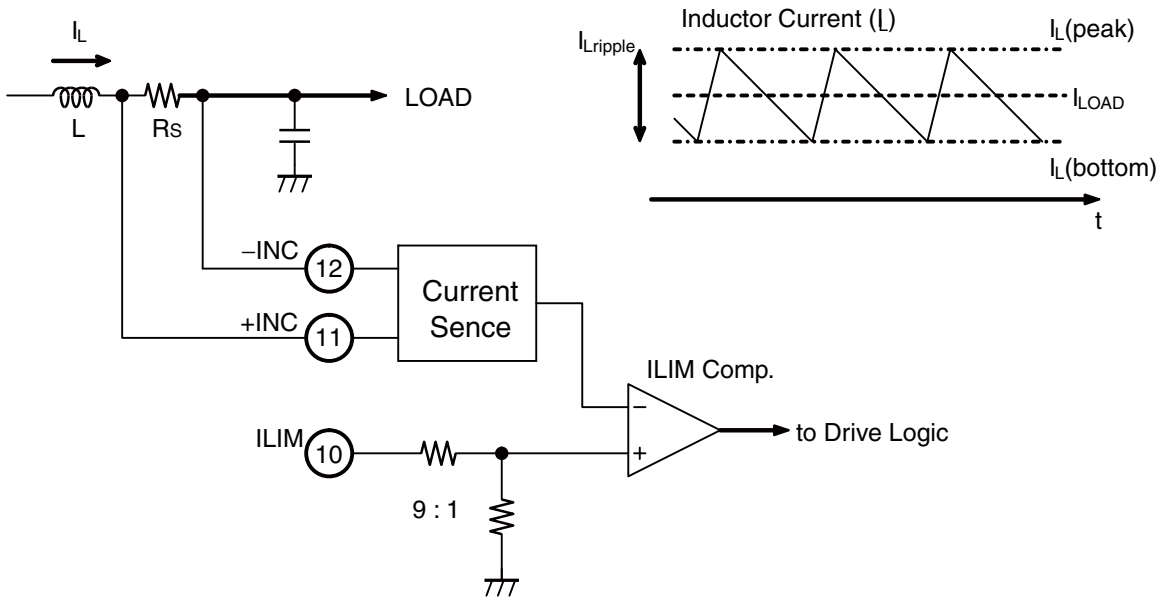
This circuit is used to detect a inductor current (I_L) . The current detection block (Current Sense) converts a voltage waveform between the +INC pin (Pin 11) and the -INC pin (Pin 12) into the GND-standard voltage waveform. Therefore, it can detect a ripple current of the inductor by the current sense resistor R_S connected between the +INC and -INC pins.

9.8 Over Current Detection Block (ILIM Comp.)

Comparing the current value of the current sense resistor and the setting value of over current detection starts the over current protection operation. The over current detection block (ILIM Comp.) compares the output voltage waveform in the current detection block and the over current detection level which is 1/10 of the voltage externally set to the ILIM pin (Pin 10). The over current detection block detects the bottom value of the ripple current which flows into the inductor. The OFF state has been kept until the output voltage waveform in the current detection block goes down below the over current detection level, and the ON state of the high-side FET is permitted when the waveform goes down below the level. This is the protection operation against the over current. The protection operation is the operation which drops the output voltage.

Moreover, the over current detection level can be set to a fixed value (50 mV Typ.) by applying 3.8 V (Typ.) or more voltage to the ILIM pin.

- Current detection block / Over current detection block



Rs : Current sense resistor

9.9 Inductor Saturation Detection Block (LSAT Comp.)

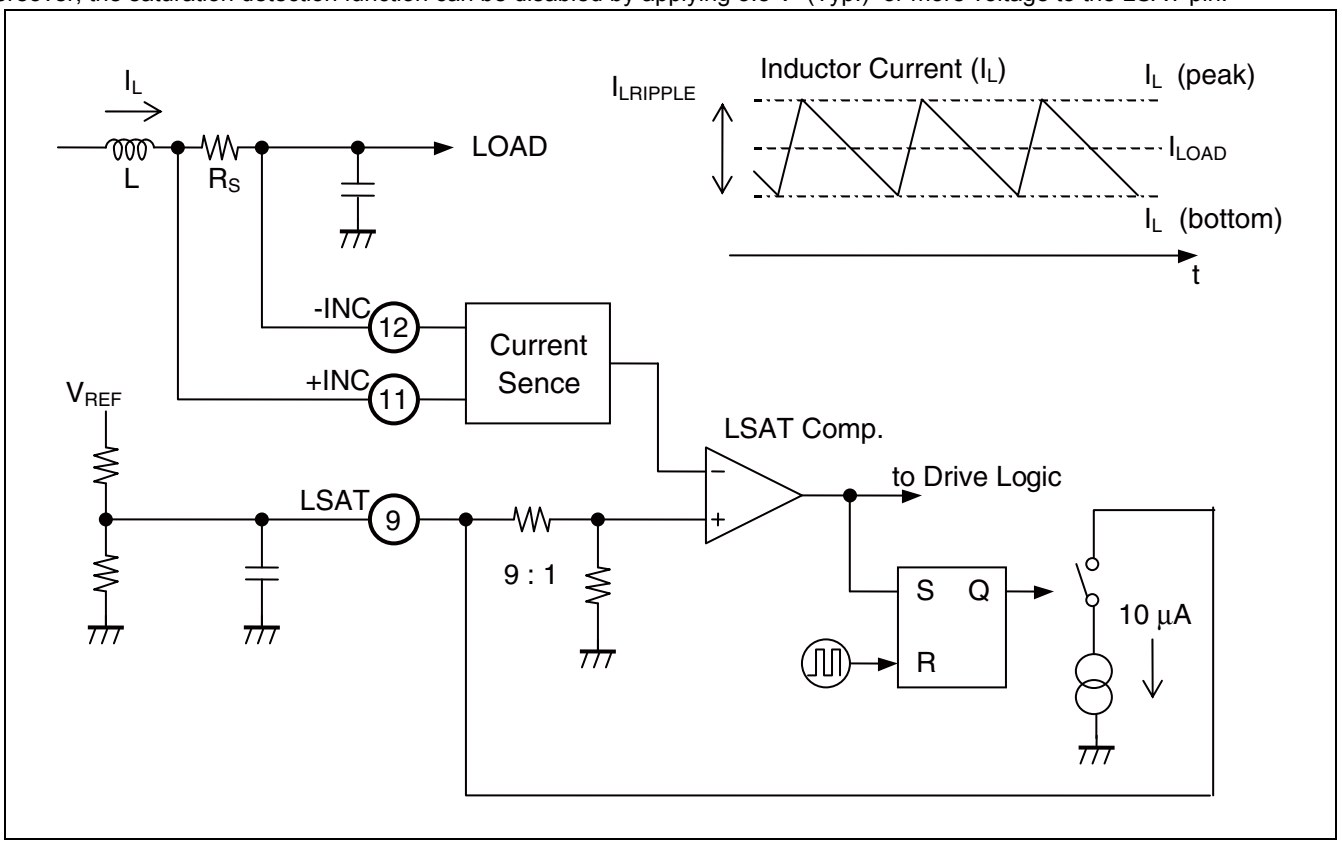
As an auxiliary function for over current protection, this circuit prevents the occurrence of excessive currents due to magnetic saturation of the inductor.

The inductor saturation detection block (LSAT Comp.) compares the output voltage waveform of the current detection block (Current Sense) with 1/10 of the saturation detection level of the voltage externally set to the LSAT pin (Pin 9) and detects the peak value of the ripple current that flows to the inductor.

During the ON period of high-side FET, the output voltage waveform of the current detection block exceeds the saturation detection level, immediately after it detected that it sets an OFF-state. Simultaneously, it also sets an SR latch in LSAT Comp. and sinks 10 µA (Typ.) of a constant current from the LSAT pin. This SR latch is reset in every cycle and the same operation is repeated. The saturation detection level goes down by sinking the electric charge of the capacitor connected to the LSAT pin in every cycle.

Depending on the external parts or use conditions, the ILIM and LSAT pins must be set to various voltages; therefore, the detection level can be set freely by the external resistor value ratio.

Moreover, the saturation detection function can be disabled by applying 3.8 V (Typ.) or more voltage to the LSAT pin.



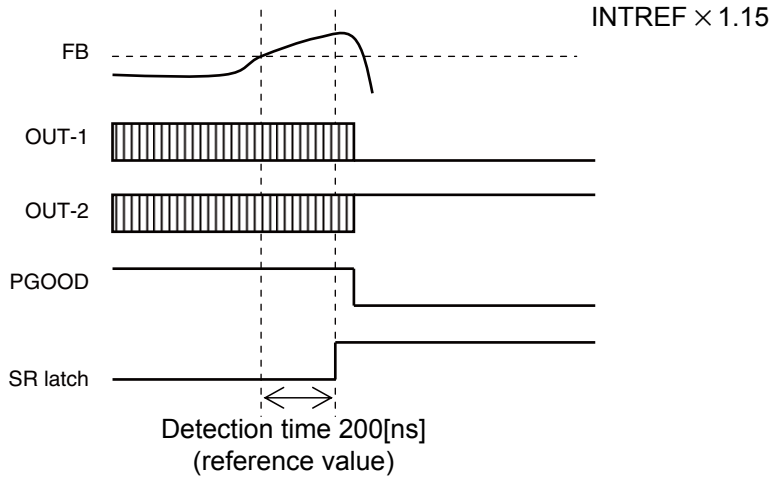
9.10 Over-voltage Protection Circuit Block (OVP Comp.)

The circuit protects an output connecting device when the output voltage (V_O) rises.
This function is that 1.15 times (Typ.) of the internal reference voltage (INTREF) that is set by the output voltage setting block (VO REFIN Control) is compared with the voltage that is inverting-input into Error Comp. If the thing that the inverting-input-voltage into Error Comp. has gone up is detected, an SR latch is set, each pin's logic is fixed as described in “Function table when the over-voltage protection circuit block is in operation”, and the voltage output is stopped.

- Function table when the over-voltage protection circuit block is in operation

OUT-1	OUT-2	CS	PGOOD
L (High-side FET : OFF)	H (Low-side FET : ON)	L	L

- Timing chart example for over-voltage protection operation (PGOOD pulled up to VB)



The over-voltage protection state can be cancelled by setting the IC to standby state first and then resetting the latch using the UVLO signal. Also, the over-voltage protection function can be disabled by causing a short between the COVP pin (Pin 5) and the GND pin (Pin 1).

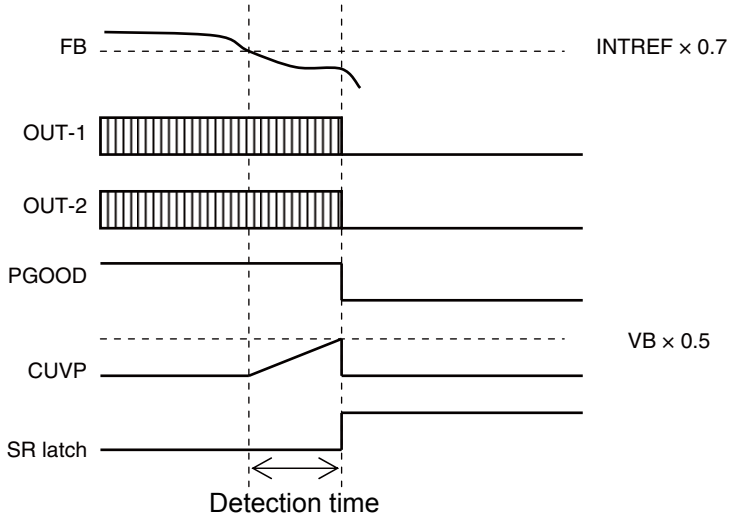
9.11 Under-voltage Protection Circuit Block (UVP Comp.)

It protects an output connecting device by stopping the output when the output voltage (V_O) drops.
This function is that 0.7 times (Typ.) of the internal reference voltage (INTREF) that is set by the output voltage setting block (VO REFIN Control) is compared with the voltage that is inverting-input into Error Comp. If the thing that the inverting input-voltage into Error Comp. has dropped is detected, the capacitor connected to the CUVP pin (Pin 6) starts charging.
When the voltage at the CUVP pin rises and an SR latch is set in UVP Comp., the PGOOD pin (Pin 7) is set to the "L" level and discharge operation is performed to stop the voltage output.

- Function table when the under-voltage protection circuit block is in operation

OUT-1	OUT-2	CS	PGOOD
L (High-side FET : OFF)	L (Low-side FET : OFF)	L	L

- Timing chart example for under-voltage protection operation (PGOOD pulled up to VB)

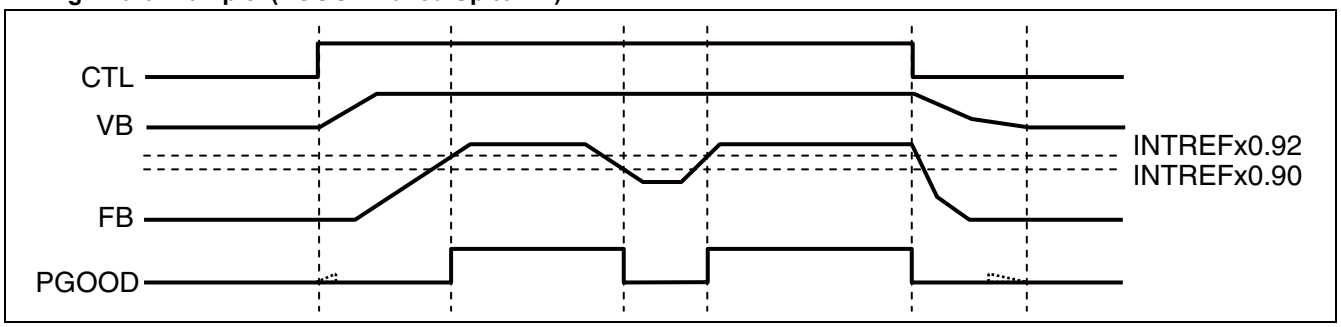


The under-voltage protection state can be cancelled by setting the IC to standby state first and then resetting the latch using the UVLO signal.
Also, the under-voltage protection function can be disabled by causing a short between the CUVP pin and the GND pin (Pin 1).

9.12 Power-Good Detection Circuit Block (PGOOD Comp.)

This function is that 0.9 times (Typ.) of the internal reference voltage (INTREF) that is set by the output voltage setting block (VO REFIN Control) is compared with the voltage that is inverting-input into Error Comp. If the thing that the inverting-input voltage into Error Comp. has raised is detected, it determines that the output voltage of the DC/DC converter has reached the setting voltage and turns off N-ch MOS which are built into the PGOOD pin (Pin 7) .

Timing Chart Example (PGOOD Pulled Up to VB)



9.13 Output Block (Drv-1, Drv-2)

This circuit drives the external N-ch MOS FET. The output circuit is configured in CMOS type for both the high-side and the low-side.

9.14 Control Block (CTL)

The block changes to standby state, when the CTL pin (Pin 8) is set to the “L” level.

(The maximum power-supply current at standby is 10 µA.)

Setting the CTL pin to the “H” level can send the DC/DC converter block into operating state.

Control Function Table

CTL	DC/DC converter
L	OFF
H	ON

9.15 Bias Voltage Block (VB Reg.)

It outputs 5 V as the power supply to the internal control circuit and for setting the bootstrap voltage.

Moreover, it can switch the 5 V power supply to external (VBIN) from internal (VB Reg.). By inputting the voltage of 4.5 V (Typ.) or more to the VBIN pin (Pin 18) from outside.

9.16 Over temperature Protection Circuit Block (OTP)

The circuit protects an IC from heat-destruction. If the junction temperature reaches + 150°C, the over temperature protection circuit sets the CS pin (Pin 4) to the “L” level, the OUT-1 pin (Pin 20) and the OUT-2 pin (Pin 15) to the “L” level, and turns on the discharge FET (RON ≈ 16 Ω) which is connected between the VO pin (Pin 23) and GND. In addition, if the junction temperature drops to + 125°C, the normal operation restarts. The condition for the over temperature protection function to operate is that the maximum rating of this IC is exceeded. Therefore, make sure to design the DC/DC power supply system so that the over temperature protection does not start frequently.