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MB39A136

2ch PFM/PWM DC/DC Converter IC with Synchronous Rectification

MB39A136 is 2ch step-down DC/DC converter IC of the current mode N-ch/N-ch synchronous rectification method. It contains the enhanced protection features, and supports the symmetrical-phase method and the ceramic capacitor. MB39A136 realizes rapid response, high efficiency, and low ripple voltage, and its high-frequency operation enables the miniaturization of inductors and I/O capacitors.

Features

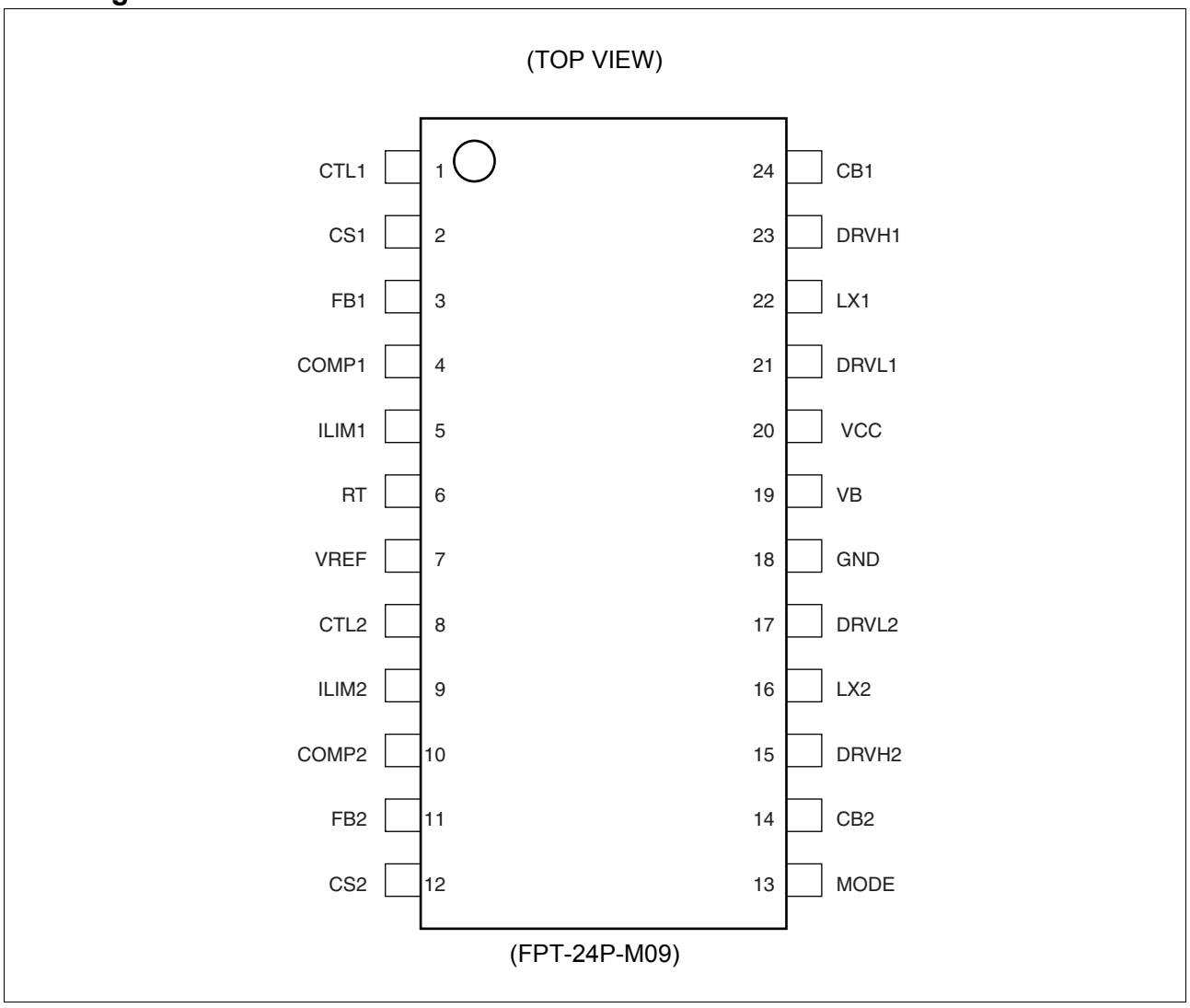
- High efficiency
- For frequency setting by external resistor : 100 kHz to 1 MHz
- Error Amp threshold voltage : 0.7 V ± 1.0%
- Minimum output voltage value : 0.7 V
- Wide range of power-supply voltage : 4.5 V to 25 V
- PFM/PWM auto switching mode and fixed PWM mode selectable
- Supports Symmetrical-Phase method
- With built-in over voltage protection function
- With built-in under voltage protection function
- With built-in over current protection function
- With built-in over-temperature protection function
- With built-in soft start/stop circuit without load dependence
- With built-in synchronous rectification type output steps for N-ch MOS FET
- Standby current : 0 [µA] Typ
- Small package : TSSOP-24

Application

- Digital TV
- Photocopiers
- Surveillance cameras
- Set-top boxes (STB)
- DVD players, DVD recorders
- Projectors
- IP phones
- Vending machine
- Consoles and other non-portable devices

Contents

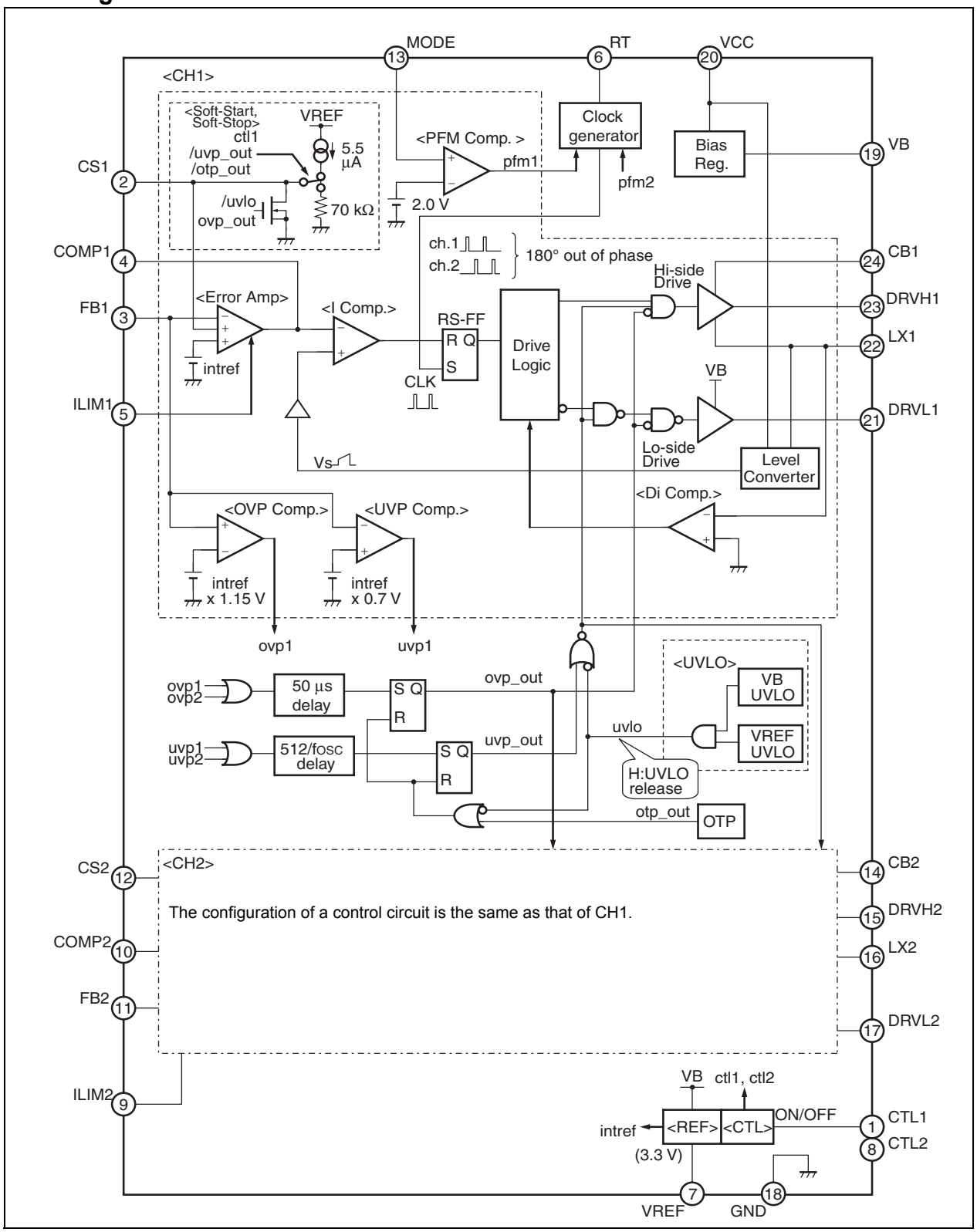
1. Pin Assignment



2. Pin Description

Pin No.	Symbol	I/O	Description
1	CTL1	I	CH1 control pin.
2	CS1	I	CH1 soft-start time setting capacitor connection pin.
3	FB1	I	CH1 Error amplifier inverted input pin.
4	COMP1	O	CH1 error amplifier output pin.
5	ILIM1	I	CH1 over current detection level setting voltage input pin.
6	RT	–	Oscillation frequency setting resistor connection pin.
7	VREF	O	Reference voltage output pin.
8	CTL2	I	CH2 control pin.
9	ILIM2	I	CH2 over current detection level setting voltage input pin.
10	COMP2	O	CH2 error amplifier output pin.
11	FB2	I	CH2 Error amplifier inverted input pin.
12	CS2	I	CH2 soft-start time setting capacitor connection pin.
13	MODE	I	PFM/PWM switch pin. (CH1 and CH2 commonness) It becomes fixed PWM operation with the VREF connection, and it becomes PFM/PWM operation with the GND connection.
14	CB2	–	CH2 connection pin for boot strap capacitor.
15	DRVH2	O	CH2 output pin for external high-side FET gate drive.
16	LX2	–	CH2 inductor and external high-side FET source connection pin.
17	DRVL2	O	CH2 output pin for external low-side FET gate drive.
18	GND	–	Ground pin.
19	VB	O	Bias voltage output pin.
20	VCC	–	Power supply pin for reference voltage and control circuit.
21	DRVL1	O	CH1 output pin for external low-side FET gate drive.
22	LX1	–	CH1 inductor and external high-side FET source connection pin.
23	DRVH1	O	CH1 output pin for external high-side FET gate drive.
24	CB1	–	CH1 connection pin for boot strap capacitor.

3. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power-supply voltage	V_{VCC}	VCC pin	—	27	V
CB pin input voltage	V_{CB}	CB1, CB2 pins	—	32	V
LX pin input voltage	V_{LX}	LX1, LX2 pins	—	27	V
Voltage between CB and LX	V_{CBLX}	—	—	7	V
Control input voltage	V_I	CTL1, CTL2 pins	—	27	V
Input voltage	V_{FB}	FB1, FB2 pins	—	V_{VREF} + 0.3	V
	V_{ILIM}	ILIM1, ILIM2 pins	—	V_{VREF} + 0.3	V
	V_{CSx}	CS1, CS2 pins	—	V_{VREF} + 0.3	V
	V_{MODE}	MODE pin	—	V_{VB} + 0.3	V
Output current	I_{OUT}	DC DRVL1, DRVL2 pins, DRVH1, DRVH2 pins	—	60	mA
Power dissipation	P_D	Ta ≤ + 25°C	—	1644	mW
Storage temperature	T_{STG}	—	− 55	+ 150	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{VCC}	—	4.5	—	25.0	V
CB pin input voltage	V_{CB}	—	—	—	30	V
Reference voltage output current	I_{VREF}	—	− 100	—	—	μA
Bias output current	I_{VB}	—	− 1	—	—	mA
CTL pin input voltage	V_I	CTL1, CTL2 pins	0	—	25	V
Input voltage	V_{FB}	FB1, FB2 pins	0	—	V_{VREF}	V
	V_{ILIM}	ILIM1, ILIM2 pins	0.3	—	1.94	V
	V_{CS}	CS1, CS2 pins	0	—	V_{VREF}	V
	V_{MODE}	MODE pin	0	—	V_{VREF}	V
Peak output current	I_{OUT}	DRVH1, DRVH2 pins DRVL1, DRVL2 pins Duty ≤ 5% (t = 1/f_{OSC}×Duty)	− 1200	—	+ 1200	mA
Operation frequency range	f_{OSC}	—	100	500	1000	kHz
Timing resistor	R_{RT}	RT pin	—	47	—	kΩ
Soft start capacitor	C_{CS}	CS1, CS2 pins	0.0075	0.0180	—	μF
CB pin capacitor	C_{CB}	CB1, CB2 pins	—	0.1	1.0	μF
Reference voltage output capacitor	C_{VREF}	VREF pin	—	0.1	1.0	μF
Bias voltage output capacitor	C_{VB}	VB pin	—	2.2	10	μF
Operating ambient temperature	Ta	—	− 30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

6. Electrical Characteristics

(Ta = + 25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 A, VB pin = 0A)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [REF]	Output voltage	V_{VREF}	7	—	3.24	3.30	3.36	V
	Input stability	VREF LINE	7	VCC pin = 4.5 V to 25 V	—	1	10	mV
	Load stability	VREF LOAD	7	VREF pin = 0 A to − 100 μA	—	1	10	mV
	Short-circuit output current	VREF IOS	7	VREF pin = 0 V	− 14.5	− 10.0	− 7.5	mA
Bias Voltage Block [VB Reg.]	Output voltage	V_{VB}	19	—	4.85	5.00	5.15	V
	Input stability	VB LINE	19	VCC pin = 6 V to 25 V	—	10	100	mV
	Load stability	VB LOAD	19	VB pin = 0 A to − 1 mA	—	10	100	mV
	Short-circuit output current	VB IOS	19	VB pin = 0 V	− 200	− 140	− 100	mA
Under voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH1}	19	VB pin	4.0	4.2	4.4	V
		V_{THL1}	19	VB pin	3.4	3.6	3.8	V
	Hysteresis width	V_{H1}	19	VB pin	—	0.6*	—	V
	Threshold voltage	V_{TLH2}	7	VREF pin	2.7	2.9	3.1	V
		V_{THL2}	7	VREF pin	2.5	2.7	2.9	V
	Hysteresis width	V_{H2}	7	VREF pin	—	0.2*	—	V
Soft-start / Soft-stop Block [Soft-Start, Soft-Stop]	Charge current	I_{CS}	2, 12	CTL1, CTL2 pins = 5 V, CS1, CS2 pins = 0 V	− 7.9	− 5.5	− 4.2	μA
	Soft-start end voltage	V_{CS}	2, 12	CTL1, CTL2 pins = 5 V	2.2	2.4	2.6	V
	Electrical discharge resistance at soft-stop	R_{DISCG}	2, 12	CTL1, CTL2 pins = 0 V, CS1, CS2 pins = 0.5 V	49	70	91	kΩ
	Soft-stop end voltage	V_{DISCG}	2, 12	CTL1, CTL2 pins = 0 V	—	0.1*	—	V
Clock Generator Block [OSC]	Oscillation frequency	f_{OSC}	6	RT pin = 47 kΩ	450	500	550	kHz
	Oscillation frequency when under voltage is detected	f_{SHORT}	6	RT pin = 47 kΩ	—	62.5	—	kHz
	Frequency Temperature variation	df/dT	6	Ta = − 30°C to + 85°C	—	3*	—	%

(Continued)

(Ta = + 25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 A, VB pin = 0 A)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error Amp Block [Error Amp1, Error Amp2]	Threshold voltage	EV_{TH}	3, 11	—	0.693	0.700	0.707	V
		EV_{THT}	3, 11	Ta = − 30°C to + 85°C	0.689*	0.700*	0.711*	V
	Input current	I_{FB}	3, 11	FB1, FB2 pins = 0 V	− 0.1	0	+ 0.1	µA
	Output current	I_{SOURCE}	4, 10	FB1, FB2 pins = 0 V, COMP1, COMP2 pins = 1 V	− 390	− 300	− 210	µA
		I_{SINK}	4, 10	FB1, FB2 pins = VREF pin, COMP1, COMP2 pins = 1 V	8.4	12.0	16.8	mA
	Output clamp voltage	V_{ILIM}	4, 10	FB1, FB2 pins = 0 V, ILIM1, ILIM2 pins = 1.5 V	1.35	1.50	1.65	V
	ILIM pin input current	I_{ILIM}	5, 9	FB1, FB2 pins = 0 V, ILIM1, ILIM2 pins = 1.5 V	− 1	0	+ 1	µA
Over-voltage Protection Circuit Block [OVP Comp.]	Over-voltage detecting voltage	V_{OVP}	3, 11	FB1, FB2 pins	0.776	0.805	0.835	V
	Over-voltage detection time	t_{OVP}	3, 11	—	49	70	91	µs
Under-voltage Protection Circuit Block [UVP Comp.]	Under-voltage detecting voltage	V_{UVP}	3, 11	FB1, FB2 pins	0.450	0.490	0.531	V
	Under-voltage detection time	t_{UVP}	3, 11	—	—	512/ f_{OSC}	—	s
Over-temperature Protection Circuit Block [OTP]	Detection temperature	T_{OTPH}	—	Junction temperature	—	+ 160*	—	°C
		T_{OTPL}	—	Junction temperature	—	+ 135*	—	°C
PFM Control Circuit Block (MODE)	Synchronous rectification stop voltage	V_{THLX}	22, 16	LX1, LX2 pins	—	0*	—	mV
	PFM/PWM mode condition	V_{PFM}	13	MODE pin	0	—	1.4	V
	Fixed PWM mode condition	V_{PWM}	13	MODE pin	2.2	—	V_{VREF}	V
	MODE pin input current	I_{MODE}	13	MODE pin = 0 V	− 1	0	+ 1	µA

(Continued)

(Ta = + 25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 A, VB pin = 0 A)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Output Block [DRV]	High-side output on-resistance	R_{ON_MH}	23, 15	DRVH1, DRVH2 pins = − 100 mA	—	4	7	Ω
		R_{ON_ML}	23, 15	DRVH1, DRVH2 pins = 100 mA	—	1.0	3.5	Ω
	Low-side output on-resistance	R_{ON_SH}	21, 17	DRVL1, DRVL2 pins = − 100 mA	—	4	7	Ω
		R_{ON_SL}	21, 17	DRVL1, DRVL2 pins = 100 mA	—	0.75	1.70	Ω
	Output source current	I_{SOURCE}	23, 15, 21, 17	LX1, LX2 pins = 0 V, CB1, CB2 pins = 5 V DRVH1, DRVH2 pins, DRVL1, DRVL2 pins = 2.5 V Duty ≤ 5%	—	− 0.5*	—	A
	Output sink current	I_{SINK}	23, 15	LX1, LX2 pins = 0 V, CB1, CB2 pins = 5 V DRVH1, DRVH2 pins = 2.5 V Duty ≤ 5%	—	0.9*	—	A
			21, 17	LX1, LX2 pins = 0 V, CB1, CB2 pins = 5 V DRVL1, DRVL2 pins = 2.5 V Duty ≤ 5%	—	1.2*	—	A
	Minimum on time	t_{ON}	23, 15	COMP1, COMP2 pins = 1 V	—	250*	—	ns
	Maximum on-duty	D_{MAX}	23, 15	FB1, FB2 pins = 0 V	75	80	—	%
	Dead time	t_D	23, 21, 15, 17	LX1, LX2 pins = 0 V, CB1, CB2 pins = 5 V	—	60	—	ns
Level Converter Block [LVCNV]	Maximum current sense voltage	V_{RANGE}	22, 16	VCC pin − LX1, LX2 pins	—	220*	—	mV
	Voltage conversion gain	A_{LV}	22, 16	—	5.4	6.8	8.2	V/V
	Offset voltage at voltage conversion	V_{IO}	22, 16	—	—	300	—	mV
	Slope compensation inclination	SLOPE	22, 16	—	—	2*	—	V/V
	LX pin input current	I_{LX}	22, 16	LX1, LX2 pins = VCC pin	320	420	600	µA

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(Continued)

(Ta = + 25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 A, VB pin = 0 A)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Control Block [CTL1, CTL2]	ON condition	V_{ON}	1, 8	CTL1, CTL2 pins	2	—	25	V
	OFF condition	V_{OFF}	1, 8	CTL1, CTL2 pins	0	—	0.8	V
	Hysteresis width	V_H	1, 8	CTL1, CTL2 pins	—	0.4*	—	V
	Input current	I_{CTLH}	1, 8	CTL1, CTL2 pins = 5 V	—	25	40	µA
		I_{CTLL}	1, 8	CTL1, CTL2 pins = 0 V	—	0	1	µA
General	Standby current	I_{CCS}	20	CTL1, CTL2 pins = 0 V	—	0	10	µA
	Power-supply current	I_{CC}	20	LX1, LX2 pins = 0 V, FB1, FB2 pins = 1.0 V, MODE pin = VREF pin	—	3.3	4.7	mA

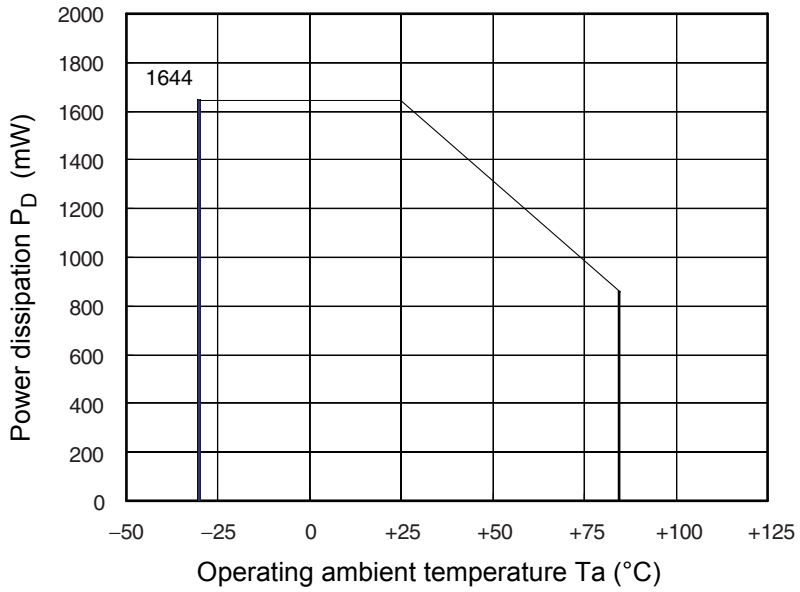
* : This value is not be specified. This should be used as a reference to support designing the circuits.

7. Typical Characteristics

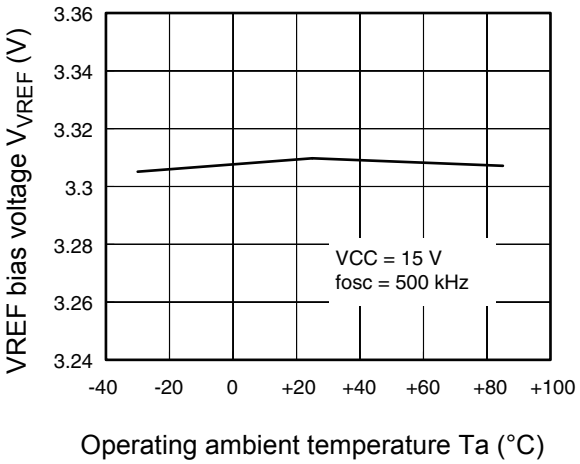
■ Typical data

Power dissipation

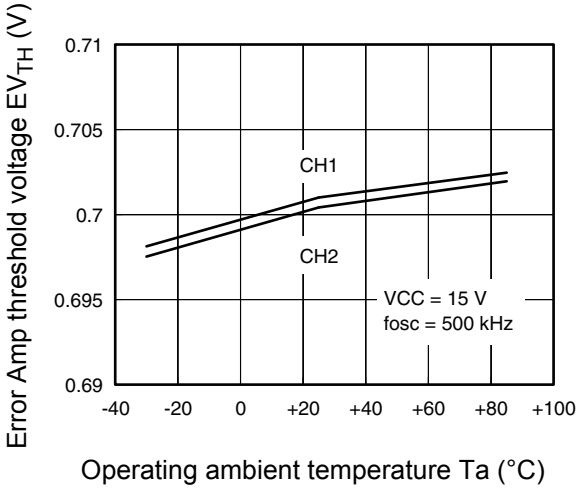
Power dissipation vs. Operating ambient temperature



VREF bias voltage vs. Operating ambient temperature



Error Amp threshold voltage vs. Operating ambient temperature



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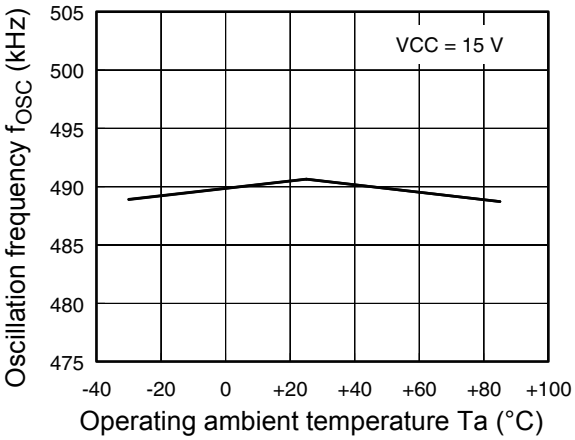
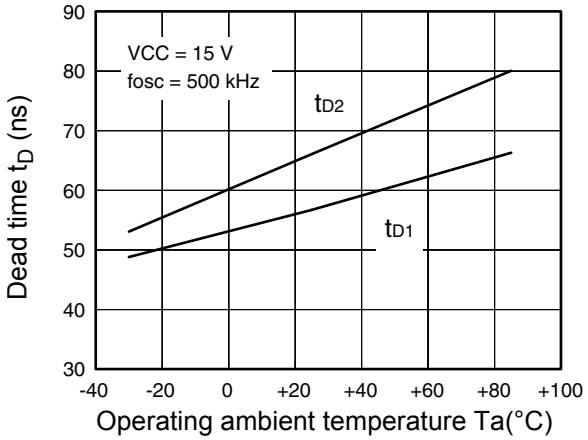
Oscillation frequency vs.
Operating ambient temperature

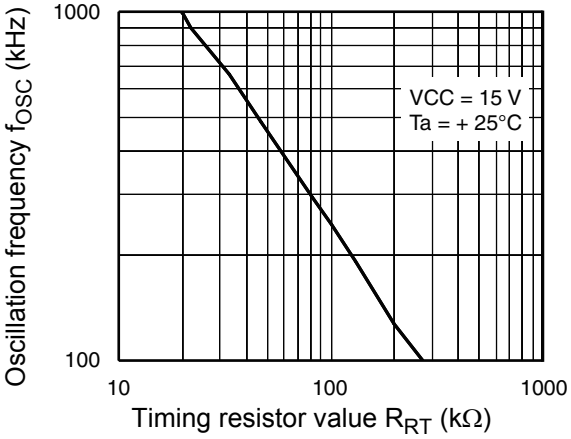


Dead time vs.
Operating ambient temperature

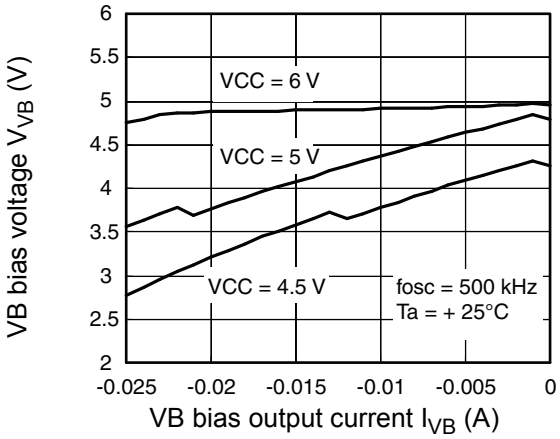


t_{D1} : period from DRVL off to DRVH on
t_{D2} : period from DRVH off to DRVL on

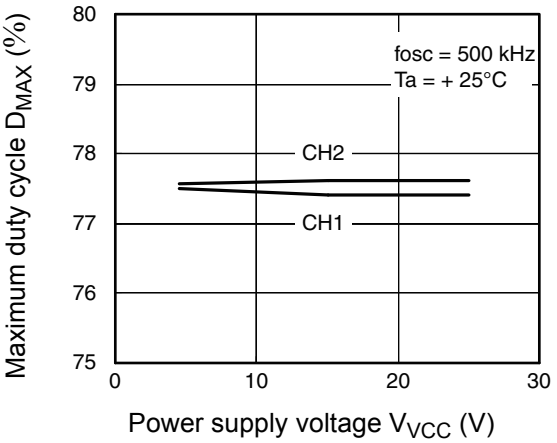
Oscillation frequency vs. Timing resistor value



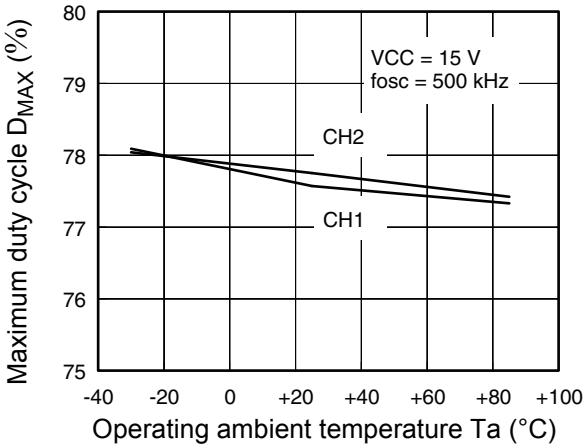
VB bias voltage vs. VB bias output current



Maximum duty cycle vs.
Power supply voltage



Maximum duty cycle vs.
Operating ambient temperature



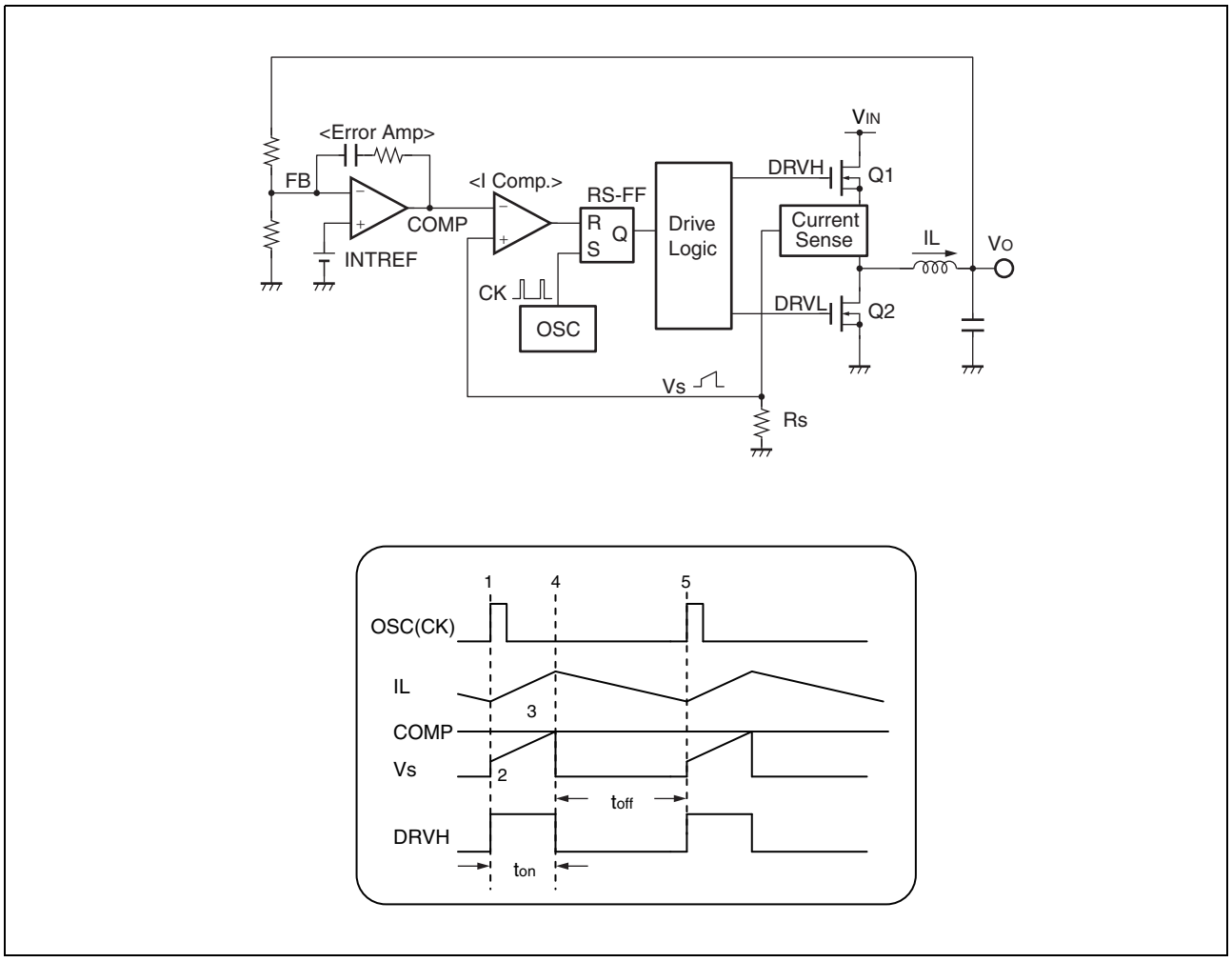
8. Function Description

8.1 Current Mode

It uses the current waveform from the switching (Q1) as a control waveform to control the output voltage, as described below:

1. The clock (CK) from the internal clock generator (OSC) sets RS-FF and turns on the high-side FET.
2. Turning on the high-side FET causes the inductor current (IL) rise. Generate Vs that converts this current into the voltage.
3. The current comparator (I Comp.) compares this Vs with the output (COMP) from the error amplifier (Error Amp) that is negative-feedback from the output voltage (Vo).
4. When I Comp. detects that Vs exceeds COMP, it resets RS-FF and turns off high-side FET.
5. The clock (CK) from the clock generator (OSC) turns on the high-side FET again.

Thus, switching is repeated.
Operate so that the FB electrical potential may become INTREF electrical potential, and stabilize the output voltage as a feedback control.



8.1.1 Reference Voltage Block (REF)

The reference voltage circuit (REF) generates a temperature-compensated reference voltage (3.3 [V] Typ) using the voltage supplied from the VCC pin. The voltage is used as the reference voltage for the IC's internal circuit. The reference voltage can be used to supply a load current of up to 100 μA to an external device through the VREF pin.

8.1.2 Bias Voltage Block (VB Reg.)

Bias Voltage Block (VB Reg.) generates the reference voltage used for IC's internal circuit, using the voltage supplied from the VCC pin. The reference voltage is a temperature-compensated stable voltage (5 [V] Typ) to supply a current of up to 100 mA through the VB pin.

8.1.3 Under Voltage Lockout Protection Circuit Block (UVLO)

The circuit protects against IC malfunction and system destruction/deterioration in a transitional state or a momentary drop when a bias voltage (VB) or an internal reference voltage (VREF) starts. It detects a voltage drop at the VB pin or the VREF pin and stops IC operation. When voltages at the VB pin and the VREF pin exceed the threshold voltage of the under voltage lockout protection circuit, the system is restored.

8.1.4 Soft-start/Soft-stop Block (Soft-Start, Soft-Stop)

Soft-start

It protects a rush current or an output voltage (V_Ox) from overshooting at the output start. Since the lamp voltage generated by charging the capacitor connecting to the CSx pin is used for the reference voltage of the error amplifier (Error Amp), it can set the soft-start time independent of a load of the output (V_Ox). When the IC starts with "H" level of the CTLx pin, the capacitor at the CSx pin (CS) starts to be charged at 5.5 μA. The output voltage (V_Ox) during the soft-start period rises in proportion to the voltage at the CSx pin generated by charging the capacitor at the CSx pin.

During the soft-start with 0.8 V > voltage at CS1 and CS2 pins, operations are as follows:

■ Fixed PWM operation only (fixed PWM even if MODE pin is set to "L")

■ Over-voltage protection function and under-voltage protection function are invalid.

Soft-stop

It discharges electrical charges stored in a smoothing capacitor at output stop. Setting the CTLx pin to "L" level starts the soft-stop function independent of a load of output (Vox). Since the capacitor connecting to the CSx pin starts to discharge through the IC-built-in soft-stop discharging resistance (70 [kΩ] Typ) when the CTLx pin sets at "L" level enters its lamp voltage into the error amplifier (Error Amp), the soft-stop time can be set independent of a load of output (V_Ox). When discharging causes the voltage at the CSx pin to drop below 100 mV (Typ), the IC shuts down and changes to the stand-by state. In addition, the soft-stop function operates after the under-voltage protection circuit block (UVP Comp.) is latched or after the over-temperature protection circuit block (OTP) detects over-temperature.

During the soft-stop with, 0.8 V > voltage at CS1 and CS2 pins, operations are as follows:

■ Fixed PWM operation only (fixed PWM even if MODE pin is set to "L")

■ Over-voltage protection function and under-voltage protection function are invalid.

8.1.5 Clock Generator Block (OSC)

The clock generator has the built-in oscillation frequency setting capacitor and generates a clock that 180°phase shifted from each channel by connecting the oscillation frequency setting resistor to the RT pin (Symmetrical-Phase method).

8.1.6 Error Amp Block (Error Amp1, Error Amp2)

The error amplifiers (Error Amp1 and Error Amp2) detect the output voltage from the DC/DC converter and output to the current comparators (I Comp.1 and I Comp.2). The output voltage setting resistor externally connected to FB1 and FB2 pins allows an arbitrary output voltage to be set.

In addition, since an external resistor and an external capacitor serially connected between COMP1 and FB1 pins and between COMP2 and FB2 pins allow an arbitrary loop gain to be set, it is possible for the system to compensate a phase stably.

8.1.7 Over Current Detection (Protection) Block (ILIM)

It is the current detection circuit to restrict an output current (I_{OX}). The over current detection block (ILIM) compares an output waveform of the level converter of each channel (see “8.1.13” Level Converter Block (LVCNV)) with the ILIMx pin voltage in every cycle. As a load resistance (R_{OX}) drops, a load current (I_{OX}) increases. Therefore, the output waveform of the level converter exceeds the ILIM pin voltage of each channel. At this time, the output current can be restricted by turning off FET on the high-side and suppressing a peak value of the inductor current.

As a result, the output voltage (V_{OX}) should drop.

Furthermore, if the output voltage drops and the electrical potential at the FBx pin drops below 0.3 V, the oscillation frequency (f_{OSC}) drops to 1/8.

8.1.8 Over-voltage Protection Circuit Block (OVP Comp.)

The circuit protects a device connecting to the output when the output voltage (V_Ox) rises.

It compares 1.15 times (Typ) of the internal reference voltage (INTREF) (0.7 V) that is non-inverting-entered into the error amplifier with the feedback voltage that is inverting-entered into the error amplifier and if it detects the state where the latter is higher than the former by 50 μs (Typ). It stops the voltage output by setting the RS latch, setting the DRVHx pin to “L” level, setting the DRVLx pin to “H” level, turning off the high-side FETs, and turning on the low-side FETs.

The conditions below cancel the protection function:

■ Setting CTL1 and CTL2 to “L”.

■ Setting the power supply voltage below the UVLO threshold voltage (V_{THL1} and V_{THL2}).

8.1.9 Under-voltage Protection Circuit Block (UVP Comp.)

It protects a device connecting to the output by stopping the output when the output voltage (V_{OX}) drops.

It compares 0.7 times (Typ) of the internal reference voltage (INTREF) (0.7 V) that is non-inverting-entered into the error amplifier with the feedback voltage that is inverting-entered into the error amplifier and if it detects the state where the latter is lower than the former by 512/fosc [s](Typ), it stops the voltage output for both channels by setting the RS latch.

The conditions below cancel the protection function:

■ Setting CTL1 and CTL2 to “L”.

■ Setting the power supply voltage below the UVLO threshold voltage (V_{THL1} and V_{THL2}).

8.1.10 Over temperature Protection Circuit Block (OTP)

The circuit protects an IC from heat-destruction. If the temperature at the joint part reaches +160°C, the circuit stops the voltage output for both channels by discharging the capacitor connecting to the CSx pin through the soft-stop discharging resistance (70 [kΩ] Typ) in the IC.
In addition, if the temperature at the joint part drops to +135°C, the output restarts again through the soft-start function.
Make sure to design the DC/DC power supply system so that the over temperature protection does not start frequently.

8.1.11 PFM Control Circuit Block (MODE)

It sets the control mode of the IC and makes control at automatic PFM/PWM switching.

MODE pin connection	Control mode	Features
“L” (GND)	Automatic PFM/PWM switching	Highly-efficient at light load
“H” (VREF)	Fixed PWM	Stable oscillation frequency Stable switching ripple voltage Excellent in rapid load change characteristic at heavy load to light load

Automatic PFM/PWM switching mode operation

It compares the LX1 pin and the LX2 pin voltages with GND electrical potential at Di Comp. In the comparison, the negative voltage at the LX pin causes the low-side FET to set on, positive voltage causes it to set off (Di Comp. method) . As a result, the method restricts the back flow of the inductor current at a light load and makes the switching of the inductor current discontinuous (DCM) . Such an operation allows the oscillation frequency to drop, resulting in high efficiency at a light load.

8.1.12 Output Block (DRV)

The output circuit is configured in CMOS type for both of the high-side and the low-side, allowing the external N-ch MOS FET to drive.

8.1.13 Level Converter Block (LVCNV)

The circuit detects and converts the current when the high-side FET turns on. It converts the voltage waveform between drain side (VCC pin voltage) and the source side (LX1 and LX2 pin voltage) on the high-side FET into the voltage waveform for GND reference.

Note: x : Each channel number

8.1.14 Control Block (CTL1, CTL2)

The circuit controls on/off of the output from the IC.

Control function table

CTL1	CTL2	DC/DC converter (V_O1)	DC/DC converter (V_O2)	Remarks
L	L	OFF	OFF	Standby
H	L	ON	OFF	—
L	H	OFF	ON	—
H	H	ON	ON	—

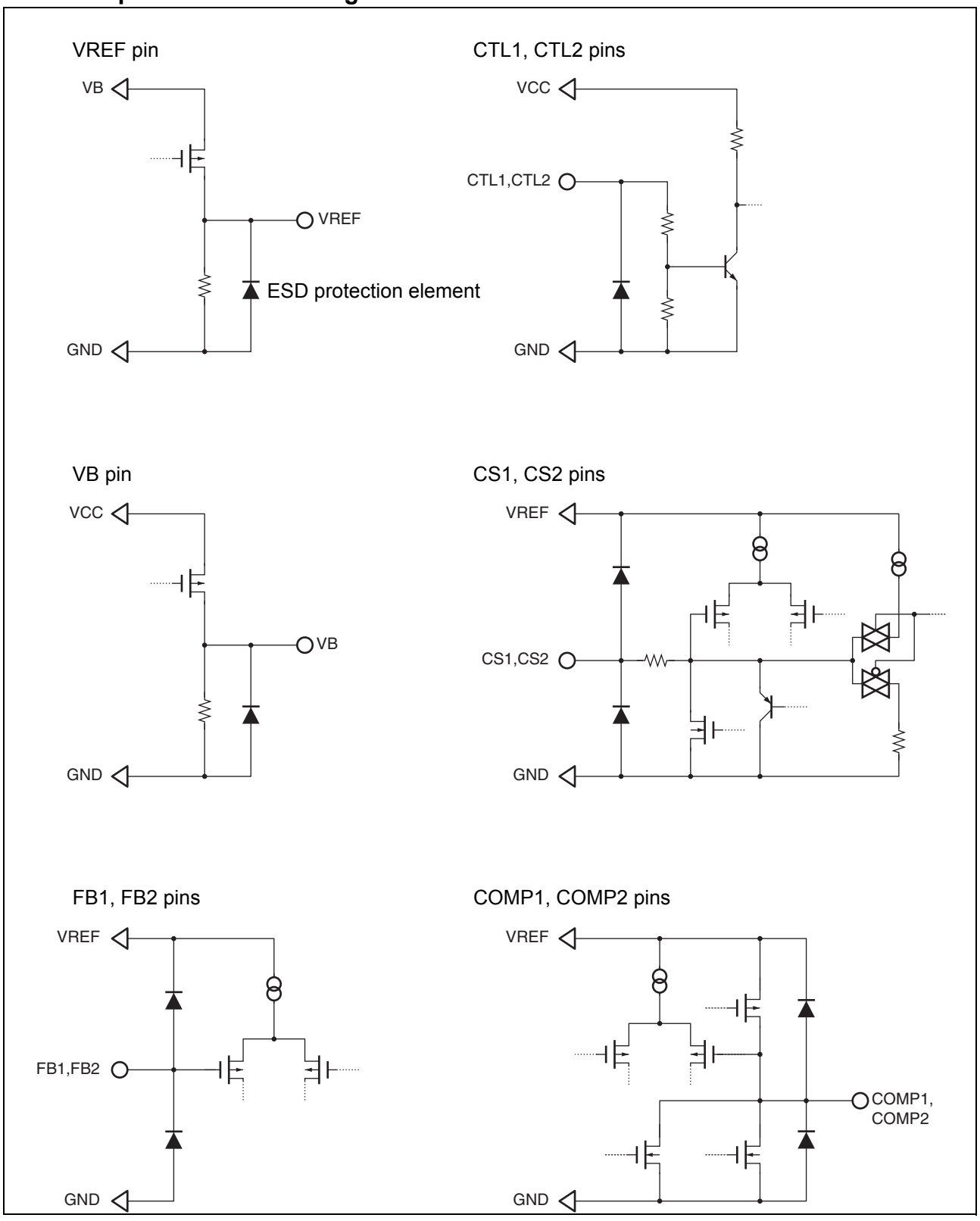
9. Protection Function Table

The following table shows the state of each pin when each protection function operates.

Protection Function	Detection condition	Output of each pin after detection				DC/DC output dropping operation
		VREF	VB	DRVHx	DRVLx	
Under Voltage Lock Out Protection (UVLO)	VB < 3.6 V VREF < 2.7 V	< 2.7 V	< 3.6 V	L	L	Self-discharge by load
Under Voltage Protection (UVP)	FBx < 0.49 V	3.3 V	5 V	L	L	Electrical discharge by soft-stop function
Over Voltage Protection (OVP)	FBx > 0.805 V	3.3 V	5 V	L	H	0 V clamping
Over Current Protection (ILIM)	COMPx > ILIMx	3.3 V	5V	switching	switching	The output voltage is dropping to keep constant output current.
Over Temperature Protection (OTP)	Tj > ＋160°C	3.3 V	5 V	L	L	Electrical discharge by soft-stop function
CONTROL (CTL)	CTLx : H→L (CSx > 0.1 V)	3.3 V	5 V	L	L	

Note: x is the each channel number

10. I/O Pin Equivalent Circuit Diagram



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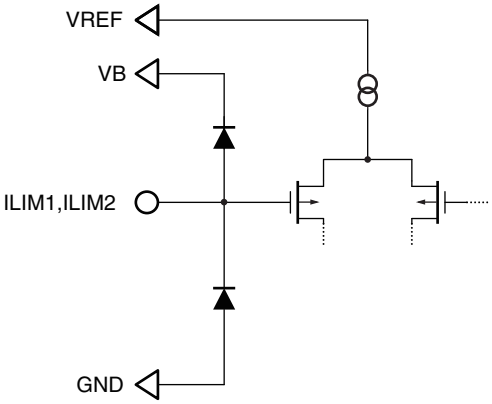
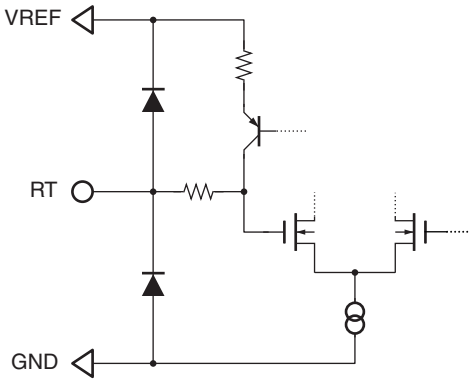
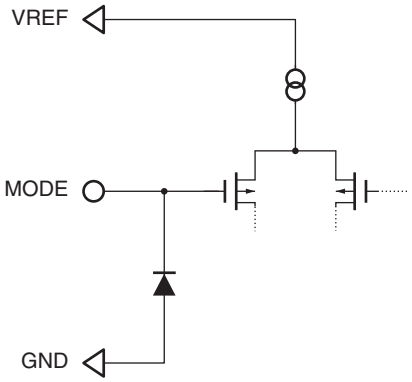
ILM1, ILM2 pins



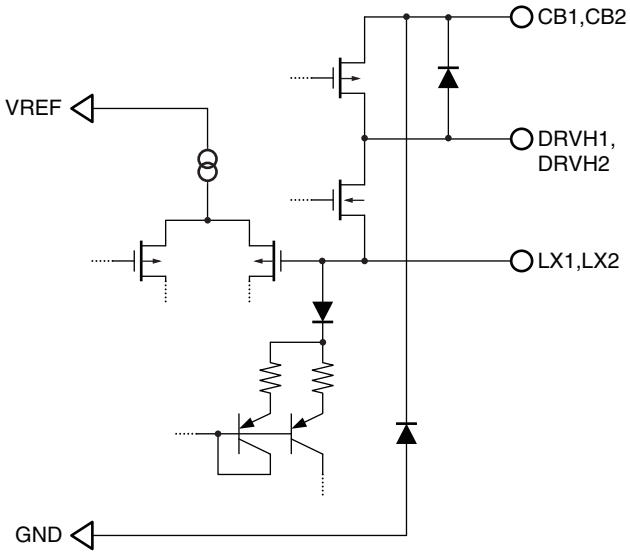
RT pin



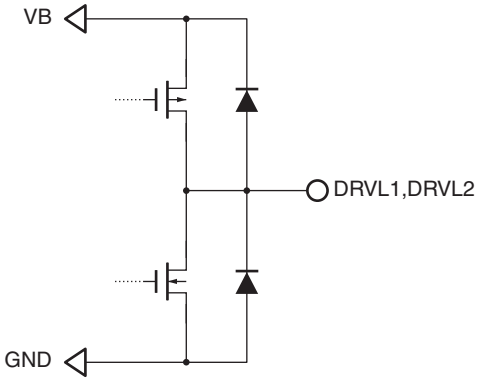
MODE pin



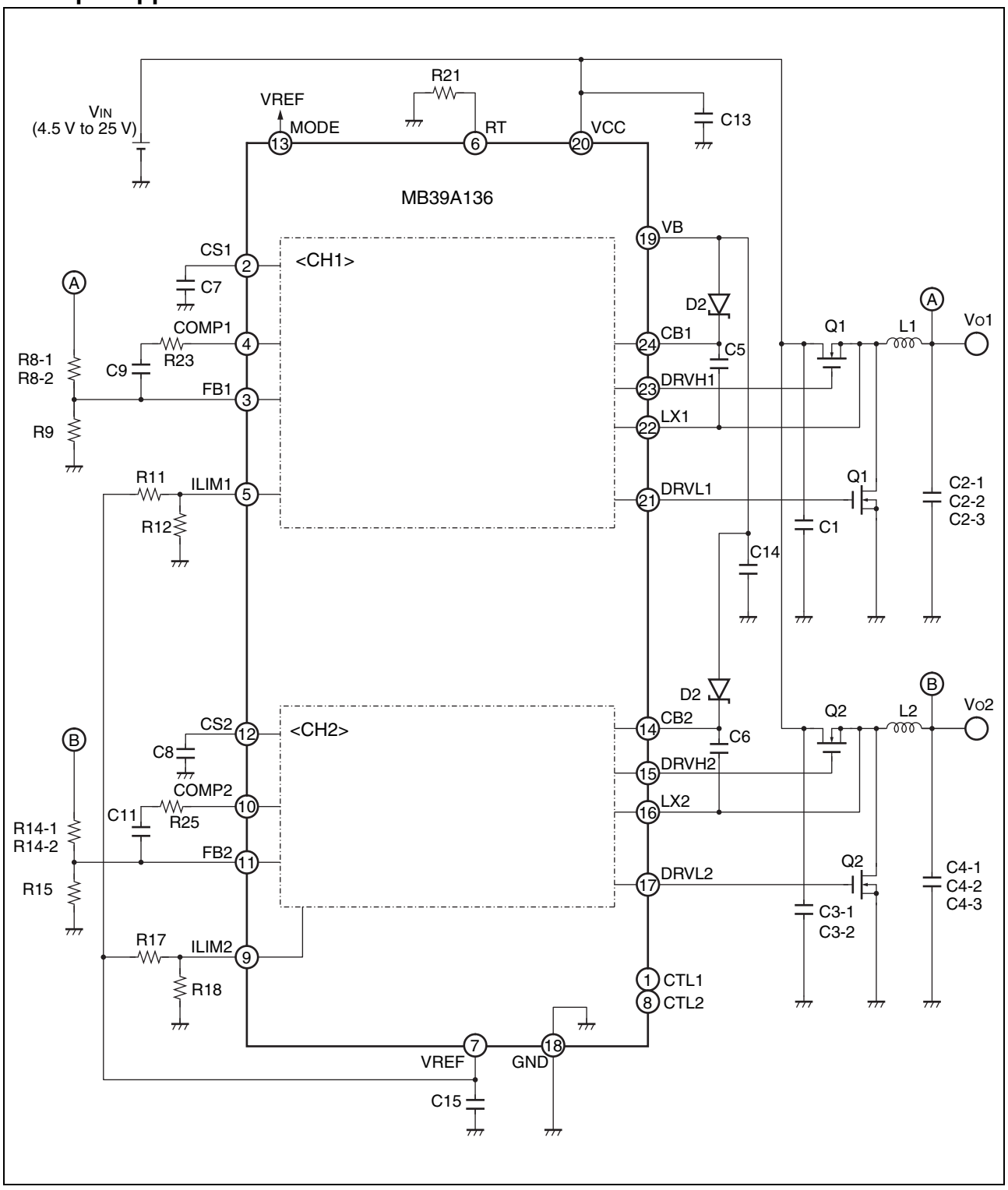
CB1, CB2, DRVH1, DRVH2, LX1, LX2 pins



DRVL1, DRVL2 pins



11. Example Application Circuit



12. Parts List

Component	Item	Specification	Vendor	Package	Parts Name	Remark
Q1	N-ch FET	VDS = 30 V, ID = 8 A, Ron = 21 mΩ	RENESAS	SO-8	μPA2755	Dual type (2 elements)
Q2	N-ch FET	VDS = 30 V, ID = 8 A, Ron = 21 mΩ	RENESAS	SO-8	μPA2755	Dual type (2 elements)
D2	Diode	VF = 0.35 V at IF = 0.2 A	ON Semi	SOT-323	BAT54AWT1	Dual type
L1	Inductor	1.5 μH (6.2 mΩ, 8.9 A)	TDK	—	VLF10040T-1R5N	
L2	Inductor	3.3 μH (9.7 mΩ, 6.9 A)	TDK	—	VLF10045T-3R3N	
C1	Ceramic capacitor	22 μF (25 V)	TDK	3225	C3225JC1E226M	
C2-1 C2-2 C2-3	Ceramic capacitor Ceramic capacitor Ceramic capacitor	22 μF (10 V) 22 μF (10 V) 22 μF (10 V)	TDK TDK TDK	3216 3216 3216	C3216JB1A226M C3216JB1A226M C3216JB1A226M	3 capacitors in parallel
C3-1 C3-2	Ceramic capacitor Ceramic capacitor	22 μF (25 V) 22 μF (25 V)	TDK TDK	3225 3225	C3225JC1E226M C3225JC1E226M	2 capacitors in parallel
C4-1 C4-2 C4-3	Ceramic capacitor Ceramic capacitor Ceramic capacitor	22 μF (10 V) 22 μF (10 V) 22 μF (10 V)	TDK TDK TDK	3216 3216 3216	C3216JB1A226M C3216JB1A226M C3216JB1A226M	3 capacitors in parallel
C5	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C6	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C7	Ceramic capacitor	0.022 μF (50 V)	TDK	1608	C1608JB1H223K	
C8	Ceramic capacitor	0.022 μF (50 V)	TDK	1608	C1608JB1H223K	
C9	Ceramic capacitor	820 pF (50 V)	TDK	1608	C1608CH1H821J	
C11	Ceramic capacitor	1000 pF (50 V)	TDK	1608	C1608CH1H102J	
C13	Ceramic capacitor	0.01 μF (50 V)	TDK	1608	C1608JB1H103K	
C14	Ceramic capacitor	2.2 μF (16 V)	TDK	1608	C1608JB1C225K	
C15	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
R8-1 R8-2	Resistor	1.6 kΩ 9.1 kΩ	SSM SSM	1608 1608	RR0816P162D RR0816P912D	2 capacitors in series
R9	Resistor	15 kΩ	SSM	1608	RR0816P153D	
R11	Resistor	56 kΩ	SSM	1608	RR0816P563D	
R12	Resistor	47 kΩ	SSM	1608	RR0816P473D	
R14-1 R14-2	Resistor	1.8 kΩ 39 kΩ	SSM SSM	1608 1608	RR0816P182D RR0816P393D	2 capacitors in series
R15	Resistor	11 kΩ	SSM	1608	RR0816P113D	

(Continued)

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Component	Item	Specification	Vendor	Package	Parts Name	Remark
R17	Resistor	56 kΩ	SSM	1608	RR0816P563D	
R18	Resistor	56 kΩ	SSM	1608	RR0816P563D	
R21	Resistor	82 kΩ	SSM	1608	RR0816P823D	
R23	Resistor	22 kΩ	SSM	1608	RR0816P223D	
R25	Resistor	56 kΩ	SSM	1608	RR0816P563D	

RENESAS : Renesas Electronics Corporation
ON Semi : ON Semiconductor
TDK : TDK Corporation
SSM : SUSUMU Co.,Ltd.

13. Application Note

Setting method for PFM/PWM and fixed PWM modes

For the setting method for each mode, see“Function Description 8.1.11 PFM Control Circuit Block (MODE)”.

Cautions at PFM/PWM mode

If a load current drops rapidly because of rapid load change and others, it tends to take a lot of time to restore overshooting of an output voltage.

As a result, the over-voltage protection may operate.

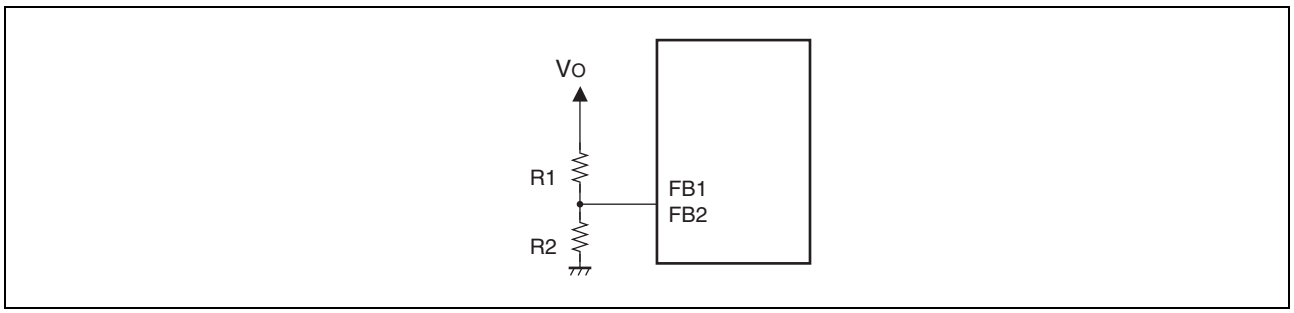
In this case, solution are possible by the addition of the load resistance of value to be able to restore the output voltage in the over-voltage detection time.

Setting method of output voltage

Set it by adjusting the output voltage setting zero-power resistance ratio.

$$V_O = \frac{R1 + R2}{R2} \times 0.7$$

V_O : Output setting voltage [V]
R1, R2 : Output setting resistor value [Ω]



Make sure that the setting does not exceed the maximum on-duty.

Calculate the on-duty by the following formula:

$$D_{MAX\_Min} = \frac{V_O + R_{ON\_Sync} \times I_{OMAX}}{V_{IN} - R_{ON\_Main} \times I_{OMAX} + R_{ON\_Sync} \times I_{OMAX}}$$

D_{MAX_Min} : Minimum value of the maximum on-duty cycle
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
R_{ON_Main} : High-side FET ON resistance [Ω]
R_{ON_Sync} : Low-side FET ON resistance [Ω]
I_{OMAX} : Maximum load current [A]

Oscillation frequency setting method

Set it by adjusting the RT pin resistor value.

$$f_{OSC} = \frac{1.09}{R_{RT} \times 40 \times 10^{-12} + 300 \times 10^{-9}}$$

R_{RT} : RT resistor value [Ω]
f_{OSC} : Oscillation frequency [Hz]

The oscillation frequency must set for on-time (t_{ON}) to become 300ns or more.
Calculate the on-time by the following formula.

$$t_{ON} = \frac{V_O}{V_{IN} \times f_{OSC}}$$

t_{ON} : On-time [s]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
f_{OSC} : Oscillation frequency [Hz]