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MB39A214A

2ch DC/DC Converter IC with PFM/PWM Synchronous Rectification

MB39A214A is a N-ch/ N-ch synchronous rectification type 2ch Buck DC/DC converter IC equipped with a bottom detection comparator for low output voltage ripple. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. It also allows the high switching frequency setting, enabling the downsized peripheral circuits and low-cost configuration. MB39A214A realizes ultra-rapid response and high efficiency with built-in enhanced protection features. It is most suitable for the power supply for ASIC or FPGA core, input/output devices, or memory.

Features

- High efficiency
- Frequency setting by internal preset function: 310 kHz, 620 kHz, 1 MHz
- High accuracy reference voltage : ± 0.7% (Ta = + 25°C)
- VIN Input voltage range : 6 V to 28 V
- Output voltage setting range : 0.7 V to 5.3 V
- Possible to select the automatic PFM/PWM selection mode or PWM-fixed mode
- PAF frequency limitation function (Prohibit Audio Frequency) : > 30 kHz (Min)
- Built-in boost diode, external fly-back diode not required
- Built-in discharge FET
- Built-in over voltage protection function
- Built-in under voltage protection function
- Built-in over temperature protection function
- Built-in over current limitation function
- Soft-start circuit without load dependence
- Current sense resistor not required
- Built-in synchronous rectification type output steps for N-ch MOS FET
- Standby current : 0 µA (Typ)
- Package : TSSOP24 (4.4 mm × 6.5 mm × 1.2 mm [Max])

Applications

- Digital TV
- Photocopiers
- STB
- BD, DVD players/recorders
- Projectors etc.

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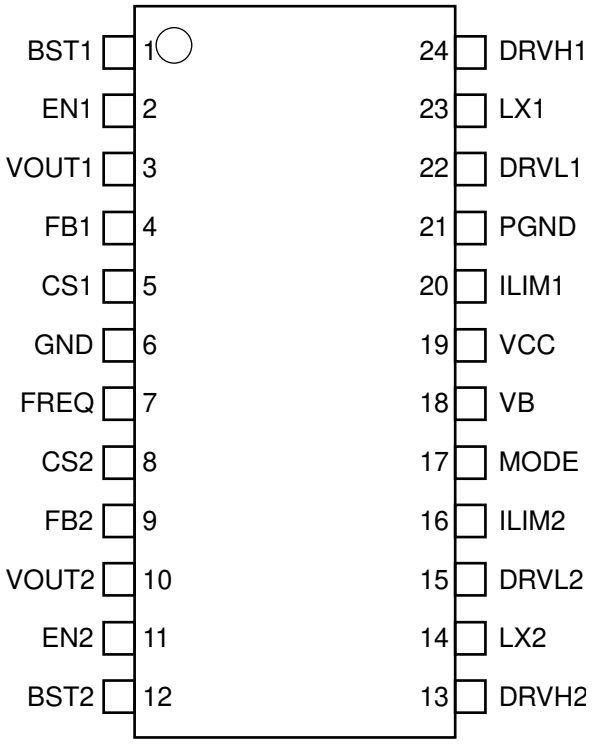
1. Pin Assignment

(TOP VIEW)

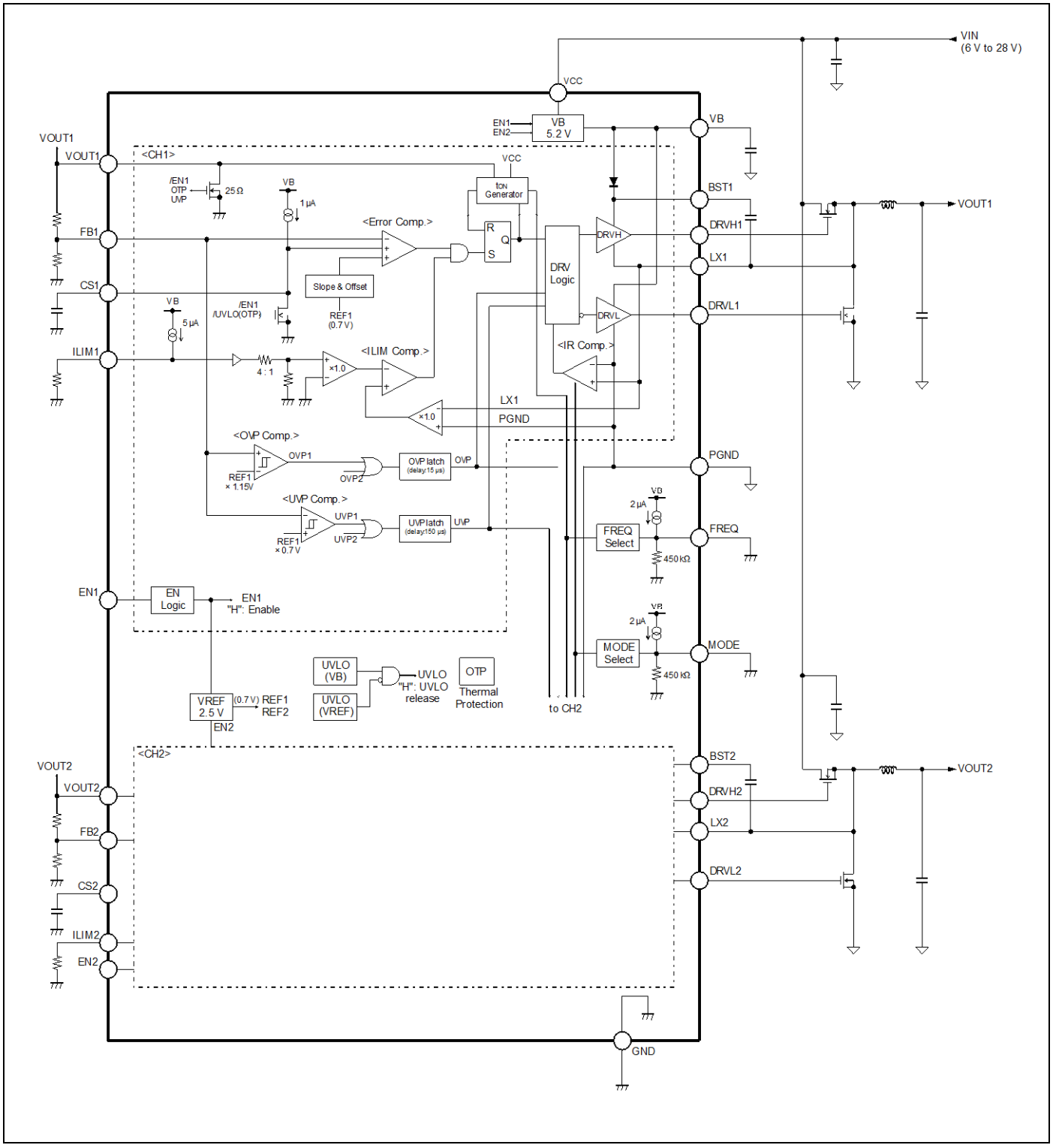


(FPT-24P-M09)

2. Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	BST1	—	CH1 boost capacitor connection pin.
2	EN1	I	CH1 enable pin.
3	VOUT1	I	CH1 input pin for DC/DC output voltage.
4	FB1	I	CH1 input pin for feedback voltage.
5	CS1	I	CH1 soft-start time setting capacitor connection pin.
6	GND	—	Ground pin.
7	FREQ	I	Frequency switching signal input pin. FREQ: GND Short Switching frequency 310 kHz FREQ: Open Switching frequency 620 kHz FREQ: VB Short Switching frequency 1 MHz
8	CS2	I	CH2 soft-start time setting capacitor connection pin.
9	FB2	I	CH2 input pin for feedback voltage.
10	VOUT2	I	CH2 input pin for DC/DC output voltage.
11	EN2	I	CH2 enable pin.
12	BST2	—	CH2 boost capacitor connection pin.
13	DRVH2	O	CH2 output pin for external high-side FET gate drive.
14	LX2	—	CH2 inductor and external high-side FET source connection pin.
15	DRVL2	—	CH2 output pin for external low-side FET gate drive.
16	ILIM2	I	CH2 over current detection level setting voltage input pin.
17	MODE	I	DC/DC control mode switching signal input pin. MODE: GND Short PFM/PWM MODE: Open PFM/PWM, PAF MODE: VB Short PWM fixed
18	VB	O	Internal circuit bias output pin.
19	VCC	I	Power input pin for control and output circuits.
20	ILIM1	I	CH1 over current detection level setting voltage input pin.
21	PGND	—	Ground pin for output circuit.
22	DRVL1	O	CH1 output pin for external low-side FET gate drive.
23	LX1	—	CH1 inductor and external high-side FET source connection pin.
24	DRVH1	O	CH1 output pin for external high-side FET gate drive.

3. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
VCC pin input voltage	V_{VCC}	VCC pin	− 0.3	+ 30	V
BST pin input voltage	V_{BST}	BST1, BST2 pins	− 0.3	+ 36	V
LX pin input voltage	V_{LX}	LX1, LX2 pins	− 1	+ 30	V
Voltage between BST and LX	V_{BST-LX}	—	− 0.3	+ 7	V
EN pin input voltage	V_{EN}	EN1, EN2 pins	− 0.3	+ 30	V
Input voltage	V_{FB}	FB1, FB2 pins	− 0.3	VB + 0.3	V
	V_{VOUT}	VOUT1, VOUT2 pins	− 0.3	+ 7	V
	V_{ILIM}	ILIM1, ILIM2 pins	− 0.3	VB + 0.3	V
	V_{CS}	CS1, CS2 pins	− 0.3	VB + 0.3	V
	V_{FREQ}	FREQ pin	− 0.3	VB + 0.3	V
	V_{MODE}	MODE pin	− 0.3	VB + 0.3	V
Output current	I_{OUT}	DRVH1, DRVH2 pins, DRVL1, DRVL2 pins	—	60	mA
Power dissipation	P_D	Ta ≤ + 25°C	—	+ 1282	mW
Storage temperature	T_{STG}	—	− 55	+ 125	°C

WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
VCC pin input voltage	V_{VCC}	VCC pin	6	-	28	V
BST pin input voltage	V_{BST}	BST1, BST2 pins	-	-	34	V
EN pin input voltage	V_{EN}	EN1, EN2 pins	0	-	28	V
Input voltage	V_{FB}	FB1, FB2 pins	0	-	VB	V
	V_{VOUT}	VOUT1, VOUT2 pins	0	-	5.5	V
	V_{ILIM}	ILIM1, ILIM2 pins	0	-	2	V
	V_{FREQ}	FREQ pin	0	-	VB	V
	V_{MODE}	MODE pin	0	-	VB	V
Peak output current	I_{OUT}	DRVH1, DRVH2 pins, DRVL1, DRVL2 pins Duty ≤ 5% ($t = 1/f_{OSC} \times Duty$)	− 1200	-	+ 1200	mA
Operating ambient temperature	Ta	—	− 30	+ 25	+ 85	°C

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
Users considering application outside the listed conditions are advised to contact their representatives beforehand.

6. Electrical Characteristics

(Ta = +25°C, VCC = 12 V, EN1, EN2 = 5 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Bias Voltage Block [VB Reg.]	Output voltage	V_{VB}	18	VB = 0 A	5.04	5.20	5.36	V
	Input stability	LINE	18	VCC = 6 V to 28 V	—	10	100	mV
	Load stability	LOAD	18	VB = 0 A to − 1 mA	—	10	100	mV
	Short-circuit output current	I_{OS}	18	VB = 0 V	− 145	− 100	− 75	mA
Under voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	18	VB pin	4.0	4.3	4.6	V
		V_{THL}	18	VB pin	3.7	4.0	4.3	V
	Hysteresis width	V_H	18	VB pin	—	0.3[1]	—	V
Soft-Start/ Discharge Block [Soft Start, Discharge]	Charge current	I_{CS}	5,8	CS1, CS2 = 0 V	− 1.5	−1.0	− 0.75	µA
	Electrical discharge resistance	R_D	3,10	EN1, EN2 = 0 V, VOUT1, VOUT2 ≥ 0.15 V	—	25[1]	—	Ω
	Discharge end voltage	V_{VOVTH}	3,10	EN1, EN2 = 0 V, VOUT1, VOUT2 pins	—	0.2[1]	—	V
ON/OFF Time Generator Block [t_{ON} Generator]	ON time (Preset value 1)	t_{ON11}	24	FREQ pin GND connection VCC = 12 V, VOUT1 = 1.5 V	430	538	646	ns
		t_{ON21}	13	FREQ pin GND connection VCC = 12 V, VOUT2 = 1.5V	320	400	480	ns
	ON time (Preset value 2)	t_{ON12}	24	FREQ pin OPEN VCC = 12 V, VOUT1 = 1.5 V	210	263	316	ns
		t_{ON22}	13	FREQ pin OPEN VCC = 12 V, VOUT2 = 1.5 V	160	200	240	ns
	ON time (Preset value 3)	t_{ON13}	24	FREQ pin VB connection VCC = 12 V, VOUT1 = 1.5 V	130	163	196	ns
		t_{ON23}	13	FREQ pin VB connection VCC = 12 V, VOUT2 = 1.5 V	100	125	150	ns
	Minimum ON time (Preset value 1)	$t_{ONMIN11}$	24	FREQ pin GND connection VCC = 12 V, VOUT1 = 0V	—	136	191	ns
		$t_{ONMIN21}$	13	FREQ pin GND connection VCC = 12 V, VOUT2 = 0 V	—	103	145	ns
	Minimum ON time (Preset value 2)	$t_{ONMIN12}$	24	FREQ pin OPEN VCC = 12 V, VOUT1 = 0 V	—	77	108	ns
		$t_{ONMIN22}$	13	FREQ pin OPEN VCC = 12 V, VOUT2 = 0 V	—	58	82	ns
	Minimum ON time (Preset value 3)	$t_{ONMIN13}$	24	FREQ pin VB connection VCC = 12V, VOUT1 = 0 V	—	55	77	ns
		$t_{ONMIN23}$	13	FREQ pin VB connection VCC = 12 V, VOUT2 = 0 V	—	43	61	ns
	Minimum OFF time	t_{OFFMIN}	24, 13	—	—	410	535	ns

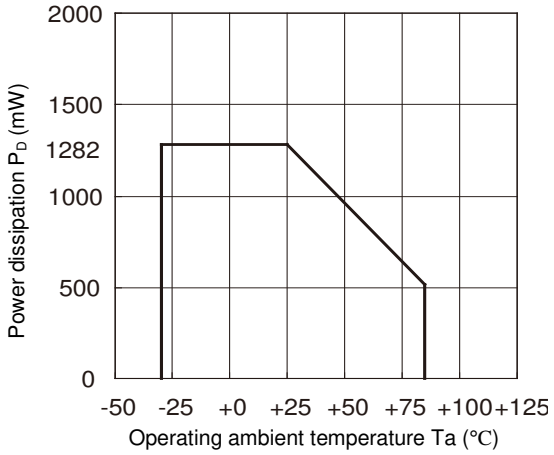
Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Error Comparison Block [Error Comp.]	Threshold voltage	V_{TH}	4, 9	Ta = +25°C	0.695	0.700	0.705	V
	FB pin input current	I_{FB}	4, 9	FB1, FB2 = 0.7 V	− 0.1	0	+0.1	µA
	VOUT pin input current	I_{VO}	3,10	VOUT1, VOUT2 = 1.5 V	—	6.0	8.6	µA
Over Current Detection Block [ILIM Comp.]	Over current detection offset voltage	$V_{OFFILIM}$	21 to 23 21 to 14	PGND − LX1, LX2 ILIM1, ILIM2 = 500 mV	− 30	0	+30	mV
	ILIM pin current	I_{ILIM}	20,16	ILIM1, ILIM2 = 0 V	− 6	− 5	− 4	µA
	ILIM pin current Temperature slope	T_{ILIM}	20,16	Ta = +25°C	—	4500[1]	—	ppm/°C
Over-voltage Protection Circuit Block [OVP Comp.]	Over-voltage detecting voltage	V_{OVP}	4, 9	For REF1, REF2 voltage	110	115	120	%
	Hysteresis width	V_{HOVP}	4, 9	—	—	5[1]	—	%
	Detection delay time	t_{OVP}	—	—	10	15	20	µs
Under-voltage Protection Circuit Block [UVP Comp.]	Under-voltage detecting voltage	V_{UVP}	4, 9	For REF1, REF2 voltage	65	70	75	%
	Hysteresis width	V_{HUVP}	4, 9	—	—	10[1]	—	%
	Detection delay time	t_{UVP}	—	—	100	150	200	µs
Over-temperature Protection Circuit Block [OTP]	Protection temperature	T_{OTPH}	—	—	—	150[1]	—	°C
		T_{OTPL}	—	—	—	125[1]	—	°C
Output Block [DRV]	High-side output on-resistance	R_{OH}	24,13	DRVH1, DRVH2 = − 100 mA	—	4	6	Ω
		R_{OL}	24,13	DRVH1, DRVH2 = 100 mA	—	1	1.5	Ω
	Low-side output on-resistance	R_{OH}	22,15	DRVL1, DRVL2 = − 100 mA	—	4	6	Ω
		R_{OL}	22,15	DRVL1, DRVL2 = 100 mA	—	1	1.5	Ω
	Output source current	I_{SOURCE}	24,13 22,15	LX1, LX2 = 0 V, BST1, BST2 = VB DRVH1, DRVH2 = 2.5 V Duty ≤ 5%	—	− 0.5[1]	—	A
	Output sink current	I_{SINK}	24,13 22,15	LX1, LX2 = 0 V, BST1, BST2 = VB DRVH1, DRVH2 = 2.5 V Duty ≤ 5%	—	0.9[1]	—	A
	Dead time	t_D	24 to 22 13 to 15	LX1, LX2 = 0 V, BST1, BST2 = VB DRVL1, DRVL2-low to DRVH1, DRVH2-on	15	25	35	ns
				LX1, LX2 = 0 V, BST1, BST2 = VB DRVH1, DRVH2-low to DRVL1, DRVL2-on	35	50	65	ns
	BST diode voltage	V_F	1,12	I_F = 10 mA	0.75	0.85	0.95	V
	Bias current	I_{BST}	1,12	LX1, LX2 = 0 V, BST1, BST2 = 5.2 V	11	15	22	µA

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Switching Frequency Control Block [FREQ]	Preset value 1 conditions	V_{FREQ1}	7	FREQ pin: GND connection	0	—	0.2	V
	Preset value 2 conditions	V_{FREQ2}	7	FREQ pin: OPEN	0.6	—	1.2	V
	Preset value 3 conditions	V_{FREQ3}	7	FREQ pin: VB connection	2.4	—	VB	V
	FREQ pin output voltage	V_{FREQ}	7	FREQ = OPEN	0.63	0.9	1.17	V
PFM Control Circuit Block [MODE]	PFM/PWM mode conditions PAF function negate	V_{PFM1}	17	MODE pin: GND connection	0	—	0.2	V
	PFM/PWM mode conditions PAF function assert	V_{PFM2}	17	MODE pin : OPEN	0.6	—	1.2	V
	PWM-fixed mode conditions	V_{PWM}	17	MODE pin : VB connection	4.6	—	VB	V
	PAF frequency	f_{PAF}	—	Ta = − 30°C to +85°C	30	45	—	kHz
	MODE pin voltage	V_{MODE}	17	MODE = OPEN	0.63	0.9	1.17	V
Enable Block [EN1 , EN2]	ON condition	V_{ON}	2, 11	EN1, EN2 pins	2.64	—	—	V
	OFF condition	V_{OFF}	2, 11	EN1, EN2 pins	—	—	0.66	V
	Hysteresis width	V_H	2, 11	EN1, EN2 pins	—	0.4[1]	—	V
	Input current	I_{EN}	2, 11	EN1, EN2 = 5V	11	15	22	µA
Power Supply Current	Standby current	I_{CCS}	19	EN1, EN2 = 0V	—	0	10	µA
	Power supply current during idle period	I_{CC1}	19	LX1, LX2 = 0 V BST1, BST2 : VB connection FB1, FB2 = 0.75 V	—	600	860	µA
	Power supply current during operation	I_{CC2}	19	LX1, LX2 = 0V BST1, BST2 : VB connection FB1, FB2 = 0.6 V	—	1200	1700	µA

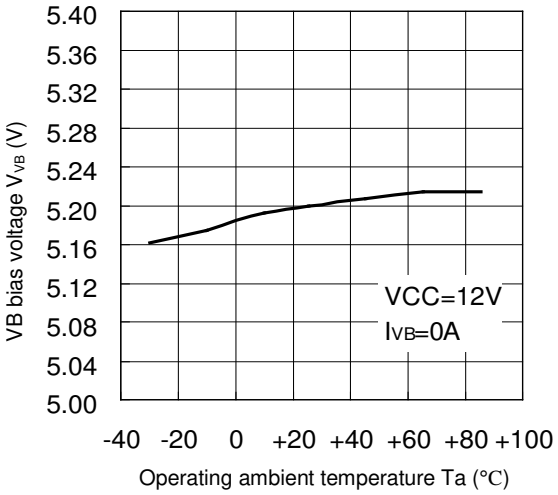
[1]: This parameter is not be specified. This should be used as a reference to support designing the circuits.

7. Typical Characteristics

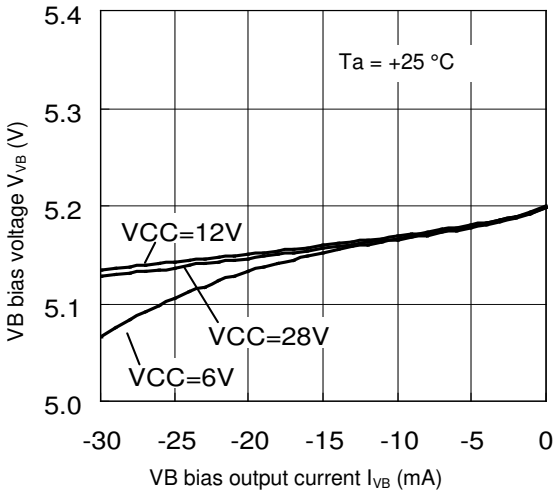
Power dissipation vs. Operating ambient temperature



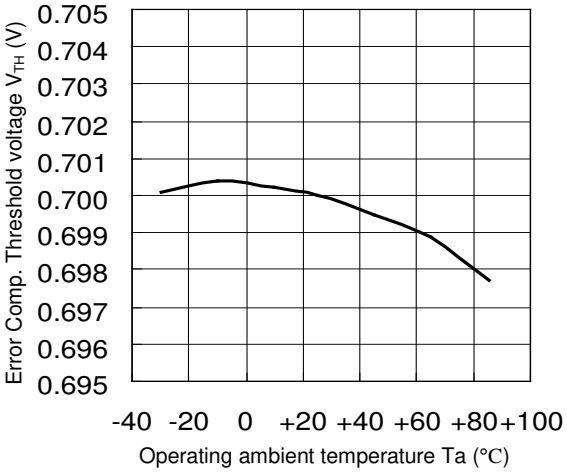
VB bias voltage vs. Operating ambient temperature



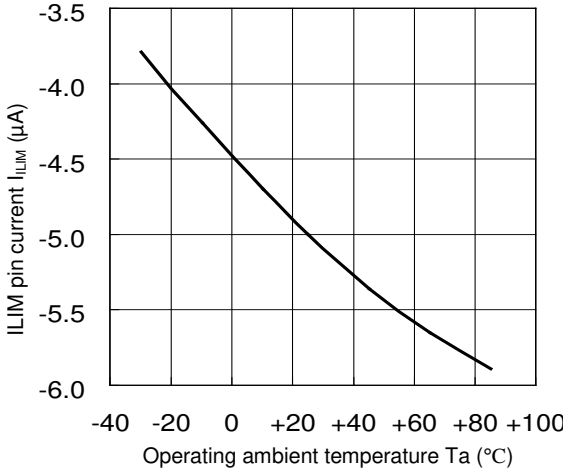
VB bias voltage vs. VB bias output current



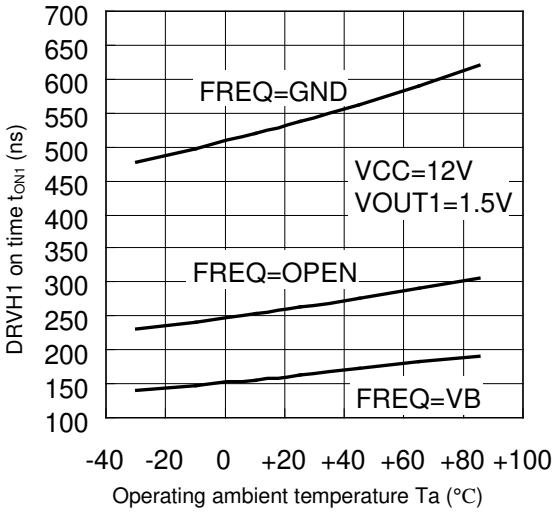
Error Comp. Threshold voltage vs. Operating ambient temperature



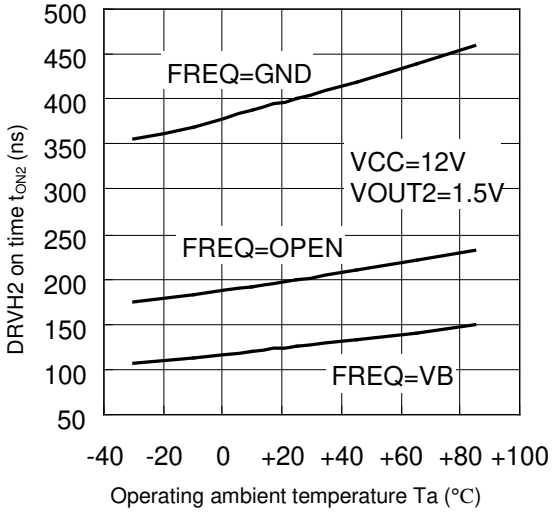
ILIM pin current vs. Operating ambient temperature



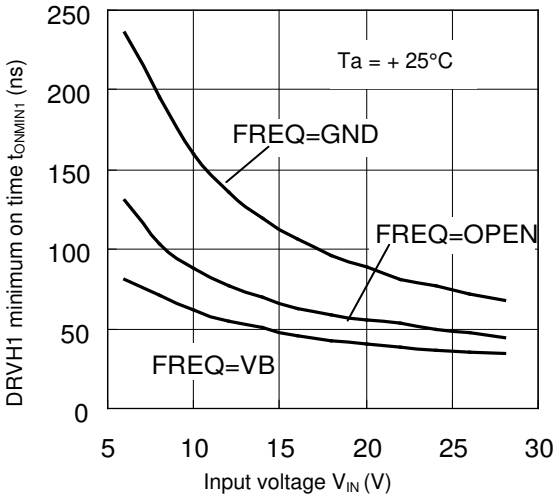
DRVH1 on time vs. Operating ambient temperature



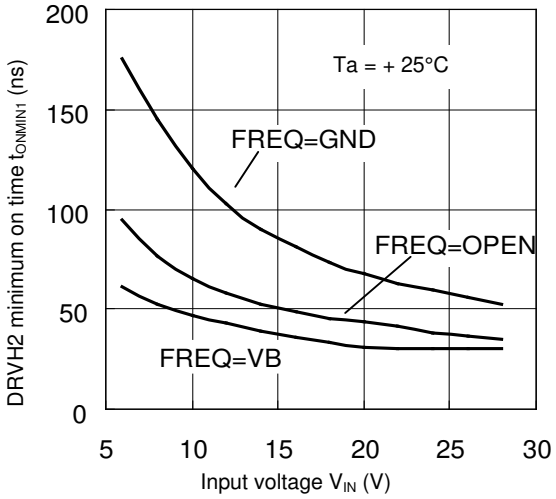
DRVH2 on time vs. Operating ambient temperature



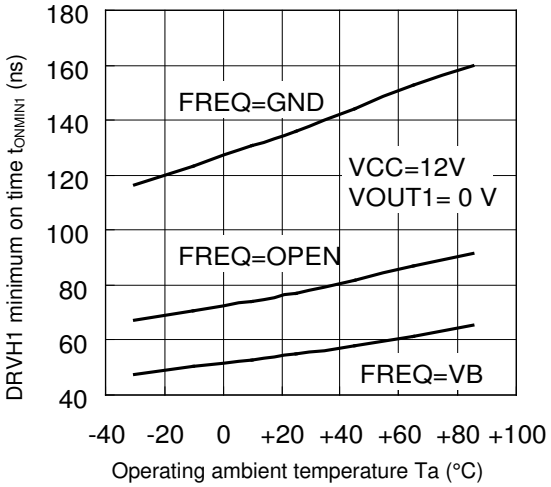
DRVH1 minimum on time vs. Input voltage



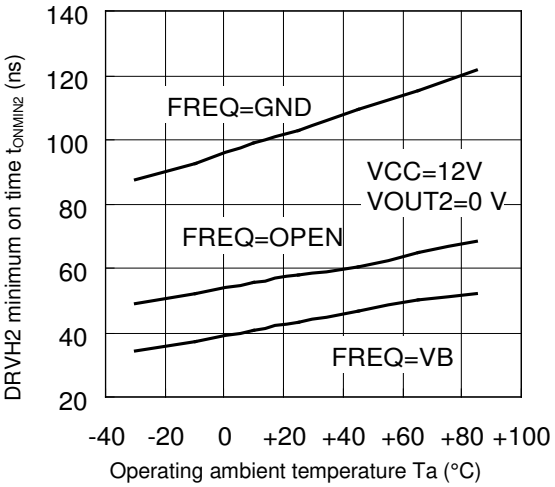
DRVH2 minimum on time vs. Input voltage



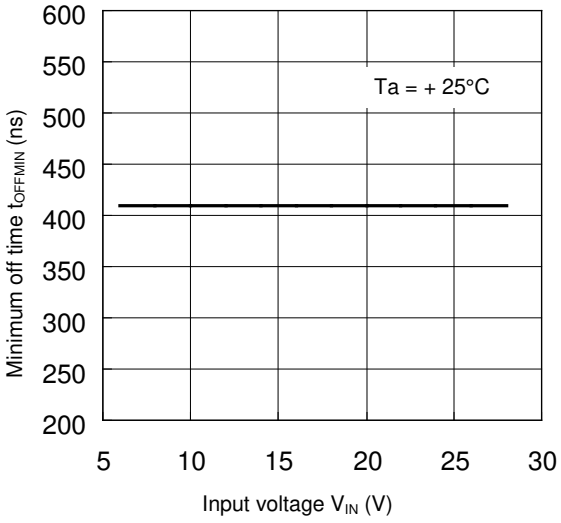
DRVH1 minimum on time vs.
Operating ambient temperature



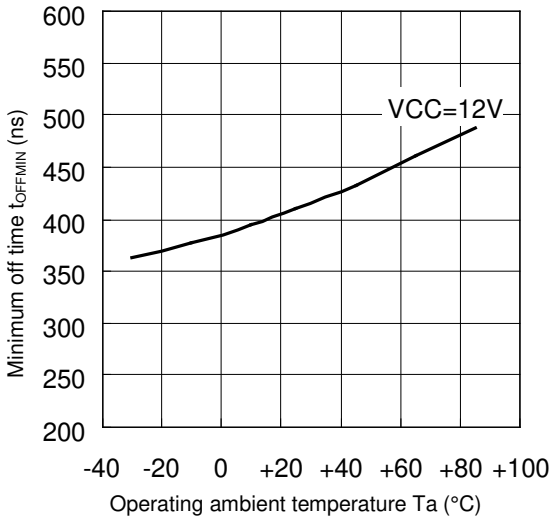
DRVH2 minimum on time vs.
Operating ambient temperature



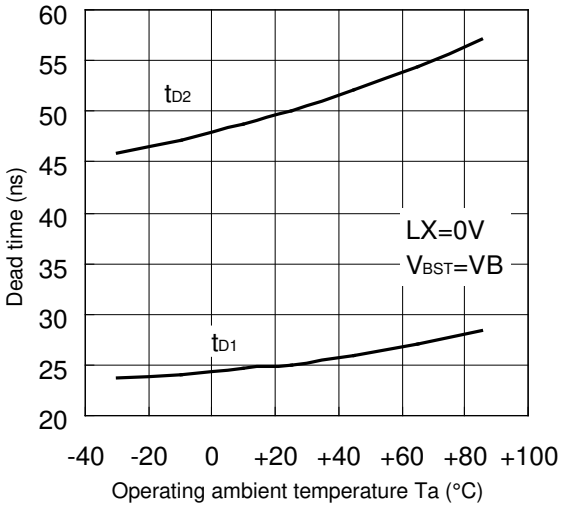
Minimum off time vs. Input voltage



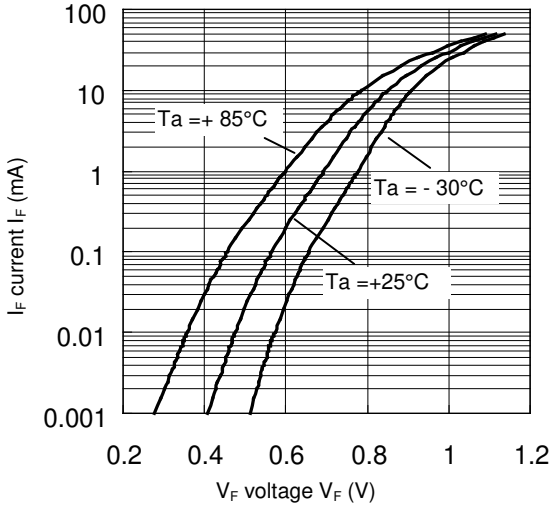
Minimum off time vs.
Operating ambient temperature



Dead time vs. Operating ambient temperature



Bootstrap diode I_F vs. V_F



t_{D1} : Period from DRVL off to DRVH on

t_{D2} : Period from DRVH off to DRVL on

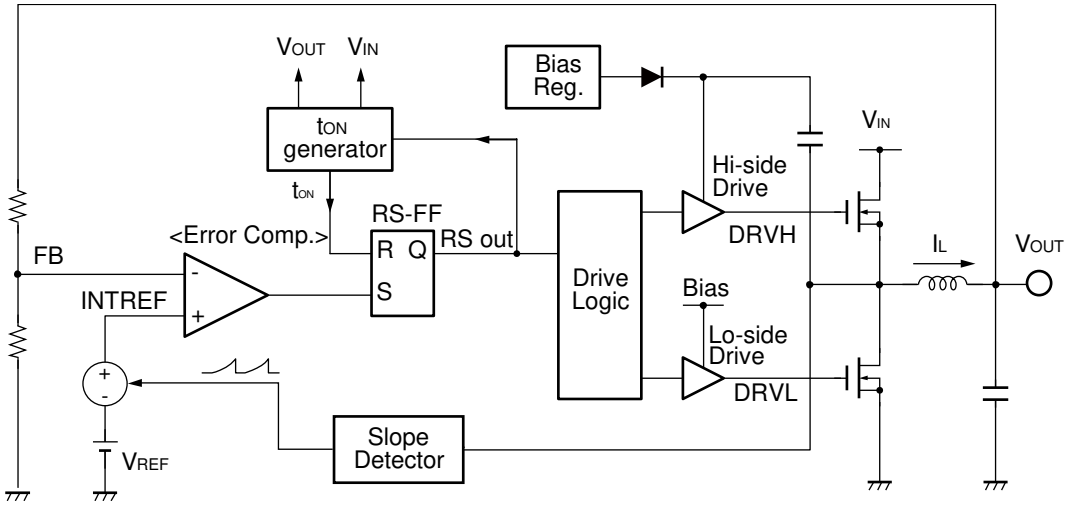
8. Function

Bottom detection comparator system for low output voltage ripple

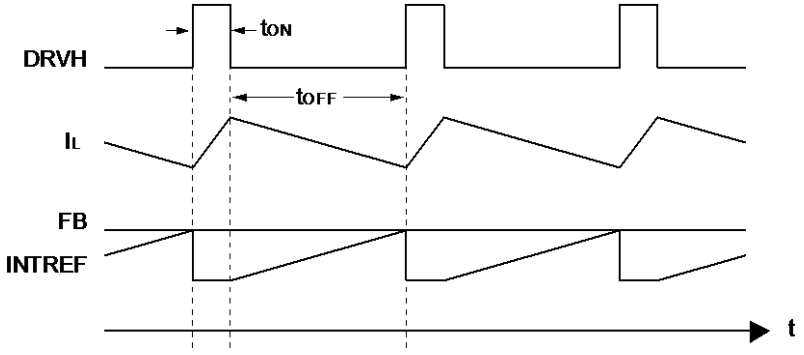
The bottom detection comparator system for low output voltage ripple determines the ON time (t_{ON}) using the input voltage (V_{IN}) and output voltage (V_{OUT}) to hold the ON state to a specified period. During the OFF period, the reference voltage (INTREF) is compared with the feedback voltage (FB) using the error comparator (Error Comp.). When the feedback voltage (FB) is below the reference voltage (INTREF), RS-FF is set and the ON period starts again. Switching is repeated as described above. Error Comp. is used to compare the reference voltage (INTREF) with the feedback voltage (FB) to control the off-duty condition in order to stabilize the output voltage.

This system adds the inductor current slope detected during the synchronous rectification period (t_{OFF}) to the reference voltage (INTREF) , and generates an output voltage slope during the OFF period, which is essential for the bottom detection comparator system, in the IC. This enables the stable control operations under the low output voltage ripple conditions.

- Circuit diagram



- Waveforms



1. Bias Voltage Block (VB Reg.)

The 5.2 V (Typ) bias voltage is generated from the VCC pin voltage for the control, output, and boost circuits. When either or both of the EN1 pin (pin 2) and EN2 pin (pin 11) are set to the “H” level, the system is restored from the standby state to supply the bias voltage from the VB pin (pin 18).

2. ON/OFF Time Generator Block (t_{ON} Generator)

This block contains a capacitor for timing setting and a resistor for timing setting and generates ON time (t_{ON}) which depends on input voltage and output voltage. The switching frequency can be switched by setting the FREQ pin (pin 7) to any one of GND connection, OPEN, and VB connection. ON time for each CH is obtained from the following formula.

<FREQ pin: GND connection>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 4300 \quad (f_{OSC1} \fallingdotseq 230\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 3200 \quad (f_{OSC2} \fallingdotseq 310\ kHz)$$

<FREQ pin: OPEN>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 2100 \quad (f_{OSC1} \fallingdotseq 460\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 1600 \quad (f_{OSC2} \fallingdotseq 620\ kHz)$$

<FREQ pin: VB connection>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 1300 \quad (f_{OSC1} \fallingdotseq 750\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 1000 \quad (f_{OSC2} \fallingdotseq 1000\ kHz)$$

The switching frequency of CH2 is set to 1.33 times that of CH1 to prevent the beat by the frequency difference of channel to channel.

3. Output Block (DRV1, DRV2)

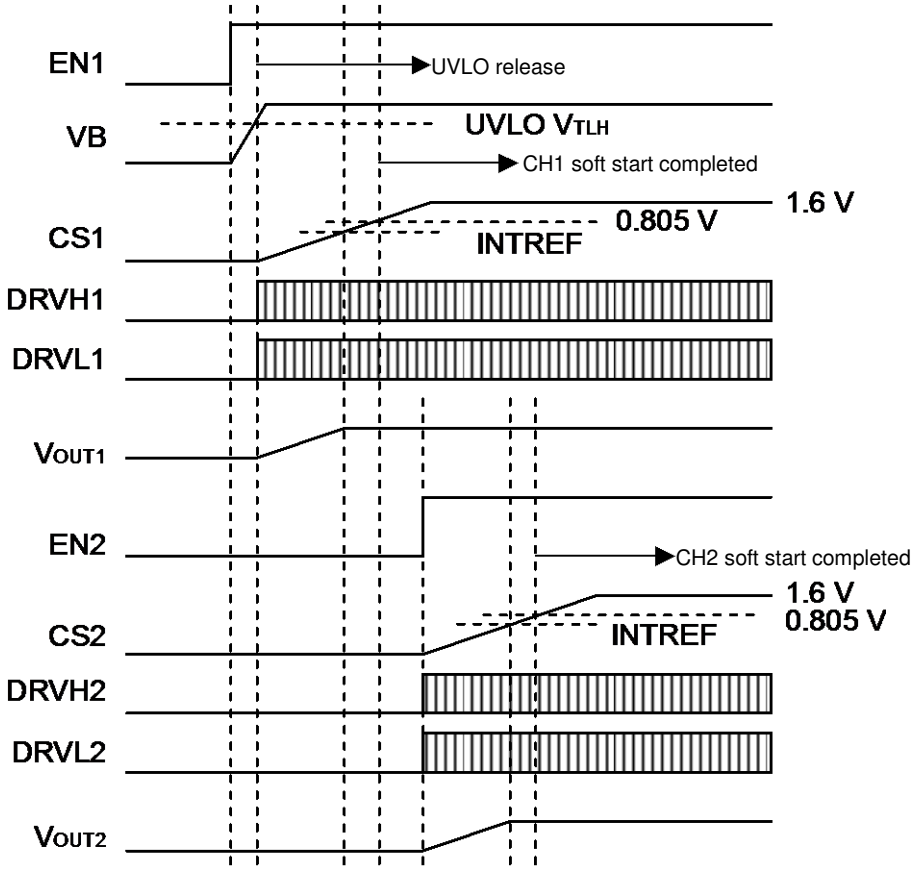
The output circuit is configured in CMOS type for both of the high-side and the low-side. It provides the 0.5 A (Typ) source current and 0.9 A (Typ) sink current, drive the external N-ch MOS FET. The output circuit of the high-side FET supplies the power from the boost circuit including the built-in boost diode. The output circuit of the low-side FET supplies the power from the VB pin. This circuit monitors the gate voltages of the high-side and low-side FETs. Until either FET is turned off, this circuit controls the ON timing of another FET, preventing the shoot-through current. The sink ON resistance of the output circuit is low 1 Ω (Typ), improve the self turn on margin of low-side FET.

4. Starting sequence

When the EN1 pin (pin 2) or EN2 pin (pin 11) is set to the “H” level, the bias voltage is supplied from the VB pin. If the voltage of the VB pin exceeds the UVLO threshold voltage, the DC/DC converter starts operations and carries out the soft start. The soft start is a function used to prevent a rush current when the power is started.

Activating the soft start initiates charging of the capacitor connected to the CS1 pin (pin 5) and CS2 pin (pin 8) and inputs the lamp voltage to the error comparator (Error Comp.) of each channel. The DC/DC converter generates the output voltage according to that lamp voltage. This results in the soft start operation that does not depend on the output load. The over voltage protection (OVP) and under voltage protection (UVP) functions are disabled while the soft start is active.

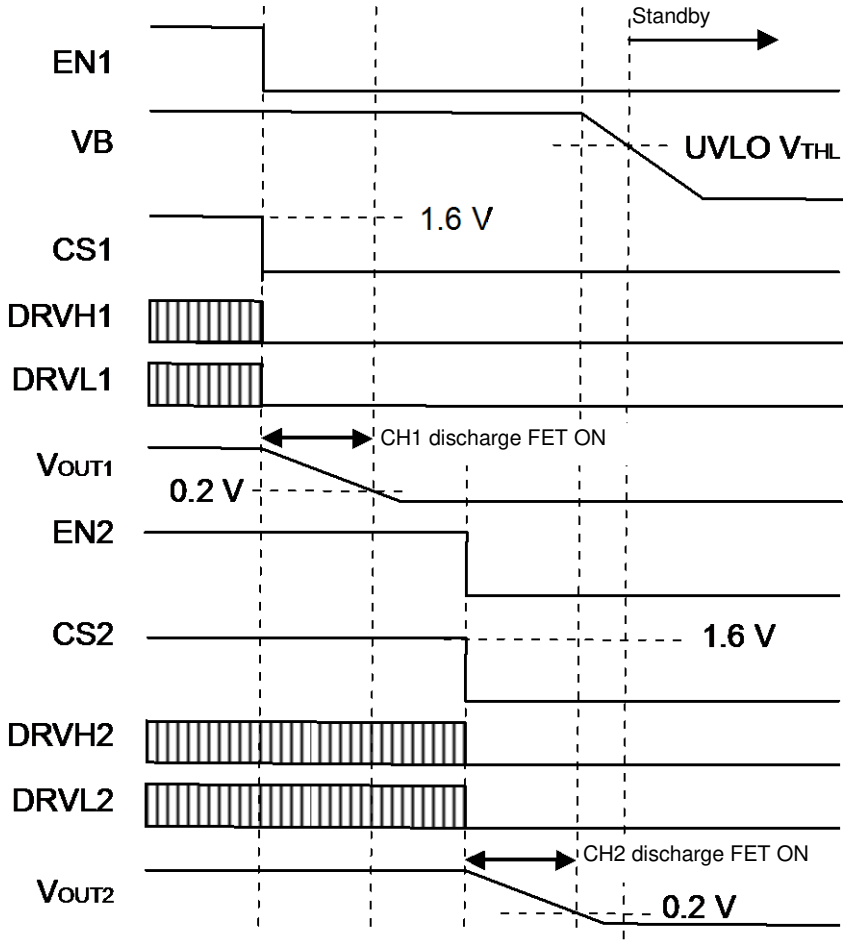
<Timing chart>



5. DC/DC converter stop sequence (Discharge, standby)

When the EN1 pin (pin 2) or EN2 pin (pin 11) is set to the “L” level, the output capacitor is discharged using the discharge FET (R_{ON} ≒ 25 Ω) in the IC. If the voltage of the VOUT1 pin (pin 3) and VOUT2 pin (pin 10) is below 0.2 V (Typ) by discharging the output capacitor, the IC stops discharge operation. Further, if both the EN1 and EN2 pins are set to the “L” level, the IC also stops the output of the VB pin and enters the standby state after detecting UVLO. The current of the VCC pin (I_{VCC}) is then 10 µA (Max).

<Timing chart>



6. Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection (UVLO) protects ICs from malfunction and protects the system from destruction/deterioration, according to the reasons mentioned below.

■Transitional state when the bias voltage (VB) or the reference voltage (VREF) starts.

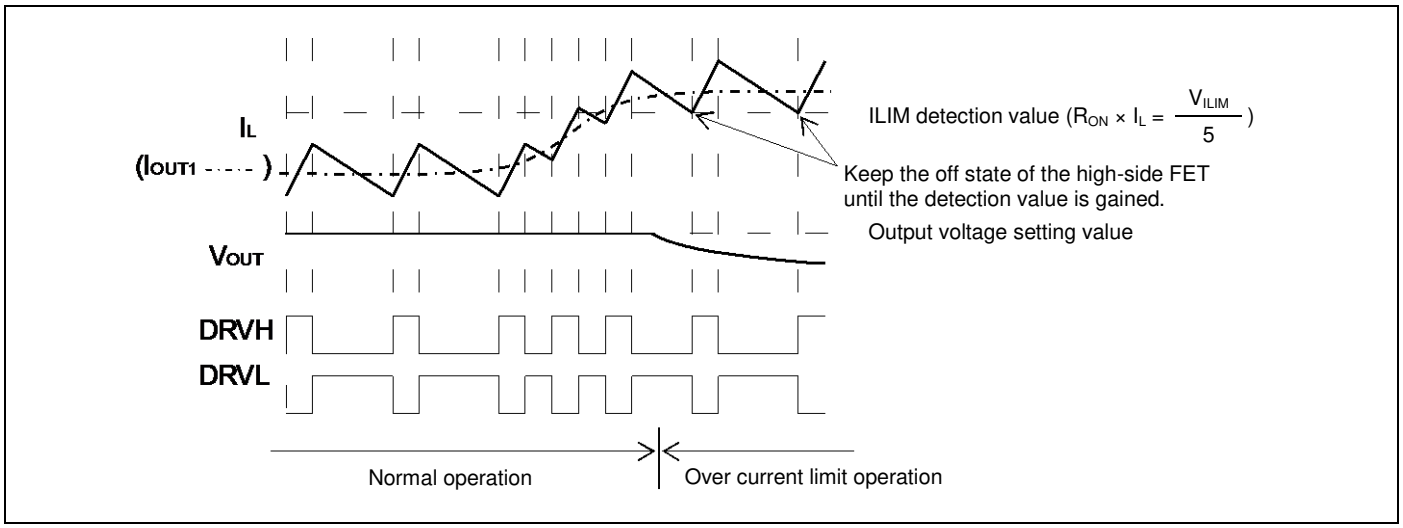
■Momentary decrease

To prevent such a malfunction, this function detects a voltage drop of the VB pin (pin 18) using the comparator (UVLO Comp.), and stops IC operations.
When the VB pin exceeds the threshold voltage of the under voltage lockout protection circuit, the system is restored.

7. Over Current Limitation (ILIM)

This function limits the output current when it has increased, and protects devices connected to the output. This function detects the inductor current I_L from the electromotive force of the low-side FET on-resistance R_{ON}, and compares this voltage with the 1/5-time value of the voltage V_{ILIM} of the ILIM1 pin (pin 20) and ILIM2 pin (pin 16) on a cyclically, using ILIM Comp. Until this voltage falls below the over current limit value, the high-side FET is held in the off state. After the voltage has fallen below the limit value, the high-side FET is placed into the on state. This limits the lower bound of the inductor current and also restricts the over current. As a result, it becomes operation that the output voltage droops.

The over current limit value is set by connecting the resistor to the ILIM pin. The ILIM pin supplies the constant current of 5 µA (Typ). However, the current value has a temperature slope up to 4500 ppm/°C to compensate the temperature dependence characteristics of the low-side FET on-resistance.



8. Over Voltage Protection (OVP)

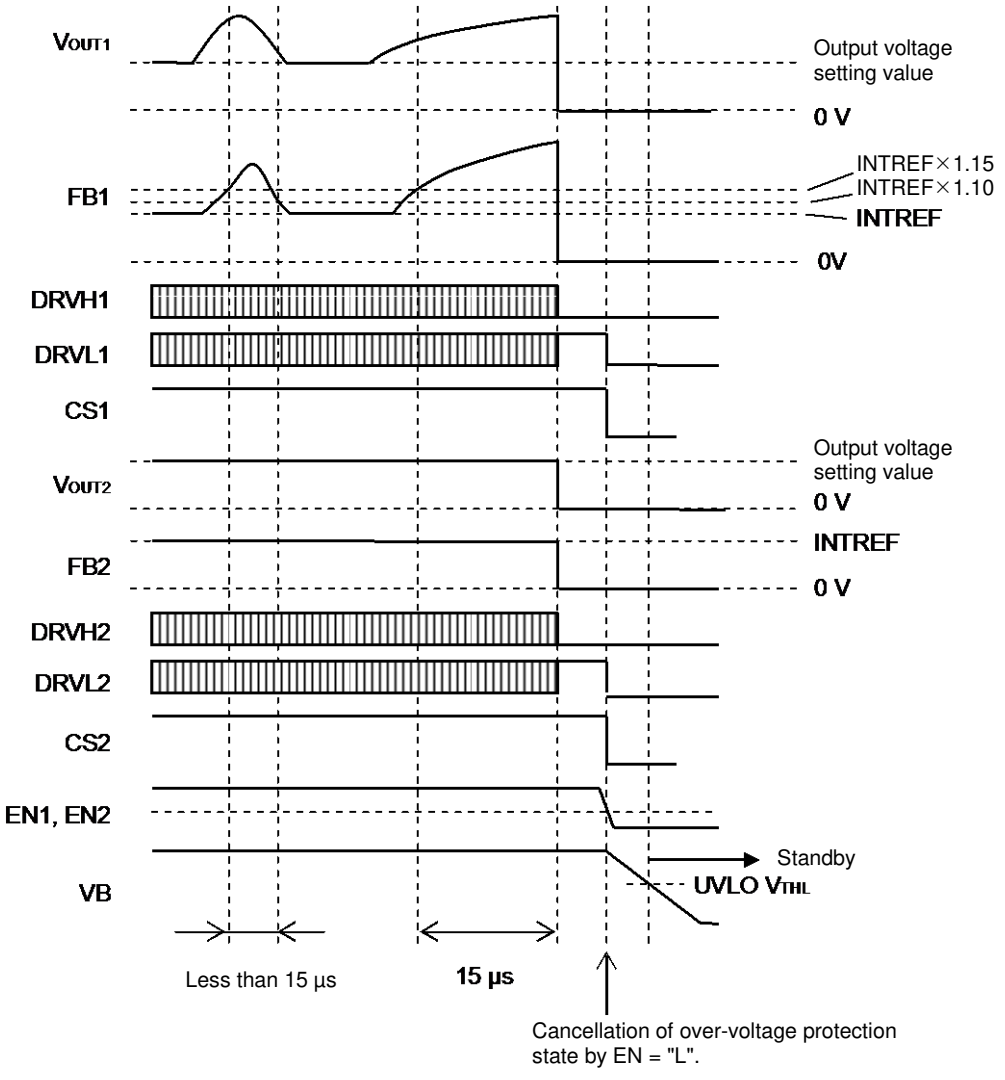
This function stops the output voltage when the output voltage has increased, and protects devices connected to the output.

(1) Using OVP Comp, this function makes a comparison between the voltage which is 1.15 times (Typ) of the internal reference voltage INTREF1 and INTREF2 (0.7 V), and the feedback voltage for the FB1 pin (pin 4) and the FB2 pin (pin 9).

(2) If the feedback voltage mentioned in 1 detects the higher state by 15 µs (Typ) or more, the operations below will be performed.
- Set the RS latch.
- Set the DRVH1 pin (pin 24) and the DRVH2 pin (pin 13) to the “L” level.
- Set the DRVL1 pin (pin 22) and the DRVL2 pin (pin 15) to the “H” level.

These operations fix the high-side FET to the off state and the low-side FET to the on state for both channels of the DC/DC converter, and stops switching (latch stop).The over-voltage protection state can be cancelled by setting both the EN1pin (pin 2) and EN2 pin (pin 11) to the “L” level or reducing the VCC power once until the bias voltage (VB) falls below V_{THL} of UVLO.

<Timing chart>



9. Under Voltage Protection (UVP)

This function stops the output voltage when the output voltage has lowered, and protects devices connected to the output.

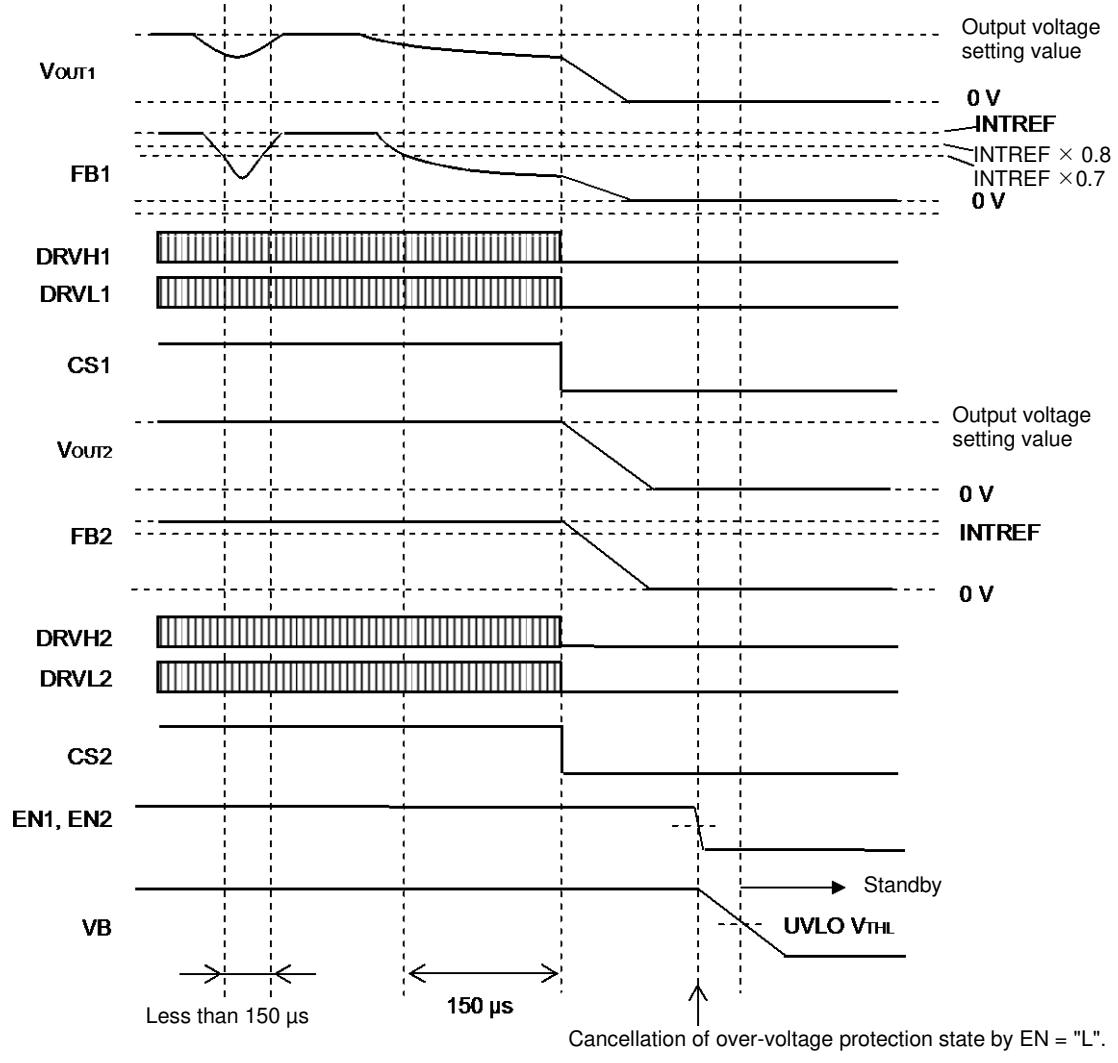
(1) Using UVP Comp, this function makes a comparison between the voltage which is 0.7 times (Typ) of the internal reference voltage REF1, REF2 (0.7 V), and the feedback voltage for the FB1 pin (pin 4) and the FB2 pin (pin 9).

(2) If the feedback voltage mentioned in 1 detects the higher state by 150µs (Typ) or more, the operations below will be performed.

- Set the RS latch.
- Set the DRVH1 pin (pin 24) and the DRVH2 pin (pin 13) to the “L” level.
- Set the DRVL1 pin (pin 22) and the DRVL2 pin (pin 15) to the “L” level.

These operations fix the high-side FET to the off state and the low-side FET to the off state for both channels of the DC/DC converter, and stops switching (latch stop). The discharge operation is then carried out to discharge the output capacitor (The discharge operation continues until the state of the under-voltage protection is released).
The under-voltage protection state can be cancelled by setting both the EN1 pin (pin 2) and EN2 pin (pin 11) to the “L” level or reducing the VCC power once until the bias voltage (VB) falls below V_{THL} of UVLO.

<Timing chart>



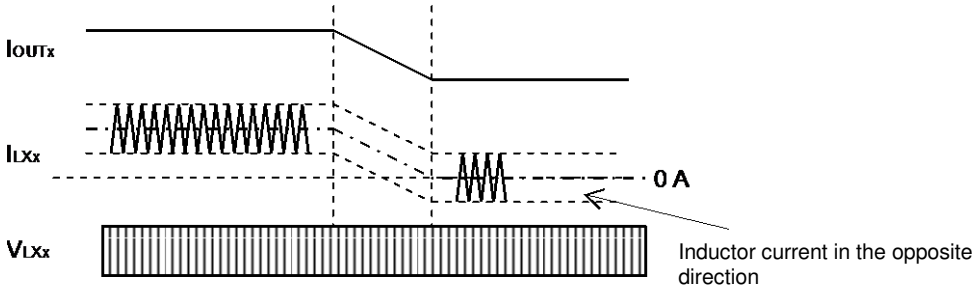
10. Over Temperature Protection (OTP)

The over-temperature protection circuit block (OTP) provides a function that prevents the IC from a thermal destruction. If the junction temperature reaches + 150°C, the DRVH1 pin (pin 24) and DRVH2 pin (pin 13) are set to the “L” level, and the DRVL1 pin (pin 22) and DRVL2 pin (pin 15) are set to the “L” level. This fixes the high-side and low-side FETs to the off-state, of both channels in the DC/DC converter, causing switching to be stopped. The discharge operation is then carried out to discharge the output capacitor (The discharge operation continues until the state of the over-temperature protection is released). If the junction temperature drops to + 125°C, the soft start is reactivated. (Restored automatically.)

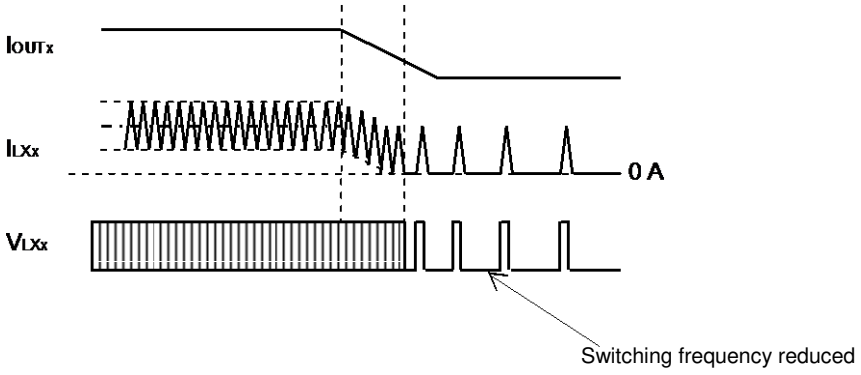
11. Operation mode

In the PWM-fixed mode, the system acts by the switching frequency specified with the FREQ pin regardless of the load.
In the automatic PFM/PWM selection mode, the switching frequency is reduced at low load, for enhancing the conversion efficiency characteristics. This function detects 0 A of the inductor current from the electromotive force of the low-side FET ON resistance when the low-side FET ON state, and places the low-side FET into the off state. This idle period continued until the output voltage decreased, this results the switching frequency being reduced automatically depending on the load current when the inductor current is below the critical current. The system acts by the switching frequency specified with the FREQ pin, when the inductor current exceeds the critical current.
For Automatic PFM/PWM selection mode with PAF function, the switching frequency at low load is held to 30 kHz (Min) or more.
The operation mode can be switched by setting the MODE pin (pin 17) to any one of GND connection, OPEN, and VB connection.

- PWM-fixed mode



- Automatic PFM/PWM selection mode



X : Each channel number

Enable function table

EN1 pin	EN2 pin	DC/DC converter (CH1)	DC/DC converter (CH2)
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

DC/DC Control mode function table

MODE pin	DC/DC control
GND connection	Automatic PFM/PWM selection mode
OPEN	Automatic PFM/PWM selection mode with PAF function
VB connection	PWM-fixed mode

Switching frequency control function table

FREQ pin	Switching frequency
GND connection	$f_{OSC1} \fallingdotseq 230$ kHz, $f_{OSC2} \fallingdotseq 310$ kHz
OPEN	$f_{OSC1} \fallingdotseq 460$ kHz, $f_{OSC2} \fallingdotseq 620$ kHz
VB connection	$f_{OSC1} \fallingdotseq 750$ kHz, $f_{OSC2} \fallingdotseq 1000$ kHz

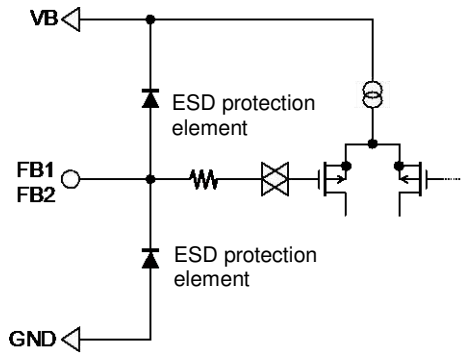
Protection function table

The following table shows the state of the VB pin (pin 18), the DRVH1 pin (pin 24), the DRVH2 pin (pin 13), the DRVL1 pin (pin 22), the DRVL2 pin (pin 15) when each protection function operates.

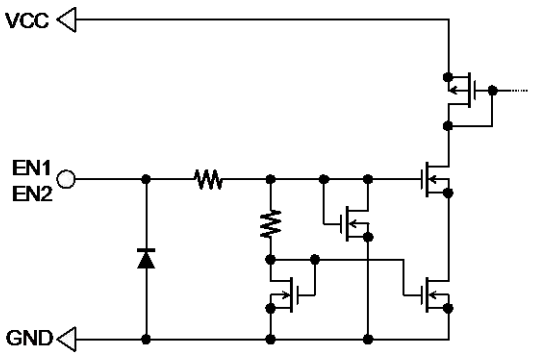
Protection function	Detection condition	Output of each pin after detection			DC/DC output dropping operation
		VB	DRVH1, DRVH2	DRVL1, DRVL2	
Under Voltage Lockout Protection (UVLO)	VB < 4.0 V	—	L	L	Natural electric discharge
Over-current limitation (ILIM)	V_{PGND} - V_{LX1}, V_{LX2} > V_{ILIM1}, V_{ILIM2}	5.2 V	Switching	Switching	The voltage is dropped by the constant current
Over Voltage Protection (OVP)	V_{FB1}, V_{FB2} > INTREF1, INTREF2×1.15 (15 µs or higher)	5.2 V	L	H	0 V clamping
Under Voltage Protection (UVP)	V_{FB1}, V_{FB2} > INTREF1, INTREF2×0.7 (150 µs or higher)	5.2 V	L	L	Electrical discharge by discharge function
Over Temperature Protection (OTP)	Tj > + 150°C	5.2 V	L	L	Electrical discharge by discharge function
Enable (EN)	EN1, EN2: H ⟶ L (V_{OUT1}, V_{OUT2} > 0.2 V)	5.2 V	L	L	Electrical discharge by discharge function

9. I/O Pin Equivalent Circuit Diagram

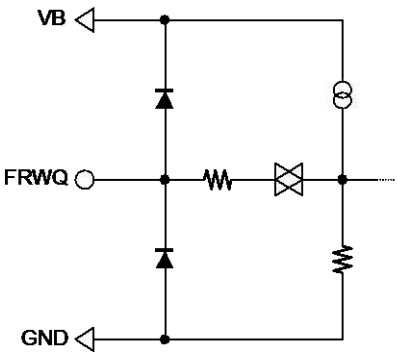
FB1, FB2 pins



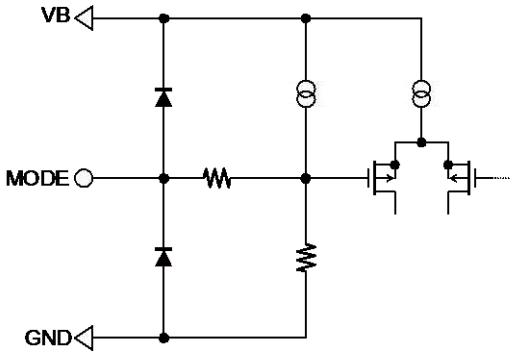
EN1, EN2 pins



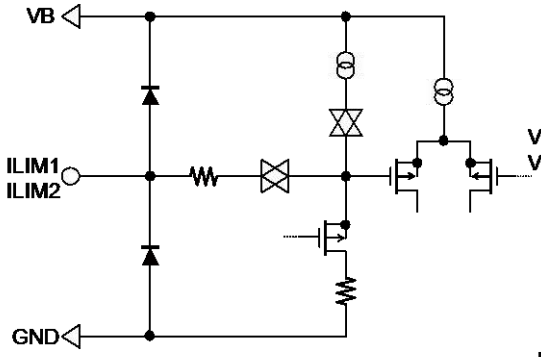
FREQ pin



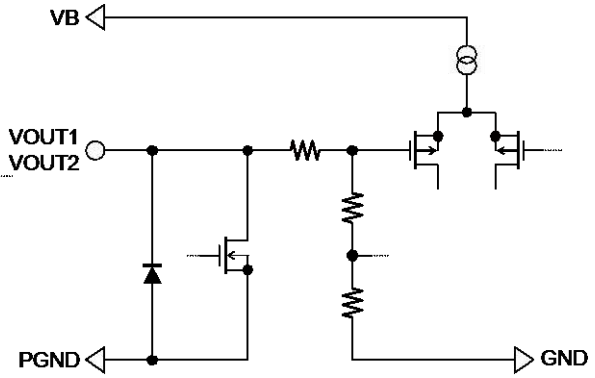
MODE pin



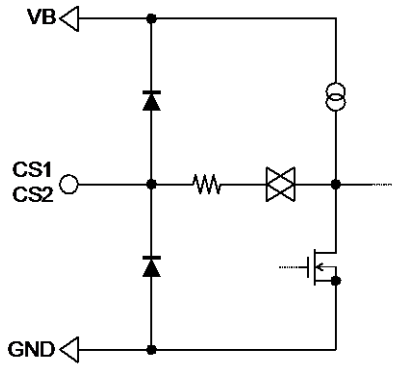
ILIM1, ILIM2 pins



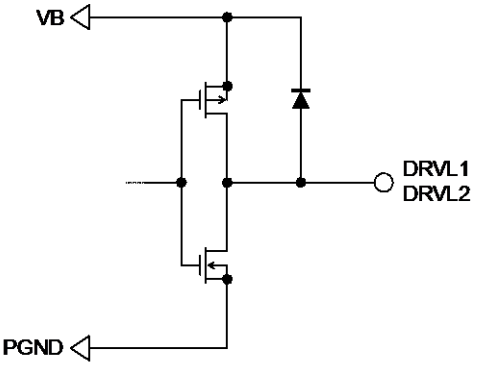
VOUT1, VOUT2 pins



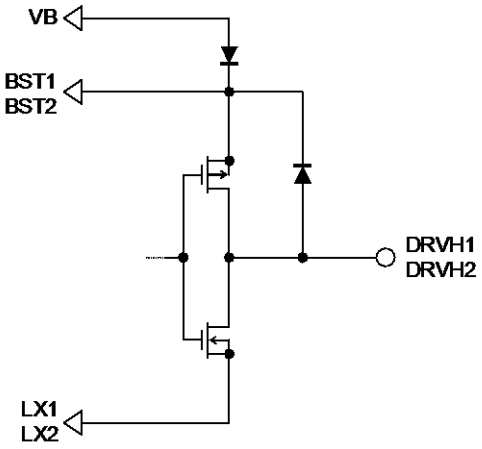
CS pin



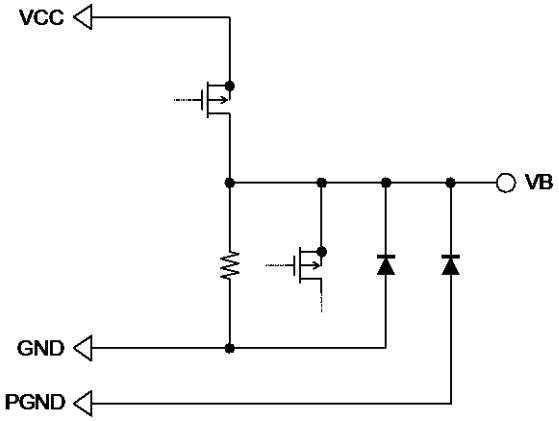
DRVL1, DRVL2 pins



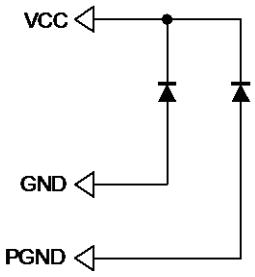
DRVH1, DRVH2, BST1, BST2, LX1, LX2 pins



VB pin



VCC pin



10. Example Application Circuit