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MB39C006A

1 ch DC/DC Converter IC with PFM/PWM Synchronous Rectification

Description

The MB39C006A is a current mode type 1-channel DC/DC converter IC built-in switching FET, synchronous rectification, and down conversion support. The device is integrated with a switching FET, oscillator, error amplifier, PFM/PWM control circuit, reference voltage source, and POWERGOOD circuit.
External inductor and decoupling capacitor are needed only for the external component.
MB39C006A is small, achieve a highly effective DC/DC converter in the full load range, this is suitable as the built-in power supply for handheld equipment such as mobile phone/PDA, DVDs, and HDDs.

Features

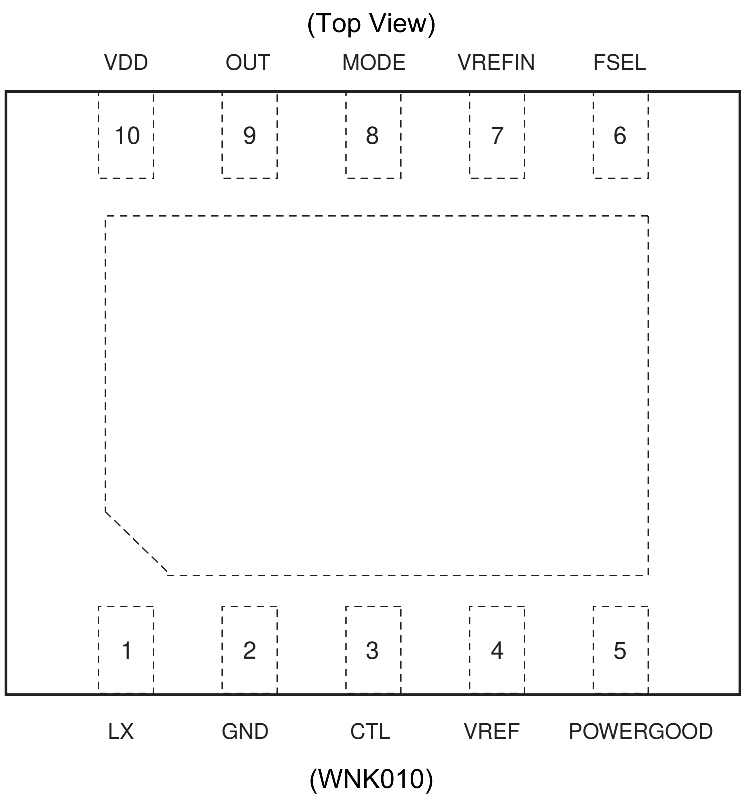
- High efficiency : 96% (Max)
- Low current consumption : 30 μA (at PFM)
- Output current (DC/DC) : 800 mA (Max)
- Input voltage range : 2.5 V to 5.5 V
- Operating frequency : 2.0/3.2 MHz (Typ)
- Built-in PWM operation fixed function
- No flyback diode needed
- Low dropout operation : For 100% on duty
- Built-in high-precision reference voltage generator : 1.20 V ± 2%
- Consumption current in shutdown mode : 1 μA or less
- Built-in switching FET : P-ch MOS 0.3 Ω (Typ) N-ch MOS 0.2 Ω (Typ)
- High speed for input and load transient response in the current mode
- Over temperature protection
- Packaged in a compact package : SON10

Applications

- Flash ROMs
- MP3 players
- Electronic dictionary devices
- Surveillance cameras
- Portable GPS navigators
- Mobile phones etc.

Contents

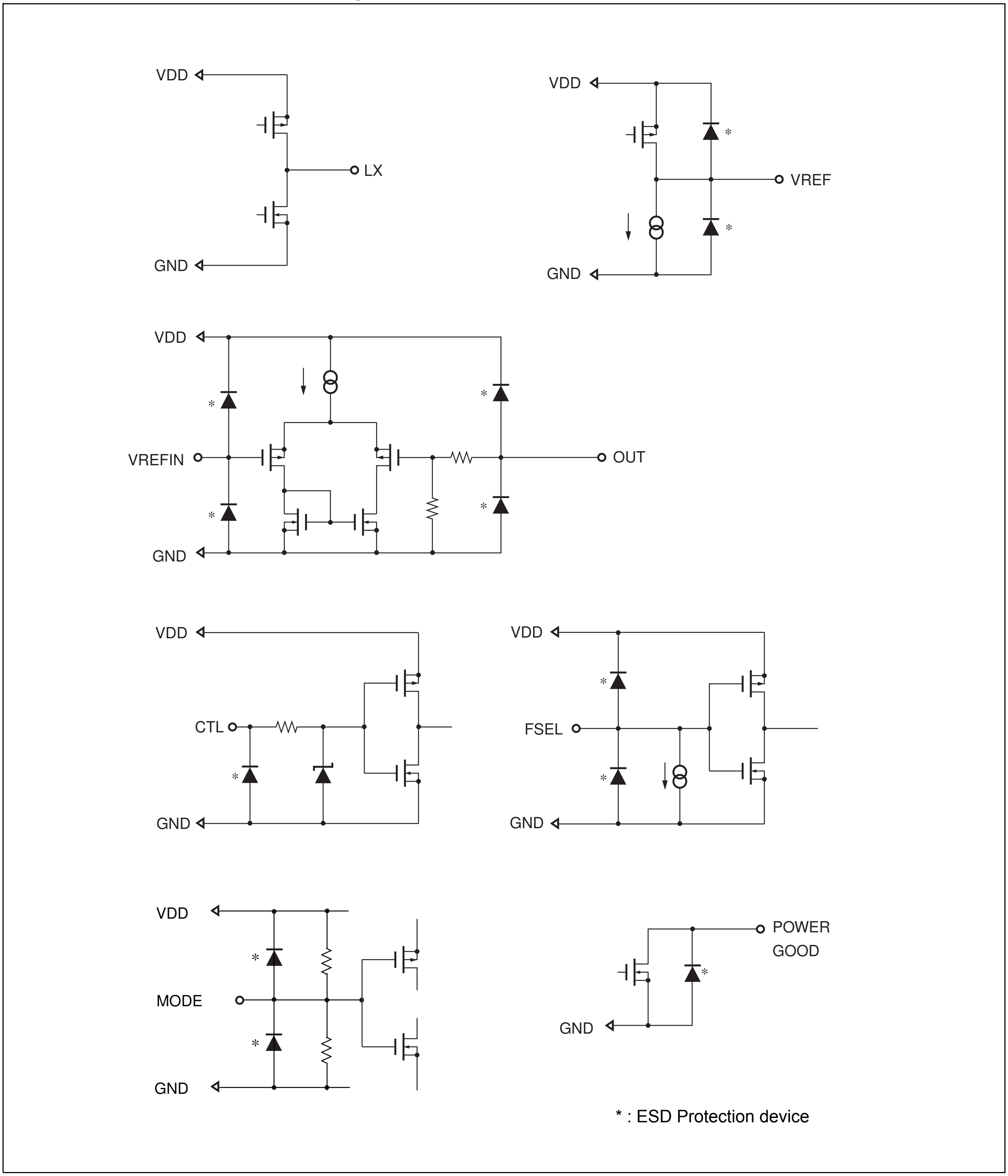
1. Pin Assignment



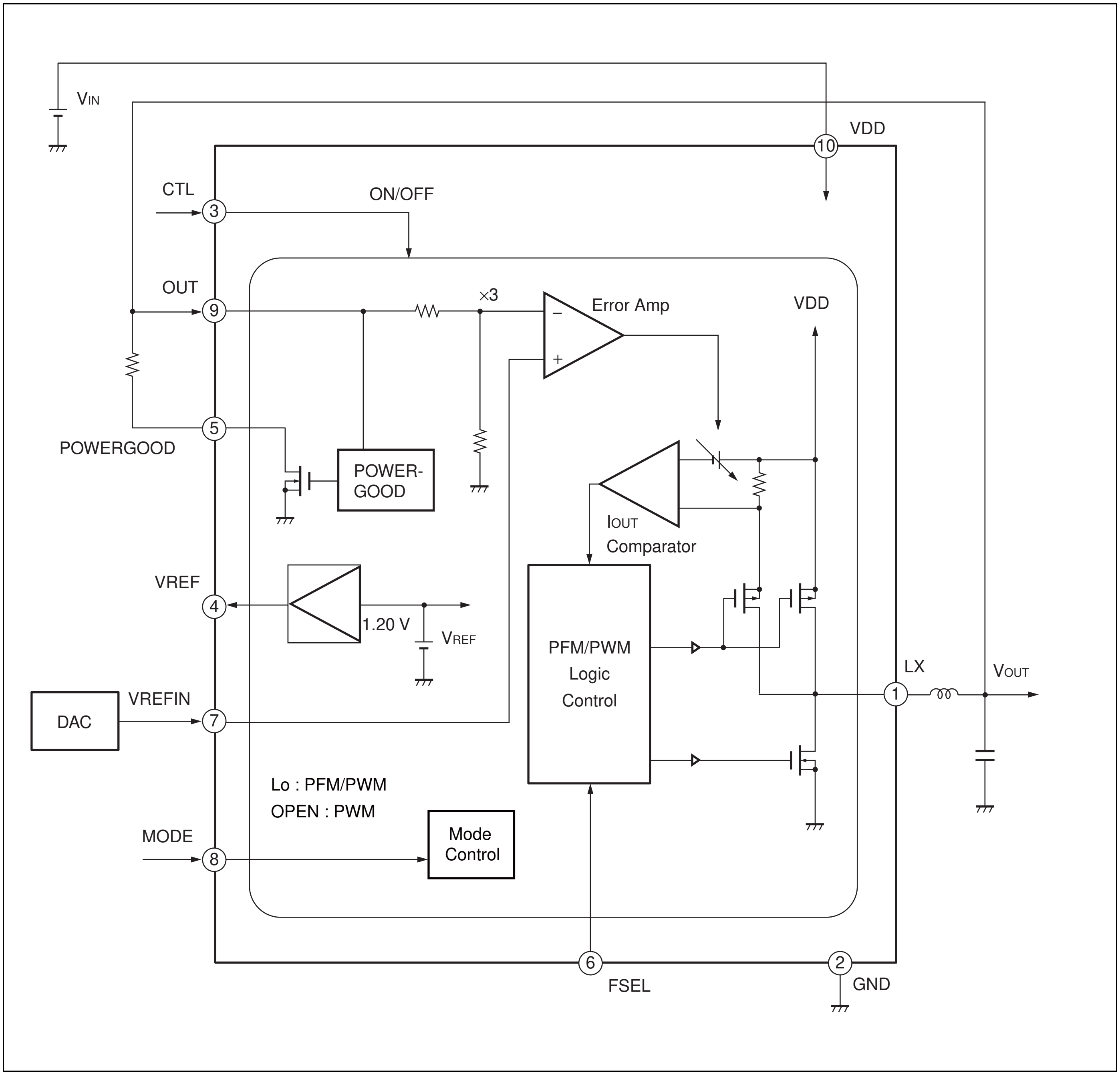
2. Pin Descriptions

Pin No	Pin Name	I/O	Description
1	LX	O	Inductor connection output pin. High impedance during shut down.
2	GND	—	Ground pin.
3	CTL	I	Control input pin. (L : Shut down / H : Normal operation)
4	VREF	O	Reference voltage output pin.
5	POWERGOOD	O	POWERGOOD circuit output pin. Internally connected to an N-ch MOS open drain circuit.
6	FSEL	I	Frequency switch pin. (L (open) : 2.0 MHz, H : 3.2 MHz)
7	VREFIN	I	Error amplifier (Error Amp) non-inverted input pin.
8	MODE	I	Operation mode switch pin. (L : PFM/PWM mode, OPEN : PWM mode)
9	OUT	I	Output voltage feedback pin.
10	VDD	—	Power supply pin.

3. I/O Pin Equivalent Circuit Diagram

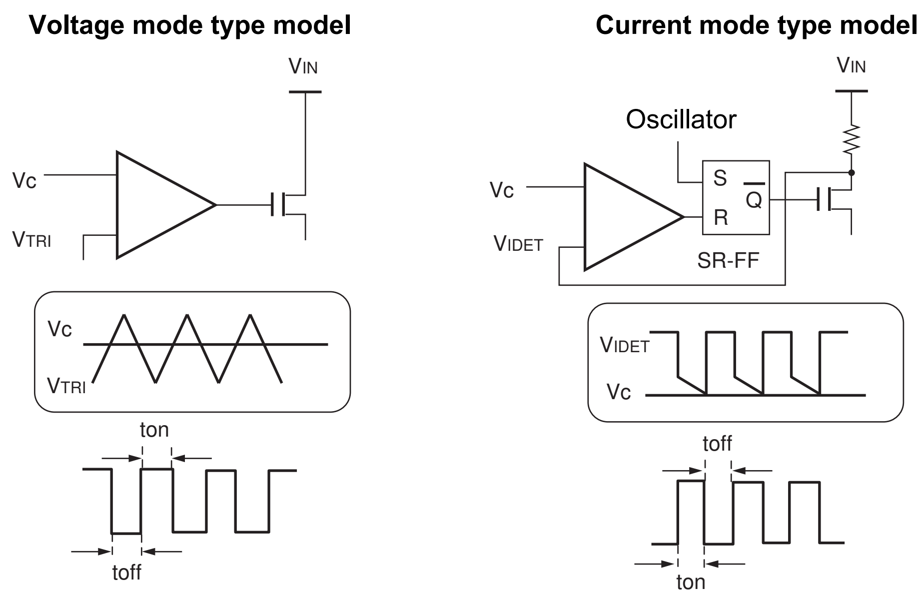


4. Block Diagram



- Current Mode
  - Original voltage mode type:
    Stabilize the output voltage by comparing two items below and on-duty control.
    - Voltage (V_C) obtained through negative feedback of the output voltage by Error Amp
    - Reference triangular wave (V_{TRI})
  - Current mode type:
    Instead of the triangular wave (V_{TRI}), the voltage (V_{IDET}) obtained through I-V conversion of the sum of currents that flow in the oscillator (rectangular wave generation circuit) and SW FET is used.
    Stabilize the output voltage by comparing two items below and on-duty control.

- Voltage (V_C) obtained through negative feedback of the output voltage by Error Amp
- Voltage (V_{IDET}) obtained through I-V conversion of the sum of current that flow in the oscillator (rectangular wave generation circuit) and SW FET



Note : The above models illustrate the general operation and an actual operation will be preferred in the IC.

5. Function of Each Block

■ PFM/PWM Logic Control Circuit

In normal operation, frequency (2.0 MHz/3.2 MHz) which is set by the built-in oscillator (square wave oscillation circuit) controls the built-in P-ch MOS FET and N-ch MOS FET for the synchronous rectification operation. In the light load mode, the intermittent (PFM) operation is executed.
This circuit protects against pass-through current caused by synchronous rectification and against reverse current caused in a non-successive operation mode.

■ I_{OUT} Comparator Circuit

This circuit detects the current (I_{LX}) which flows to the external inductor from the built-in P-ch MOS FET.
By comparing V_{IDET} obtained through I-V conversion of peak current I_{PK} of I_{LX} with the Error Amp output, the built-in P-ch MOS FET is turned off via the PFM/PWM Logic Control circuit.

■ Error Amp Phase Compensation Circuit

This circuit compares the output voltage to reference voltages such as VREF. The MB39C006A has a built-in phase compensation circuit that is designed to optimize the operation of the MB39C006A. This needs neither to be considered nor addition of a phase compensation circuit and an external phase compensation device.

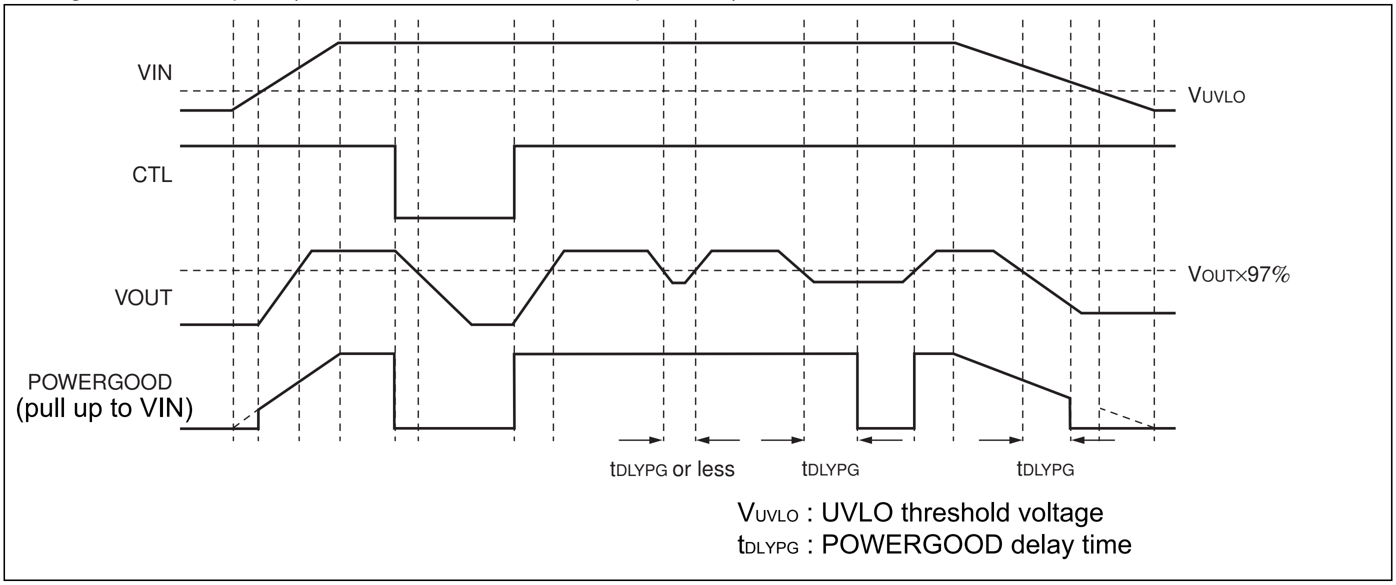
■ VREF Circuit

A high accuracy reference voltage is generated with BGR (bandgap reference) circuit. The output voltage is 1.20 V (Typ).

■ POWERGOOD Circuit

The POWERGOOD circuit monitors the voltage at the OUT pin. The POWERGOOD pin is open drain output. Use the pin with pull-up using the external resistor in the normal operation.
When the CTL is at the H level, the POWERGOOD pin becomes the H level. However, if the output voltage drops because of over current and etc, the POWERGOOD pin becomes the L level.

Timing Chart Example : (POWERGOOD Pin Pulled Up to VIN)



■ Protection Circuit

The MB39C006A has a built-in over-temperature protection circuit.
The over-temperature protection circuit turns off both N-ch and P-ch switching FETs when the junction temperature reaches +135 °C. When the junction temperature drops to + 110 °C, the switching FET returns to the normal operation.
Since the PFM/PWM control circuit of the MB39C006A is in the control method in current mode, the current peak value is also monitored and controlled as required.

■ Function Table

MODE		Input			Output		
	Switching Frequency	CTL	MODE	FSEL	OUTPUT Pin Voltage	VREF	POWERGOOD
Shutdown mode	—	L	*	*	Output stop	Output stop	Function stop
PFM/PWM mode	2.0 MHz	H	L	L	VOUT voltage output	1.2 V	Operation
PWM fixed mode	2.0 MHz	H	OPEN	L	VOUT voltage output	1.2 V	Operation
PFM/PWM mode	3.2 MHz	H	L	H	VOUT voltage output	1.2 V	Operation
PWM fixed mode	3.2 MHz	H	OPEN	H	VOUT voltage output	1.2 V	Operation

* : Don't care

6. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{DD}	VDD pin	− 0.3	+ 6.0	V
Signal input voltage	V_{ISIG}	OUT pin	− 0.3	V_{DD} + 0.3	V
		CTL, MODE, FSEL pins	− 0.3	V_{DD} + 0.3	
		VREFIN pin	− 0.3	V_{DD} + 0.3	
POWERGOOD pull-up voltage	V_{IPG}	POWERGOOD pin	− 0.3	+ 6.0	V
LX voltage	V_{LX}	LX pin	− 0.3	V_{DD} + 0.3	V
LX peak current	I_{PK}	The upper limit value of I_{LX}	—	1.8	A
Power dissipation	P_D	Ta ≤ + 25 °C	—	2632*1, *2, *3	mW
			—	980*1, *2, *4	
		Ta = + 85 °C	—	1053*1, *2, *3	mW
			—	392*1, *2, *4	
Operating ambient temperature	Ta	—	− 40	+ 85	°C
Storage temperature	T_{STG}	—	− 55	+ 125	°C

*1 : See "Example of Standard Operation Characteristics ● Power dissipation vs. Operating ambient temperature" for the package power dissipation of Ta from + 25 °C to + 85 °C.

*2 : When mounted on a four- layer epoxy board of 11.7 cm × 8.4 cm

*3 : IC is mounted on a four-layer epoxy board, which has thermal via, and the IC's thermal pad is connected to the epoxy board (Thermal via is 4 holes).

*4 : IC is mounted on a four-layer epoxy board, which has no thermal via, and the IC's thermal pad is connected to the epoxy board.

Notes:

- The use of negative voltages below − 0.3 V to the GND pin may create parasitic transistors on LSI lines, which can cause abnormal operation.
- This device can be damaged if the LX pin is short-circuited to VDD pin or GND pin.
- Take measures not to keep the FSEL pin falling below the GND pin potential of the MB39C006A as much as possible. In addition to erroneous operation, the IC may latch up and destroy itself if 110 mA or more current flows from this pin.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

7. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	—	2.5	3.7	5.5	V
VREFIN voltage	V_{REFIN}	—	0.15	—	1.20	V
CTL voltage	V_{CTL}	—	0	—	5.0	V
LX current	I_{LX}	—	—	—	800	mA
POWERGOOD current	I_{PG}	—	—	—	1	mA
VREF output current	I_{ROUT}	$2.5\ V \leq V_{DD} \leq 3.0\ V$	—	—	0.5	mA
		$3.0\ V \leq V_{DD} \leq 5.5\ V$	—	—	1	
Inductor value	L	$f_{OSC1} = 2.0$ MHz (FSEL = L)	—	2.2	—	µH
		$f_{OSC2} = 3.2$ MHz (FSEL = H)	—	1.5	—	

Note : The output current from this device has a situation to decrease if the power supply voltage (V_{IN}) and the DC/DC converter output voltage (V_{OUT}) differ only by a small amount. This is a result of slope compensation and will not damage this device.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

8. Electrical Characteristics

(Ta = + 25 °C, VDD = 3.7 V, VOUT setting value = 2.5 V, MODE = 0 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
DC/DC converter block	Input current	$I_{REFIN}M$	7	V_{REFIN} = 0.833 V	–100	0	+ 100	nA
		$I_{REFIN}L$		V_{REFIN} = 0.15 V	–100	0	+ 100	nA
		$I_{REFIN}H$		V_{REFIN} = 1.20 V	–100	0	+ 100	nA
	Output voltage	V_{OUT}	9	V_{REFIN} = 0.833 V, OUT = –100 mA	2.45	2.50	2.55	V
	Input stability	LINE		2.5 V ≤ V_{DD} ≤ 5.5 V *1	—	10	—	mV
	Load stability	LOAD		– 100 mA ≥ OUT ≥ – 800 mA	—	10	—	mV
	Out pin input impedance	R_{OUT}		OUT = 2.0 V	0.6	1.0	1.5	MΩ
	LX peak current	I_{PK}	1	Output shorted to GND	0.9	1.2	1.7	A
	PFM/PWM switch current	I_{MSW}		FSEL = 0 V, L = 2.2 µH	—	30	—	mA
	Oscillation frequency	f_{OSC1}		FSEL = 0 V	1.6	2.0	2.4	MHz
		f_{OSC2}		FSEL = 3.7 V	2.56	3.20	3.84	MHz
	Rise delay time	t_{PG}	3, 9	C1 = 4.7 µF, OUT = 0 A, VOUT = 90%	—	45	80	µs
	SW NMOS FET OFF voltage	V_{NOFF}	1	—	—	–20*	—	mV
	SW PMOS FET ON resistance	R_{ONP}		LX = –100 mA	—	0.30	0.47	Ω
	SW NMOS FET ON resistance	R_{ONN}		LX = –100 mA	—	0.20	0.36	Ω
	LX leak current	$I_{LEAK}M$		0 ≤ LX ≤ V_{DD}*2	–1.0	—	+ 8.0	µA
		$I_{LEAK}H$		V_{DD} = 5.5 V, 0 ≤ LX ≤ V_{DD}*2	–2.0	—	+ 16.0	µA
Protection circuit block	Over temperature protection (Junction Temp.)	T_{OTPH}	—	—	+ 120*	+ 135*	+ 155*	°C
		T_{OTPL}			+ 95*	+ 110*	+ 130*	°C
	UVLO threshold voltage	V_{THH}	10	—	2.07	2.20	2.33	V
		V_{THL}			1.92	2.05	2.18	V
	UVLO hysteresis width	V_{HYS}		—	0.08	0.15	0.25	V

* : This value isn't be specified. This should be used as a reference to support designing the circuits.

(Ta = + 25 °C, VDD = 3.7 V, VOUT setting value = 2.5 V, MODE = 0 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
POWER-GOOD block	POWERGOOD threshold voltage	V_{THPG}	5	*3	V_{REFIN} × 3 × 0.93	V_{REFIN} × 3 × 0.97	V_{REFIN} × 3 × 0.99	V
	POWERGOOD delay time	t_{DLYPG1}		FSEL = 0 V	—	250	—	µs
		t_{DLYPG2}		FSEL = 3.7 V	—	170	—	µs
	POWERGOOD output voltage	V_{OL}		POWERGOOD = 250 µA	—	—	0.1	V
	POWERGOOD output current	I_{OH}		POWERGOOD = 5.5 V	—	—	1.0	µA
Control block	CTL threshold voltage	V_{THHCT}	3	—	0.55	0.95	1.45	V
		V_{THLCT}		—	0.40	0.80	1.30	V
	CTL pin input current	I_{ICTL}		CTL = 3.7 V	—	—	1.0	µA
	MODE threshold voltage	V_{THMMD}	8	OPEN setting	—	1.5	—	V
		V_{THLMD}		—	—	—	0.4	V
	MODE pin input current	I_{LMD}		MODE = 0 V	− 0.8	− 0.4	—	µA
	FSEL threshold voltage	V_{THHFS}	6	—	2.96	—	—	V
		V_{THLFS}		—	—	—	0.74	V
Reference voltage block	VREF voltage	V_{REF}	4	VREF = −2.7 µA, OUT = −100 mA	1.176	1.200	1.224	V
	VREF load stability	L_{OADREF}		VREF = −1.0 mA	—	—	20	mV
General	Shut down power supply current	I_{VDD1}	10	CTL = 0 V, All circuits in OFF state	—	—	1.0	µA
		I_{VDD1H}		CTL = 0 V, VDD = 5.5 V	—	—	1.0	µA
	Power supply current at DC/DC operation (PFM mode)	I_{VDD2}		CTL = 3.7 V, MODE = 0 V, OUT = 0 A	—	30	48	µA
	Power supply current at DC/DC operation (PWM fixed mode)	I_{VDD2}		CTL = 3.7 V, MODE = OPEN, OUT = 0 A, FSEL = 0 V	—	4.8	8.0	mA
	Power-on invalid current	I_{VDD}		CTL = 3.7 V, VOUT = 90%*4	—	800	1500	µA

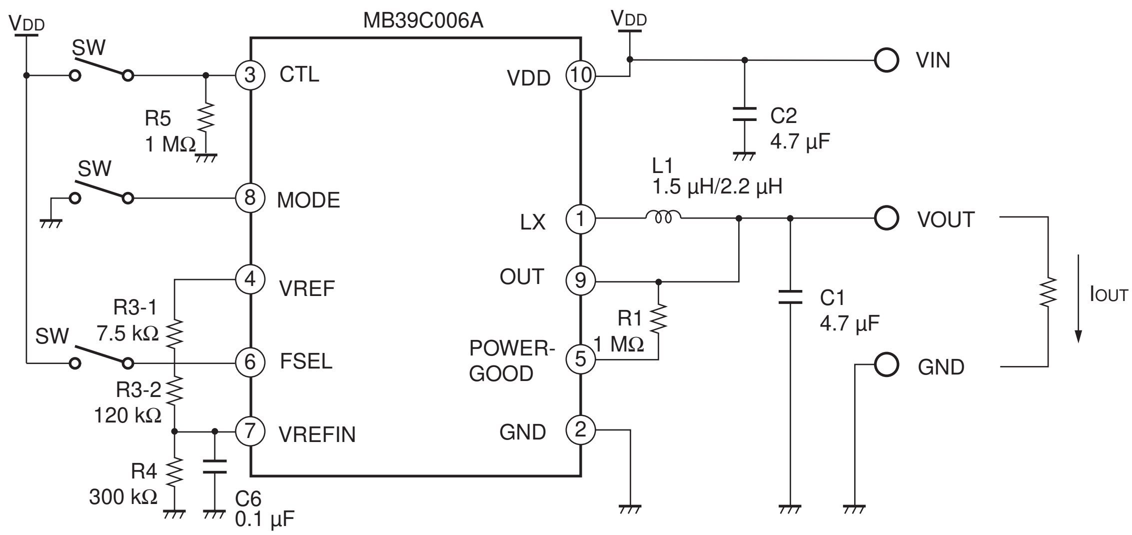
*1 : The minimum value of V_{DD} is the 2.5 V or V_{OUT} setting value + 0.6 V, whichever is higher.

*2 : The + leak at the LX pin includes the current of the internal circuit.

*3 : Detected with respect to the output voltage setting value of V_{REFIN}

*4 : Current consumption based on 100% ON-duty (High side FET in full ON state). The SW FET gate drive current is not included because the device is in full ON state (no switching operation). Also the load current is not included.

9. Test Circuit for Measuring Typical Operating Characteristics



$$VOUT = VREFIN \times 2.97$$

Component	Specification	Vendor	Part Number	Remark
R1	1 MΩ	KOA	RK73G1JTTD D 1 MΩ	
R3-1 R3-2	7.5 kΩ 120 kΩ	SSM SSM	RR0816-752-D RR0816-124-D	At VOUT = 2.5 V setting
R4	300 kΩ	SSM	RR0816-304-D	
R5	1 MΩ	KOA	RK73G1JTTD D 1 MΩ	
C1	4.7 µF	TDK	C2012JB1A475K	
C2	4.7 µF	TDK	C2012JB1A475K	
C6	0.1 µF	TDK	C1608JB1H104K	For adjusting slow start time
L1	2.2 µH	TDK	VLF4012AT-2R2M	2.0 MHz operation
	1.5 µH	TDK	VLF4012AT-1R5M	3.2 MHz operation

Note : These components are recommended based on the operating tests authorized.

TDK : TDK Corporation

SSM : SUSUMU Co., Ltd

KOA : KOA Corporation

10. Application Notes

10.1 Selection of Components

■ Selection of an External Inductor

Basically it dose not need to design inductor. The MB39C006A is designed to operate efficiently with a 2.2 μH (2.0 MHz operation) or 1.5 μH (3.2 MHz operation) external inductor.

The inductor should be rated for a saturation current higher than the LX peak current value during normal operating conditions, and should have a minimal DC resistance. (100 mΩ or less is recommended.)

The LX peak current value I_{PK} is obtained by the following formula.

$$I_{PK} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{fosc} \times \frac{1}{2} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}}$$

L : External inductor value

I_{OUT} : Load current

V_{IN} : Power supply voltage

V_{OUT} : Output setting voltage

D : ON- duty to be switched($= V_{OUT}/V_{IN}$)

fosc : Switching frequency (2.0 MHz or 3.2 MHz)

ex) At $V_{IN} = 3.7$ V, $V_{OUT} = 2.5$ V, $I_{OUT} = 0.8$ A, L = 2.2 μH, fosc = 2.0 MHz
The maximum peak current value I_{PK};

$$I_{PK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}} = 0.8\ A + \frac{(3.7\ V - 2.5\ V) \times 2.5\ V}{2 \times 2.2\ \mu H \times 2\ MHz \times 3.7\ V} \approx 0.89\ A$$

■ I/O Capacitor Selection

❐ Select a low equivalent series resistance (ESR) for the VDD input capacitor to suppress dissipation from ripple currents.

❐ Also select a low equivalent series resistance (ESR) for the output capacitor. The variation in the inductor current causes ripple currents on the output capacitor which, in turn, causes ripple voltages an output equal to the amount of variation multiplied by the ESR value. The output capacitor value has a significant impact on the operating stability of the device when used as a DC/DC converter. Therefore, Cypress generally recommends a 4.7 μF capacitor, or a larger capacitor value can be used if ripple voltages are not suitable. If the V_{IN}/V_{OUT} voltage difference is within 0.6 V, the use of a 10 μF output capacitor value is recommended.

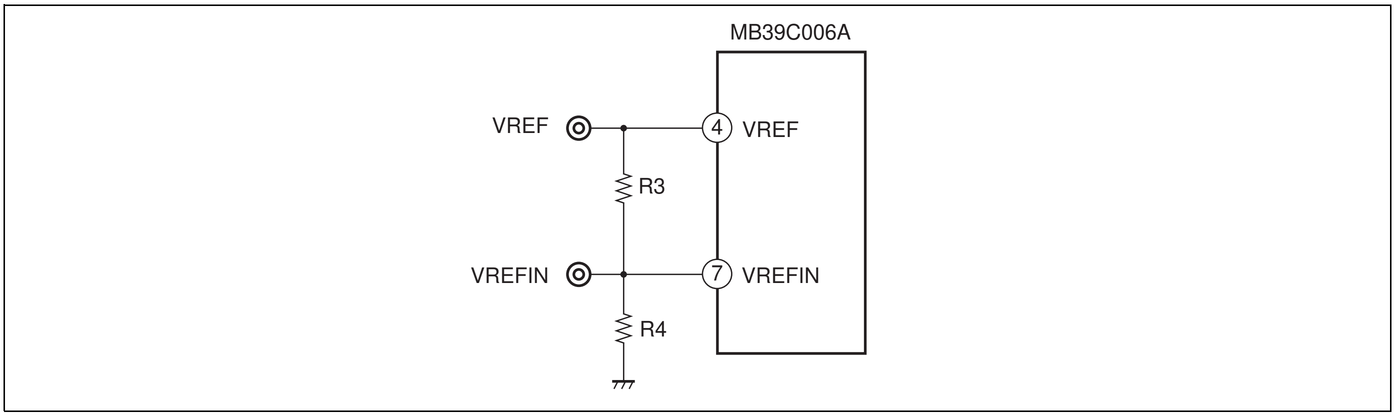
❐ Types of capacitors
Ceramic capacitors are effective for reducing the ESR and afford smaller DC/DC converter circuit. However, power supply functions as a heat generator, therefore avoid to use capacitor with the F-temperature rating
(− 80% to + 20%) . Cypress recommends capacitors with the B-temperature rating (± 10% to ± 20%).
Normal electrolytic capacitors are not recommended due to their high ESR.
Tantalum capacitor will reduce ESR, however, it is dangerous to use because it turns into short mode when damaged. If you insist on using a tantalum capacitor, Cypress recommends the type with an internal fuse.

10.2 Output Voltage Setting

The output voltage V_{OUT} of the MB39C006A is defined by the voltage input to VREFIN. Supply the voltage for inputting to VREFIN from an external power supply, or set the VREF output by dividing it with resistors.
The output voltage when the VREFIN voltage is set by dividing the VREF voltage with resistors is shown in the following formula.

$$V_{OUT} = 2.97 \times V_{REFIN}, \quad V_{REFIN} = \frac{R4}{R3 + R4} \times V_{REF}$$

$(V_{REF} = 1.20\ V)$



Note : See “Application Circuit Examples” for an example of this circuit.

Although the output voltage is defined according to the dividing ratio of resistance, select the resistance value so that the current flowing through the resistance does not exceed the VREF current rating (1 mA) .

10.3 About Conversion Efficiency

The conversion efficiency can be improved by reducing the loss of the DC/DC converter circuit.

The total loss (P_{LOSS}) of the DC/DC converter is roughly divided as follows :

$$P_{LOSS} = P_{CONT} + P_{SW} + P_{C}$$

P_{CONT} : Control system circuit loss (The power to operate the MB39C006A, including the gate driving power for internal SW FETs)

P_{SW} : Switching loss (The loss caused during the switch of the IC's internal SW FETs)

P_{C} : Continuity loss (The loss caused when currents flow through the IC's internal SW FETs and external circuits)

The IC's control circuit loss (P_{CONT}) is extremely small, several tens of mW* with no load.

As the IC contains FETs which can switch faster with less power, the continuity loss (P_{C}) is more predominant as the loss during heavy-load operation than the control circuit loss (P_{CONT}) and switching loss (P_{SW}) .

* : The loss in the successive operation mode. This IC suppresses the loss in order to execute the PFM operation in the low load mode (less than 100 μA in no load mode). Mode is changed by the current peak value I_{PK} which flows into switching FET. The threshold value is about 30 mA.

Furthermore, the continuity loss (P_{C}) is divided roughly into the loss by internal SW FET ON-resistance and by external inductor series resistance.

$$P_{C} = I_{OUT}^2 \times (RDC + D \times R_{ONP} + (1 - D) \times R_{ONN})$$

D : Switching ON-duty cycle ($= V_{OUT} / V_{IN}$)

R_{ONP} : Internal P-ch SW FET ON resistance

R_{ONN} : Internal N-ch SW FET ON resistance

RDC : External inductor series resistance

I_{OUT} : Load current

The above formula indicates that it is important to reduce RDC as much as possible to improve efficiency by selecting components.

10.4 Power Dissipation and Heat Considerations

The IC is so efficient that no consideration is required in most of the cases. However, if the IC is used at a low power supply voltage, heavy load, high output voltage, or high temperature, it requires further consideration for higher efficiency.

The internal loss (P) is roughly obtained from the following formula :

$$P = I_{OUT}^2 \times (D \times R_{ONP} + (1 - D) \times R_{ONN})$$

D : Switching ON-duty cycle ($= V_{OUT} / V_{IN}$)

R_{ONP} : Internal P-ch SW FET ON resistance

R_{ONN} : Internal N-ch SW FET ON resistance

I_{OUT} : Output current

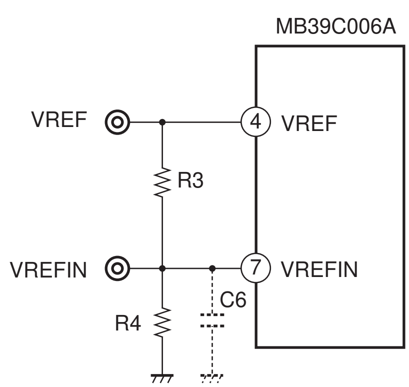
The loss expressed by the above formula is mainly continuity loss. The internal loss includes the switching loss and the control circuit loss as well but they are so small compared to the continuity loss they can be ignored.

In the MB39C006A with R_{ONP} greater than R_{ONN}, the larger the on-duty cycle, the greater the loss.

When assuming $V_{IN} = 3.7$ V, Ta = + 70 °C for example, $R_{ONP} = 0.42\ \Omega$ and $R_{ONN} = 0.36\ \Omega$ according to the graph "MOS FET ON resistance vs. Operating ambient temperature". The IC's internal loss P is 144 mW at $V_{OUT} = 2.5$ V and $I_{OUT} = 0.6$ A. According to the graph "Power dissipation vs. Operating ambient temperature", the power dissipation at an operating ambient temperature Ta of + 70 °C is 539 mW and the internal loss is smaller than the power dissipation.

10.5 Transient Response

Normally, I_{OUT} is suddenly changed while V_{IN} and V_{OUT} are maintained constant, responsiveness including the response time and overshoot/undershoot voltage is checked. As the MB39C006A has built-in Error Amp with an optimized design, it shows good transient response characteristics. However, if ringing upon sudden change of the load is high due to the operating conditions, add capacitor C6 (e.g. 0.1 µF). (Since this capacitor C6 changes the start time, check the start waveform as well.) This action is not required for DAC input.



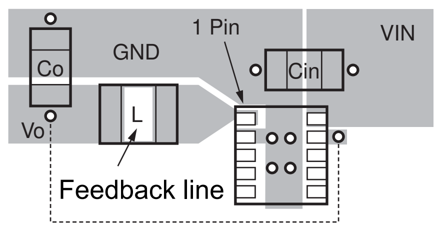
10.6 Board Layout, Design Example

The board layout needs to be designed to ensure the stable operation of the MB39C006A.
Follow the procedure below for designing the layout.

- Arrange the input capacitor (Cin) as close as possible to both the VDD and GND pins. Make a through hole (TH) near the pins of this capacitor if the board has planes for power and GND.
- Large AC currents flow between the MB39C006A and the input capacitor (Cin), output capacitor (C_O), and external inductor (L). Group these components as close as possible to the MB39C006A to reduce the overall loop area occupied by this group. Also try to mount these components on the same surface and arrange wiring without through hole wiring. Use thick, short, and straight routes to wire the net (The layout by planes is recommended.).
- The feedback wiring to the OUT should be wired from the voltage output pin closest to the output capacitor (C_O). The OUT pin is extremely sensitive and should thus be kept wired away from the LX pin of the MB39C006A as far as possible.

- ❐ If applying voltage to the VREFIN pin through dividing resistors, arrange the resistors so that the wiring can be kept as short as possible. Also arrange them so that the GND pin of the VREFIN resistor is close to the IC's GND pin. Further, provide a GND exclusively for the control line so that the resistor can be connected via a path that does not carry current. If installing a bypass capacitor for the VREFIN, put it close to the VREFIN pin.
- ❐ Try to make a GND plane on the surface to which the MB39C006A will be mounted. For efficient heat dissipation when using the SON 10 package, Cypress recommends providing a thermal via in the footprint of the thermal pad.

■ Layout Example of IC SW Components

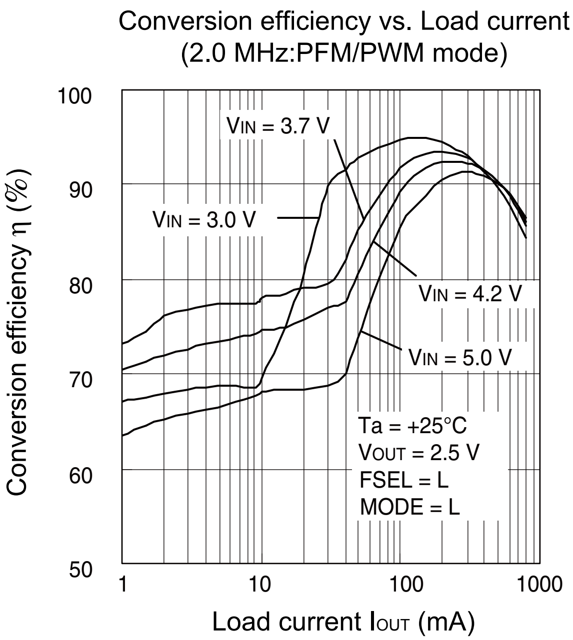


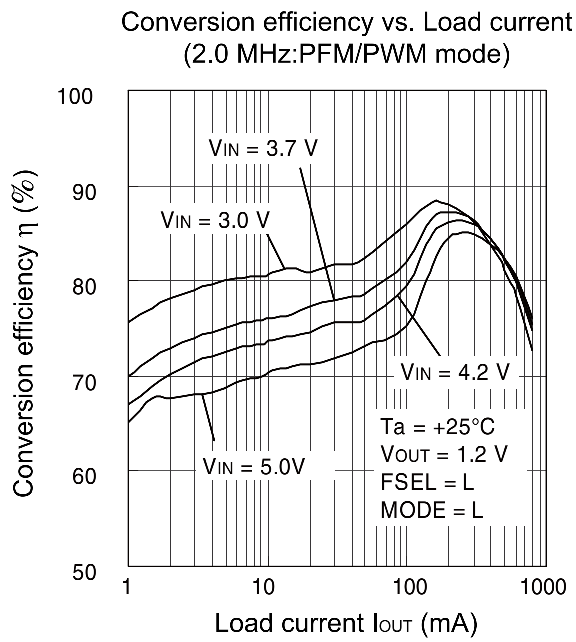
■ Notes for Circuit Design

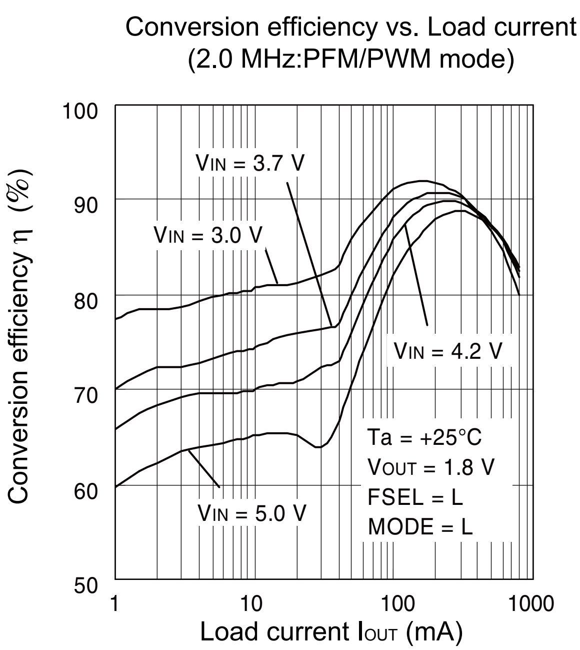
The switching operation of the MB39C006A works by monitoring and controlling the peak current which, incidentally, serves as form of short-circuit protection. However, do not leave the output short-circuited for long periods of time. If the output is short-circuited where VIN < 2.9 V, the current limit value (peak current to the inductor) tends to rise. Leaving in the short-circuit state, the temperature of the MB39C006A will continue rising and activate the thermal protection.
Once the thermal protection stops the output, the temperature of the IC will go down and operation will resume, after which the output will repeat the starting and stopping.
Although this effect will not destroy the IC, the thermal exposure to the IC over prolonged hours may affect the peripherals surrounding it.

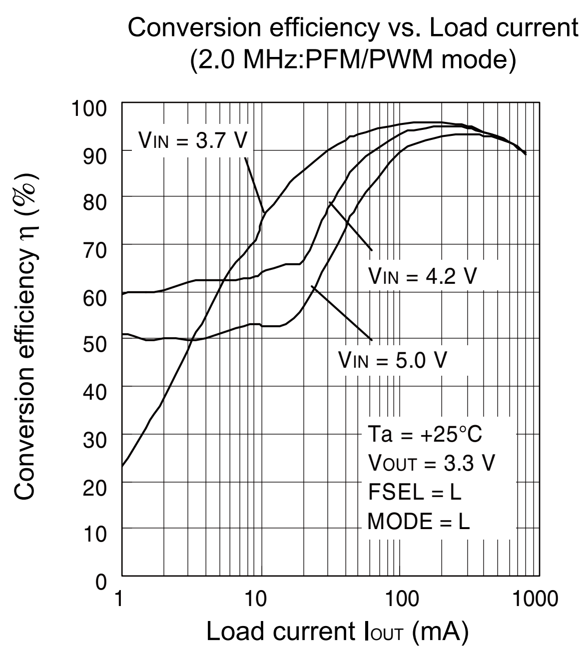
11. Example of Standard Operation Characteristics

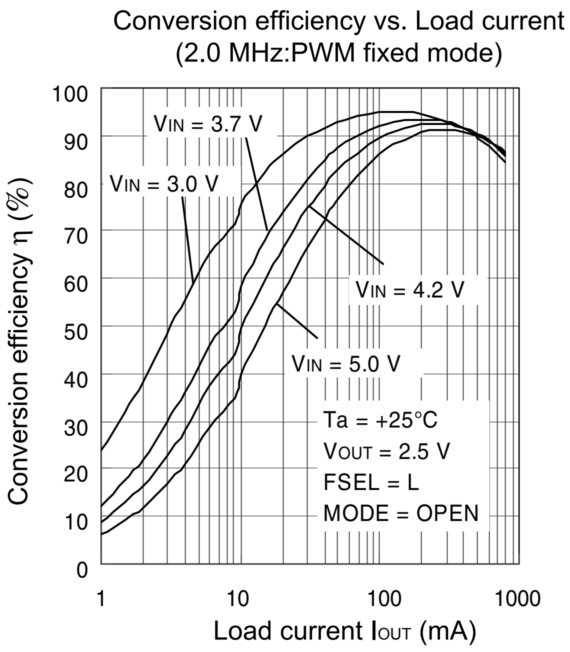
(Shown below is an example of characteristics for connection according to Test Circuit for Measuring Typical Operating Characteristics.)

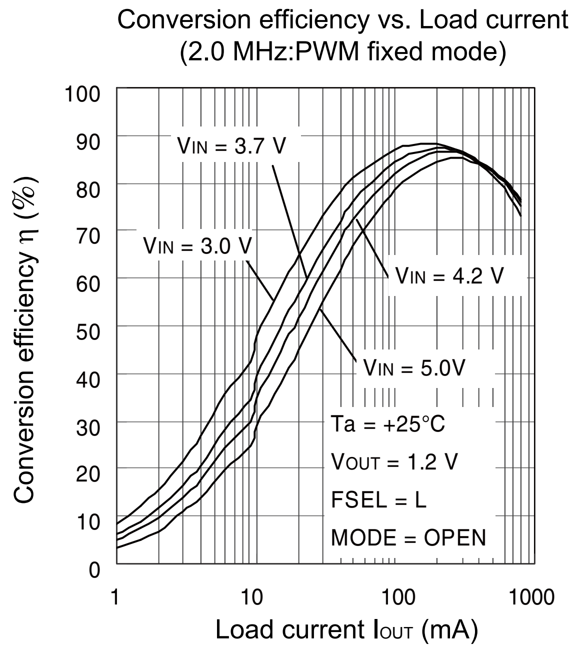


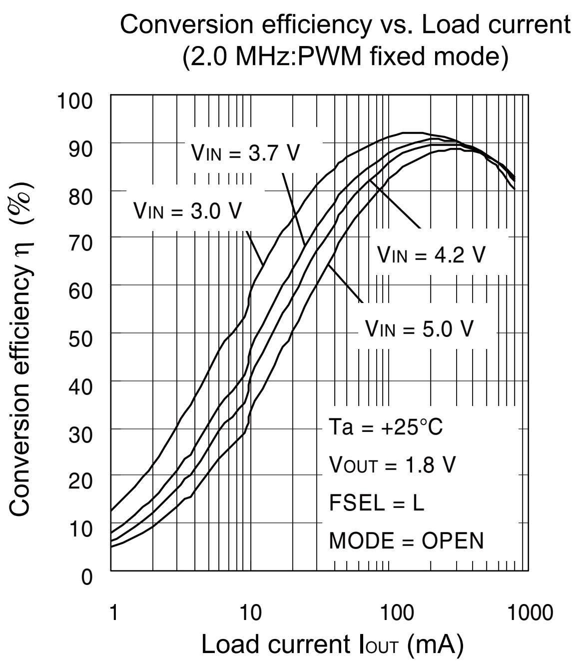


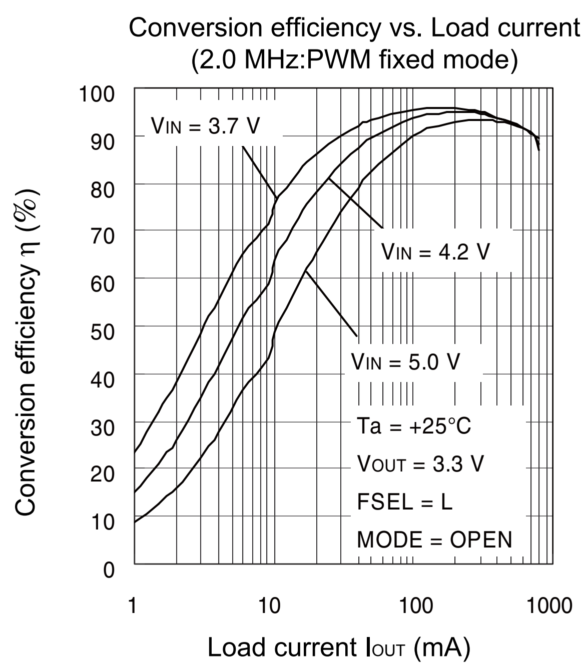




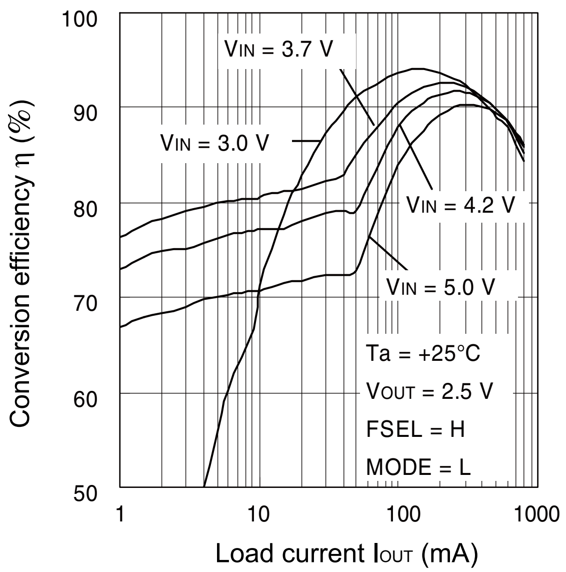

Conversion efficiency vs. Load current
(2.0 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 3.0 V
VIN = 4.2 V
VIN = 5.0 V
Ta = +25°C
VOUT = 2.5 V
FSEL = L
MODE = OPEN
Conversion efficiency η (%)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000
Load current IOUT (mA)


Conversion efficiency vs. Load current
(2.0 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 3.0 V
VIN = 4.2 V
VIN = 5.0V
Ta = +25°C
VOUT = 1.2 V
FSEL = L
MODE = OPEN
Conversion efficiency η (%)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000
Load current IOUT (mA)

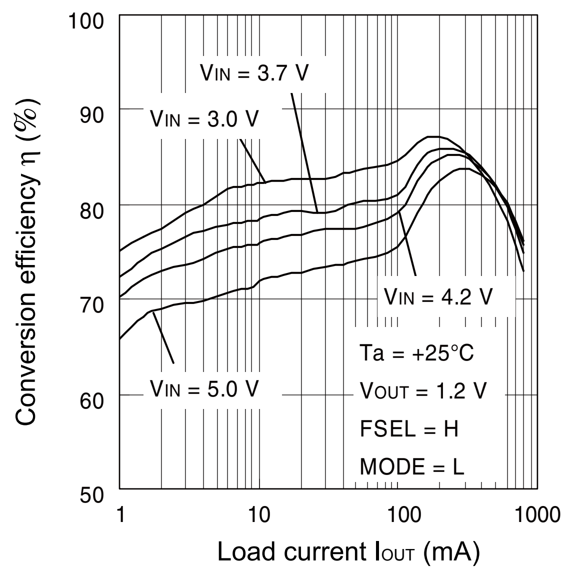

Conversion efficiency vs. Load current
(2.0 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 3.0 V
VIN = 4.2 V
VIN = 5.0 V
Ta = +25°C
VOUT = 1.8 V
FSEL = L
MODE = OPEN
Conversion efficiency η (%)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000
Load current IOUT (mA)


Conversion efficiency vs. Load current
(2.0 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 4.2 V
VIN = 5.0 V
Ta = +25°C
VOUT = 3.3 V
FSEL = L
MODE = OPEN
Conversion efficiency η (%)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000
Load current IOUT (mA)

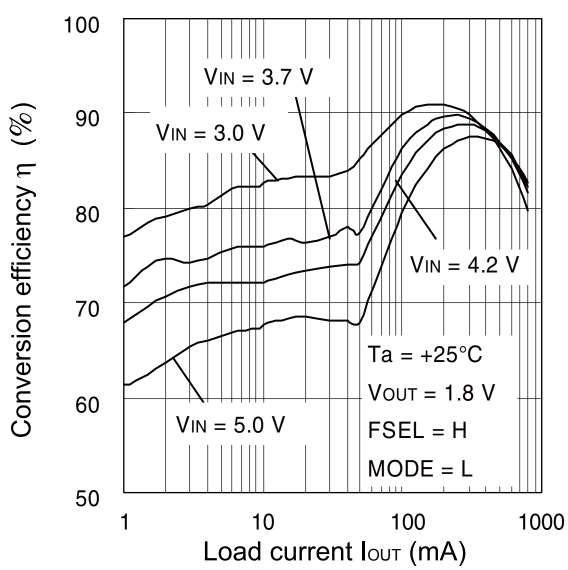
Conversion efficiency vs. Load current
(3.2 MHz: PFM/PWM mode)



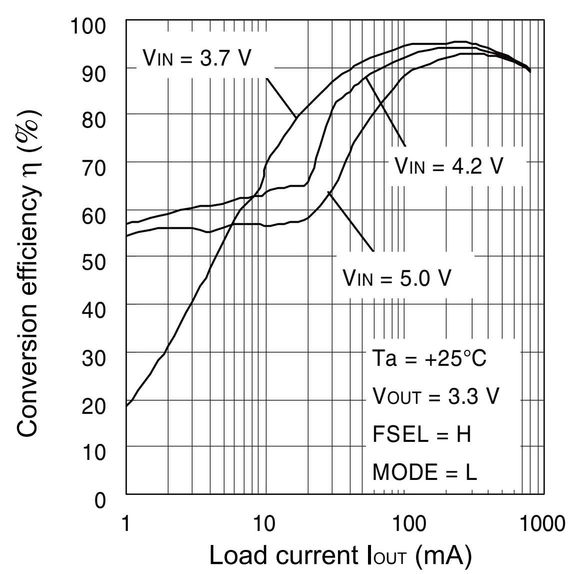
Conversion efficiency vs. Load current
(3.2 MHz: PFM/PWM mode)

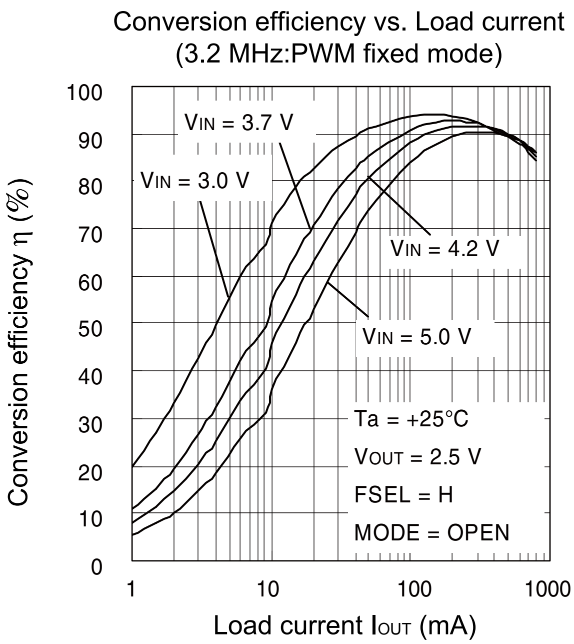


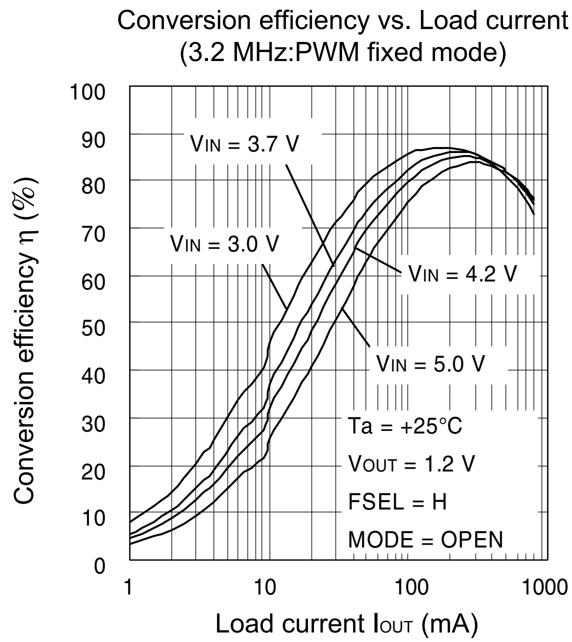
Conversion efficiency vs. Load current
(3.2 MHz:PFM/PWM mode)

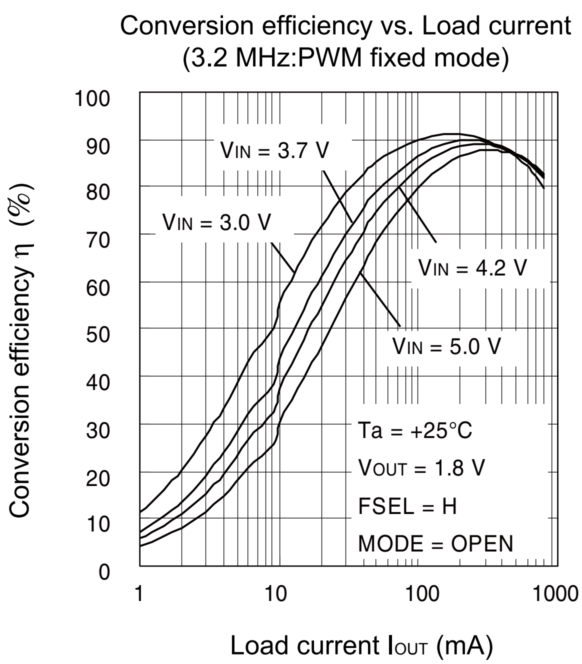


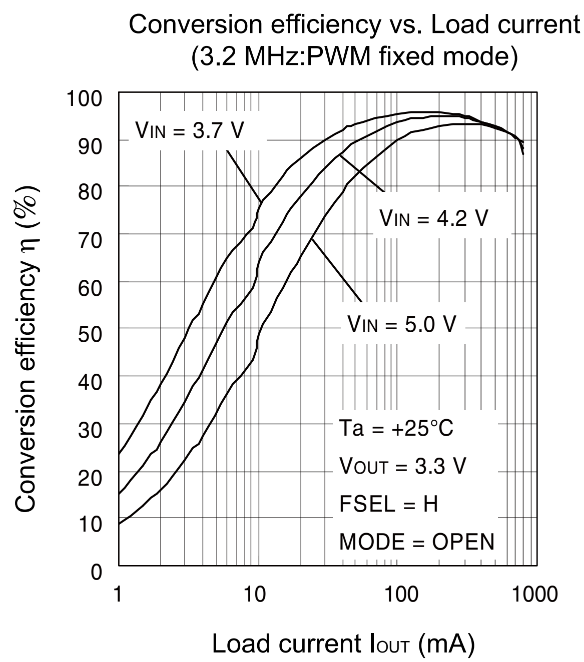
Conversion efficiency vs. Load current
(3.2 MHz:PFM/PWM mode)

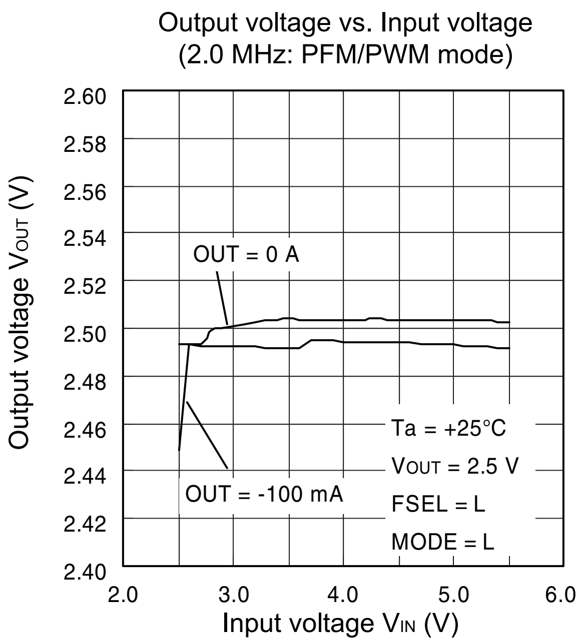


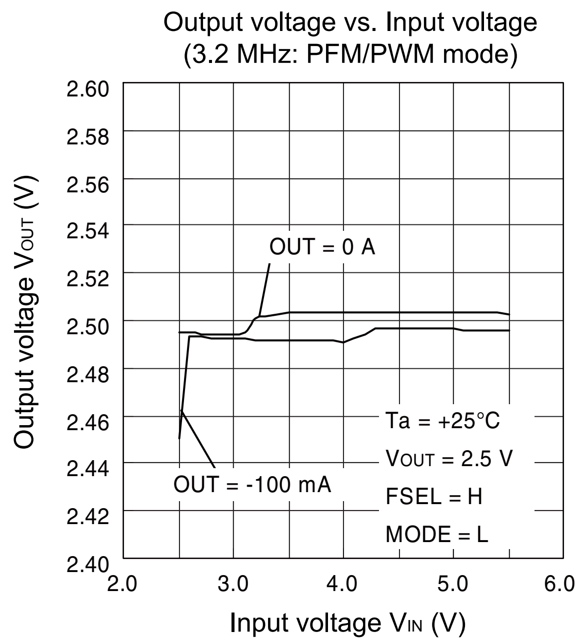

Conversion efficiency vs. Load current
(3.2 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 3.0 V
VIN = 4.2 V
VIN = 5.0 V
Ta = +25°C
VOUT = 2.5 V
FSEL = H
MODE = OPEN
Conversion efficiency η (%)
Load current IOUT (mA)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000

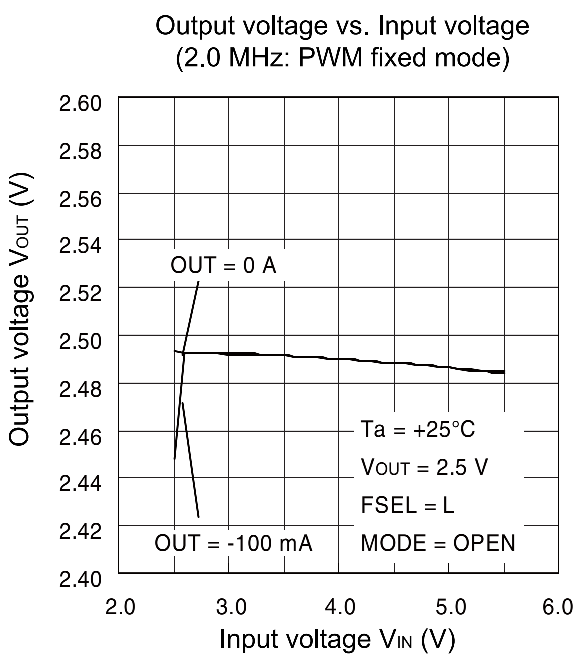

Conversion efficiency vs. Load current
(3.2 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 3.0 V
VIN = 4.2 V
VIN = 5.0 V
Ta = +25°C
VOUT = 1.2 V
FSEL = H
MODE = OPEN
Conversion efficiency η (%)
Load current IOUT (mA)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000

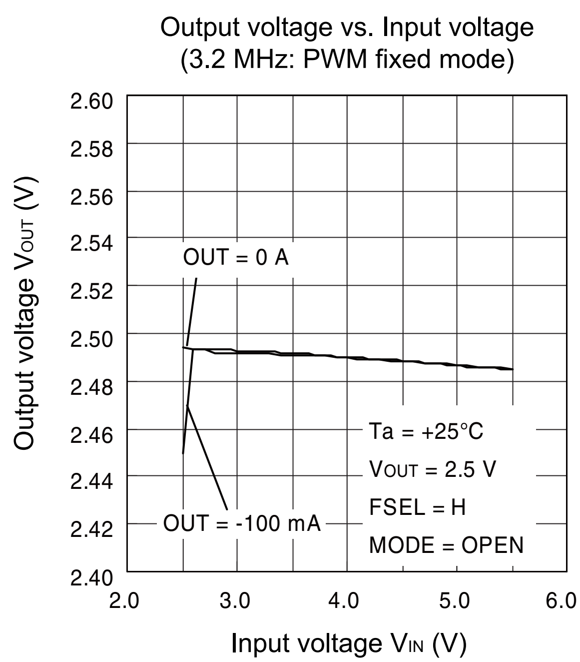

Conversion efficiency vs. Load current
(3.2 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 3.0 V
VIN = 4.2 V
VIN = 5.0 V
Ta = +25°C
VOUT = 1.8 V
FSEL = H
MODE = OPEN
Conversion efficiency η (%)
Load current IOUT (mA)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000

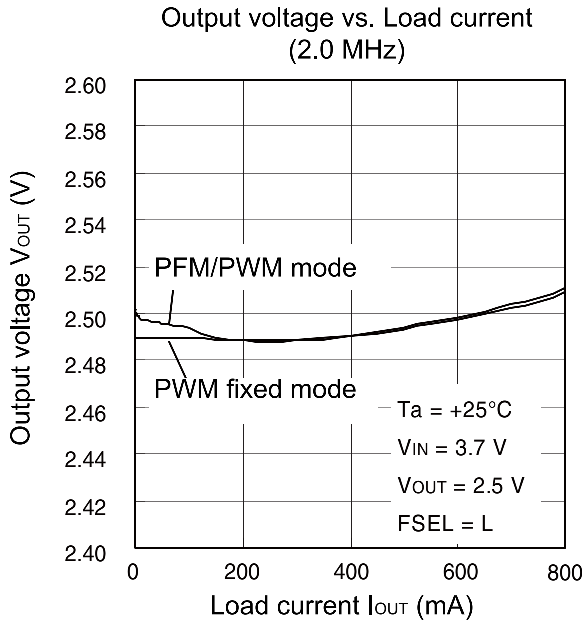

Conversion efficiency vs. Load current
(3.2 MHz:PWM fixed mode)
VIN = 3.7 V
VIN = 4.2 V
VIN = 5.0 V
Ta = +25°C
VOUT = 3.3 V
FSEL = H
MODE = OPEN
Conversion efficiency η (%)
Load current IOUT (mA)
100
90
80
70
60
50
40
30
20
10
0
1
10
100
1000

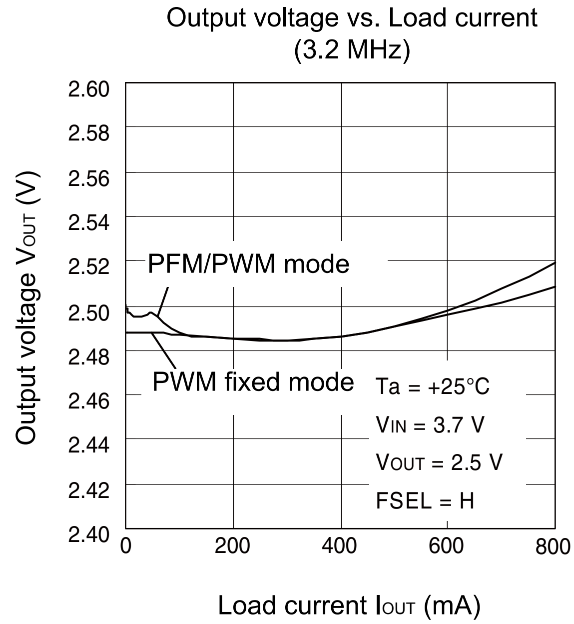

Output voltage vs. Input voltage
(2.0 MHz: PFM/PWM mode)
2.60
2.58
2.56
2.54
2.52
2.50
2.48
2.46
2.44
2.42
2.40
Output voltage VOUT (V)
OUT = 0 A
OUT = -100 mA
Ta = +25°C
VOUT = 2.5 V
FSEL = L
MODE = L
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)

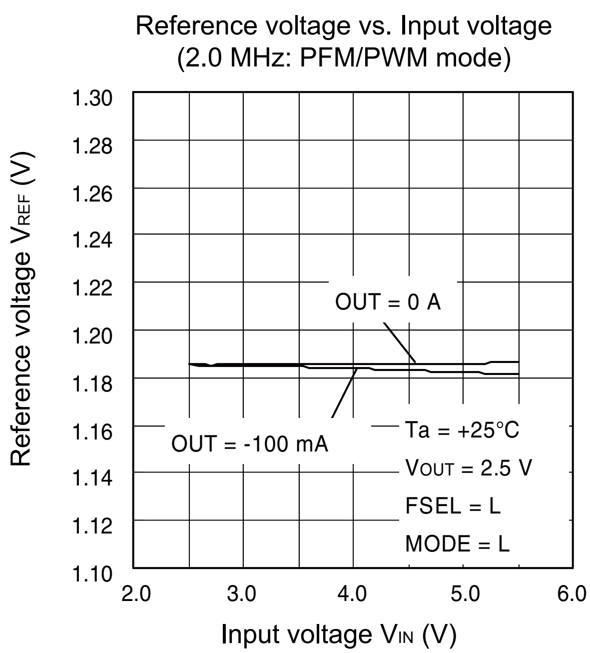

Output voltage vs. Input voltage
(3.2 MHz: PFM/PWM mode)
2.60
2.58
2.56
2.54
2.52
2.50
2.48
2.46
2.44
2.42
2.40
Output voltage VOUT (V)
OUT = 0 A
OUT = -100 mA
Ta = +25°C
VOUT = 2.5 V
FSEL = H
MODE = L
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)

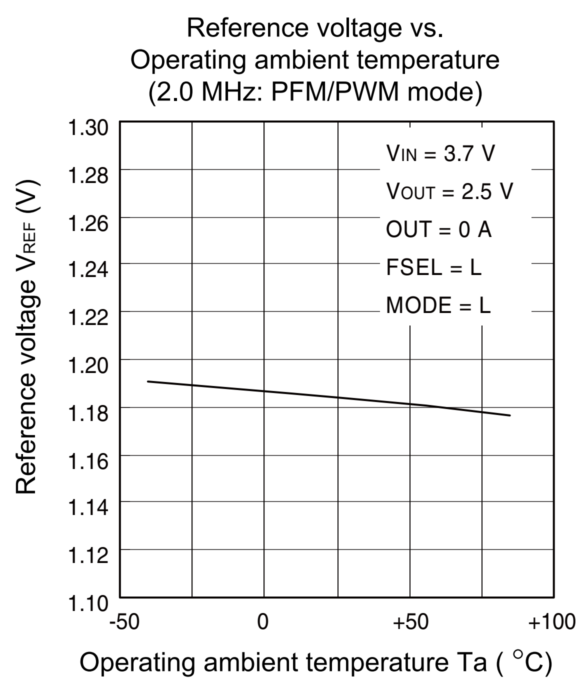

Output voltage vs. Input voltage
(2.0 MHz: PWM fixed mode)
2.60
2.58
2.56
2.54
2.52
2.50
2.48
2.46
2.44
2.42
2.40
Output voltage VOUT (V)
OUT = 0 A
OUT = -100 mA
Ta = +25°C
VOUT = 2.5 V
FSEL = L
MODE = OPEN
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)


Output voltage vs. Input voltage
(3.2 MHz: PWM fixed mode)
2.60
2.58
2.56
2.54
2.52
2.50
2.48
2.46
2.44
2.42
2.40
Output voltage VOUT (V)
OUT = 0 A
OUT = -100 mA
Ta = +25°C
VOUT = 2.5 V
FSEL = H
MODE = OPEN
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)

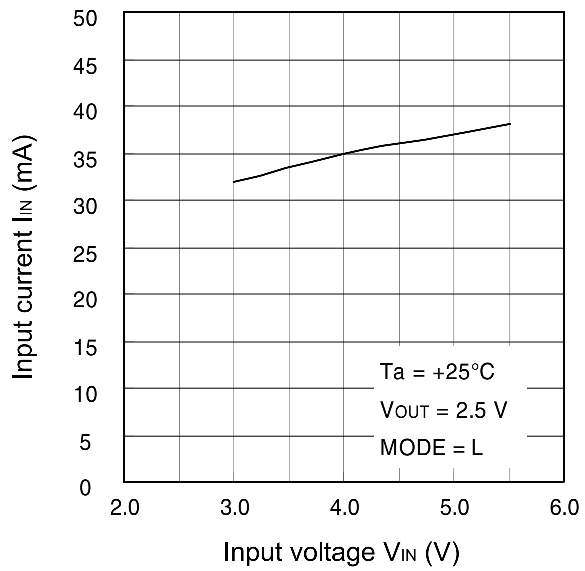

Output voltage vs. Load current
(2.0 MHz)
Output voltage VOUT (V)
2.60
2.58
2.56
2.54
2.52
2.50
2.48
2.46
2.44
2.42
2.40
PFM/PWM mode
PWM fixed mode
Ta = +25°C
VIN = 3.7 V
VOUT = 2.5 V
FSEL = L
0
200
400
600
800
Load current IOUT (mA)


Output voltage vs. Load current
(3.2 MHz)
Output voltage VOUT (V)
2.60
2.58
2.56
2.54
2.52
2.50
2.48
2.46
2.44
2.42
2.40
PFM/PWM mode
PWM fixed mode
Ta = +25°C
VIN = 3.7 V
VOUT = 2.5 V
FSEL = H
0
200
400
600
800
Load current IOUT (mA)

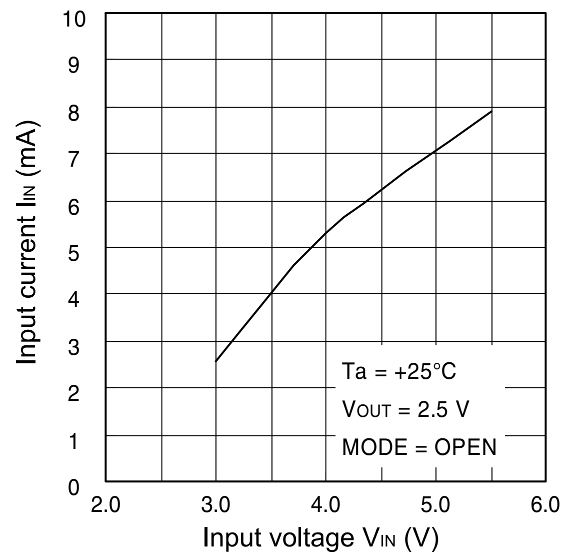

Reference voltage vs. Input voltage
(2.0 MHz: PFM/PWM mode)
Reference voltage VREF (V)
1.30
1.28
1.26
1.24
1.22
1.20
1.18
1.16
1.14
1.12
1.10
OUT = 0 A
OUT = -100 mA
Ta = +25°C
VOUT = 2.5 V
FSEL = L
MODE = L
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)


Reference voltage vs.
Operating ambient temperature
(2.0 MHz: PFM/PWM mode)
Reference voltage VREF (V)
1.30
1.28
1.26
1.24
1.22
1.20
1.18
1.16
1.14
1.12
1.10
VIN = 3.7 V
VOUT = 2.5 V
OUT = 0 A
FSEL = L
MODE = L
-50
0
+50
+100
Operating ambient temperature Ta (°C)

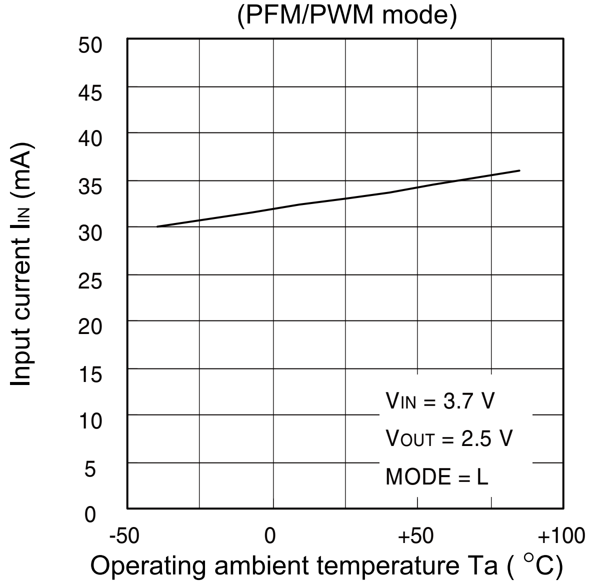
Input current vs. Input voltage
(PFM/PWM mode)



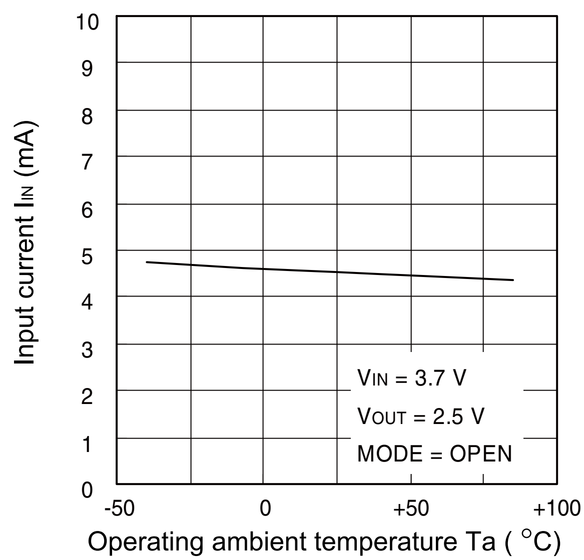
Input current vs. Input voltage
(PWM fixed mode)

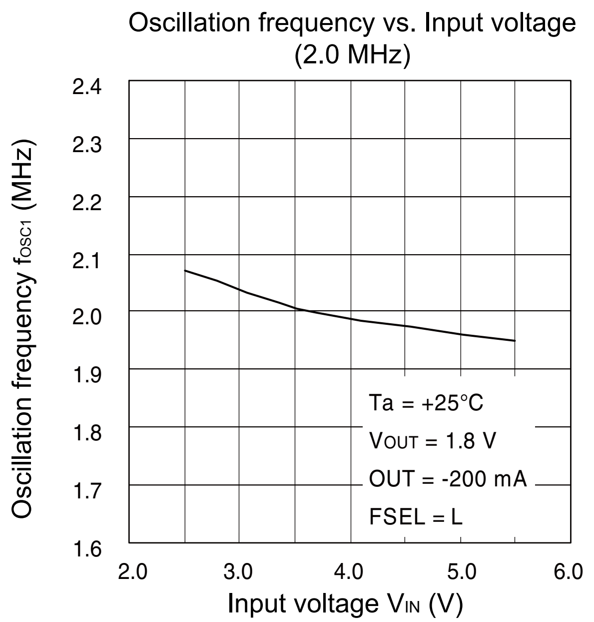


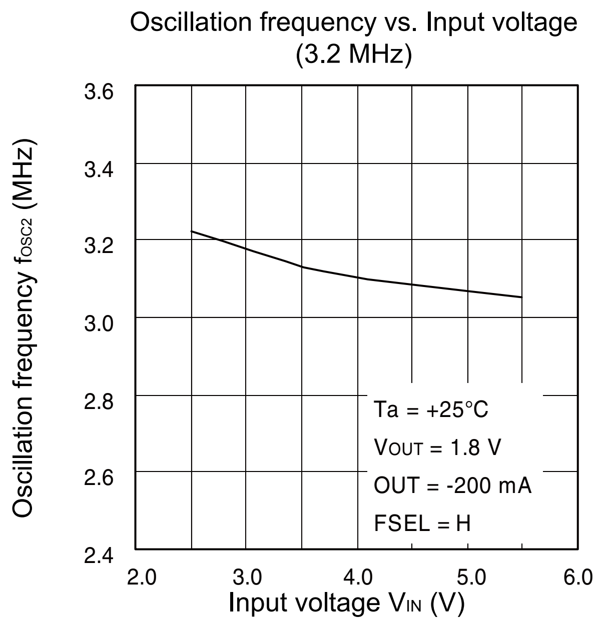
Input current vs.
Operating ambient temperature
(PFM/PWM mode)

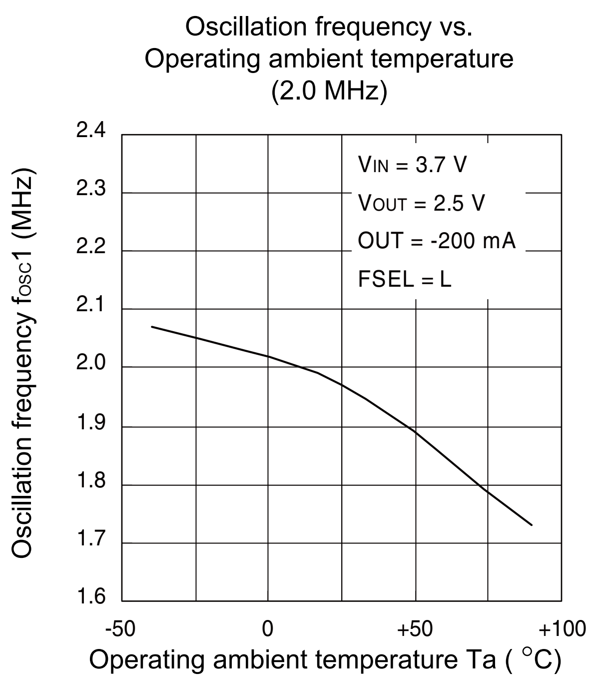


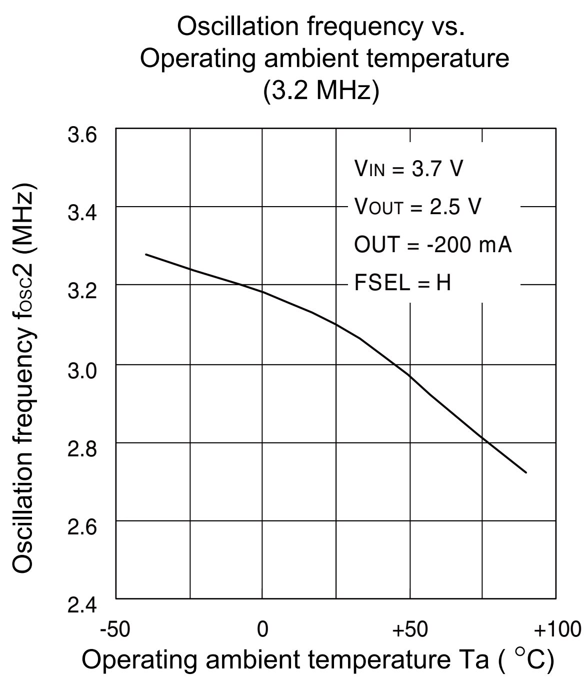
Input current vs.
Operating ambient temperature
(PWM fixed mode)

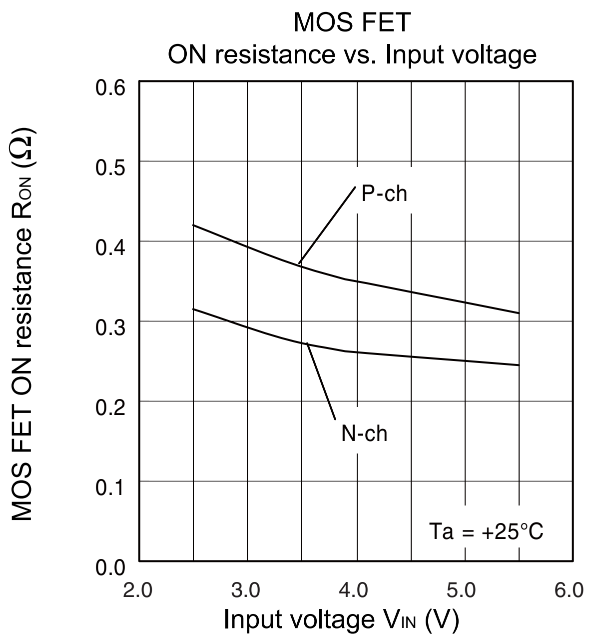


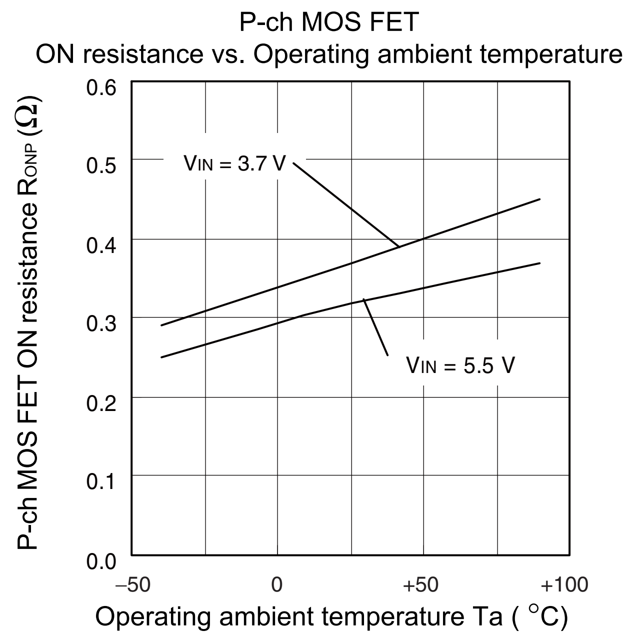

Oscillation frequency vs. Input voltage
(2.0 MHz)
Oscillation frequency fosc1 (MHz)
2.4
2.3
2.2
2.1
2.0
1.9
1.8
1.7
1.6
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)
Ta = +25°C
VOUT = 1.8 V
OUT = -200 mA
FSEL = L

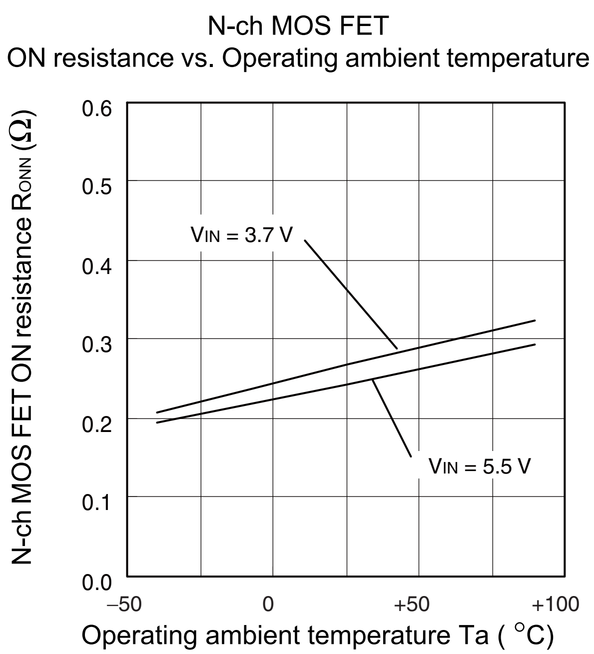

Oscillation frequency vs. Input voltage
(3.2 MHz)
Oscillation frequency fosc2 (MHz)
3.6
3.4
3.2
3.0
2.8
2.6
2.4
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)
Ta = +25°C
VOUT = 1.8 V
OUT = -200 mA
FSEL = H


Oscillation frequency vs.
Operating ambient temperature
(2.0 MHz)
Oscillation frequency fosc1 (MHz)
2.4
2.3
2.2
2.1
2.0
1.9
1.8
1.7
1.6
-50
0
+50
+100
Operating ambient temperature Ta (°C)
VIN = 3.7 V
VOUT = 2.5 V
OUT = -200 mA
FSEL = L


Oscillation frequency vs.
Operating ambient temperature
(3.2 MHz)
Oscillation frequency fosc2 (MHz)
3.6
3.4
3.2
3.0
2.8
2.6
2.4
-50
0
+50
+100
Operating ambient temperature Ta (°C)
VIN = 3.7 V
VOUT = 2.5 V
OUT = -200 mA
FSEL = H


MOS FET
ON resistance vs. Input voltage
MOS FET ON resistance RON (Ω)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
P-ch
N-ch
Ta = +25°C
2.0
3.0
4.0
5.0
6.0
Input voltage VIN (V)


P-ch MOS FET
ON resistance vs. Operating ambient temperature
P-ch MOS FET ON resistance RONP (Ω)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
VIN = 3.7 V
VIN = 5.5 V
–50
0
+50
+100
Operating ambient temperature Ta (°C)


N-ch MOS FET
ON resistance vs. Operating ambient temperature
N-ch MOS FET ON resistance RONN (Ω)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
VIN = 3.7 V
VIN = 5.5 V
–50
0
+50
+100
Operating ambient temperature Ta (°C)