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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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MB39C011A

2 ch DC/DC Converter IC with Synchronous Rectification Datasheet

The MB39C011A is a two-channel DC/DC converter IC suitable for down-conversion that utilizes synchronous rectification and pulse width modulation (PWM). The MB39C011A can operate over a wide range of power supply voltages (4.5 V to 17 V), making it optimal as a built-in power supply in digital audio visual equipment and various other electronic devices.

Features

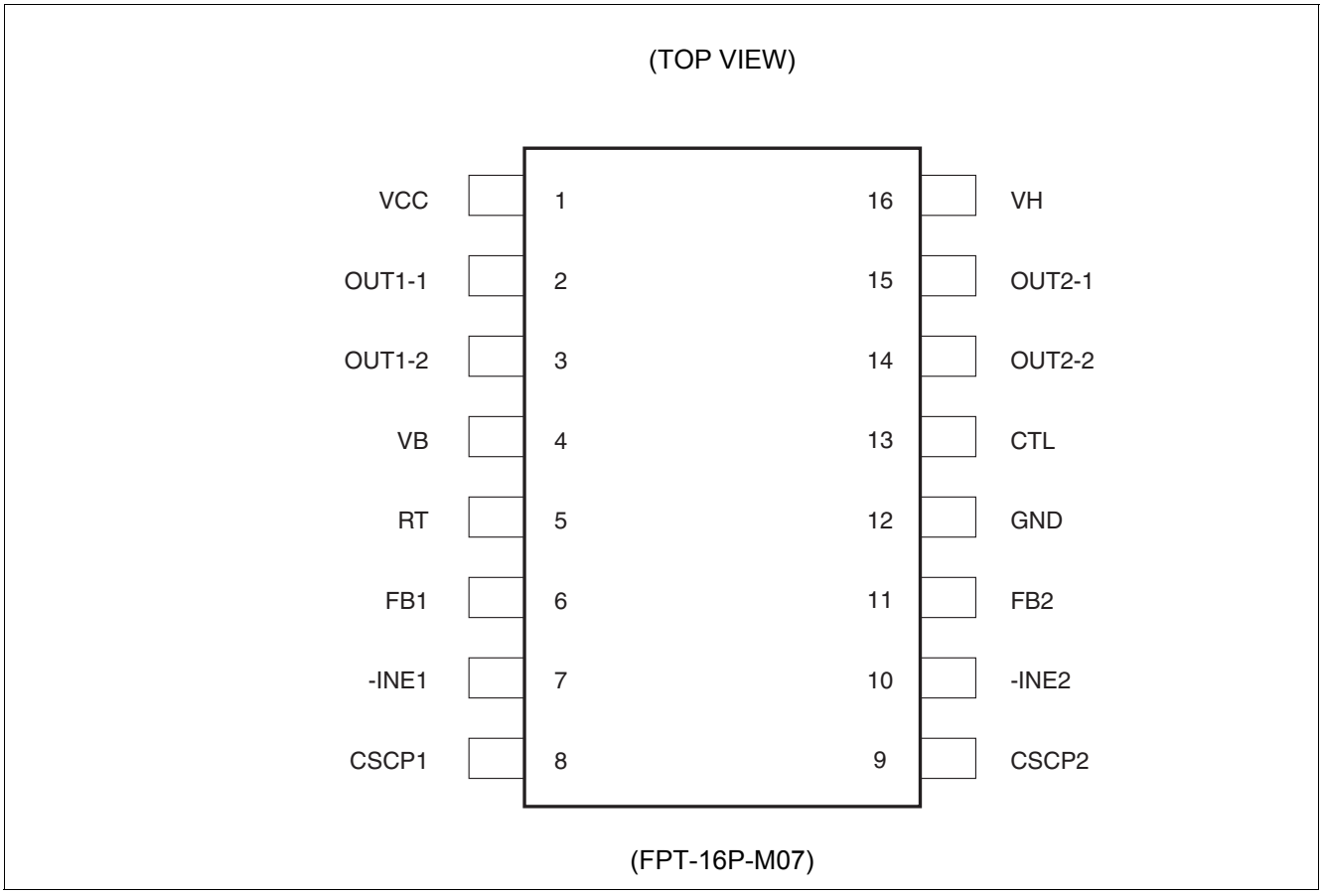
- Wide range of power supply voltages: 4.5 V to 17 V
- Supports high frequency operation: 2.0 MHz (Max)
- Supports synchronous rectification method (CH1, CH2)
- An arbitrary output voltage can be configured using an external resistance.
- Built-in standby function: 0 μA (Typ)
- Low current consumption: 2.2 mA (Typ, At quiescence)
- Built-in soft-start circuit that can control each channel separately independent of the load
- Built-in timer latch type short-circuit protection circuit (shares the soft-start capacitor)
- Built-in totem pole type output stage for external P-ch/N-ch MOS FET devices
- Package : TSSOP-16-pin

Applications

- Digital TV
- Photocopiers
- Surveillance cameras
- Set-top boxes (STB)
- DVD players, DVD recorders
- Projectors
- IP phones
- Vending machines
- Consoles and other non-portable devices

Contents

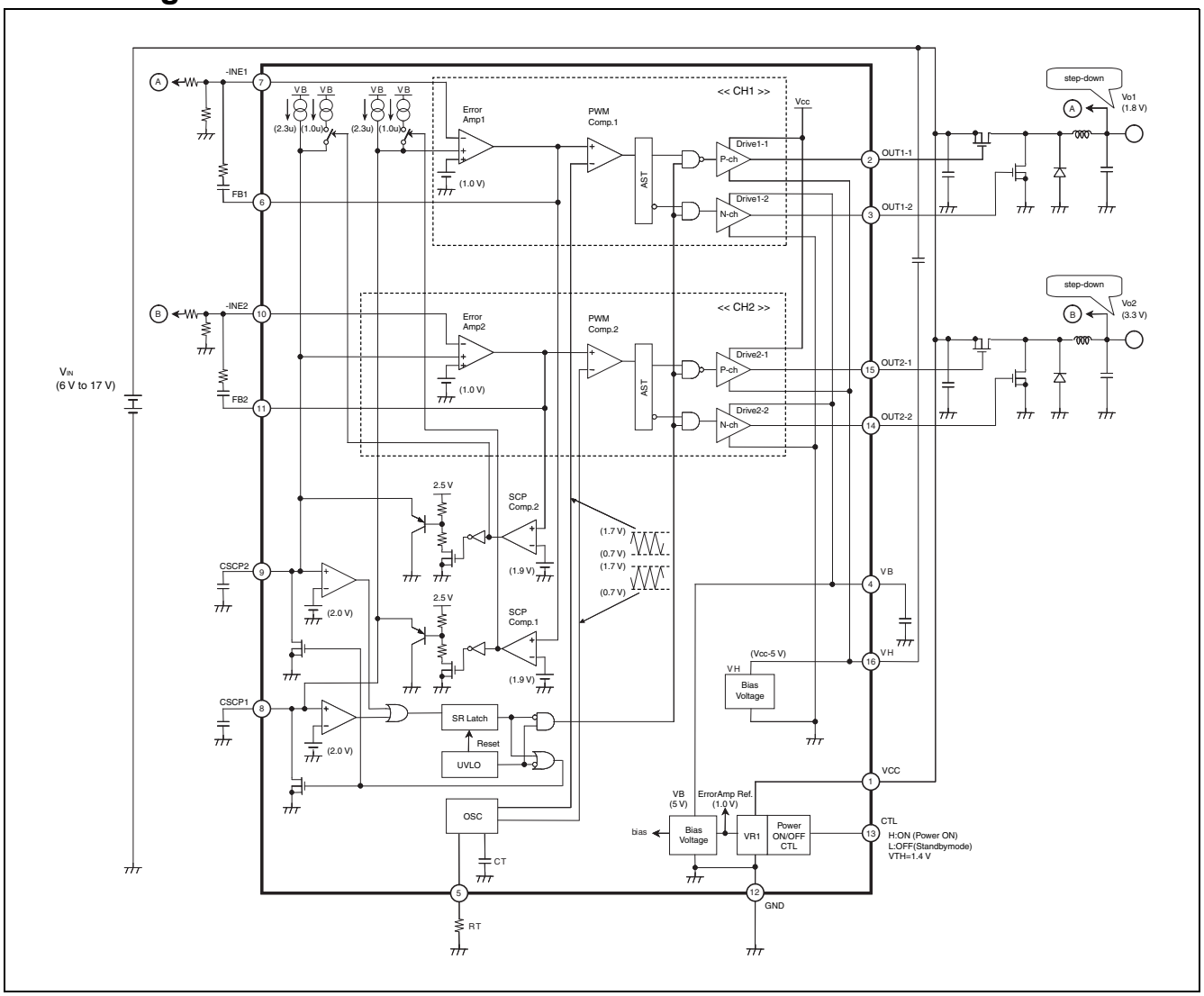
1. Pin Assignment



2. Pin Description

Pin No.	Pin Name	I/O	Description
1	VCC	-	Power supply pin for the reference voltage circuit and control circuit.
2	OUT1-1	O	Output pin for P-ch drive (drives the gate of the external High side FET).
3	OUT1-2	O	Output pin for N-ch drive (drives the gate of the external Low side FET).
4	VB	I/O	Power supply pin for the N-ch FET drive circuit (VB = 5 V).
5	RT	-	Triangular-wave oscillation frequency setting resistor connection pin.
6	FB1	O	Error amplifier (Error Amp1) output pin.
7	-INE1	I	Error amplifier (Error Amp1) inverted input pin.
8	CSCP1	-	Timer-latch short-circuit protection circuit 1 capacitor connection pin.
9	CSCP2	-	Timer-latch short-circuit protection circuit 2 capacitor connection pin.
10	-INE2	I	Error amplifier (Error Amp2) inverted input pin.
11	FB2	O	Error amplifier (Error Amp2) output pin.
12	GND	-	Ground pin for the reference voltage circuit, control circuit, and output circuit.
13	CTL	I	Power supply control pin. IC becomes a stand-by mode by setting CTL pin “L” level.
14	OUT2-2	O	Output pin for N-ch drive (drives the gate of the external Low side FET).
15	OUT2-1	O	Output pin for P-ch drive (drives the gate of the external High side FET).
16	VH	O	Power supply pin for the N-ch FET drive circuit (VH = VCC – 5 V).

3. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC pin	-	18	V
Input voltage	V_B	VB pin (When VCC pin connected to VB pin)	-	7	V
	V_{INE}	-INE1, -INE2 pins	− 0.3	V_B	V
	V_{CTL}	CTL pin	-	18	V
Output current	I_O	OUT1-1, OUT1-2, OUT2-1, OUT2-2 pins	-	60	mA
Peak output current	I_{OP}	Duty ≤ 5% (t = 1/fosc × Duty)	-	700	mA
Power dissipation	P_D	Ta ≤ + 25°C	-	1060[1]	mW
Storage temperature	T_{STG}	-	− 55	+ 125	°C

[1] : When mounted on a 10 cm square double-sided epoxy circuit board.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	VCC pin	4.5	12	17	V
VH pin output current	I_{VH}	VH pin	0	-	40	mA
VB pin output current	I_{VB}	VB pin	− 40	-	0	mA
VB pin input voltage	V_B	VB pin(When VCC pin connected to VB pin)	4.5	5	6	V
Input voltage	V_{INE}	-INE1, -INE2 pins	0	-	V_B − 0.9	V
CTL pin input voltage	V_{CTL}	CTL pin	0	-	17	V
Output current	I_{OUT}	OUT1-1, OUT1-2, OUT2-1, OUT2-2 pins	− 45	-	+ 45	mA
Oscillation frequency	f_{OSC}	Tj ≤ + 85°C	100	500	2000	kHz
Timing resistor	R_T	RT pin	3.6	16	100	kΩ
VH pin capacitor	C_{VH}	VH pin	-	1.0	4.7	μF
VB pin capacitor	C_{VB}	VB pin	-	1.0	4.7	μF
CSCP1, CSCP2 pin capacitor	CSCP1, CSCP2	CSCP1, CSCP2 pins	-	0.047	1.0	μF
Operating ambient temperature	Ta	-	− 30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

6. Electrical Characteristics

(Ta = +25°C, V_{CC} = 12 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Under Voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	4	VB ↑	3.8	4.0	4.2	V
		V_{THL}	4	VB ↓	3.6	3.8	4.0	V
	Hysteresis width	V_H	4	-	-	0.2[1]	-	V
Short-circuit protection circuit Block [SCP]	Threshold voltage	V_{TH}	8, 9	-	1.9	2.0	2.1	V
	Input source current	I_{CSCP}	8, 9	RT = 16 kΩ	− 3.2	− 2.3	− 1.4	µA
	Reset voltage	V_{RST}	4	VB = ↓	3.6	3.8	4.0	V
Triangular Wave Oscillator Block [OSC]	Oscillation frequency	fosc	2, 15	RT = 16 kΩ	450	500	550	kHz
Soft-Start Block [CS]	Charge current	I_{CS}	8, 9	CSCP1, 2 = 0 V, RT = 16 kΩ	− 4.6	− 3.3	− 2.0	µA
Error Amp Block [Error Amp1, Error Amp2]	Threshold voltage	V_{TH}	6, 11	FB1 = 1 V, FB2 = 1 V	0.99	1.00	1.01	V
	Input bias current	I_B	7, 10	-INE1 = 0 V, -INE2 = 0 V	− 100	0	+ 100	nA
	Voltage gain	A_V	6, 11	DC	-	80[1]	-	dB
	Frequency bandwidth	BW	6, 11	A_V = 0 dB	-	5.0[1]	-	MHz
	Output voltage	V_{OH}	6, 11	-	V_B − 0.3	V_B − 0.1	-	V
		V_{OL}	6, 11	-	-	40	200	mV
	Output source current	I_{SOURCE}	6, 11	FB1 = 1 V, FB2 = 1 V	-	-400	− 300	µA
	Output sink current	I_{SINK}	6, 11	FB1 = 1 V, FB2 = 1 V	4.0	8.0	-	mA
PWM Comparator Block [PWM Comp.1, PWM Comp.2]	Threshold voltage	V_{T0}	6, 11	Duty cycle = 0 %	0.6	0.7	-	V
		V_{T100}	6, 11	Duty cycle = 100 %	-	1.7	1.8	V
VH Bias Voltage Block [VH]	Output voltage	V_H	16	VCC = 6 V to 17 V VH = 0 to 40 mA	V_{CC} − 5.5	V_{CC} − 5.0	V_{CC} − 4.5	V
VB Bias Voltage Block [VB]	Output voltage	V_B	4	VCC = 6 V to 17 V VB = 0 to − 40 mA	4.5	5.0	5.5	V

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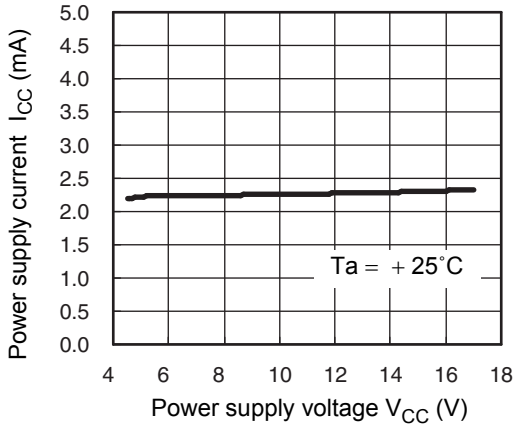
(Continued)
(Ta = +25°C, V_{CC} = 12 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Block[Drive1 to 2]	Output source current	I_{SOURCE}	2, 15	OUT1-1 = 7 V OUT2-1 = 7 V Duty ≤ 5%	-	– 500[1]	-	mA
			3, 14	VB = VCC = 5 V OUT1-2 = 0 V OUT2-2 = 0 V Duty ≤ 5%				
	Output sink current	I_{SINK}	2, 15	VCC = 5 V, At connect VH-GND OUT1-1 = 5 V OUT2-1 = 5 V Duty ≤ 5%	-	500[1]	-	mA
			3, 14	OUT1-2 = 5 V OUT2-2 = 5 V Duty ≤ 5%				
	Output on resistor	R_{OH}	2, 3, 14, 15	OUT1-1, OUT1-2, OUT2-1, OUT2-2 = – 45 mA	-	4.0	6.0	Ω
		R_{OL}	2, 15	OUT1-1, OUT2-1 = 45 mA	-	4.0	6.0	Ω
			3, 14	OUT1-2, OUT2-2 = 45 mA	-	2.6	3.9	Ω
	Dead time	td	2, 3, 14, 15	OUT1-1, OUT2-1 : H→L OUT1-2, OUT2-2 : H→L	20	40	80	ns
				OUT1-1, OUT2-1 : L →H OUT1-2, OUT2-2: L →H				
Control Block	CTL input voltage	V_{IH}	13	IC active mode	2	-	17	V
		V_{IL}	13	IC standby mode	0	-	0.8	V
	Input current	I_{CTLH}	13	CTL = 5 V	-	50	100	μA
		I_{CTLL}	13	CTL = 0 V	-	-	1	μA
General	Standby current	I_{CCS}	1	CTL = 0 V	-	0	10	μA
	Power supply current	I_{CC}	1	CTL = 5 V	-	2.2	3.3	mA

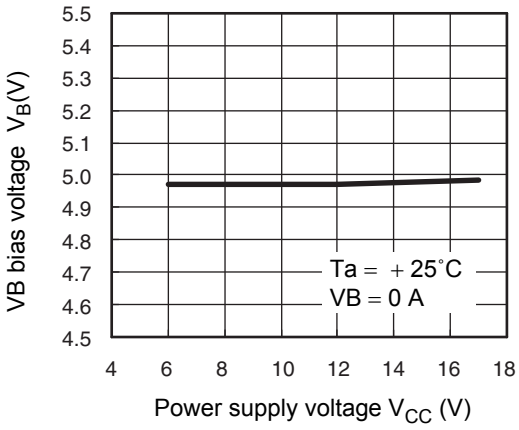
[1] : Standard design value

7. Typical Characteristics

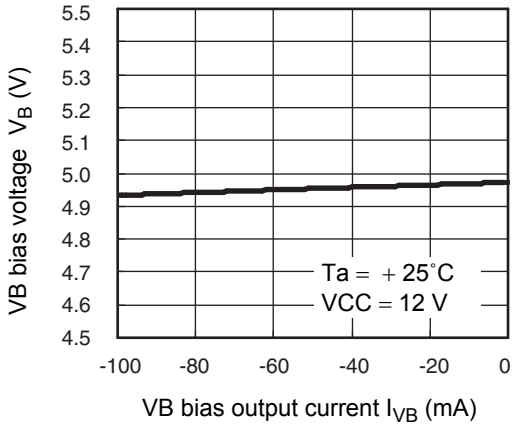
Power supply current vs.Power supply voltage



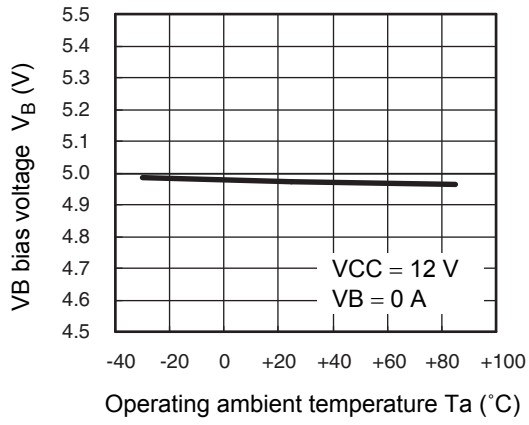
VB bias voltage vs.Power supply voltage



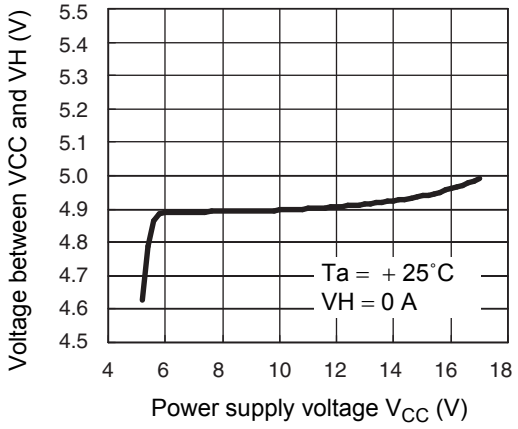
VB bias voltage vs.VB bias output current



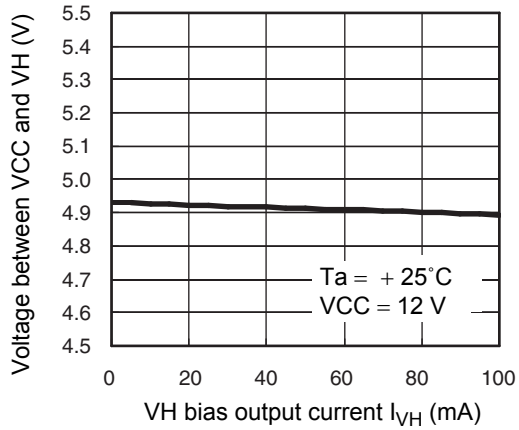
VB bias voltage vs.Operating ambient temperature



Voltage between VCC and VH vs.Power supply voltage



Voltage between VCC and VH vs.VH bias output current



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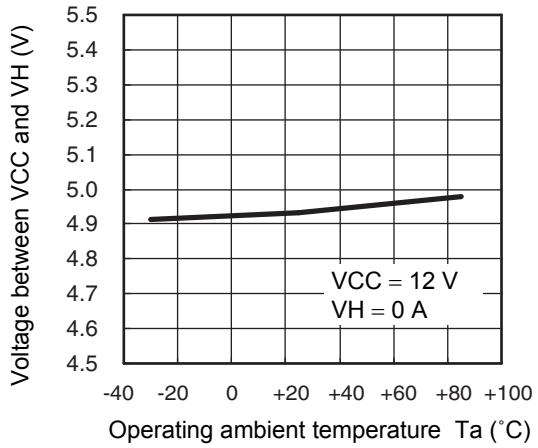
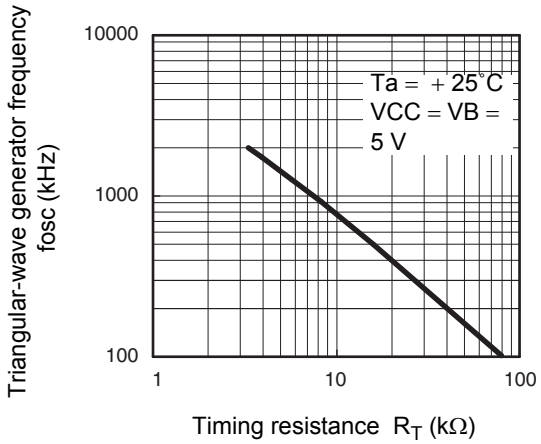
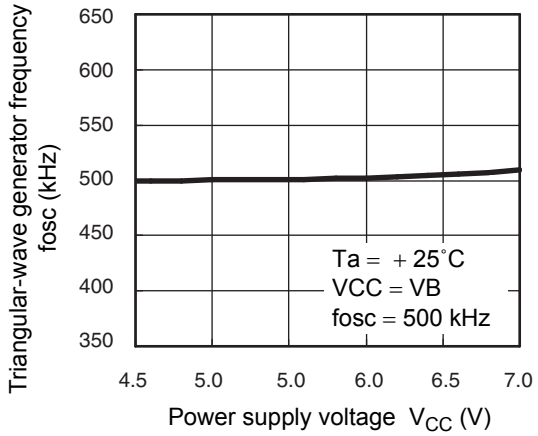
Voltage between VCC and VH vs. Operating ambient temperature



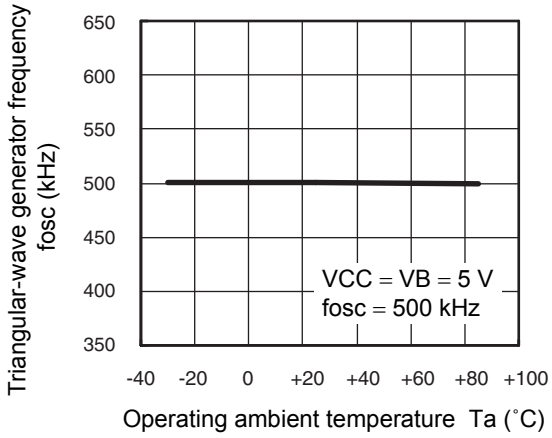
Triangular-wave generator frequency vs. Timing resistance



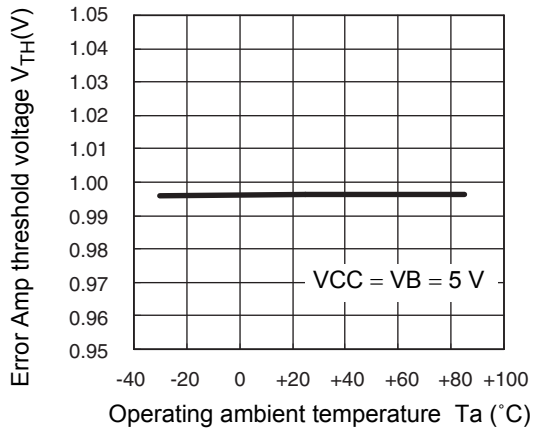
Triangular-wave generator frequency vs. Power supply voltage



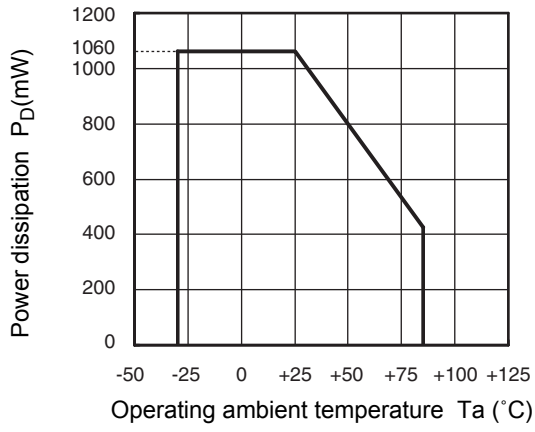
Triangular-wave generator frequency vs. Operating ambient temperature



Error Amp threshold voltage vs. Operating ambient temperature



Power dissipation vs. Operating ambient temperature



8. Functional Description

8.1 DC/DC Converter Block

8.1.1 Triangular Wave Oscillator Block (OSC)

The triangular wave oscillator block has a built-in capacitor for setting the oscillator frequency. The triangular wave is generated by connecting a resistor for selecting the frequency of the triangular wave to the RT pin (pin 5).The triangular wave is input internally to the PWM comparator in the IC.

8.1.2 Error Amplifier Block (Error Amp1, Error Amp2)

The error amplifiers (Error Amp1, Error Amp2) detect the DC/DC converter output voltages and output the PWM control signals. The output voltages can be set to an arbitrary level by externally connecting output voltage setting resistors to the error amplifier inverted input pins.
In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the error amplifier output (FB1 pin (pin 6), FB2 pin (pin 11)) to inverted input terminal (-INE1 pin (pin 7), -INE2 pin (pin 10)), enabling stable phase compensation of the system.Connecting a soft-start capacitor to the CSCP1 and CSCP2 pins (pins 8 and 9) prevents rush currents when the IC is turned on. Using an error amplifier for soft-start detection makes the soft-start time constant, independent of the output load of DC/DC converter.

8.1.3 PWM Comparator Block (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp1, Error Amp2) depending on their output voltage.
The PWM comparator circuit compares the triangular wave generated by the triangular wave oscillator to the error amplifier output voltage and turns on the external output transistor during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

8.1.4 Output Block (Drive1-1, 1-2, Drive 2-1, 2-2)

The output circuit consists of CMOS drivers on both the high side and the low side, and is capable of driving an external P-ch MOS FET on the high side and an external N-ch MOS FET on the low side.

8.1.5 Power Supply Control Block (CTL)

The DC/DC converter can be put into standby mode by setting the CTL pin (pin 13) to the “L” level (the maximum power supply current in standby mode is 10 μA), and put into operating mode by setting the CTL pin (pin 13) to the “H” level.

Control Function Table

CTL	IC
L	OFF (Standby)
H	ON (Operating)

8.2 Protection Function

8.2.1 Soft-start Circuit

To prevent rush currents when the IC is turned on, soft-start can be performed by connecting soft-start capacitors (CSCP1 and CSCP2) to the CSCP1 and CSCP2 pins (pins 8 and 9). When CTL pin (pin 13) is driven to the “H” level and the IC begins operation (VCC ≥ UVLO threshold voltage), the external soft-start capacitors (CSCP1 and CSCP2) connected to the CSCP1 and CSCP2 pins (pins 8 and 9) are charged by the charging current obtained from the following formula.

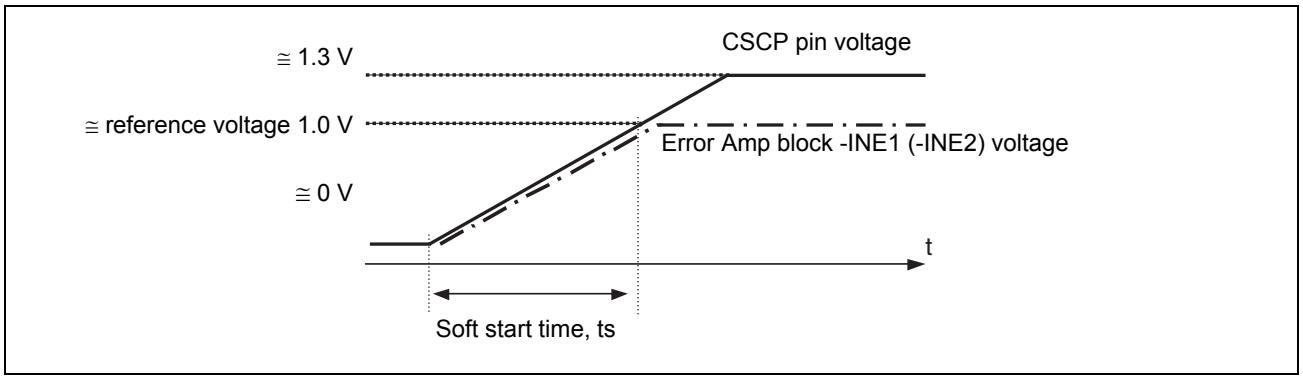
$I_{CS} \cong 5.4 \times 10^{-5} / R_T$

I_{CS} :Charge current [A]
R_T :Timing resistance [kΩ]

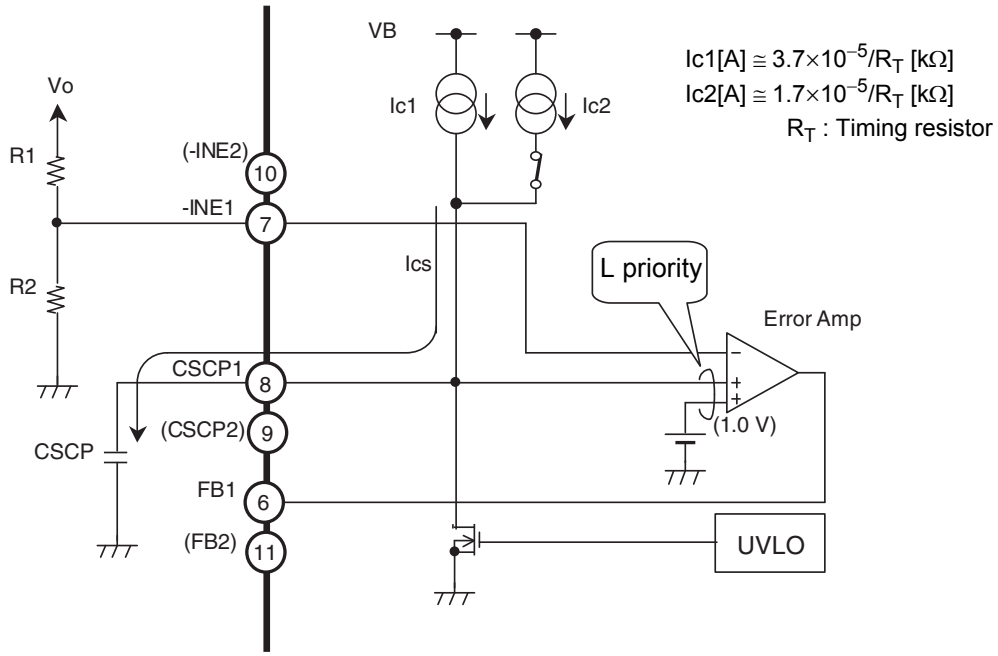
The error amplifier output (FB1 pin (pin 6), FB2 pin (pin 11)) is determined by comparing the voltages of the two non-inverted input pins (whichever of the internal 1.0 V reference voltage and the CSCP1 and CSCP2 pins (pin 8 and pin 9) has the lowest voltage) against the inverted input pin voltages (-INE1 pin (pin 7) voltage, -INE2 pin (pin 10) voltage). During the soft-start period, FB1 and FB2 are determined by comparing the internal 1.0 V reference voltage against the voltages of the CSCP1 and CSCP2 pins (pins 8 and 9), and the DC/DC converter output voltages rise in proportion to voltages of the CSCP1 and CSCP2 pins (pins 8 and 9) as the soft-start capacitors (CSCP1 and CSCP2) connected to the CSCP1 and CSCP2 pins (pins 8 and 9) are charged.
The soft-start time can be found from the following formula.

$ts \cong 0.019 \times CSCP \times R_T$

ts :Soft-start time (time to output voltage 100%) [s]
CSCP :Capacitance of CSCP pin [μF]
R_T :Timing resistance [kΩ]



Soft-start circuit



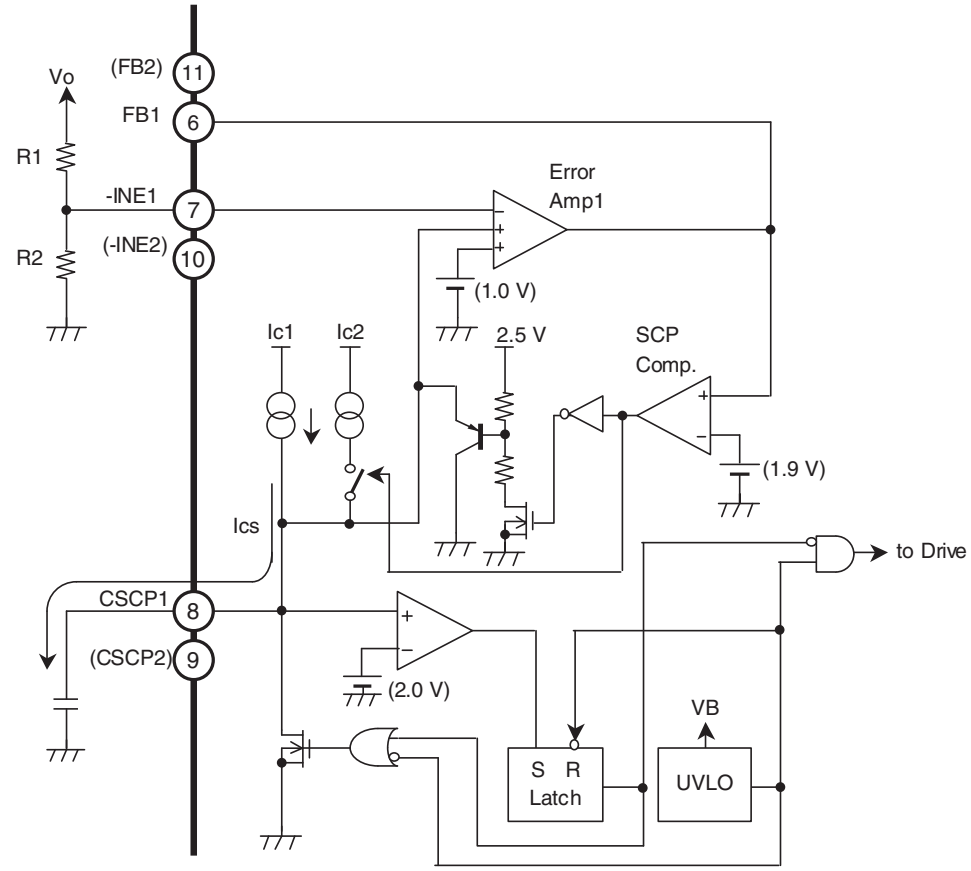
8.2.2 Timer-Latch Short-Circuit Protection Circuit

Each channel has a short-circuit detection comparator (SCP Comp1 and Comp2) that constantly compares the output level of the error amplifier against the reference voltage. While the DC/DC converter load conditions remain stable, the error amplifier output does not change and the short-circuit protection comparator remains in an equilibrium state. At this time, the CSCP1 and CSCP2 pins (pins 8 and 9) maintain the voltage from when the soft-start finished (about 1.3 V). If the output voltage of the DC/DC converter falls drastically due to a short-circuit or other load conditions, the output voltage of the error amplifier rises 1.9 V or more, and the external CSCP1 and CSCP2 capacitors are further charged. When the CSCP1 or CSCP2 capacitors are charged to about 2.0 V, a latch is set that turns off the external P-ch/N-ch MOSFETs (dead time is set to 100%). At this time, the latch input is closed and the CSCP1 and CSCP2 pins (pins 8 and 9) are held at the “L” level. Once the protection circuit has been activated, it can be reset by allowing the VB pin (pin 4) voltage to 3.8 V (minimum) or loss by turning the power off and on again.

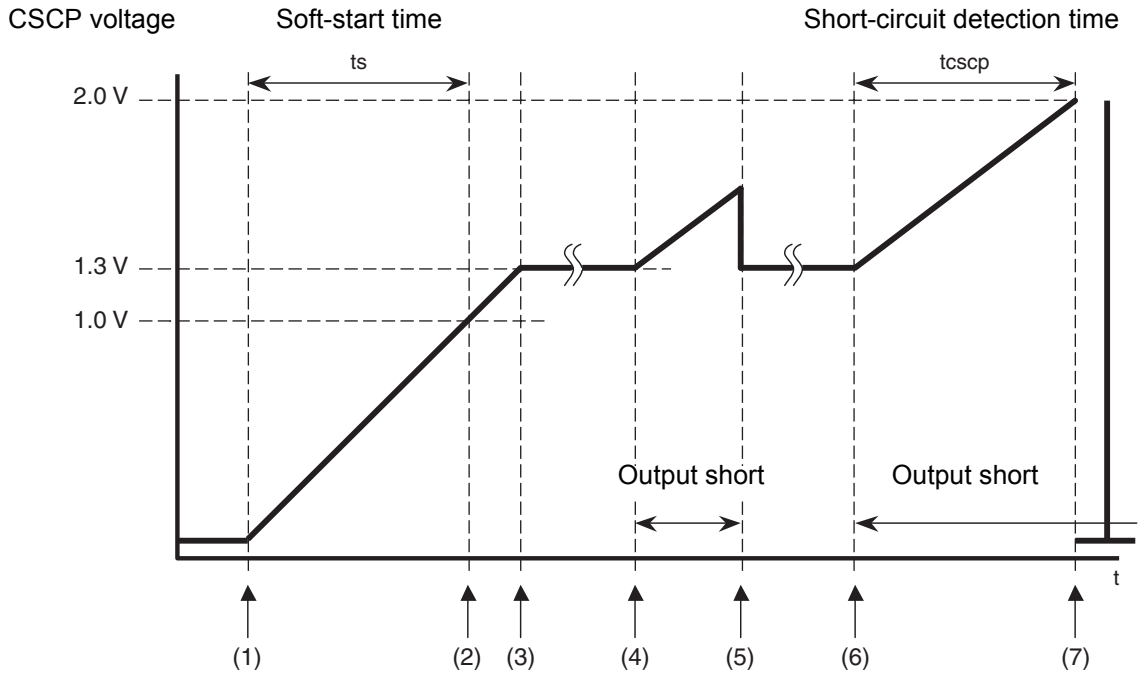
$t_{CSCP} \cong 0.019 \times CSCP \times R_T$

t_{CSCP} :Short-circuit detection time [s]
CSCP :Capacitance of CSCP pin [μF]
R_T :Timing resistance [kΩ]

Timer-latch short-circuit protection circuit



Soft-start and short-circuit protection timing chart



1. When the CTL pin (pin 13) is set to the “H” level and the IC becomes active, the voltages of the CSCP1 and CSCP2 pins (pins 8 and 9) rise due to the capacitors attached externally to the CSCP1 and CSCP2 pins (pins 8 and 9) being charged. During this time, Error Amp1 and Error Amp2 are controlled by the CSCP1 and CSCP2 pins (pins 8 and 9) and the -INE1 and -INE2 pins (pins 7 and 10) inputs, thus performing a soft-start.
2. When the CSCP1 and CSCP2 pins (pins 8 and 9) reach 1 V or more, Error Amp1 and Error Amp2 become controlled by the internal reference voltage (1 V) and the -INE1 and -INE2 pin (pins 7 and 10) inputs, and the output voltage is held at a constant level.
3. The CSCP1 and CSCP2 pins (pins 8 and 9) are clamped to about 1.3 V.
4. When there is a short circuit in the load and the error amplifier output becomes 1.9 V or more, the short-circuit protection comparator (SCP Comp.) is activated and the CSCP1 and CSCP2 capacitors are charged further.
5. If the short-circuit in the load is cleared within the short-circuit detection time t_{CSCP}, the CSCP1 and CSCP2 pins (pins 8 and 9) return to the clamping voltage of about 1.3 V.
6. When there is a short-circuit in the load and the error amplifier output becomes 1.9 V or more, the short-circuit protection comparator (SCP Comp.) is activated and the CSCP1 and CSCP2 capacitors are charged further.
7. The latch is set when the load short-circuit is not released even if short-circuit detection time t_{CSCP} passes, external MOS FET P-ch/N-ch are turned off, and the CSCP1,CSCP2 pins (pins 8 and 9) are hold at “L” level.

Notes :

- The output is stopped by the short-circuit protection (SCP) function when the DC/DC output is short-circuited to GND etc. However, care needs to be taken because the short-circuit protection (SCP) function will not stop the output when a half short-circuit occurs. Measures such as placing a fuse in the input can be used for this situation. [Half short-circuit refers to a short-circuit condition where an overcurrent flows, but it is not sufficient to reduce the output voltage.]
- In the event that an output short current flows that exceeds the capacity of the input power supply, the power supply voltage may drop. If the power supply voltage at this time drops below 3.8 V, the output is stopped by the under voltage lockout protection circuit (UVLO). However, once the input power supply voltage recovers after the output has been stopped, the output will begin again. Care needs to be taken because this situation may result in a repeating cycle of “short-circuit → power-supply voltage drop → output stop → power-supply voltage recovery → output start → short-circuit”. There are putting a fuse in the input etc. as measures.
- Notes the short-circuit protection (SCP) function when the DC/DC converter is started/stopped. The output may also be stopped by the short-circuit protection (SCP) function under the following conditions.
  - Operations that act on the input power supply and the CTL pin (for example, shorting the input power supply to the CTL pin).
  - During the transition period when the input power supply voltage (V_{IN}) is changing (such as when the input power supply is turned on or turned off), the condition is met that input power supply voltage (V_{IN}) < output setting voltage (V_O).

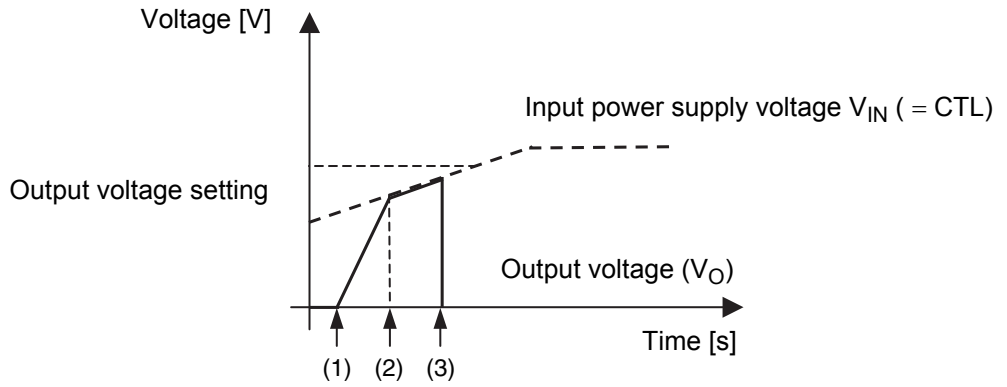
Although this is normal IC operation, as an example of startup of the IC, the output may be stopped due to the following process.

(1) DC/DC converter output begins when V_{IN} (= VB) > UVLO threshold voltage.

(2) A period of time occurs where the input power supply voltage (V_{IN}) < the output voltage setting (V_O), and the duty cycle becomes 100% on. The error amplifier output rises above 1.9 V due to the feedback control.

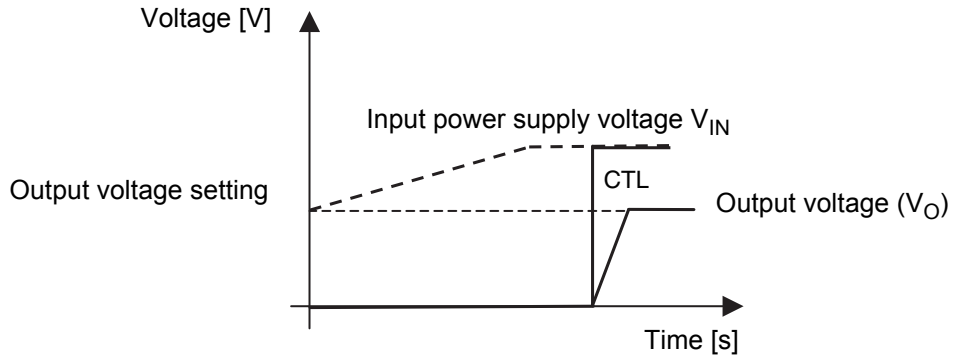
(3) The output is stopped after the short-circuit detection time has elapsed.

Example where the output stops when the DC/DC converter is activated by the input power supply (example of output stopped by SCP during startup)



In this case, the output can be prevented from being stopped by the SCP function during startup by controlling the CTL pin independently.

Example of the DC/DC converter being started by the CTL pin



Furthermore, when turning off the input power supply, set the CTL pin to “L” before turning off the input power supply.

8.2.3 Under Voltage Lockout Protection Circuit (UVLO)

A drop in the power supply voltage may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, the under voltage lockout protection circuit detects decreases in VB voltage due to the power supply voltage, and locks, the OUT1-1 pin (pin 2) and OUT2-1 pin (pin 15) at the “H” level and the OUT1-2 pin (pin 3) and OUT2-2 pin (pin 14) at the “L” level. The system is restored if the VB voltage rises above the threshold voltage of the under voltage lockout protection circuit.

Function Table When the Protection Circuit (UVLO) is Operating

When the UVLO circuit is operating (the VB voltage is below the UVLO threshold voltage), the following pins are fixed at the following logic levels.

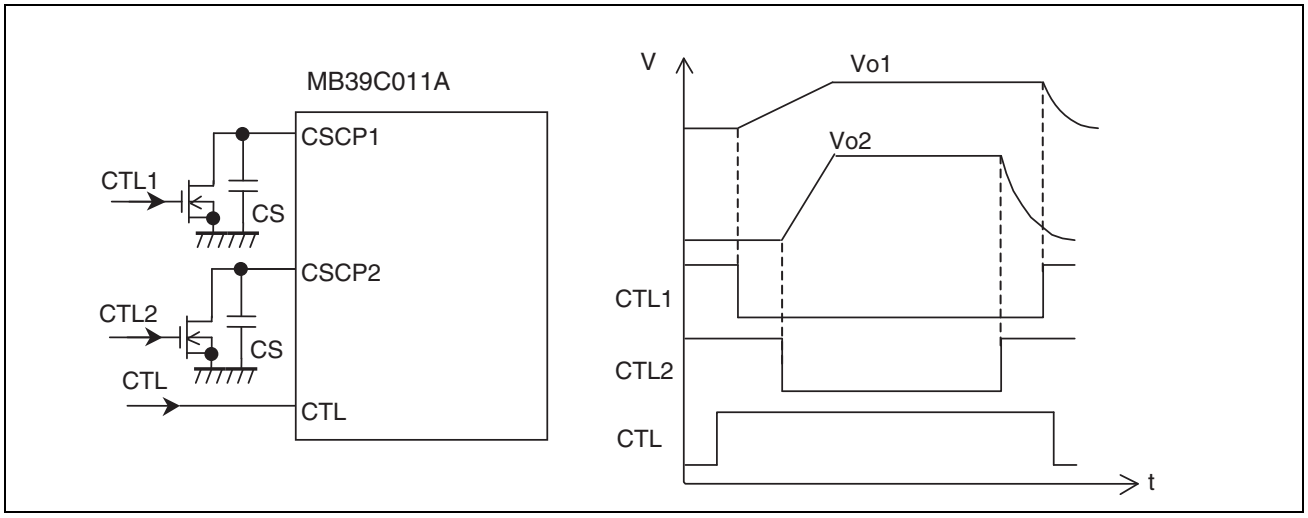
OUT1-1	OUT1-2	OUT2-1	OUT2-2	CSCP1	CSCP2
H	L	H	L	L	L

8.2.4 Operation When CTL is Turned On and Off

When CTL is turned on, the internal reference voltages VR1 and VB begin to rise. When VB exceeds the threshold voltage (VTH) of UVLO (under voltage lockout protection circuit), UVLO is released, and the output drive circuits of each channel are allowed to operate.When CTL is off, the output drive circuit of each channel is locked in the full off state and the CSCP1 and CSCP2 pins (pins 8 and 9) are fixed at the “L” level, even if the UVLO circuit is in the clear state. When the internal reference voltages VR1 and VB begin to fall and when VB falls below the threshold voltage of the UVLO (under voltage lockout protection circuit), the UVLO circuit is activated.

8.2.5 Independent Control Of Each Channel

The on/off state of each output voltage can be controlled independently by externally connecting the CSCP1 and CSCP2 pins (pins 8 and 9) to the drain pin of an NMOS transistor or to an NMOS open drain pin of a microcontroller, etc. When the CSCP1 or CSCP2 pins (pins 8 and 9) is set to the “L” level by turning on the external NMOS transistor, the output voltage turns off. Furthermore, when the external NMOS transistor is turned off, the soft-start function begins and the output voltage turns on. Note that the internal operation of the IC continues when the output voltages are turned off using the CSCP1 and CSCP2 pins (pins 8 and 9). Set the CTL pin (pin 13) to the “L” level to enter standby mode (the maximum power supply current in standby mode is 10 μA).



9. Switching Scheme Selection

This device can operate even by a synchronous rectification and an asynchronous rectification. There is superiority or inferiority respectively. Select the switching type considering the features as a guide.

Switching type	Parts	Feature
Asynchronous rectification	P-ch FET + Fly-back diode	■ Superior cost advantages ■ Under large load currents and low output voltages, it is inefficient because generation of heat of the Fly-back diode (SBD) is large.
Synchronous rectification	P-ch FET + N-ch FET	■ Offers a balance between cost and efficiency. ■ Supports large load currents and low output voltages
	P-ch FET + N-ch FET + Fly-back diode	■ Emphasis on efficiency (particularly effective at high oscillator frequencies) ■ Supports large load currents and low output voltages ■ Because of the increased number of parts, the cost is a disadvantage.

10. Setting The Output Voltage

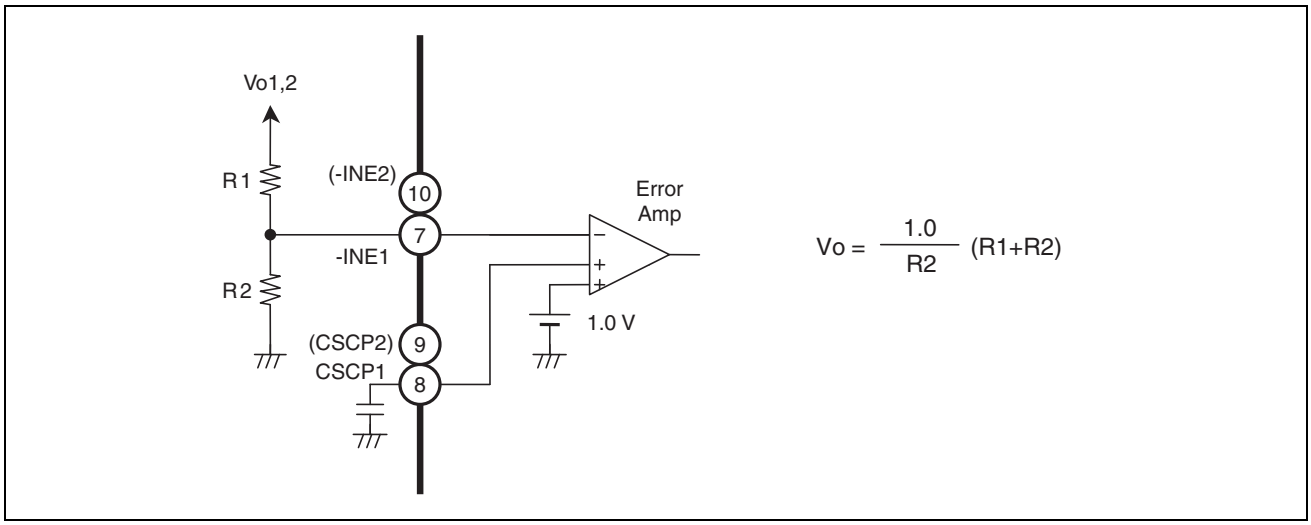
The output voltage can be set to an arbitrary value by the ratio of the feedback resistance to -INE1 (-INE2).

■Set the output voltage to a value higher than the reference voltage (1 V) of the Error Amp.

■Under usage conditions where the duty cycle is 30% or less, set $V_O1 < V_O2$ as much as possible.

$$D = \frac{V_O}{V_{IN}} \times 100$$

D :Duty cycle [%]
V_{IN} :Power supply voltage of switching system [V]
V_O :Output setting voltage [V]
R1, R2 :Output voltage setting resistors [Ω]



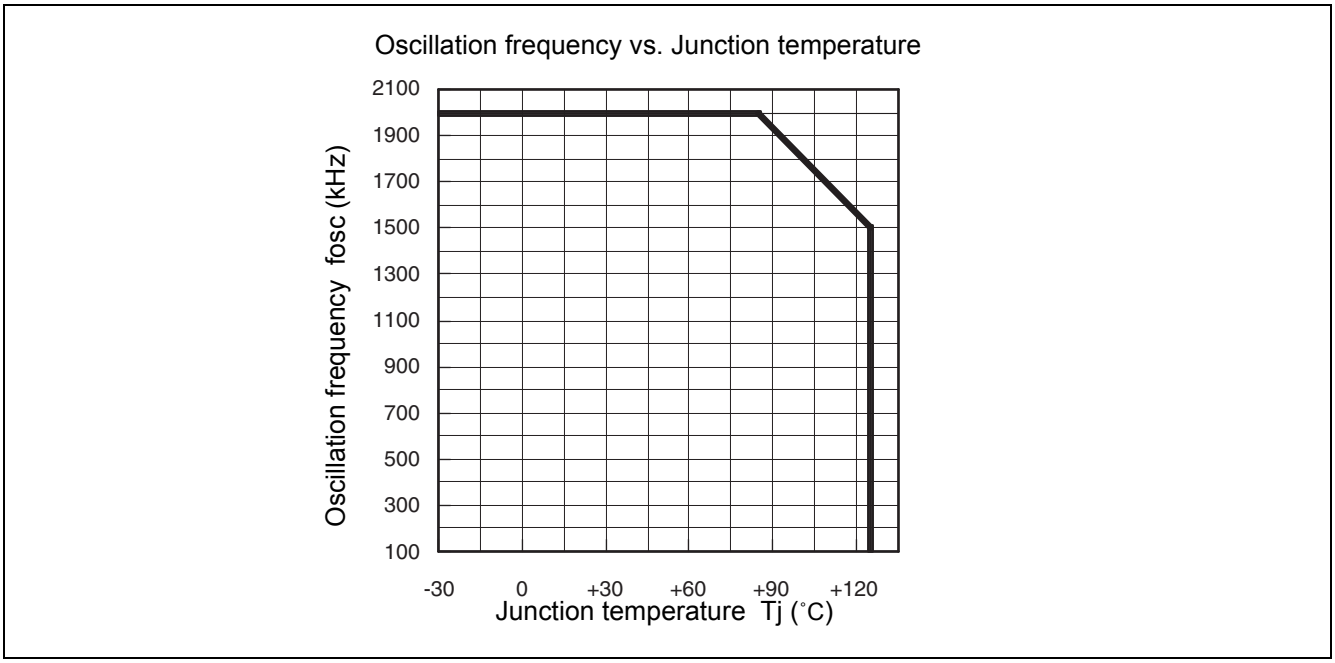
11. Setting The Triangular Oscillation Frequency

The triangular oscillation frequency is determined by the timing resistor (R_T) connected to the RT pin (pin 5).

$$fosc \cong \frac{0.001}{122.4 \times 10^{-12} \times R_T \times 10^3 + 96 \times 10^{-9}}$$

fosc : Triangular oscillation frequency [kHz]
R_T : Timing resistance [kΩ]

The upper limit on the oscillation frequency that can be set depends on the junction temperature and duty cycle. It is recommended that the device is used within the range shown in the following graph.



Note : Refer to " Power Dissipation and Thermal Design" for details on calculating the junction temperature.

11.1 Power Dissipation and Thermal Design

It is necessary to examine it for the use at a high power-supply voltage, a high oscillation frequency, and the high temperature. Also use within the range of "Oscillation frequency vs. Junction temperature".

The junction temperature can be investigated from the internal power dissipation of the IC.

The internal power dissipation of the IC (P_{IC}) is given by the following formula.

$P_{IC} = V_{CC} \times (I_{CC} + Qg \times fosc)$

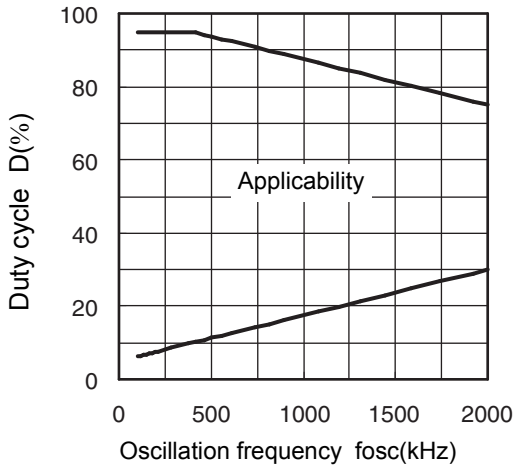
P_{IC} : Internal IC power dissipation [W]
V_{CC} : Power supply voltage (VIN : [V])
I_{CC} : Power supply current (3.3 mA Max)
Qg : Total electric charge (Vgs = 5 V) of all SW FET for 2ch [C]
fosc : Oscillation frequency [Hz]

The junction temperature is given by the following formula.

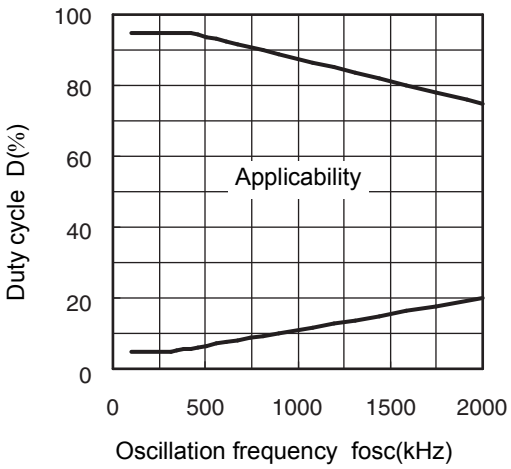
$Tj = Ta + \theta ja \times P_{IC}$

Tj :Junction temperature (+ 125˚C Max)
Ta :Ambient temperature [˚C]
θja :TSSOP-16 package thermal resistance (94˚C/W)
P_{IC} :Internal IC power dissipation [W]

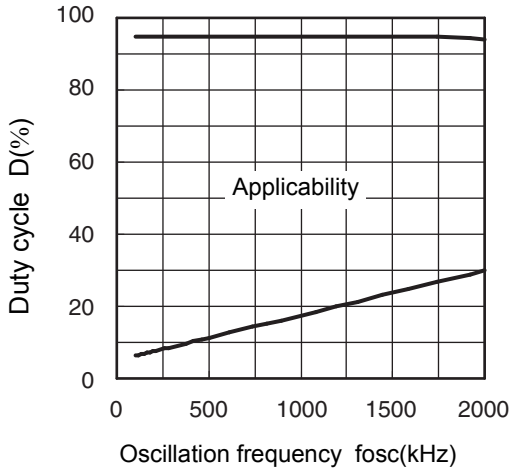
Synchronous rectification,
at 4.5 V ≤ V_{IN} ≤ 6 V (VCC = VB)
Duty cycle vs. Oscillation frequency



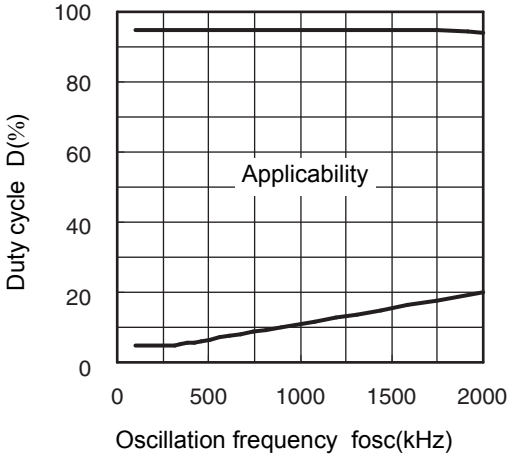
Synchronous rectification,
at V_{IN} > 6 V(VB = 5 V)
Duty cycle vs. Oscillation frequency



Asynchronous rectification,
at 4.5 V ≤ V_{IN} ≤ 6 V(VCC = VB)
Duty cycle vs. Oscillation frequency



Asynchronous rectification,
at V_{IN} > 6 V(VB = 5 V)
Duty cycle vs. Oscillation frequency



Notes :

■Refer to "Setting The Output Voltage" for details on calculating the duty cycle.

■When using the IC outside of the ranges shown in the above graphs, check for jitter and other adverse effects on the output voltage before use.

12. Setting The Soft-start And Short-circuit Detection Times

Set the soft-start time and the short-circuit detection time using the CSCP pins. Both become the same time.

$ts = t_{CSCP} \cong 0.019 \times CSCP \times R_T$

ts :Soft-start time (time to output voltage 100%) [s]
t_{CSCP} :Short-circuit detection time [s]
CSCP :CSCP pin capacitor [μF]
R_T :Timing resistance [kΩ]

13. VB Pin And VH Pin Connections In Condition Of Vcc Voltage

In the range of 4.5 V ≤ VCC ≤ 6.0 V, there is a chance that the VB voltage[1] and VH voltage[2] may drop due to the internal IC regulator saturating. As a result, there are drive voltage shortage and a bird clapper of SW FET. It is therefore recommended that the VB pin (pin 4) and VH pin (pin 16) are connected as shown in the “VB pin and VH pin connection table”.

[1]: Voltage between VB pin (pin 4) and GND pin (pin 12) : 5 V

[2] : Voltage between VCC pin (pin 1) and VH pin (pin 16) : 5 V

VB pin and VH pin connection table

VCC condition	VB pin	VH pin
4.5 ≤ VCC ≤ 6 V	Connected to VCC	Connected to GND
6 V ≤ VCC ≤ 17 V	VB capacitor connection[4]	VH capacitor connection[4]
Used with VCC crossing 6 V[3](ex. 5 V ≤ VCC ≤ 7 V)	VB capacitor connection[4]	VH capacitor connection[4]

[3]: Check that the switching operation is functioning normally.
[4]: Refer to the connection of the VB pin (pin 4) and the VH pin (pin 16) in the “Block Diagram”.

Transition diagram of the VB voltage and VH voltage (VB pin: VB capacitor connection, VH pin: VH capacitor connection)