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MB39C031

2ch Buck DC/DC Converter + 1ch LDO with I²C interface and SW FET

Description

The MB39C031 contains 2ch buck DC/DC converter and 1ch LDO. It is possible to supply the main power supply line in a system by using only one chip. The current mode system is adopted for the DC/DC converter, and it is possible to use the chip inductor with the high switching frequency operation which contains internal SW FET. The MB39C031 contains the output setting resistor and the the phase compensation circuit, and contributes to reduce the number of external components and the mounting area. Also, it contains the CTL input pin which can control the ON/OFF for each CH, the Power Good signal output pin and the I2C communication interface, therefore it is easy to design the power supply sequence.

It is possible to tune in the output voltage exactly using the I²C communication and possible to correspond to the DVS/ASV system.

Features

- Operating input voltage range:2.5V to 5.5V (Maximum rating: 7V)
- Output voltage setting range, Maximum output current: DD1*:1.0V to 1.3V (20mV/step), 1.4A (DC)
  DD2*:1.2V to 1.95V (50mV/step), 0.6A (DC)
  LDO:2.8V/2.85V/3.0V/3.3V, 0.25A (DC)

  Note: Each channel has selective preset voltage (Lineup for a total of 32 kinds) .
- Soft-start time setting range: 0.9ms to 14.3ms (approximately 0.9ms/step)
- Switching frequency for the DC/DC block:3MHz (fixed)
- Communication interface: I²C (ON/OFF, Output voltage, Soft-start time setting)
- Built-in PFM/PWM auto switching mode
- Built-in function: Output setting resistor, Phase compensation circuit, Discharge resistor, Soft-start
- Each Channel Power Good output function (Open-drain)
- Protection function: Under voltage lockout protection circuit (UVLO), Over current protection circuit (OCP), Thermal shutdown protection circuit (TSD)
- Error signal output pin installed (Open-drain)
- Small package: QFN28 (4mm × 4mm × 0.8mm, 0.4mm pitch)

*: DD1,DD2 : DC/DC converter block 1, 2

Application

Network equipment: Wifi-tuner, Surveillance camera

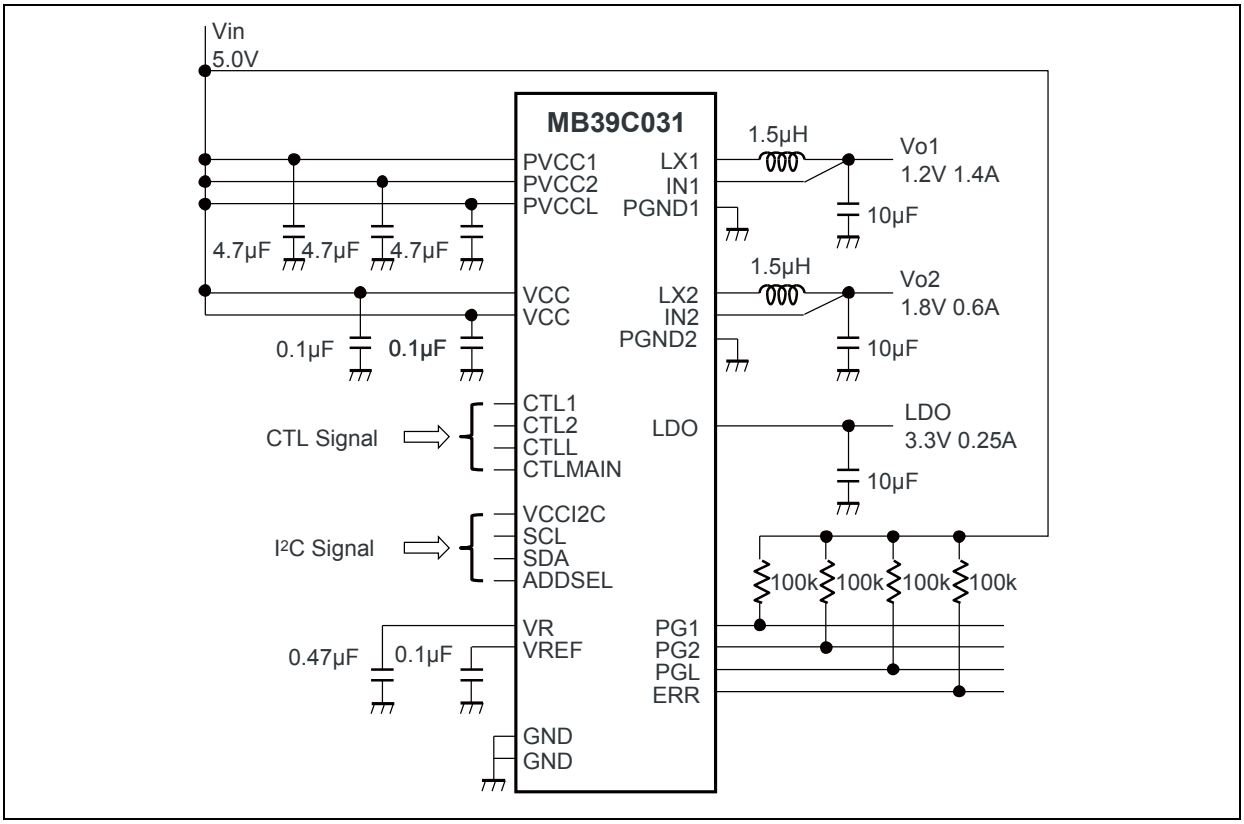
Data-storage device: HDD, SSD, Picture recording equipment

Image and voice output equipment: MFP, Printer, Scanner, Projector, Electrophone, STB

Various terminals: POS, FA, HEMS etc.

Contents

1. Application Circuit Example



2. Recommended Application Specifications

[Input Voltage Range]

Input voltage VCC (V)		
Min	**Typ**	**Max**
2.5	3.6	5.5

Output Specification

(Ta=+25°C)

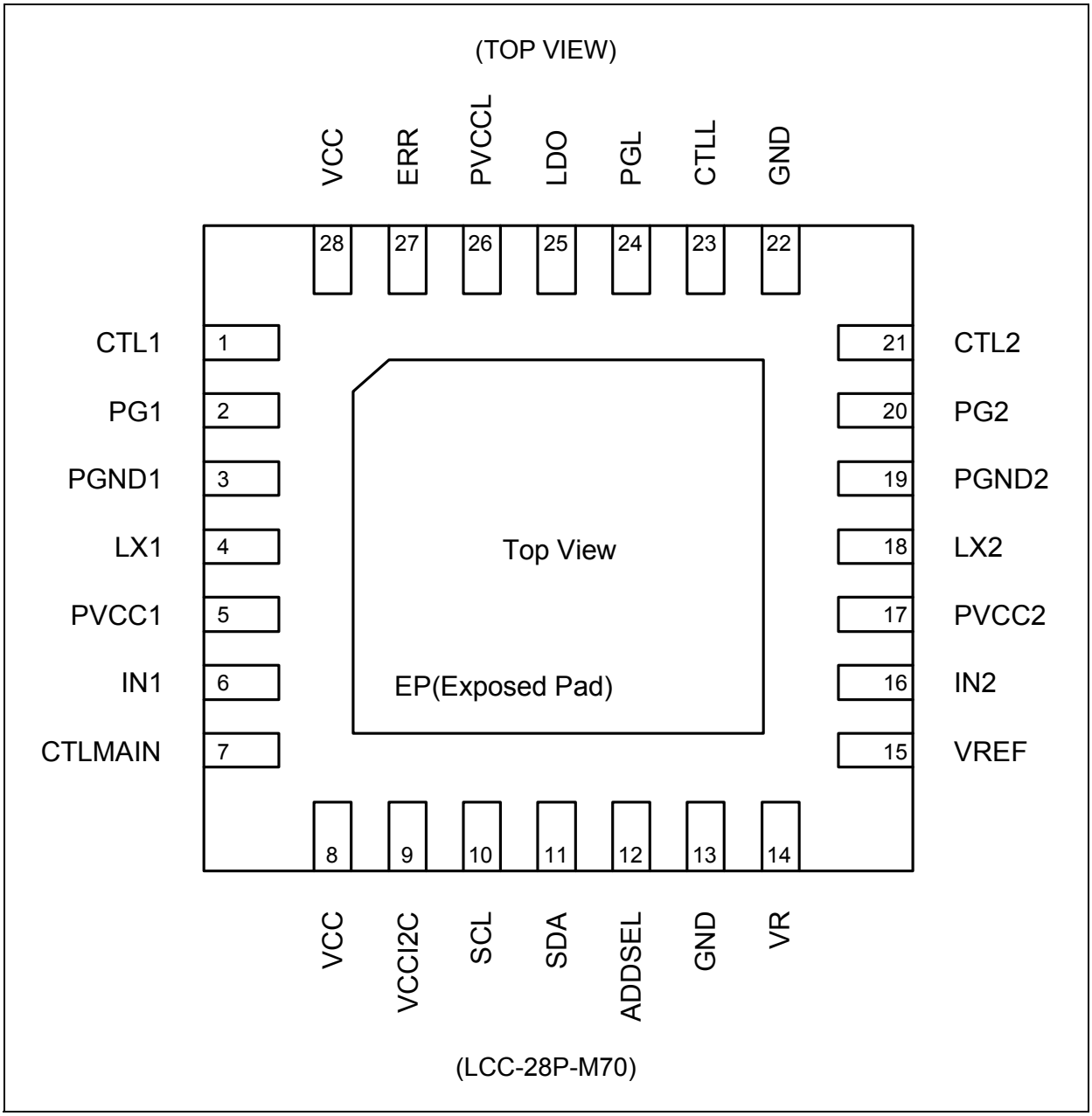
Channel	Symbol	Accuracy	Output voltage (V)			Output current (mA)	Limit Current (mA)	Mode	Switching frequency (MHz)	Coil (µH)	Output capacitance (µF)	Soft-start time (ms)	Discharge resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
DD1	Vo1	±1.2%	0.99*	1.00*	1.01*	1400	2000	Buck (synchronous rectification) C-mode	3.0	1.5	10	14.3	5	Built-in SW FET Built-in output setting resistors Operation mode switching (Fixed PWM, PFM/PWM)
			1.01	1.02	1.03							0.9*		
			1.03	1.04	1.05							1.8		
			1.05	1.06	1.07							2.7		
			1.07	1.08	1.09							3.6		
			1.09*	1.10*	1.11*							4.5		
			1.11	1.12	1.13							5.4		
			1.13	1.14	1.15							6.3		
			1.15	1.16	1.17							7.2		
			1.17	1.18	1.19							8.1		
			1.19*	1.20*	1.21*							9.0		
			1.21	1.22	1.23							9.9		
			1.23	1.24	1.25							10.8		
			1.24	1.26	1.28							11.6		
			1.26	1.28	1.30							12.5		
			1.28*	1.30*	1.32*							13.4		
DD2	Vo2	±1.2%	1.19*	1.20*	1.21*	600	900	Buck (synchronous rectification) C-mode	3.0	1.5	10	14.3	5	Built-in SW FET Built-in output setting resistors Operation mode switching (Fixed PWM, PFM/PWM)
			1.24	1.25	1.27							0.9*		
			1.28	1.30	1.32							1.8		
			1.33*	1.35*	1.37*							2.7		
			1.38	1.40	1.42							3.6		
			1.43	1.45	1.47							4.5		
			1.48*	1.50*	1.52*							5.4		
			1.53	1.55	1.57							6.3		
			1.58	1.60	1.62							7.2		
			1.63	1.65	1.67							8.1		
			1.68	1.70	1.72							9.0		
			1.73	1.75	1.77							9.9		
			1.78*	1.80*	1.82*							10.8		
			1.83	1.85	1.87							11.6		
			1.88	1.90	1.92							12.5		
			1.93	1.95	1.97							13.4		

Channel	Symbol	Accuracy	Output voltage (V)			Output current (mA)	Limit Current (mA)	Mode	Switching frequency (MHz)	Coil (µH)	Output capacitance (µF)	Soft-start time (ms)	Discharge resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
LDO	LDO	±1.8%	2.75	2.80	2.85	250	300	LDO	-	-	4.7	14.3	5	
			2.80*	2.85*	2.90*							0.9		
			2.95	3.00	3.05							1.8		
			3.24*	3.30*	3.36*							2.7*		
			-	-	-							3.6		
			-	-	-							4.5		
			-	-	-							5.4		
			-	-	-							6.3		
			-	-	-							7.2		
			-	-	-							8.1		
			-	-	-							9.0		
			-	-	-							9.9		
			-	-	-							10.8		
			-	-	-							11.6		
			-	-	-							12.5		
			-	-	-							13.4		

*: Preset value

Note: It is possible to set the output voltage and to change the soft-start time using I^2C.

3. Pin Assignment



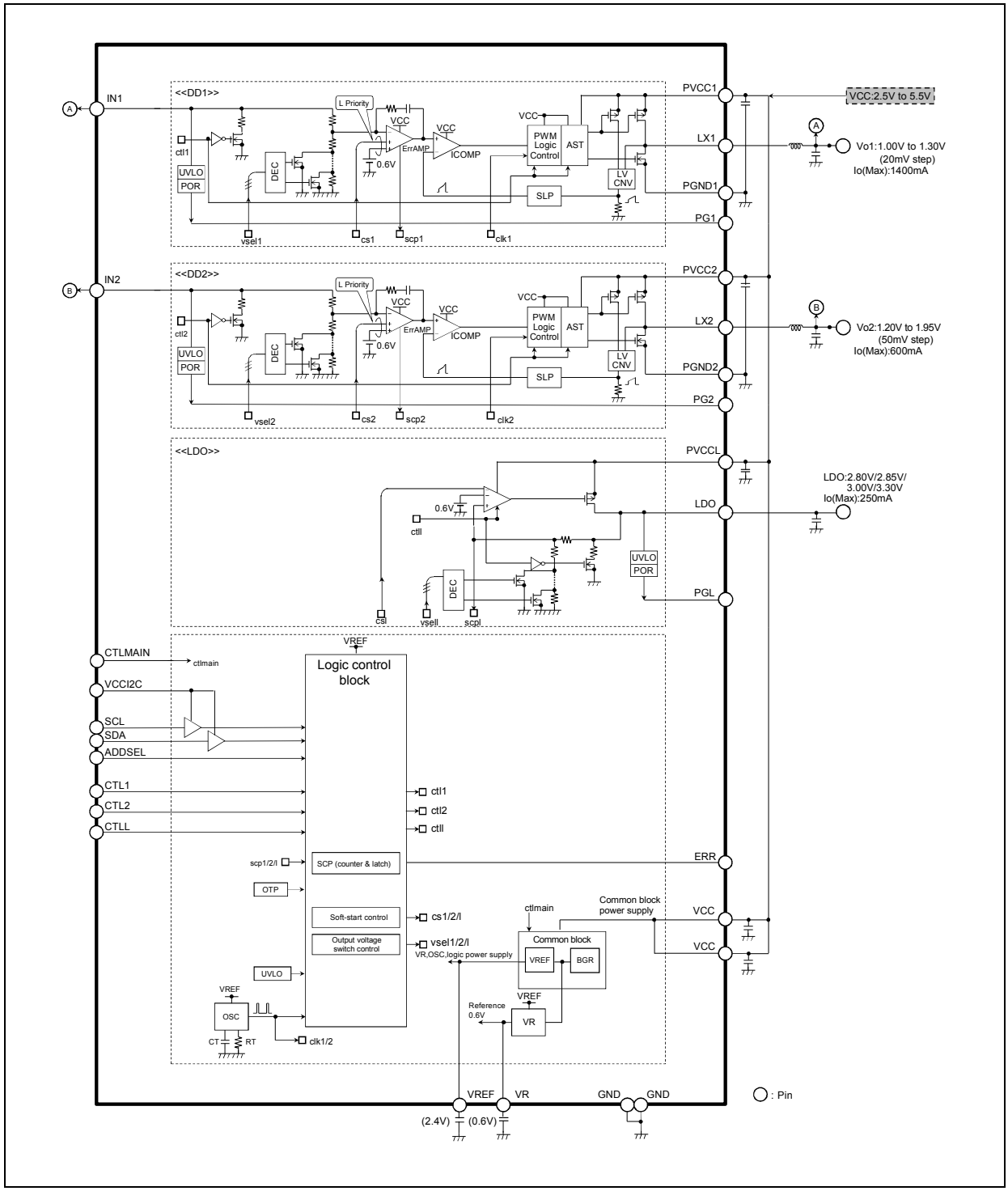
4. Pin Descriptions (PKG)

Circuit block	Pin name	Number of pin for PKG	Pin No	I/O	Description (PKG)	Pull-down resistance	PAD treatment when not using DD1	PAD treatment when not using DD2	PAD treatment when not using LDO	PAD treatment when not using I^2C communication
DD1	IN1	1	6	I	DD1·Output voltage feedback pin.	-	GND connection	-	-	-
	PVCC1	1	5	-	DD1·Output block power supply pin	-	VCC connection	-	-	-
	LX1	1	4	O	DD1·Pin for inductance connection.	-	Open	-	-	-
	PG1	1	2	O	DD1·POWERGOOD output pin	-	Open	-	-	-
	PGND1	1	3	-	DD1·Output block ground pin	-	GND connection	-	-	-
DD2	IN2	1	16	I	DD2·Output voltage feedback pin.	-	-	GND connection	-	-
	PVCC2	1	17	-	DD2·Output block power supply pin	-	-	VCC connection	-	-
	LX2	1	18	O	DD2·Pin for inductance connection.	-	-	Open	-	-
	PG2	1	20	O	DD2·POWERGOOD output pin	-	-	Open	-	-
	PGND2	1	19	-	DD2·Output block ground pin	-	-	GND connection	-	-
LDO	PVCCL	1	26	-	LDO·Power supply pin	-	-	-	VCC connection	-
	LDO	1	25	O	LDO·Output pin	-	-	-	Open	-
	PGL	1	24	O	LDO·POWERGOOD output pin	-	-	-	Open	-
CTL	CTL1	1	1	I	DD1 Control pin	❍	Open	-	-	-
	CTL2	1	21	I	DD2 Control pin	❍	-	Open	-	-
	CTLL	1	23	I	LDO Control pin	❍	-	-	Open	-
	CTLMAIN	1	7	I	Control pin for common block and digital block *	❍	-	-	-	-
ERR	ERR	1	27	O	ERR signal output pin	-	-	-	-	-

Circuit block	Pin name	Number of pin for PKG	Pin No	I/O	Description (PKG)	Pull-down resistance	PAD treatment when not using DD1	PAD treatment when not using DD2	PAD treatment when not using LDO	PAD treatment when not using I^2C communication
I^2C	VCCI2C	1	9	-	Power supply pin for I^2C.	-	-	-	-	GND connection
	SCL	1	10	I	I^2C clock pin	×	-	-	-	Open
	SDA	1	11	I/O	I^2C data I/O pin	×	-	-	-	Open
	ADDSEL	1	12	I	Switch pin for slave address	❍	-	-	-	Open
Common	VCC	2	8, 28	-	Control circuit block power supply pin	-	-	-	-	-
	VREF	1	15	O	Reference voltage (2.4V) output pin	-	-	-	-	-
	VR	1	14	O	Reference voltage (0.6V) output pin	-	-	-	-	-
	GND	2	13, 22	-	Control circuit block ground pin	-	-	-	-	-
-	GND	1	EP	-	Ground pin	-	-	-	-	-

*: When turning on DD1, DD2 and LDO, it is also necessary to set CTLMAIN to "H". See ■OPERATION MODE LIST for the details.

5. Block Diagram



6. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC, PVCC1, PVCC2, PVCCL, VCCI2C pins	-	7	V
Input voltage	V_{CTL}	CTLMAIN, 1, 2, L pins	-	7	V
	V_{OUT}	IN1, IN2 pins	-	7	V
	Vlogic	SDA, SCL pins	-	7	V
LX voltage	V_{LX}	LX1, LX2 pins	-0.3	+7	V
Power dissipation	P_D	Ta ≤ +25°C Thermal resistor value (θj-a):(50°C/W*)	-	1720	mW
Maximum junction temperature	T_{jmax}	-	-	+125	°C
Storage temperature	T_{STG}	-	-55	+125	°C

*: When mounted on a QFN28 (LCC-28P-M70) PKG, 4layers 0.8mm thickness 117mm × 84mm

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

7. Recommended Operating Conditions

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
General	Power supply voltage	V_{CC}	VCC pin	2.5	3.6	5.5	V
	Reference voltage output current	I_{REF}	VREF pin	-1	-	0	mA
		I_R	VR pin	-1	-	0	µA
	Operating temperature	Ta	-	-30	+25	+85	°C
DC/DC CH	Power supply voltage	V_{CC}	VCC, PVCC1, PVCC2 pins	2.5	3.6	5.5	V
	Input voltage	V_{OUT}	IN1, IN2 pins	0	-	VCC	V
LDO CH	Power supply voltage	V_{CC}	VCC, PVCCL pins Output voltage setting: default (3.3V)	3.5	3.6	5.5	V
CTL block	Input voltage	V_{CTL}	CTL* pin	0	-	VCC	V
Digital block (I^2C)	Power supply voltage	V_{CC}	VCCI2C pin	1.76	-	3.37	V
	Logic input voltage	Vlogic	SDA, SCL pin	0	-	VCCI2C	V

*: CTLMAIN, CTL1, CTL2, CTLL

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

8. Electrical Characteristics

Common Block

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Reference Voltage Block [VR, VREF]	Output voltage	V_R	VR pin =0mA	0.594	0.600	0.606	V
		V_{REF1}	VREF pin =0mA	2.376	2.400	2.424	V
		V_{REF2}	VCC pin =2.5V to 5.5V	2.370	2.400	2.430	V
		V_{REF3}	VREF pin =0mA to -1mA	2.370	2.400	2.430	V
Under Voltage Lockout Protection Circuit Block [VCC UVLO]	Threshold voltage	V_{TH}	VCC pin = 	2.156	2.20	2.244	V
	Hysteresis width	V_H	-	-	0.20	-	V
Over Current Protection Circuit Block [OCP]	Timer time	t_{OCP1}	DD1, DD2, LDO Default value	0.5	1	1.5	ms
Thermal shutdown Protection Circuit Block [TSD]	Stop temperature	T_{TSDH}	-	-	150*	-	°C
Control Block (CTL) [CTL]	Input voltage	V_{IH}	CTL* pin	VCC × 0.7	-	VCC	V
		V_{IL}	CTL* pin	0	-	0.4	V
	Input current	I_{CTLH}	CTL* pin =3.6V	2.7	3.6	5.1	µA
		I_{CTLL}	CTL* pin =0V	-	-	1	µA
	Input pull-down resistor	R_P	CTL* pin	-	1	-	MΩ
General (DC/DC block)	Power supply current	I_{VCCS1}	CTL* pin =0V	-	0	1.0	µA
		I_{VCCS2}	CTLMAIN=3.6V CTL1, CTL2.L pins =0V	-	80	120	µA
		I_{VCC}	CTLMAIN, L pins =3.6V Only LDO operation No load	-	200	300	µA
		I_{VCC}	CTL* pin = 3.6V all CH No load (DD operation mode: PFM/PWM mode)	-	450	680	µA
		I_{VCC}	CTL* pin = 3.6V all CH No load (DD operation mode: Fixed PWM mode)	-	10.8	16.2	mA
		I_{VCCI2C}	CTLMAIN, L pin=3.6V VCCI2C pin = 1.8V	-	7.2	12.0	µA

*: These are not the rated values. Use these values as reference when planning.

DD1, DD2

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
DC/DC Converter Block [DD1]	Output voltage	V_{OUT}	Output voltage setting: 1.2V IOUT=-10mA	1.186	1.20	1.214	V
	Input stability	V_{LINE}	IOUT=-10mA, VCC=2.5V to 5.5V	-5	-	+5	mV
	Load stability	V_{LOAD}	IOUT=-1mA to -1400mA (when in Fixed PWM mode)	-10	-	-	mV
			IOUT=-1mA to -1400mA (when in PFM/PWM mode)	-10	-	+15	mV
	IN1 pin input impedance	R_{IN}	IN1 pin=1.5V output voltage setting: 1.2V	-	400	-	kΩ
	SW PMOS-Tr ON resistance	R_{PMOS}	LX1 pin=-30mA	-	0.12*	-	Ω
	SW NMOS-Tr ON resistance	R_{NMOS}	LX1 pin= 30mA	-	0.09*	-	Ω
	SW PMOS-Tr leak current	I_{LEAK}	LX1 pin=0V	-1	-	-	µA
	SW NMOS-Tr leak current	I_{LEAK}	LX1 pin=3.6V	-	-	1	µA
	Overcurrent protection value	I_{LIMIT}	L=1.5µH	2000	-	-	mA
	PFM/PWM reshuffling electric current	I_{PFM}	L=1.5µH	-	40*	-	mA
	Discharge resistor	R_{DIS}	-	-	5	-	kΩ
	Soft-start time	t_{SS}	Preset value	0.8	0.9	1.0	ms
	Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
DC/DC Converter Block [DD2]	Output voltage	V_{OUT}	Output voltage setting: 1.8V IOUT=-10mA	1.778	1.80	1.822	V
	Input stability	V_{LINE}	IOUT=-10mA VCC=2.5V to 5.5V	-5	-	+5	mV
	Load stability	V_{LOAD}	IOUT=-1mA to -600mA (when in Fixed PWM mode)	-10	-	-	mV
			IOUT=-1mA to -600mA (when in PFM/PWM mode)	-10	-	+20	mV
	IN2 pin input impedance	R_{IN}	IN2 pin =2.0V Output voltage setting: 1.8V	-	300	-	kΩ
	SW PMOS-Tr ON resistance	R_{PMOS}	LX2 pin =-30mA	-	0.16*	-	Ω
	SW NMOS-Tr ON resistance	R_{NMOS}	LX2 pin = 30mA	-	0.14*	-	Ω
	SW PMOS-Tr leak current	I_{LEAK}	LX2 pin =0V	-1	-	-	µA
	SW NMOS-Tr leak current	I_{LEAK}	LX2 pin =3.6V	-	-	1	µA
	Overcurrent protection value	I_{LIMIT}	L=1.5µH	900	-	-	mA
	PFM/PWM reshuffling electric current	I_{PFM}	L=1.5µH	-	70*	-	mA
	Discharge resistor	R_{DIS}	-	-	5	-	kΩ
	Soft-start time	t_{SS}	Preset value	0.8	0.9	1.0	ms
	Switching frequency	f_{OSC}	-	2.7	3.0	3.3	MHz

*: These are not the rated values. Use these values as reference when planning.

LDO

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
LDO Block [LDO]	Output voltage	V_{OUT}	Output voltage setting : 3.3V IOUT=-10mA	3.241	3.300	3.359	V
	I/O voltage difference	V_{DIF}	IOUT=-10mA	-	-	0.20	V
	Input stability	V_{LINE}	IOUT=-10mA, VCC=3.5V to 5.5V	-5	-	+5	mV
	Load stability	V_{LOAD}	IOUT=-1mA to -150mA	-30	-20	-	mV
	Ripple remove ratio	RR	PVCCL=0.2Vrms, f=10Hz, IOUT=-150mA	35	75	-	dB
			PVCCL=0.2Vrms, f=10kHz, IOUT=-150mA	15	50	-	dB
	Overcurrent protection value	I_{LIMIT}	Vout×0.9	300	-	-	mA
	Control macro consumption current	I_{PVCCLS}	At stand-by	-	0	1	µA
		I_{PVCCL}	IOUT=0mA	-	80	105	µA
	Discharge resistor	R_{DIS}	-	-	5	-	kΩ
	Soft-start time	t_{SS}	Preset value	2.4	2.7	3.0	ms

Digital Block

(Ta=+25°C, VCC=PVCC1, PVCC2, L=3.6V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
POWER-GOOD Block [Power Good]	Output voltage	V_{OL}	PG1, PG2, L pins I_{OL}=1mA	-	-	0.4	V
	Output current	I_{OL}	PG1, PG2, L pins	1	-	-	mA
	Low-voltage detection	V_{th}	IN1, IN2, LDO pins = ↓	-	Vo × 0.75*	-	V
	Power-on detection voltage	V_{th}	IN1, IN2, LDO pins = ↑	-	Vo × 0.85*	-	V
Error Block [ERR]	Output voltage	V_{OL}	ERR pin I_{OL} = 1mA	-	-	0.4	V
	Output current	I_{OL}	ERR pin	1	-	-	mA
I^2C Block [I^2C]	Input voltage	V_{IH}	SCL, SDA pins VCCI2C=3.3V	VCCI2C × 0.7	-	VCCI2C	V
		V_{IL}	SCL, SDA pins VCCI2C=3.3V	0	-	VCCI2C × 0.3	V
	Input current	I_{IH}	SCL, SDA pins VCCI2C=3.3V	-	-	10	µA
		I_{IL}	SCL, SDA pins VCCI2C=3.3V	-10	-	-	µA
	Output voltage	V_{OL}	SDA pin I_{OL} =3mA	-	-	0.4	V
	Output current	I_{OL}	SDA pin	3	-	-	mA
	Input pull-down resistor	R_P	ADDSEL pin	-	1	-	MΩ

*: These are not the rated values. Use these values as reference when planning.

9. Operation Mode List

	Mode	Stand-by	Stand-by 2	General	ERR detection
CTL Signal	CTLMAIN (External)	L	H	H	H
	CTL1 (External / I^2C)	L	L	H/L	X
	CTL2 (External / I^2C)	L	L	H/L	X
	CTLL (External / I^2C)	L	L	H/L	X
Operation Block	General	OFF	ON	ON	ON
	Digital Block	OFF	ON	ON	ON
	OSC, VR Block	OFF	OFF	ON*2	OFF
	DD1	OFF	OFF	ON/OFF	OFF
	DD2	OFF	OFF	ON/OFF	OFF
	LDO	OFF	OFF	ON/OFF	OFF
I^2C Communication	I^2C communication	Disabled	Enabled	Enabled	Enabled
Protection Operating	Thermal shutdown Protection (TSD)	Not available	Not available	Available	*1
	Over Current Protection (OCP)	Not available	Not available	Available	*1

*1:This is the state after detection of ERR. It is possible to release the ERR detection mode by turning the power supply on again or turning CTLMAIN on again.

*2:When only LDO is operating, the OSC block stops (OFF) after LDO activation. Also, the VR block keeps operating (ON) after LDO activation.

■ Priority of the external pin/I^2C communication for CTL1, CTL2 and L

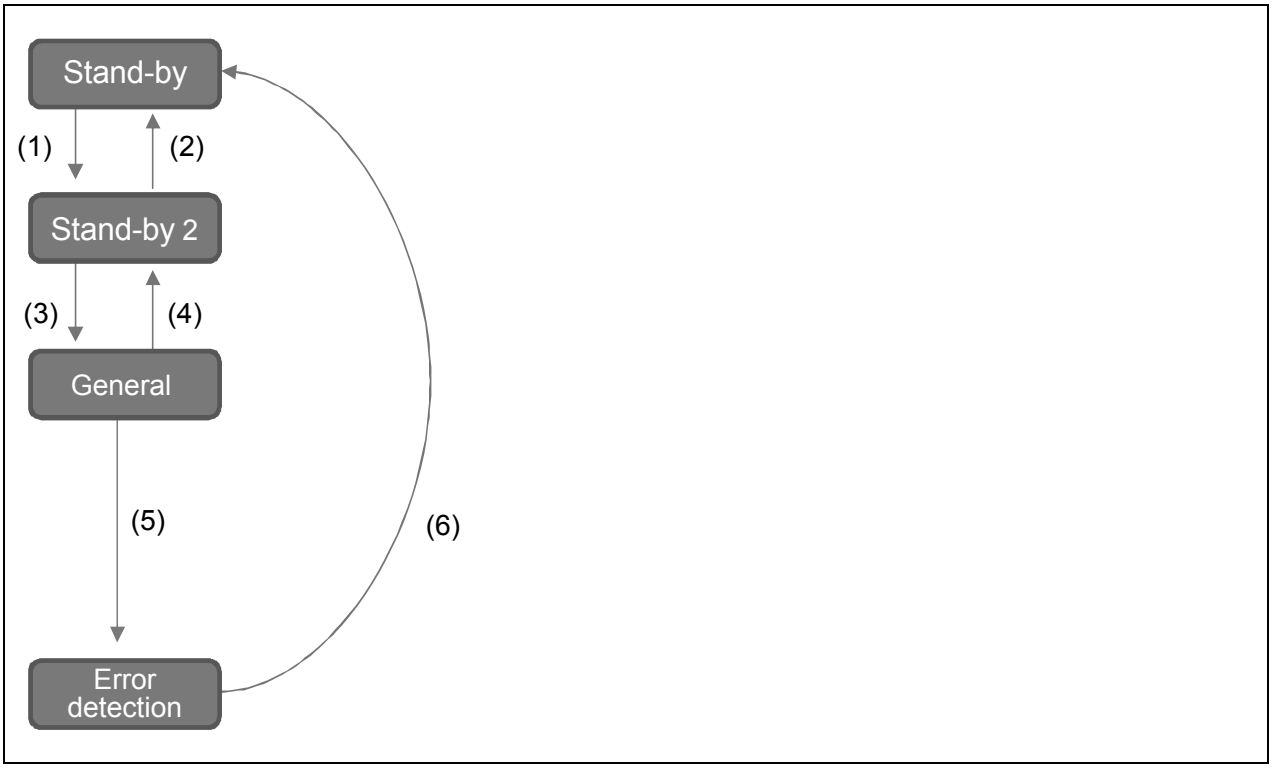
CTLMAIN (External pin)	CTL* (External pin)	CTL* (I^2C communication)	Relevant CH
H	H	H	Unavailable
H	H	L	ON
H	L	H	ON
H	L	L	OFF
L	X	Communication disabled	OFF

■ *:The I^2C communication is enabled after the common block and digital block activation setting the external CTLMAIN pin to "H".

■ When executing the ON/OFF control for DD1, DD2 and LDO using the external pin, don't execute the ON/OFF control using I^2C. Aside from the ON/OFF control, it is possible to control everything else using I^2C.

■ When executing the ON/OFF control for DD1, DD2 and LDO using I^2C, input "L" to the CTL* pin (the pin is open or in the GND connection condition).

10. State Transition Diagram



(1)External CTLMAIN pin "H"

(2)External CTLMAIN pin "L"

(3)External CTL pin "H" / I^2C communication "relevant CH_ON"

(4)External CTL pin "L" / I^2C communication "relevant CH_OFF"

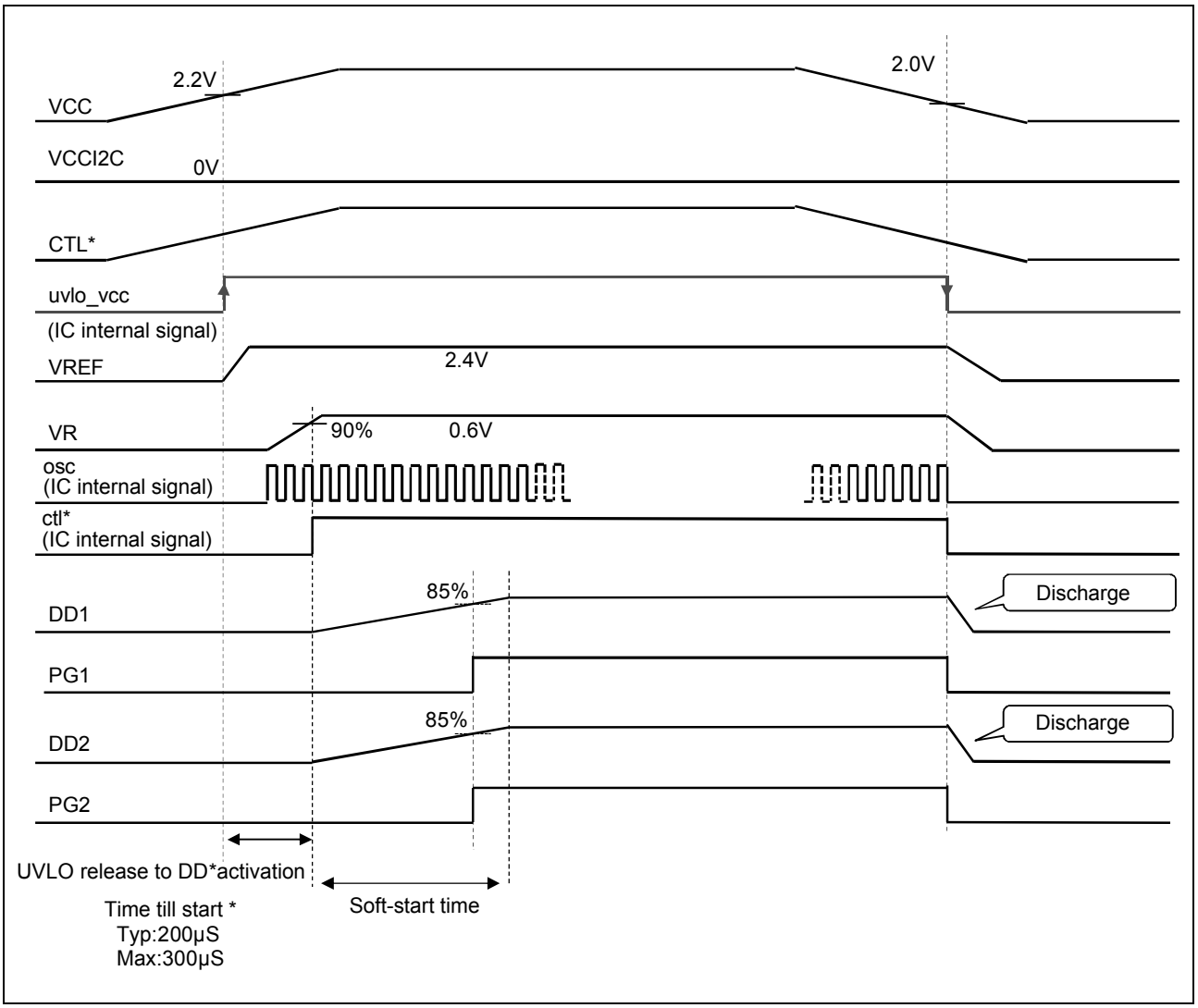
(5)Error detection (OCP, OCP_1ms continuation)

(6)Turning on the power supply again (equal to or less than uvlo_vcc reset voltage) or setting CTLMAIN to "L"

Notes:

- When executing the ON/OFF control for DD1, DD2 and LDO using the external pin, don't execute the ON/OFF control using I^2C. Aside from the ON/OFF control, it is possible to control everything else using I^2C.
- When executing the ON/OFF control for DD1, DD2 and LDO using I^2C, input "L" to the CTL* pin (the pin is open or in the GND connection condition).

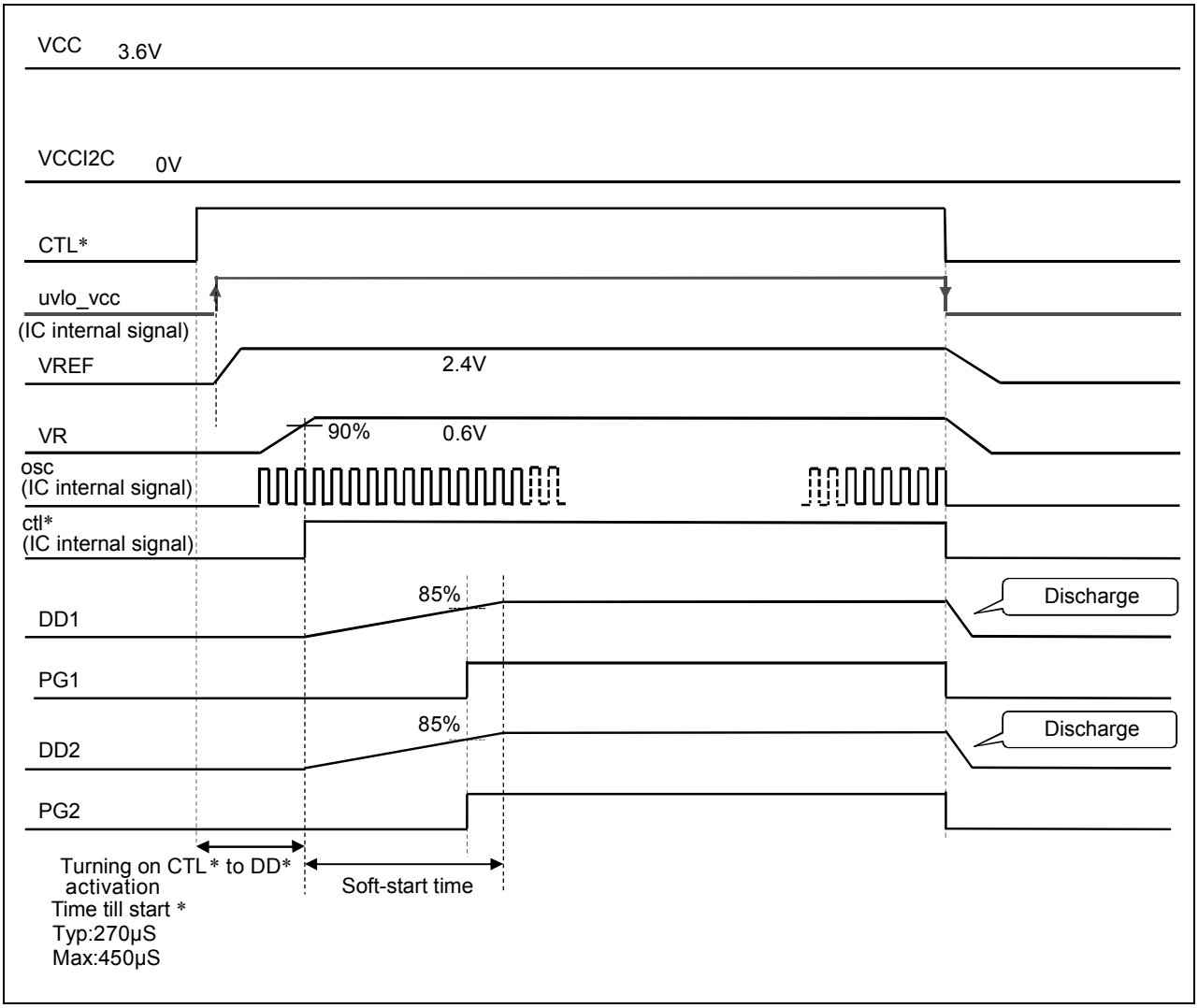
11. Turning On and Off Sequence (Turning On CTL*:CTL1, CTL2, CTLMAIN=VCC Simultaneously)



*:VREF and VR activations depend on the VREF pin capacitance and VR pin capacitance.
Time in the sequence figure above is applied for the following condition.

- VREF pin capacitance : 0.1µF
- VR pin capacitance : 0.47µF

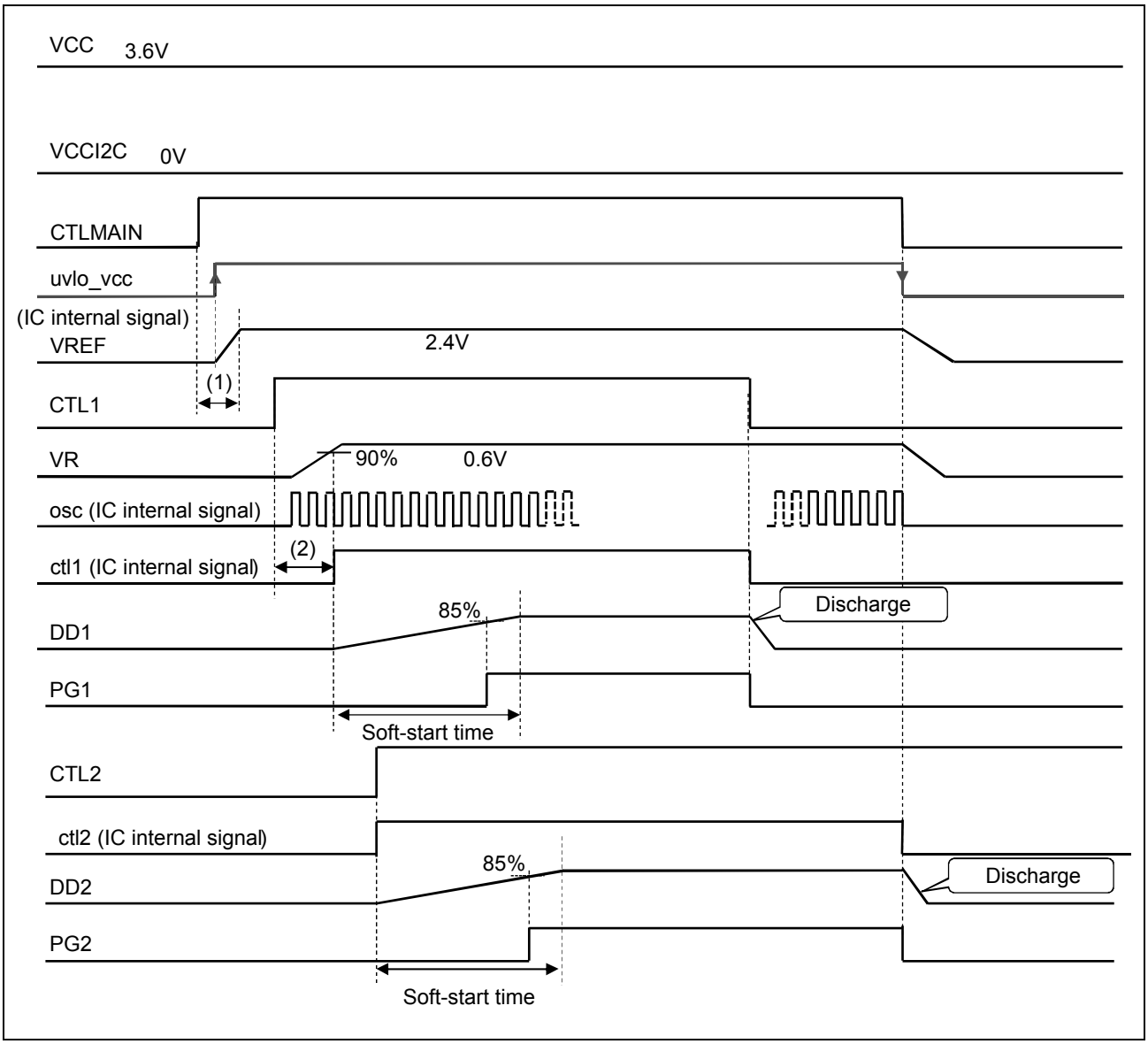
12. CTL* Turning On and Off Sequence 1 (VCC → CTL*: CTL1, CTL2, CTLMAIN)



*:VREF and VR activations depend on the VREF pin capacitance and VR pin capacitance.
Time in the sequence figure above is applied for the following condition.

- VREF pin capacitance : 0.1µF
- VR pin capacitance : 0.47µF

13. CTL* Turning On and Off Sequence 2(VCC→CTLMAIN→CTL1→CTL2)



(1) Time from turning on CTLMAIN to VREF activation completion (=communication enabled)*
Typ: 130µS, Max: 200µS

(2) Time from turning on CTL1 to ctll (IC internal signal) "H"

Typ: 150µS, Max: 250µS

*:VREF and VR activations depend on the VREF pin capacitance and VR pin capacitance.
Time in the sequence figure above is applied for the following condition.

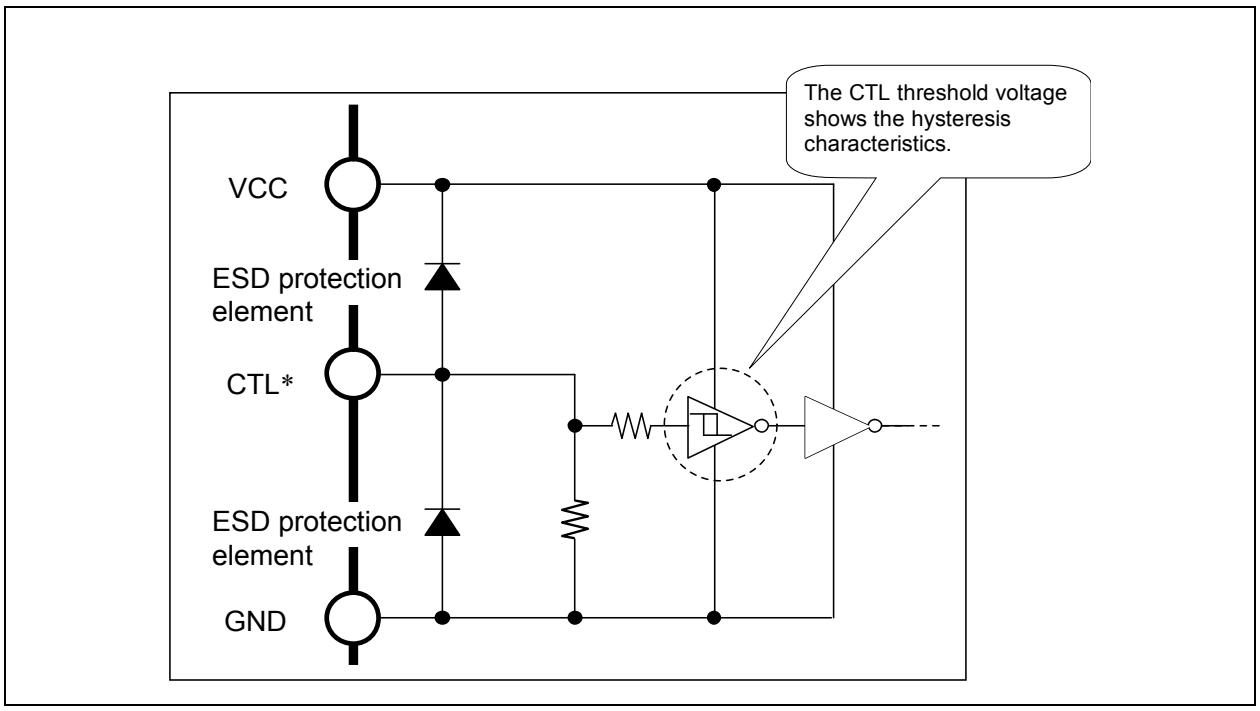
- VREF pin capacitance : 0.1µF
- VR pin capacitance : 0.47µF

14. CTL* Pin Threshold Voltage

The input circuit structure for the CTL* pin is the schmitt trigger style, and the threshold voltage shows the hysteresis characteristics when CTL* OFF → ON and ON → OFF. (See "･CTL* pin equivalent circuit diagram" below.)

Also, the threshold voltage level depends on the VCC pin voltage.
Moreover, make sure to input either the "H" level (>"VCC×0.7"V) or "L" level (<0.4V) to the CTL* pin when in use.

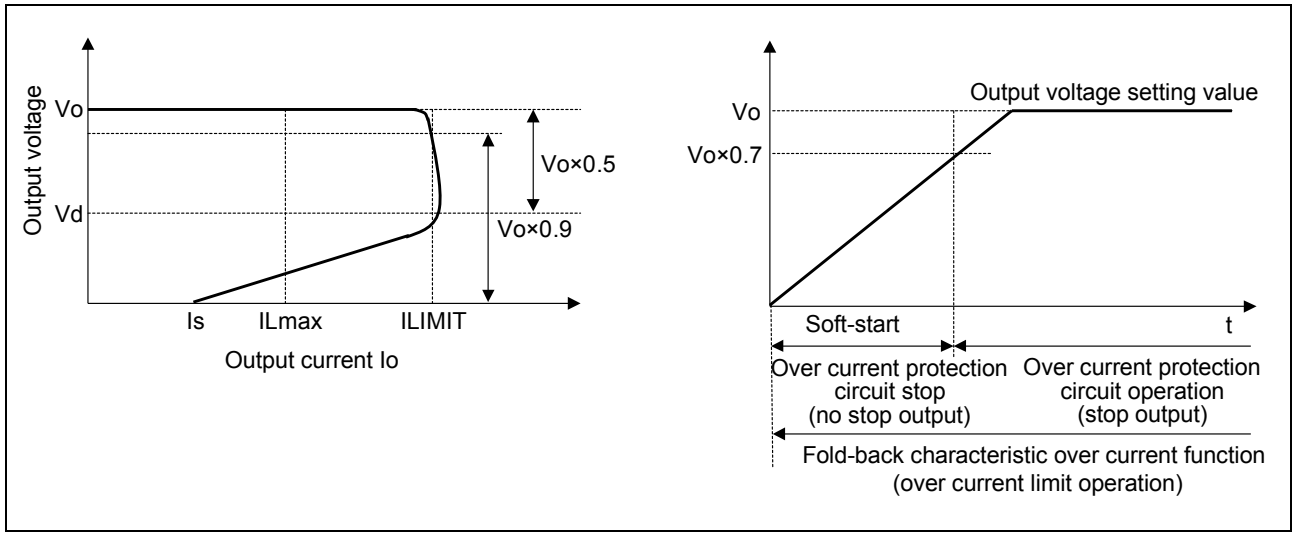
CTL* pin equivalent circuit diagram



15. Protection Operation Sequence

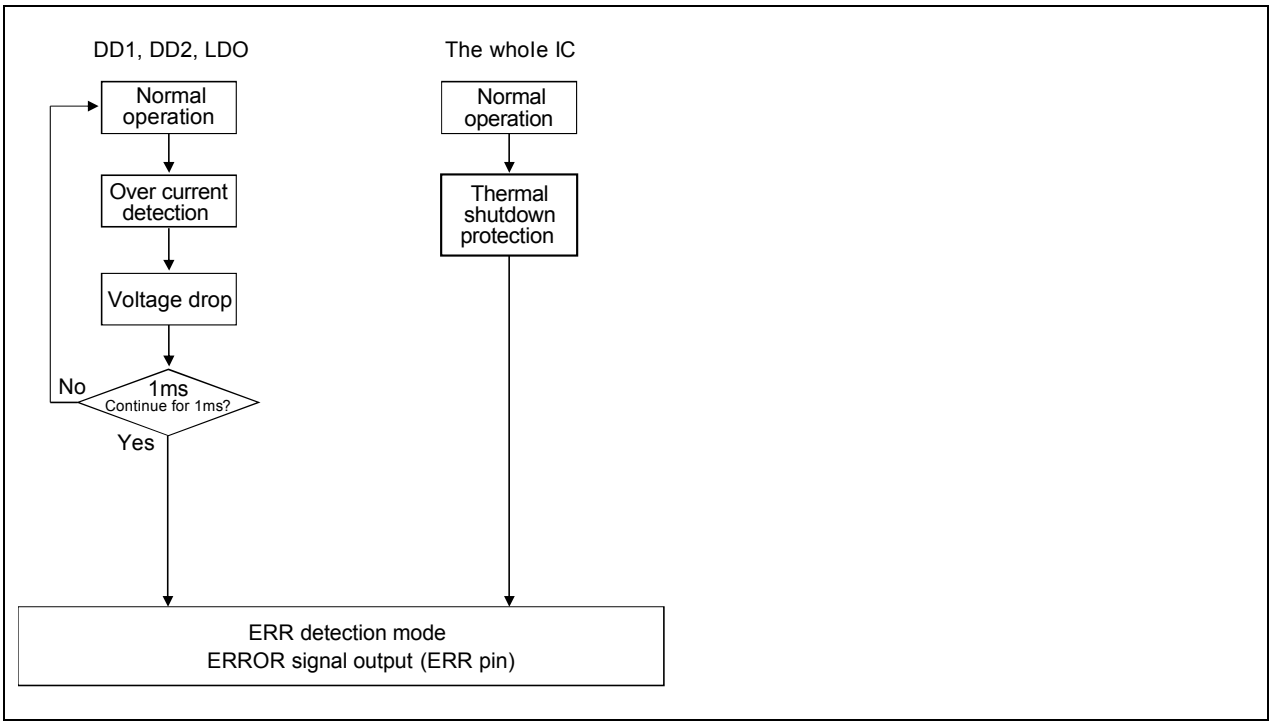
DD channel
The DD channel monitors the FET current peak value at any time during the operation. When the DD output becomes the over current state, the output voltage is decreased. Afterward, the timer operation is performed and the output stops after about 1ms progress.

LDO channel
It contains the fold-back type over current protection circuit in order to prevent destroy because of the over load and the output over current. It limits the output current and the output voltage from the peak around the over current protection value for LDO (ILIMIT) to the over current current (Is).
At this time, if the output voltage Vo gets lower than the detection voltage Vd (Vd: Vo×0.5), the timer operation starts and the output stops after about 1ms progress. Moreover, because the over current protection circuit does not operate at the soft-start (0V to Vo × 0.7), neither the output stops nor the error signal outputs. However, the fold-back type over current protection characteristic functions. The following shows the fold-back type over current protection characteristic.



Thermal shutdown protection
If the temperature at the junction part reaches +150°C, the thermal shutdown protection circuit turns all channels off.

Error detection sequence



ERR detection mode release

It is necessary to turn the power supply on again, or to turn CTLMAIN on again to release the ERR detection mode.