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FUJITSU MICROELECTRONICS
DATA SHEET

DS04-27261-6E

ASSP for Power Management Applications of Ultra Mobile PC

6ch DC/DC Converter IC for LPIA Platform VR

MB39C308

■ DESCRIPTION

The MB39C308 is a 6ch DC/DC buck converter LSI, which integrates all of necessary power supplies for Ultra-Mobile PC powered by 2-cell Li-ion battery. And the MB39C308 uses current mode topology with N-channel synchronous rectification to realize high conversion efficiency.
The MB39C308 is the Power Management IC supporting the LPIA(Low Power Intel Architecture) which Intel Corporation proposes as the low power consumption platform for UMPC.

The CH1 and CH2 are flexible to adopt the output current capability by selection of external FETs and easy to optimize efficiency. The CH3, CH4, CH5 and CH6 integrate the switching FETs capable of high current for down-sizing the power supply solution.

The MB39C308 uses Fujitsu's LDMOS process technology and supplies all power without dispersing power from a lithium-ion battery.

■ FEATURES

- Input voltage range : 5.5 V to 12.6 V
- Topology : Current Mode
- Integrated FET Driver for external MOSFETs : CH1, CH2
- Integrated Switching MOSFETs : CH3, CH4, CH5, CH6
- Fixed Preset Output Voltage : CH1, CH2, CH5
- Selectable Preset Output Voltage : CH3, CH4, CH6

Channel	Output voltage	Output current	Remarks
CH1	5 V	2 A*	—
CH2	3.3 V	4.5 A*	—
CH3	1.8 V/1.5 V	Max : 2.7 A	DDR2/DDR3 are selectable.
CH4	0.9 V/0.75 V	Max : 1.5 A	
CH5	1.5 V	Max : 2.5 A	—
CH6	1.1 V/1.05 V	Max : 3.5 A	Two values are selectable.

* : It is the reference value at the typical EVB.

(Continued)

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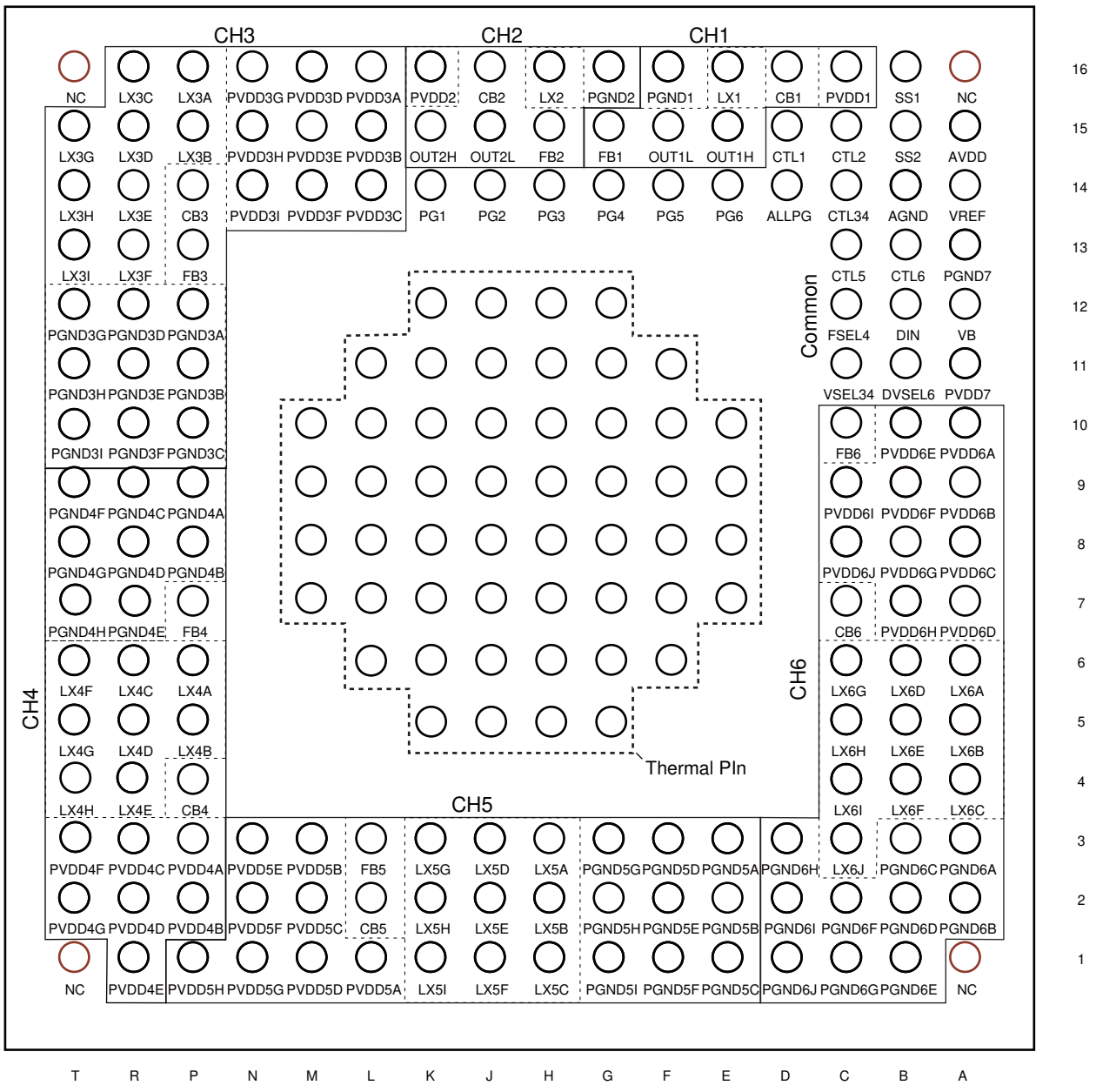
- PWM switching frequency : 0.7 MHz
  (CH4 : 0.7 MHz/0.35 MHz)
- Various protection
  - Over current protection (OCP)
  - Input over voltage protection (IVP)
  - Output short circuit protection (SCP)
  - Under voltage lock out protection (UVLO)
  - Output over voltage protection (OVP)
  - Over temperature protection (OTP)
- POWERGOOD function
- Soft start function independent from output loads.
- Soft stop function independent from output loads.
- High conversion efficiency in wide range of load current.
- Packaged in a compact package : PFBGA-208 (9.00 mm × 9.00 mm × 1.30 mm)

■ APPLICATIONS

- UMPC (Ultra Mobile PC)
- MID (Mobile Internet Device)
- Mobile equipment etc.

■ PIN ASSIGNMENT

(BOTTOM VIEW)



(BGA-208P-M02)(156-pin + Thermal 52-pin)

■ PIN DESCRIPTIONS

Block	Pin Name	I/O	Description
CH1	FB1	I	CH1 Error amplifier input pin, being connected to output of CH1.
	PVDD1	—	Power supply pin of the CH1 output block.
	CB1	O	Internal power supply pin of the CH1 gate driver block.
	LX1	—	CH1 inductor connection pin.
	OUT1H	O	CH1 High-side N-ch FET drive output pin.
	OUT1L	O	CH1 Low-side N-ch FET drive output pin.
	PGND1	—	Ground pin of the CH1 output block.
CH2	FB2	I	CH2 Error amplifier input pin, being connected to output of CH2.
	PVDD2	—	Power supply pin of the CH2 output block.
	CB2	O	Internal power supply pin of the CH2 gate driver block.
	LX2	—	CH2 inductor connection pin.
	OUT2H	O	CH2 High-side N-ch FET drive output pin.
	OUT2L	O	CH2 Low-side N-ch FET drive output pin.
	PGND2	—	Ground pin of the CH2 output block.
CH3	FB3	I	CH3 Error amplifier input pin, being connected to output of CH3.
	PVDD3A to PVDD3I	—	Power supply pins of the CH3 output block.
	CB3	O	Internal power supply pin of the CH3 gate driver block.
	LX3A to LX3I	—	CH3 inductor connection pins.
	PGND3A to PGND3I	—	Ground pins of the CH3 output block.
CH4	FB4	I	CH4 Error amplifier input pin, being connected to output of CH4.
	PVDD4A to PVDD4G	—	Power supply pins of the CH4 output block.
	CB4	O	Internal power supply pin of the CH4 gate driver block.
	LX4A to LX4H	—	CH4 inductor connection pins.
	PGND4A to PGND4H	—	Ground pins of the CH4 output block.

(Continued)

Block	Pin Name	I/O	Description
CH5	FB5	I	CH5 Error amplifier input pin, being connected to output of CH5.
	PVDD5A to PVDD5H	—	Power supply pins of the CH5 output block.
	CB5	O	Internal power supply pin of the CH5 gate driver block.
	LX5A to LX5I	—	CH5 inductor connection pins.
	PGND5A to PGND5I	—	Ground pins of the CH5 output block.
CH6	FB6	I	CH6 Error amplifier input pin, being connected to output of CH6.
	PVDD6A to PVDD6J	—	Power supply pins of the CH6 output block.
	CB6	O	Internal power supply pin of the CH6 gate driver block.
	LX6A to LX6J	—	CH6 inductor connection pins.
	PGND6A to PGND6J	—	Ground pins of the CH6 output block.
Common	CTL1	I	CH1 Control input pin. (L : Standby / H : Normal operation)
	CTL2	I	CH2 Control input pin. (L : Standby / H : Normal operation)
	CTL34	I	CH3 and CH4 control input pin. (L : Standby / H : Normal operation)
	CTL5	I	CH5 Control input pin. (L : Standby / H : Normal operation)
	CTL6	I	CH6 Control input pin. (L : Standby / H : Normal operation)
	PG1	O	CH1 POWERGOOD output pin. (N-ch MOS open drain output)
	PG2	O	CH2 POWERGOOD output pin. (N-ch MOS open drain output)
	PG3	O	CH3 POWERGOOD output pin. (N-ch MOS open drain output)
	PG4	O	CH4 POWERGOOD output pin. (N-ch MOS open drain output)
	PG5	O	CH5 POWERGOOD output pin. (N-ch MOS open drain output)
	PG6	O	CH6 POWERGOOD output pin. (N-ch MOS open drain output)
	ALLPG	O	POWERGOOD output pin (The ALLPG pin outputs “H”, When channels CH3, CH4, CH5 and CH6 are the power good).
	FSEL4	I	CH4 switching frequency setting pin. FSEL4 = “H” : 700 kHz FSEL4 = “L” : 0.35 MHz (Shown in the “■ ELECTRICAL CHARACTERISTICS”)

(Continued)

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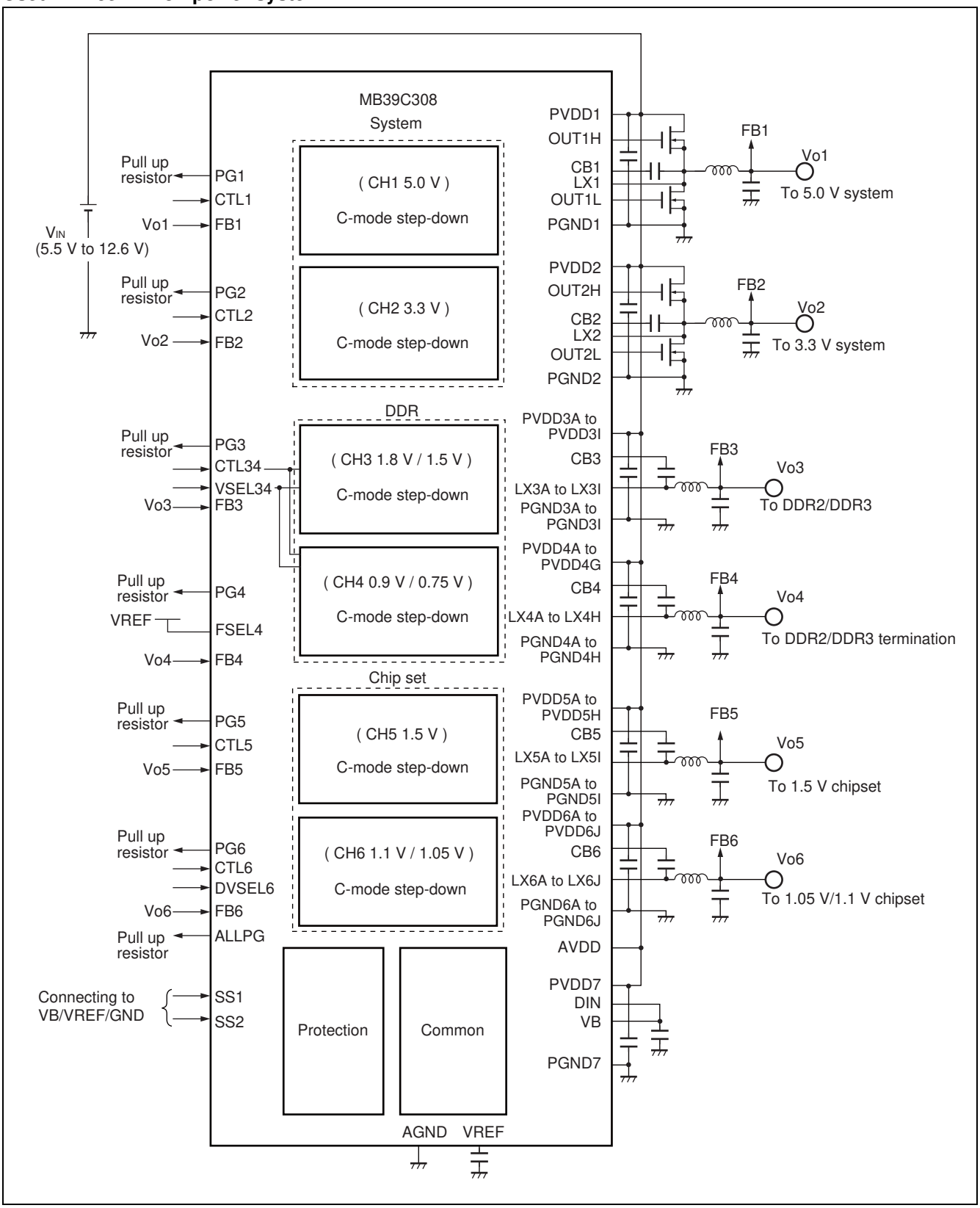
Block	Pin Name	I/O	Description
Common	VSEL34	I	Preset output voltage setting pin for CH3/CH4. VSEL34 = “H” : Vout_CH3 =1.8 V, Vout_CH4 = 0.9 V VSEL34 = “L” : Vout_CH3 =1.5 V, Vout_CH4 = 0.75 V
	DVSEL6	I	Preset output voltage setting pin for CH6 dynamically. DVSEL6 = “H” : Vout_CH6 = 1.1 V DVSEL6 = “L” : Vout_CH6 = 1.05 V
	SS1	I	Soft-Start and Soft-Stop time setting pin (Shown in the “■ DESCRIPTION OF SOFT-START AND SOFT-STOP OPERATION • Soft-Start/Soft-Stop time (tson/tsoff) Setting Conditions”).
	SS2		
	VB	O	Bias voltage output pin for bootstrap and low-side N-ch gate driver of all channels.
	DIN	I	Bias voltage input pin for bootstrap. DIN pin should be connected with VB pin. (Shown in the “■ BLOCK DIAGRAM”)
	PVDD7	—	Power supply pin of VB block.
	PGND7	—	Ground pin of VB block.
	AVDD	—	Power supply pin for common block.
	VREF	O	Reference voltage output pin.
	AGND	—	Ground pin of common block.

■ BLOCK DIAGRAM

Used in 2-cell Li-Ion power system



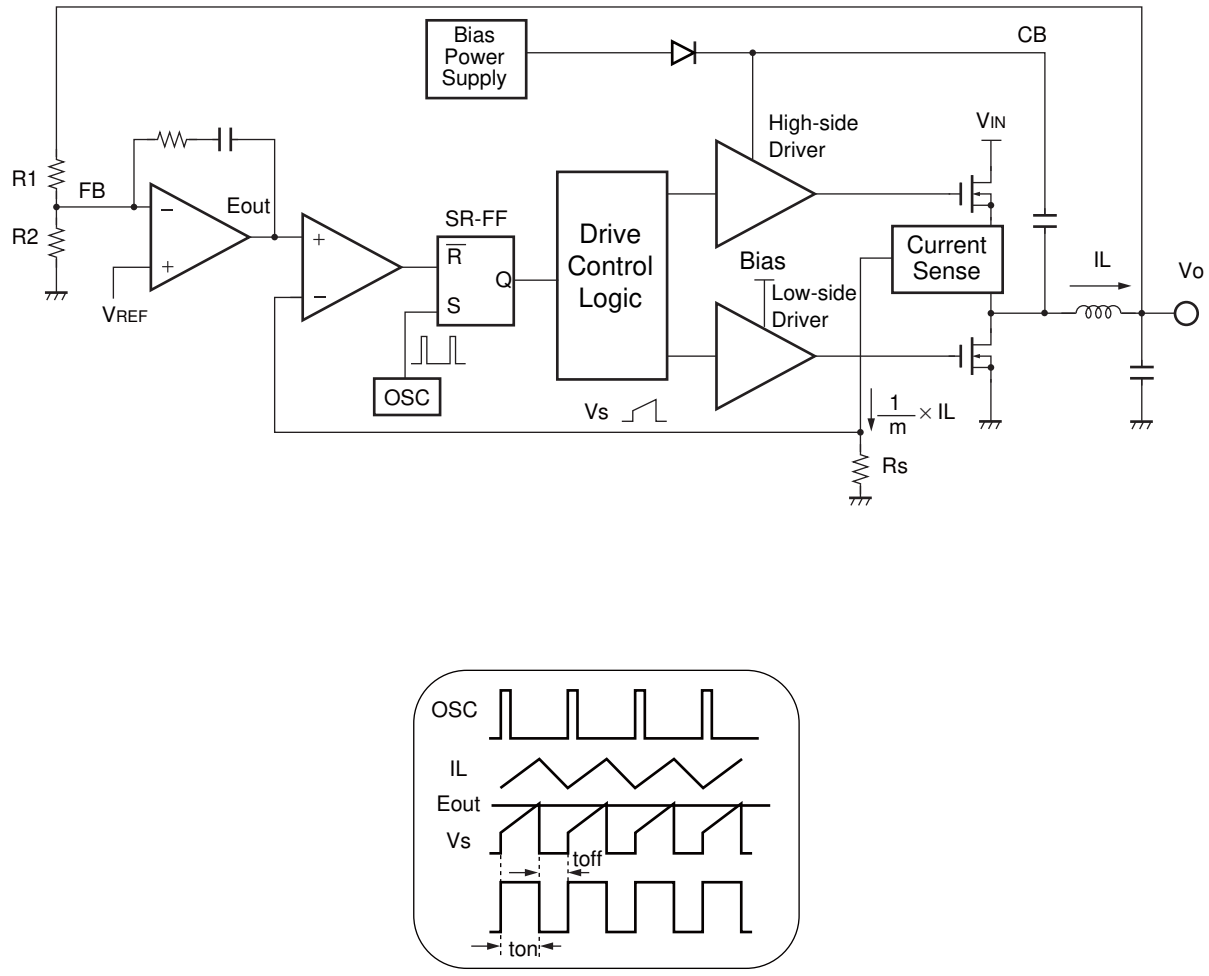
CURRENT MODE TOPOLOGY

A DC/DC regulation block of Current-mode (C-mode) is illustrated in the "• DC/DC topology, Current mode operation".

In this C-mode, the High-side FET is turned ON while the SR-FF is set at every clock cycle generated by on chip oscillator. During ON period (ton), the current is supplied by V_{IN}, then Inductor current(IL) is increased. Besides a current (IL/m), which senses the inductor current(IL), flows across a resistor (Rs) then the resister voltage (Vs) is increased. When the Vs reaches Eout , which is an output of the Error amp, the SR-FF is reset and the High-side FET is turned OFF (toff) until the next rising clock comes.

The voltage regulation is done by controlling a peak current of the inductor current (IL).

• DC/DC topology, Current mode operation



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{DD}	AVDD, PVDD1 to PVDD7 pin	–0.3	+ 13.5	V
CB voltage	V_{CB}	CB1 to CB6 pin	–0.3	+ 18.5	V
LX voltage	V_{LX}	LX1 to LX6 pin	–0.3	V_{DD}	V
CB to LX voltage	V_{CBLX}	CB pin to LX pin	–0.3	+ 7	V
OUTH voltage	V_{OUTH}	OUT1H, OUT2H pin	V_{LX} – 0.3	V_{CB}	V
OUTL voltage	V_{OUTL}	OUT1L, OUT2L pin	–0.3	+ 7	V
DIN voltage	V_{DIN}	DIN pin	–0.3	+ 7	V
VB voltage	V_{VB}	VB pin	–0.3	+ 7	V
VREF voltage	V_{VREF}	VREF pin	–0.3	+ 7	V
CTL voltage	V_{CTL}	CTL1 to CTL6 pin	–0.3	+ 13.5	V
VSEL voltage	V_{SEL}	VSEL34, DVSEL6 pin	–0.3	+ 7	V
FSEL voltage	V_{FSEL}	FSEL4 pin	–0.3	+ 7	V
FB voltage	V_{FB}	FB1 to FB6 pin	–0.3	+ 7	V
PG voltage	V_{PG}	PG1 to PG6, ALLPG pin	–0.3	+ 7	V
SS voltage	V_{SS}	—	–0.3	+ 7	V
Package power dissipation	P_D	Ta ≤ + 25 °C	—	2940*	mW
		Ta = + 85 °C	—	1180*	mW
Operating ambient temperature	Ta	—	–40	+ 85	°C
Storage temperature	T_{STG}	—	–55	+ 125	°C

* : See the diagram of "■ TYPICAL CHARACTERISTICS • Maximum Power Dissipation vs. Operating Ambient Temperature", for the package power dissipation of Ta from + 25 °C to + 85 °C.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

WARNING: The use of negative voltage below –0.3 Volts on the GND pins (AGND, PGND1 to PGND7) may activate parasitic transistors on the silicon, which can introduce abnormal operation.
Connecting the LX pin to either VDD pins (AVDD, PVDD1 to PVDD7) or GND pins (AGND, PGND1 to PGND7) directly may cause permanently damage to the device.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	AVDD = PVDD1 to PVDD7 pin	5.5	—	12.6	V
Input capacitor	C_{IN}	VDD to GND pin	—	4.7	—	µF
CB to LX capacitor	C_{CB}	CB to LX pin	—	0.1	—	µF
LX inductor	L1	LX1 pin	—	3.3	—	µH
	L2	LX2 pin	—	3.3	—	µH
	L3	LX3 pin	—	1.5	—	µH
	L4	LX4 pin, FSEL4 pin = H fosc = 0.7 MHz	—	1.5	—	µH
		LX4 pin, FSEL4 pin = L fosc = 0.35 MHz	—	1.5	—	
	L5	LX5 pin	—	1.5	—	µH
	L6	LX6 pin	—	1.5	—	µH
Output current	I_O1	Vo1 (5 V), DC, when Ron_{H1} = 32 mΩ	—	1	2*	A
	I_O2	Vo2 (3.3 V), DC, when Ron_{H2} = 16 mΩ	—	2.25	4.5*	A
	I_O3	Vo3 (1.8 V/1.5 V), DC	—	1.35	2.7*	A
	I_O4	Vo4 (0.9 V/0.75 V), DC	—	1	1.5*	A
	I_O5	Vo5 (1.5 V), DC	—	1.25	2.5*	A
	I_O6	Vo6 (1.1 V/1.05 V), DC	—	1.75	3.5*	A
Output capacitor	C_O1	Vo1 (5 V), when Ron_{H1} = 32 mΩ, L = 3.3 µH, SS1,SS2 pin = GND	—	100	300	µF
	C_O2	Vo2 (3.3 V), when Ron_{H1} = 16 mΩ, L = 3.3 µH, SS1,SS2 pin = GND	—	100	700	µF
	C_O3	Vo3 (1.8 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	100	300	µF
	C_O4	Vo4 (0.9 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	100	500	µF
	C_O5	Vo5 (1.5 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	100	300	µF
	C_O6	Vo6 (1.05 V), when L = 1.5 µH, SS1, SS2 pin = GND	—	200	500	µF
External FET On-resistance	R_{onH1}	CH1 High-side FET connected to OUT1H pin	—	32	—	mΩ
	R_{onL1}	CH1 Low-side FET connected to OUT1L pin	—	32	—	mΩ
	R_{onH2}	CH2 High-side FET connected to OUT2H pin	12	16	20	mΩ
	R_{onL2}	CH2 Low-side FET connected to OUT2L pin	—	16	—	mΩ

(Continued)

(Continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
VB output capacitor	C_{VB}	VB pin	—	1	—	µF
VREF output capacitor	C_{VREF}	VREF pin	—	4.7	—	µF
VREF output current	I_{VREF}	VREF pin	– 1	—	0	mA
PG input voltage	V_{PG}	PG1 to PG6, ALLPG pin	—	—	6	V
PG sink current	I_{PG}	PG1 to PG6, ALLPG pin	—	—	2	mA
CTL input voltage	V_{CTL}	CTL1 to CTL6 pin	—	—	AVDD	V
VSEL input voltage	V_{SEL}	VSEL34, DVSEL6 pin	—	—	6	V
FSEL input voltage	V_{FSEL}	FSEL4 pin	—	—	6	V
SS input voltage	V_{SS}	SS1, SS2 pin	—	—	V_B	V

* : The MB39C308 is designed with assumed operating conditions, which is 60% of the maximum output current on the each channel and being operated with recommended input voltage range.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Reference voltage block [VREF]	Reference voltage	V_{REF}	VREF pin = 0 mA	2.45	2.5	2.55	V
	Line regulation	VREF Line	AVDD pin = 5.5 V to 12.6 V	−10	—	+ 10	mV
	Load regulation	VREF Load	VREF pin = 0 mA to −1 mA	−15	—	+ 15	mV
Bias voltage block [VB]	Bias voltage	V_{VB}	5.5 V ≤ AVDD ≤ 12.6 V VB pin = 0 mA	4.8	5	5.2	V
	Load regulation	VB Load	VB pin = 0 mA to −1 mA	−15	—	+ 15	mV
Under-voltage lockout protection circuit block [UVLO]	Threshold voltage	V_{TLH}	AVDD pin	4.5	5.0	5.2	V
	Hysteresis width	V_{HU}	AVDD pin	0.05	0.1	0.4	V
Over-temperature protection circuit block [OTP]	Shutdown temperature	T_{OTPH}		—	+ 150*1	—	°C
	Hysteresis width	T_H		—	+ 25*1	—	°C
Input over voltage protection circuit block [IVP]	Threshold voltage	V_{IVPH}	AVDD pin	12.6	13.0	13.4	V
	Release voltage	V_{IVPL}	AVDD pin	12.5	12.85	13.3	V
	Hysteresis width	V_{HI}	AVDD pin	—	0.15	—	V
Oscillator block [OSC]	Oscillation frequency*2	fosc	CH1 to CH3, CH5, CH6 CH4 : FSEL4 pin = “H” Level	0.56	0.7	0.84	MHz
			CH4 : FSEL4 pin = “L” Level	0.28	0.35	0.42	MHz
Control block [CTL1 to CTL6]	Output on level	V_{IH}	CTL1 to CTL6 pin	2	—	—	V
	Output off level	V_{IL}	CTL1 to CTL6 pin	—	—	0.8	V
	Input current	I_{CTLH}	CTL1 to CTL6 pin = 3 V	23	30	43	µA
		I_{CTLL}	CTL1 to CTL6 pin = 0 V	—	—	1	µA

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Output voltage select block [VSEL34, DVSEL6]	VSEL34, “H” level	V_{LGH}	VSEL34, DVSEL6 pin	2	—	—	V
	VSEL34, “L” level	V_{LGL}	VSEL34, DVSEL6 pin	—	—	0.8	V
	Input current	I_{SELH}	VSEL34, DVSEL6 pin = 3 V	23	30	43	µA
		I_{SELL}	VSEL34, DVSEL6 pin = 0 V	—	—	1	µA
Power good detection circuit block [PG1 to PG6, ALLPG]	Low side threshold voltage	V_{PGL}	FB1 to FB6 pin ↓ PG1 to PG6 pin	Vo × 0.85	Vo × 0.9	Vo × 0.95	V
	High side threshold voltage	V_{PGH}	FB1 to FB6 pin ↑ PG1 to PG6 pin	Vo × 1.05	Vo × 1.1	Vo × 1.15	V
	Hysteresis width	V_H	—	—	Vo × 0.03	—	V
	PG output low voltage	V_{OL}	PG1 to PG6, ALLPG pin = 1 mA	—	0.1	0.3	V
	PG leak current	I_{LKPG}	PG1 to PG6, ALLPG pin = 6 V	—	—	1	µA
Common block	AVDD standby current	I_{AVDDS}	CTL1 to CTL6 pin = 0 V, AVDD pin = 12.6 V	—	—	1	µA
	AVDD power supply current	I_{AVDD}	CTL1 to CTL6 pin = 3 V	—	0.25	—	mA
CH1 block [CH1]	CH1 output voltage	Vo1	FB1 pin	4.75	5	5.25	V
	PVDD1 standby current	I_{PVDD1S}	CTL1 pin = 0 V, PVDD1 pin = 12.6 V	—	—	15	µA
	CH1 efficiency	ηL1	0.05 × Io (Max) < Io < 0.3 × Io (Max)	87*3	—	—	%
		ηT1	0.3 × Io (Max) < Io < 0.6 × Io (Max)	92*3	—	—	%
		ηF1	0.6 × Io (Max) < Io< Io (Max)	92*3	—	—	%
	OUT1H source current	IsourceH1	Duty ≤ 5%, CB1 pin = 5 V, LX1 pin = 0 V, OUT1H pin = 0 V	—	–400*1	—	mA
	OUT1H sink current	IsinkH1	Duty ≤ 5%, CB1 pin = 5 V, LX1 pin = 0 V, OUT1H pin = 5 V	—	400*1	—	mA
	OUT1L source current	IsourceN1	Duty ≤ 5%, VB pin = 5 V, LX1 pin = 0 V, OUT1L pin = 0 V	—	–400*1	—	mA

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH1 block [CH1]	OUT1L sink current	IsinkN1	Duty ≤ 5%, VB pin = 5 V, LX1 pin = 0 V, OUT1L pin = 5 V	—	400*1	—	mA
	OUT1H on resistance	R_{OH1}	OUT1H pin = –15 mA	—	12	18	Ω
		R_{OL1}	OUT1H pin = 15 mA	—	12	18	Ω
	OUT1L on resistance	R_{OH1}	OUT1L pin = –15 mA	—	12	18	Ω
		R_{OL1}	OUT1L pin = 15 mA	—	12	18	Ω
	Vo1 output over voltage threshold	Vo1	FB1 pin	5.9*1	6*1	6.1*1	V
	Vo1 over current limit	I_{OCP1}	Io1 Ron_{H1} = 32 mΩ, L = 3.3 μH	3.4*1	4.0*1	4.6*1	A
	FB1 input resistance	R_{FB1}	FB1 pin	—	340	—	kΩ
	Soft Start time	SS1	FB1 pin SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH2 block [CH2]	CH2 output voltage	Vo2	FB2 pin	3.135	3.3	3.465	V
	PVDD2 standby current	I_{PVDD2S}	CTL2 pin = 0 V, PVDD2 pin = 12.6 V	—	—	15	μA
	CH2 efficiency	ηL2	0.05 × Io (Max) < Io < 0.3 × Io (Max)	87*3	—	—	%
		ηT2	0.3 × Io (Max) < Io < 0.6 × Io (Max)	92*3	—	—	%
		ηF2	0.6 × Io (Max) < Io < Io (Max)	92*3	—	—	%
	OUT2H source current	IsourceH2	Duty ≤ 5%, CB2 pin = 5 V, LX2 pin = 0 V, OUT2H pin = 0 V	—	– 400	—	mA
	OUT2H sink current	IsinkH2	Duty ≤ 5%, CB2 pin = 5 V, LX2 pin = 0 V, OUT2H pin = 5 V	—	400	—	mA
	OUT2L source current	IsourceN2	Duty ≤ 5%, VB pin = 5 V, LX2 pin = 0 V, OUT2L pin = 0 V	—	– 400	—	mA
	OUT2L sink current	IsinkN2	Duty ≤ 5%, VB pin = 5 V, LX2 pin = 0 V, OUT2L pin = 5 V	—	400	—	mA
	OUT2H on resistance	R_{OH2}	OUT2H pin = –15 mA	—	12	18	Ω
		R_{OL2}	OUT2H pin = 15 mA	—	12	18	Ω
	OUT2L on resistance	R_{OH2}	OUT2L pin = –15 mA	—	12	18	Ω
		R_{OL2}	OUT2L pin = 15 mA	—	12	18	Ω

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH2 block [CH2]	Vo2 output over voltage threshold	Vo2	FB2 pin	3.894*1	3.96*1	4.026*1	V
	Vo2 over current limit	I_{OCP2}	I_O2 Ron_{H1} = 16 mΩ, L = 3.3 μH	6.7*1	7.9*1	9.0*1	A
	FB2 input resistance	R_{FB2}	FB2 pin	—	220	—	kΩ
	Soft start time	SS2	FB2 pin SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH3 block [CH3]	CH3 output voltage	Vo3	VSEL34 = "H" Level, FB3 pin	1.71	1.8	1.89	V
			VSEL34 = "L" Level, FB3 pin	1.425	1.5	1.575	V
	High-side FET on-resistance	R_{ONH3}	LX3 pin = –100 mA, V_{GS} = 5 V	—	65*1	—	mΩ
	Low-side FET on-resistance	R_{ONL3}	LX3 pin = 100 mA, V_{GS} = 5 V	—	40*1	—	mΩ
	PVDD3 standby current	I_{PVDD3S}	CTL34 pin = 0 V, PVDD3 pin = 12.6 V	—	—	15	μA
	CH3 efficiency	ηL31	VSEL34 pin = "H" Level, Vo3 = 1.8 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	85*3	—	—	%
		ηL32	VSEL34 pin = "L" Level, Vo3 = 1.5 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	82*3	—	—	%
		ηT31	VSEL34 pin = "H" Level, Vo3 = 1.8 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	87*3	—	—	%
		ηT32	VSEL34 pin = "L" Level, Vo3 = 1.5 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	85*3	—	—	%
		ηF31	VSEL34 pin = "H" Level, Vo3 = 1.8 V 0.6 × Io (Max) < Io < Io (Max)	87*3	—	—	%
		ηF32	VSEL34 pin = "L" Level, Vo3 = 1.5 V 0.6 × Io (Max) < Io < Io (Max)	85*3	—	—	%

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH3 block [CH3]	Vo3 output over voltage threshold	V_{OVP3}	VSEL34 pin = “H” Level, Vo3 = 1.8 V, FB3 pin	2.124*1	2.16*1	2.196*1	V
			VSEL34 pin = “L” Level, Vo3 = 1.5 V, FB3 pin	1.77*1	1.8*1	1.83*1	V
	Vo3 over current limit	I_{OCP3}	Io3, L = 1.5 µH	3.0*1	3.75*1	4.5*1	A
	FB3 input resistance	R_{FB3}	FB3 pin	—	250	—	kΩ
	Soft start time	SS3	FB3 pin SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH4 block [CH4]	CH4 output voltage	Vo4	VSEL34 pin = “H” Level, FB4 pin	0.855	0.9	0.945	V
			VSEL34 pin = “L” Level, FB4 pin	0.7125	0.75	0.7875	V
	High-side FET on-resistance	R_{ONH4}	LX4 pin = −100 mA, V_{GS} = 5 V	—	130*1	—	mΩ
	Low-side FET on-resistance	R_{ONL4}	LX4 pin = 100 mA, V_{GS} = 5 V	—	55*1	—	mΩ
	PVDD4 standby current	I_{PVDD4S}	CTL34 pin = 0 V, PVDD4 pin = 12.6 V	—	—	15	µA
	CH4 efficiency	ηT41	VSEL34 pin = “H” Level, FSEL4 pin =“H” Level, Vo4 = 0.9 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	80*3	—	—	%
		ηT42	VSEL34 pin = “L” Level, FSEL4 pin =“H” Level, Vo4 = 0.75 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	80*3	—	—	%
		ηF41	VSEL34 pin = “H” Level, FSEL4 pin =“H” Level, Vo4 = 0.9 V 0.6 × Io (Max) < Io < Io (Max)	83*3	—	—	%
		ηF42	VSEL34 pin = “L” Level, FSEL4 pin =“H” Level, Vo4 = 0.75 V 0.6 × Io (Max) < Io < Io (Max)	83*3	—	—	%
	Vo4 output over voltage threshold	V_{OVP4}	VSEL34 pin = “H” Level, Vo4 = 0.9 V, FB4 pin	1.035*1	1.08*1	1.125*1	V
			VSEL34 pin = “L” Level, Vo4 = 0.75 V, FB4 pin	0.862*1	0.90*1	0.938*1	V

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH4 block [CH4]	Vo4 over current limit	I_{OCP4}	Io4, L = 1.5 µH,fosc = 700 kHz	1.92*1	2.4*1	2.88*1	A
	FB4 input resistance	R_{FB4}	FB4 pin	—	750	—	kΩ
	Soft start time	SS4	FB4 pin, SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
	FSEL4, “H” level	V_{FLGH4}	FSEL4 pin	2	—	—	V
	FSEL4, “L” level	V_{FLGL4}	FSEL4 pin	—	—	0.8	V
	FSEL4 input current	I_{FSELH4}	FSEL4 pin = 3 V	23	30	43	µA
		I_{FSELL4}	FSEL4 pin = 0 V	—	—	1	µA
CH5 block [CH5]	CH5 output voltage	Vo5	FB5 pin	1.425	1.5	1.575	V
	High-side FET on-resistance	R_{ONH5}	LX5 pin = –100 mA, V_{GS} = 5 V	—	65*1	—	mΩ
	Low-side FET on-resistance	R_{ONL5}	LX5 pin = 100 mA, V_{GS} = 5 V	—	40*1	—	mΩ
	PVDD5 standby current	I_{PVDD5S}	CTL5 pin = 0 V, PVDD5 pin = 12.6 V	—	—	15	µA
	CH5 efficiency	ηL5	0.05 × Io (Max) < Io < 0.3 × Io (Max)	82*3	—	—	%
		ηT5	0.3 × Io (Max) < Io < 0.6 × Io (Max)	85*3	—	—	%
		ηF5	0.6 × Io (Max) < Io < Io (Max)	85*3	—	—	%
	Vo5 output over voltage threshold	V_{OVP5}	FB5 pin	1.77*1	1.8*1	1.83*1	V
	Vo5 over current limit	I_{OCP5}	Io5, L = 1.5 µH	2.8*1	3.5*1	4.2*1	A
	FB5 input resistance	R_{FB5}	FB5 pin	—	250	—	kΩ
	Soft start time	SS5	FB5 pin, SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms
CH6 block [CH6]	CH6 output voltage	Vo6	DVSEL6 = “H” Level, FB6 pin	1.045	1.1	1.155	V
			DVSEL6 = “L” Level, FB6 pin	0.9975	1.05	1.1025	V
	High-side FET on-resistance	R_{ONH6}	LX6 pin = –100 mA, V_{GS} = 5 V	—	61*1	—	mΩ
	Low-side FET on-resistance	R_{ONL6}	LX6 pin = 100 mA, V_{GS} = 5 V	—	35*1	—	mΩ
	PVDD6 standby current	I_{PVDD6S}	CTL6 pin = 0 V, PVDD6 pin = 12.6 V	—	—	15	µA

(Continued)

(Continued)

(Ta = + 25 °C, AVDD = PVDD1 to PVDD7 = 7.2 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
CH6 block [CH6]	CH6 efficiency	ηL61	DVSEL6 pin = "H" Level, Vo6 = 1.1 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	80*3	—	—	%
		ηL62	DVSEL6 pin = "L" Level, Vo6 = 1.05 V 0.05 × Io (Max) < Io < 0.3 × Io (Max)	80*3	—	—	%
		ηT61	DVSEL6 pin = "H" Level, Vo6 = 1.1 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	82*3	—	—	%
		ηT62	DVSEL6 pin = "L" Level, Vo6 = 1.05 V 0.3 × Io (Max) < Io < 0.6 × Io (Max)	82*3	—	—	%
		ηF61	DVSEL6 pin = "H" Level, Vo6 = 1.1 V 0.6 × Io (Max) < Io < Io (Max)	81*3	—	—	%
		ηF62	DVSEL6 pin = "L" Level, Vo6 = 1.05 V 0.6 × Io (Max) < Io < Io (Max)	81*3	—	—	%
	Vo6 output over voltage threshold	V_{OVP6}	DVSEL6 pin = "H" Level, Vo6 = 1.1 V, FB6 pin	1.298*1	1.32*1	1.342*1	V
			DVSEL6 pin = "L" Level, Vo6 = 1.05 V, FB6 pin	1.239*1	1.26*1	1.281*1	V
	Vo6 over current limit	I_{OCP6}	Io6, L = 1.5 µH	4.0*1	5.0*1	6.0*1	A
	FB6 input resistance	R_{FB6}	FB6 pin	—	350	—	kΩ
	Soft start time	SS6	FB6 pin, SS1 = SS2 = AGND pin	1.19	1.4	1.61	ms

*1 : This parameter isn't be specified. This should be used as a reference to support designing the circuits.

*2 : FSEL4 pin is typically recommended to set to "H" level for fosc = 700 kHz setting. When Vo4 is preset to 0.75 V, the ON duty becomes so small at high input voltage. Then, there is a case CH4 output regulation becomes worse at light load condition. In that case, please set FSEL4 pin to "L" level for fosc = 350 kHz setting.

*3 : This is a reference value, which is evaluated by the recommended EVB circuit. This should be used as a reference to support designing the circuits.

■ CHANNEL CONTROL FUNCTION

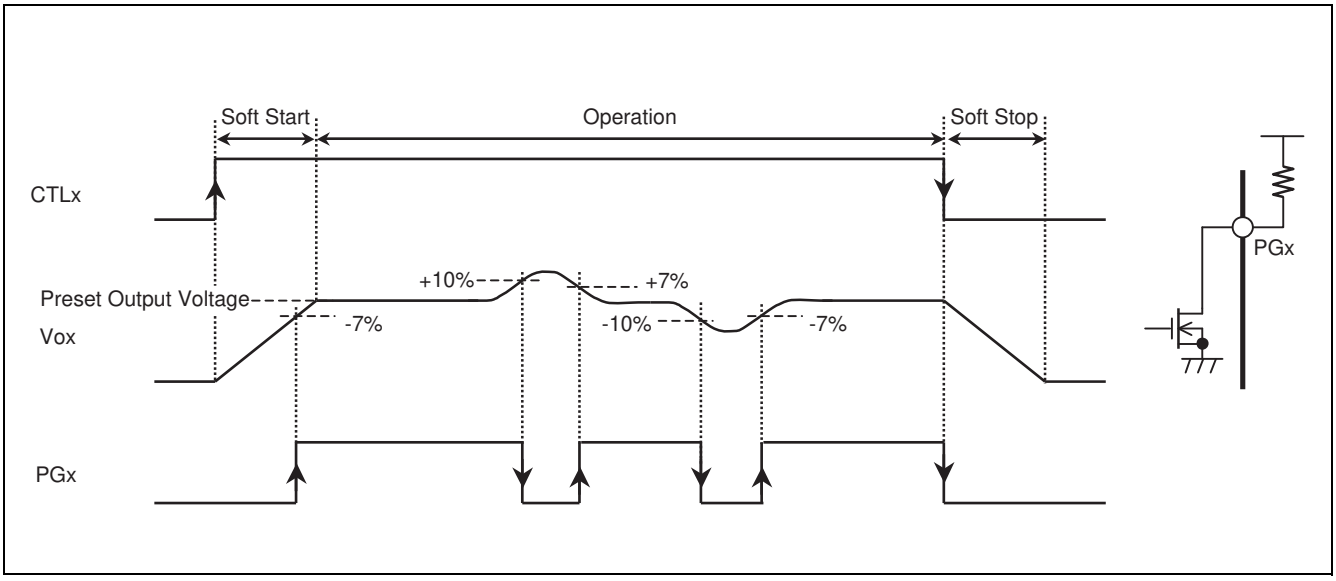
The each channel is turned on and off depending on the voltage levels at the CTL1 pin, CTL2 pin, CTL34 pin, CTL5 pin and CTL6 pin.

• Channel On/Off Setting Conditions

CTL1	CTL2	CTL34	CTL5	CTL6	CH1	CH2	CH3	CH4	CH5	CH6
L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF
L	H	L	L	L	OFF	ON	OFF	OFF	OFF	OFF
L	L	H	L	L	OFF	OFF	ON	ON	OFF	OFF
L	L	L	H	L	OFF	OFF	OFF	OFF	ON	OFF
L	L	L	L	H	OFF	OFF	OFF	OFF	OFF	ON
H	H	H	H	H	ON	ON	ON	ON	ON	ON

■ POWER GOOD FUNCTION

The Power Good function is shown in the following figure. The ALLPG pin and the PGx pins are connected to the open drain of the NMOS, and are used by connecting the resistor. When the CTLx pin is turned on, and the output voltage becomes within 7% of the preset voltage, the PGx pin is changed from “L” to “H”. PGx = “H” means the status of Power Good. When the change of the output voltage exceeds 10% of the preset voltage, the PGx pin becomes “L”. And when the output voltage becomes within 7% of the preset voltage, the PGx pin becomes “H”. Moreover, when all of the channels from CH3 to CH6 are the Power Good, the ALLPG pin becomes “H”.



■ PROTECTION

<1> Under Voltage Lock Out Protection (UVLO)

The UVLO prevents IC malfunctions or system damage and the degradation caused by the excessive voltage or instantaneous voltage drop of the power supply voltage (AVDD), bias voltage (VB), internal reference voltage (VREF).
The UVLO turns off all the high- and low-side FETs of CH1 to CH6 when the AVDD pin drops below 5.0 V(Typ).
The UVLO is released when the AVDD pin is above 5.1 V (Typ). This is the non-latch type protection.

<2> Input Over Voltage Protection (IVP)

The circuit prevents IC malfunctions or system damage and the degradation caused by the excessive voltage or instantaneous voltage drop of the power supply voltage (AVDD).
The IVP turns off all the high- and low-side FETs of CH1 to CH6 when the AVDD pin exceeds 13.0 V(Typ). The IVP is released when the AVDD pin drops below 12.85 V (Typ). This is the non-latch type protection.

<3> Over Temperature Protection (OTP)

The OTP prevents thermal damages on ICs. The IVP function turns off all the high- and low-side FETs of CH1 to CH6 when the junction temperature exceeds +150 °C (Typ). The OPT is released when the temperature drops below +125 °C (Typ). This is the non-latch type protection.

<4> Output Short Circuit Protection (SCP)

The SCP function stops outputting data when the output voltage falls and protects the devices connected to outputs.
The SCP timer will start to count when either of output voltages CH1 to CH6 falls due to the output short-circuit to GND or excessive currents. The SCP function starts to operate the latch protection and turns off all the high- and low-side FETs when the output voltage continues to fall to 1.4 ms (Typ).
Follow either of the steps to release the latch of output short circuit protection.

- After all of CTL signals from CH1 to CH6 are set to “L” level, turn on the each CTL signal again.
- When the voltage of the AVDD pin is below the threshold voltage of the UVLO, and then the voltage of the AVDD pin becomes higher than the threshold voltage of UVLO again, the each output will start up.

<5> Output Over Voltage Protection (OVP)

The OVP protects the devices which are connected to outputs when the output voltage rises. When either output voltage of the CH1 to CH6 is higher than 120% of each channel's preset voltage (Typ), the OVP turns off all the high- and low-side FETs of the channels (However, the only CH4 is turned off the high-side FET and turned on the low-side FET. The CH4 logic is different from other channels as it is controlled with PWM). The OVP is released when the output voltage is below 103% of the preset voltage (Typ). This is the non-latch type protection.

<6> Over Current Protection (OCP)

The OCP function controls the output current. When drain-to-source current excessively increases, the OCP controls the output current to the preset value for each channel. Then, because of the OCP functions, the output voltage usually drops. As a result, the SCP stop the all outputs with the latch setting.
The OCP functions only for the corresponding channels only, however, the SCP stops all of the channels in the end.

■ DESCRIPTION OF SOFT-START AND SOFT-STOP OPERATION

Soft-start function is featured to avoid inrush current when each channels is turned-on. When the CTL1, CTL2, CTL34, CTL5 and CTL6 are set to “H” level, ramped-up voltage is fed on an inverting input of an error amplifier of a channel. Start-time of the soft-start can be predefined and the start time is kept constant independent from a load of the output of the channels. When the CTL1, CTL2, CTL34, CTL5 and CTL6 are set to “L” level, ramped-down voltage is fed on an inverting input of an error amplifier of a channel then the output voltage goes low. Stop-time of the Soft-stop can be predefined and the stop-time is kept constant independent from a load of the output of the channel.

The time of both soft-start and soft-stop can be predefined with combination of the level on the SS1 and the SS2 pins as shown in the “• Soft-Start/Soft-Stop time (tson/tsoff) Setting Conditions”, and external capacitors and resistors aren't required

• Soft-Start/Soft-Stop time (tson/tsoff) Setting Conditions

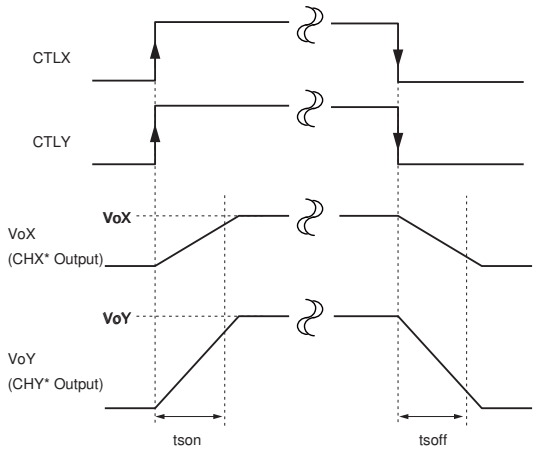
SS1 pin	SS2 pin	Soft-Start time (tson) (Typ) *	Soft-Stop time (tsoff) (Typ) *	Unit
Connecting to AGND pin	Connecting to AGND pin	1.4	1.4	ms
Connecting to AGND pin	Connecting to VREF pin	2.2	2.2	ms
Connecting to AGND pin	Connecting to VB pin	2.9	2.9	ms
Connecting to VREF pin	Connecting to AGND pin	3.5	3.5	ms
Connecting to VREF pin	Connecting to VREF pin	4.1	4.1	ms
Connecting to VREF pin	Connecting to VB pin	5.1	5.1	ms
Connecting to VB pin	Connecting to AGND pin	5.9	5.9	ms
Connecting to VB pin	Connecting to VREF pin	7.3	7.3	ms
Connecting to VB pin	Connecting to VB pin	8.2	8.2	ms

* : Accuracy : Typ ±15%

<< Trace of the Output voltage on each channel, during Soft-Start/Soft-Stop operations>>

The sequence of turning on/off different output channels is defined by the CTL1, CTL2, CTL34, CTL5 and CTL6 pins.

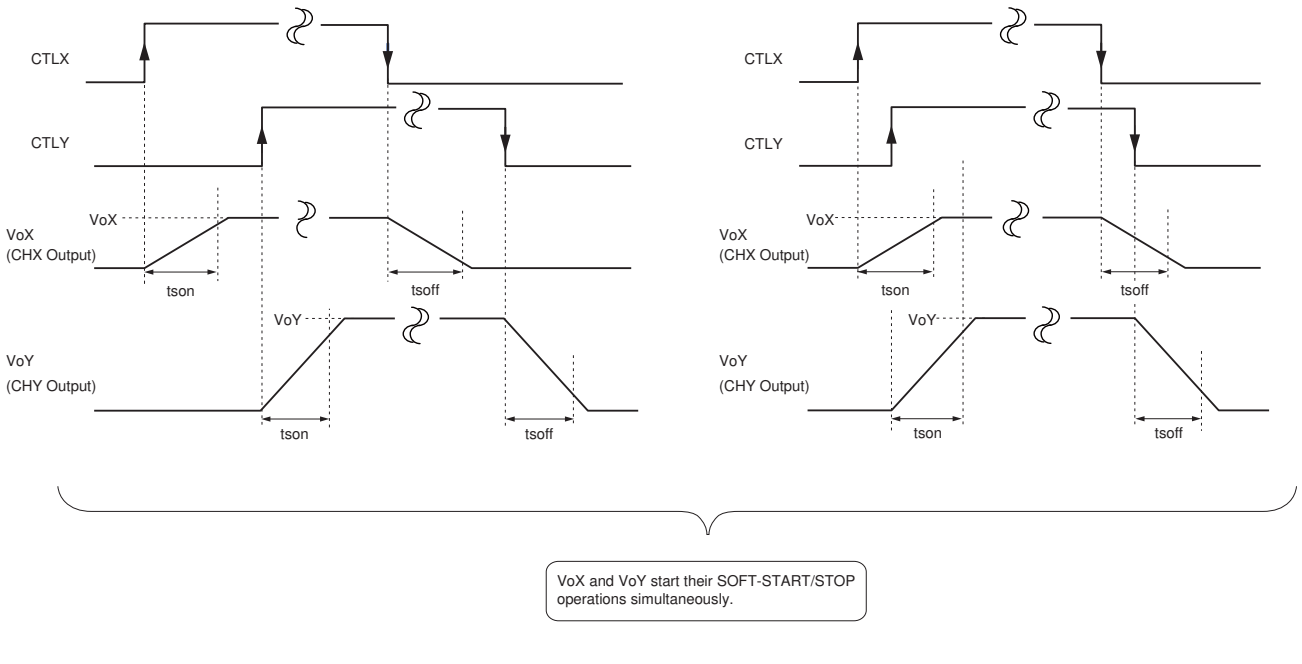
(1) When CTLX and CTLY are set to “H” or “L” simultaneously.



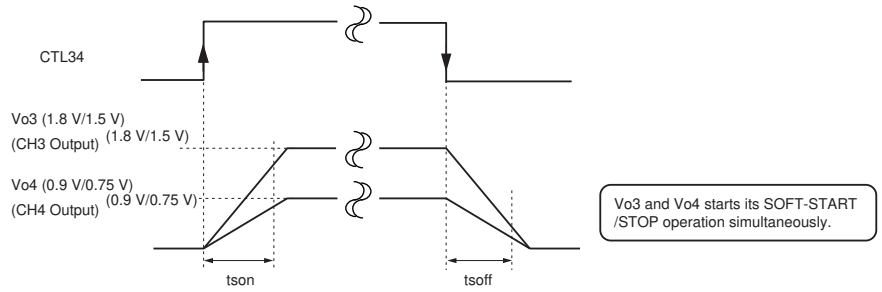
* : CHY and CHX are different CH.

(2) When CTLY is set to “H” or “L” after completion of SOFT-START or -STOP on VoX .

(3) When CTLY is set to “H” or “L” after VoX has started its SOFT-START or -STOP operation.



(4) When CTL34 is set to “H” or “L”.



■ PRESET FUNCTION OF CH3/CH4/CH6 OUTPUT VOLTAGE

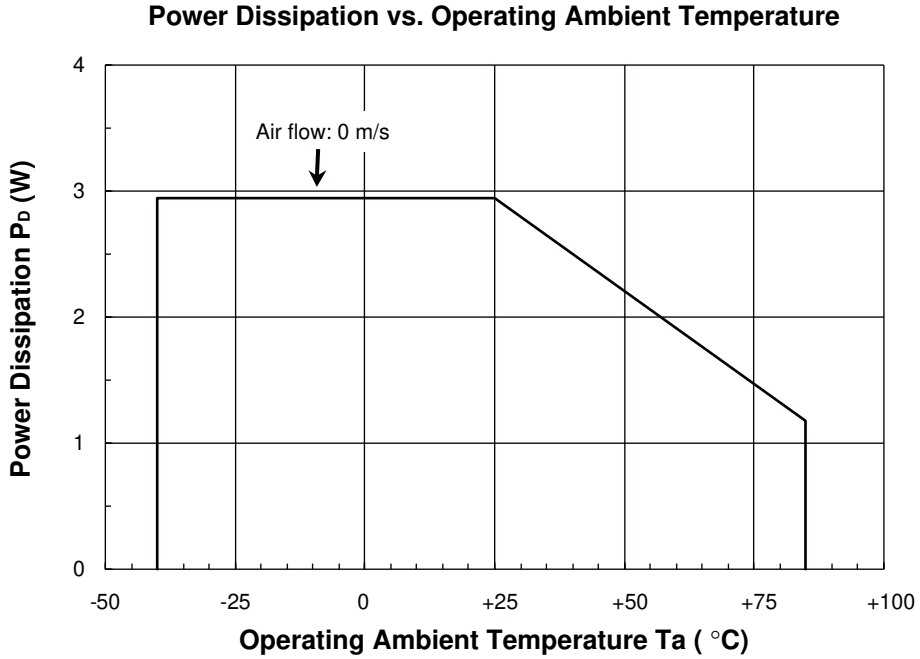
The preset output voltage of CH3 and CH4 are selected by VSEL34 pin condition. Please refer the following table. The preset output voltage of CH6 is selected by DVSEL6 pin condition. Please refer the following table.

• CH3/CH4/CH6 Preset Output Voltage Conditions

CONNECTION	VREF	GND
VSEL34	Vo3 = 1.8 V setting Vo4 = 0.9 V setting	Vo3 = 1.5 V setting Vo4 = 0.75 V setting
DVSEL6	Vo6 = 1.1 V setting	Vo6 = 1.05 V setting

■ TYPICAL CHARACTERISTICS

• Maximum Power Dissipation vs. Operating Ambient Temperature



The Allowable power dissipation is shown in the "• Maximum Power Dissipation vs. Operating Ambient Temperature". The maximum power dissipation depends on the thermal capability of the given package, and the ambient temperature.

Sum of power dissipation of each channel (CH1 to CH6) should not exceed the maximum rating. Expected power loss of the each channel's over load current are shown in the "• Power Loss Curve for each channel".

• The condition of the thermal model