Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

The following document contains information on Cypress products. Although the document is marked with the name "Spansion" and "Fujitsu", the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

Continuity of Specifications
There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

Continuity of Ordering Part Numbers
Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information
Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress
Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

FUJITSU MICROELECTRONICS
DATA SHEET

DS04–27266–2E

ASSP (for Mobile Terminals)

Power Management IC for Mobile Terminals 3ch DC/DC Converter + 4ch LDO

MB39C316

■ DESCRIPTION

The MB39C316 is equipped with the 3 ch DC/DC converter and the 4 ch linear regulator (LDO), and is the power supply LSI for mobile terminals which operate in the range of power supply voltage with 1-cell Li-ion power by 1ch high efficiency voltage step-up/down DC/DC.
The MB39C316 contains the 2ch synchronous rectification DC/DC converter with current mode system and the 1ch voltage step-up/down DC/DC converter. Detecting load current by each DC/DC converter alternates the Normal mode (PWM) with the ECO mode (PFM) automatically.
MB39C316 has the built-in 4ch LDO which is suitable to supply voltage to the system block and the built-in 1ch LDO which generates stable internal reference voltage.
It is possible to control a notice of internal condition, the power supply and reset in order to support the communication interface which is compliant with the I^2C bus standard.

■ FEATURES

- Input voltage range : 2.7 V to 5.5 V
- Step-down regulators : 2 channels
- Step-up/down regulator : 1 channel
- Linear regulator (LDO) : 4 channels
- Possible to select output voltage : LDO3 1.2 V/1.3 V (register setting)
- On/Off control of LDO and DC/DC converter by external signals and register settings
- Compliant with I^2C bus standard (Max 400 kbps)
- Possible to output the 32.768 kHz clock by connecting crystal oscillator
- Protection function:Over current protection (OCP), Output short circuit protection (SCP), Under voltage lock out protection (UVLO), Over temperature protection (OTP)
- Package : 49 pin, WL-CSP (3.14 mm × 3.11 mm × 0.8 mm)

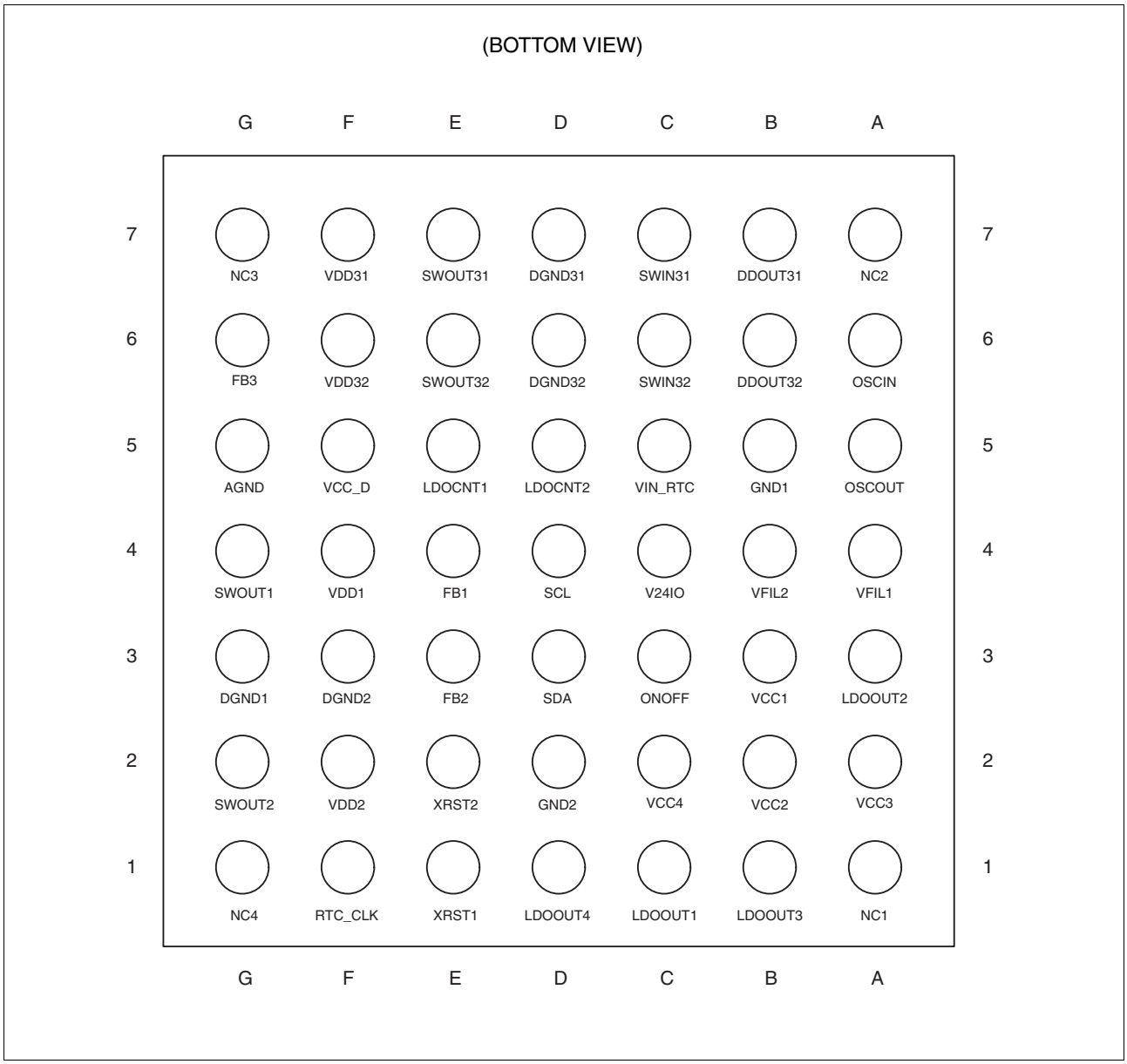
■ APPLICATIONS

- Mobile WiMAX terminals
- Other mobile terminals etc.

2009.1

FUJITSU

■ PIN ASSIGNMENT



■ PIN DISCRIPTIONS

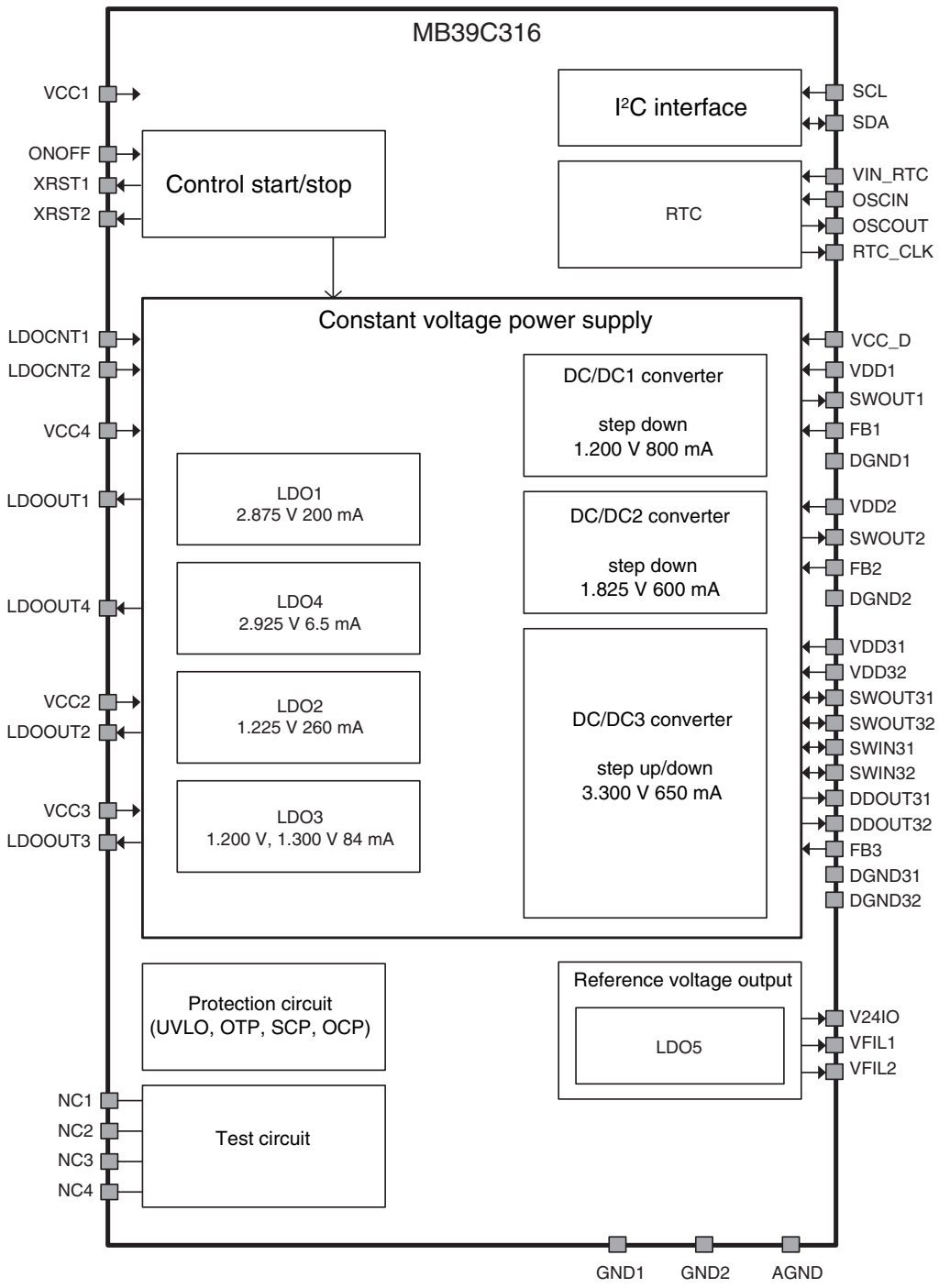
Block	Pin No.	Pin name	I/O	Descriptions
External power supply	B3	VCC1	I	Power supply input, Power supply input pin for LDO2, LDO3 control
	B2	VCC2	I	Power supply input pin for LDO2 power
	A2	VCC3	I	Power supply input pin for LDO3 power
	C2	VCC4	I	Power supply input pin for LDO1, LDO4 control/power
	F5	VCC_D	I	Power supply input pin for DC/DC converter control
	F4	VDD1	I	Power supply input pin for DC/DC1 converter power
	F2	VDD2	I	Power supply input pin for DC/DC2 converter power
	F7	VDD31	I	Power supply input pin 1 for DC/DC3 converter power
	F6	VDD32	I	Power supply input pin 2 for DC/DC3 converter power
	C5	VIN_RTC	I	Power supply input pin for RTC
Constant voltage power supply	E5	LDOCNT1	I	LDO output control input pin 1
	D5	LDOCNT2	I	LDO output control input pin 2
	D1	LDOOUT4	O	LDO4 output pin (+ 2.9 V)
	B1	LDOOUT3	O	LDO3 output pin (+ 1.2 V/1.3 V)
	C1	LDOOUT1	O	LDO1 output pin (+ 2.9 V)
	A3	LDOOUT2	O	LDO2 output pin (+ 1.2 V)
	G4	SWOUT1	O	DC/DC1 converter inductance connection output pin
	E4	FB1	I	DC/DC1 converter output voltage feedback input pin (1.2 V)
	G2	SWOUT2	O	DC/DC2 converter inductance connection output pin
	E3	FB2	I	DC/DC2 converter output voltage feedback input pin (1.8 V)
	E7	SWOUT31	—	DC/DC3 converter inductance connection pin 1
	E6	SWOUT32	—	DC/DC3 converter inductance connection pin 2
	C7	SWIN31	—	DC/DC3 converter inductance connection pin 1
	C6	SWIN32	—	DC/DC3 converter inductance connection pin 2
	B7	DDOUT31	O	DC/DC3 converter output pin 1
	B6	DDOUT32	O	DC/DC3 converter output pin 2
	G6	FB3	I	DC/DC3 converter output voltage feedback input pin (3.3 V)
I^2C interface	D4	SCL	I	I^2C interface clock input pin
	D3	SDA	I/O	I^2C interface data I/O pin
RTC	A6	OSCIN	I	Input pin for crystal oscillator connection
	A5	OSCOUT	O	Output pin for crystal oscillator connection
	F1	RTC_CLK	O	32.768 kHz Clock output pin
Start/Stop	C3	ONOFF	I	Enable pin for the MB39C316
	E1	XRST1	O	Reset output pin 1
	E2	XRST2	O	Reset output pin 2
Reference voltage	C4	V24IO	O	Power supply output pin for internal 2.4 V I/O
	A4	VFIL1	O	Reference voltage output pin 1 (0.47 µF connected)
	B4	VFIL2	O	Reference voltage output pin 2 (0.47 µF connected)

(Continued)

(Continued)

Block	Pin No.	Pin name	I/O	Descriptions
TEST	A1	NC1	—	Pin for TEST (Set to Non Connect. Prohibited to connect to others.)
	A7	NC2	—	Pin for TEST (Set to Non Connect. Prohibited to connect to others.)
	G7	NC3	—	Pin for TEST (Set to Non Connect. Prohibited to connect to others.)
	G1	NC4	—	Pin for TEST (Set to Non Connect. Prohibited to connect to others.)
GND	B5	GND1	—	Ground pin (COMMON, RTC)
	D2	GND2	—	Ground pin (LDO, INPUT_IF, OUTPUT_IF)
	G5	AGND	—	Ground pin (DC/DC converter control block)
	G3	DGND1	—	DC/DC1 converter ground pin
	F3	DGND2	—	DC/DC2 converter ground pin
	D7	DGND31	—	DC/DC3 converter ground pin 1
	D6	DGND32	—	DC/DC3 converter ground pin 2

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	Vmax1	VCC1, VCC_D, VDD1, VDD2, VDD31, VDD32	− 0.3	+ 6.0	V
	Vmax2	VCC2, VCC3	− 0.3	+ 6.0	V
	Vmax3	VCC4	− 0.3	+ 6.0	V
	Vmax4	VIN_RTC	− 0.3	+ 3.6	V
Input voltage	Vinmax1	LDOCNT1, LDOCNT2, SCL, SDA	− 0.3	Vvcc3 + 0.3	V
	Vinmax2	ONOFF, FB1, FB2, FB3	− 0.3	Vvcc1 + 0.3	V
	Vinmax3	OSCIN	− 0.3	Vrtc	V
Storage temperature range	Tstg	—	− 55	+ 125	°C
ESD withstand voltage	Vesdh	Human Body Model (100 pF, 1.5 kΩ)	− 1000	+ 1000	V
	Vesdm	Machine Model (200 pF, 0 Ω)	− 100	+ 100	V
latch-up withstand voltage	Vlatchup	EIA/JEDEC Standard	− 150	+ 150	mA

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	Vvcc1	VCC1, VCC_D, VDD1, VDD2, VDD31, VDD32	2.7	3.3	5.5	V
	Vvcc2	VCC2, VCC3	1.75	—	1.90	V
	Vvcc3	VCC4	3.2	—	5.5	V
	Vrtc	VIN_RTC	2.325	—	2.475	V
Input voltage	Vlvcc1	ONOFF	0.0	—	Vvcc1	V
	Vlvcc3	LDOCNT1, LDOCNT2, SCL, SDA	0.0	—	Vvcc3	V
	Vldd1	FB1	0.0	—	Voutdd1	V
	Vldd2	FB2	0.0	—	Voutdd2	V
	Vldd3	FB3	0.0	—	Voutdd3	V
	Vlrtc	OSCIN	0.0	—	Vrtc	V
Operating temperature range	Ta	—	− 30	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC characteristics

(Ta = − 30 °C to + 85 °C, Vvcc1 = 2.7 V to 5.5 V ,Vvcc3 = 3.2 V to 5.5 V, Vvcc2 = 1.75 V to 1.90 V,Vrtc = 2.325 V to 2.475 V)

Parameter		Symbol	Condition		Value			Unit
					Min	Typ	Max	
LDO1	Output voltage	Voutld1	Iout = 0 to Iomax		2.800	2.875	3.000	V
	Maximum output current	Ioutld1	—		200	—	—	mA
	Input stability	Vlineld1	Iout = − 10 mA		—	5	—	mV
	Load stability	Vloadld1	Iout = 0 to Iomax		—	20	—	mV
	Ripple removal ratio	RR1kld1	Vinput = 0.2 Vpp, Vvcc1 = 3.3 V, Iout = Iomax/2	f = 1 kHz	—	60	—	dB
		RR10kld1		f = 10 kHz	—	40	—	dB
	Output noise voltage	Vnoiseld1	f = 10 Hz to 100 kHz, Iout = 10 mA to Iomax		—	30	45	µVrms
	Rise time	Trld1	Vvcc1 = 3.3 V, Iout = 0 mA, Vout = 90%		—	200	—	µs
	Fall time	Tfld1	Vvcc1 = 3.3 V, Iout = 0 mA, Vout = 10%		—	70	—	µs
LDO2	Output voltage	Voutld2	Iout = 0 to Iomax		1.150	1.225	1.300	V
	Maximum output current	Ioutld2	—		260	—	—	mA
	Input stability	Vlineld2	Iout = − 10mA		—	5	—	mV
	Load stability	Vloadld2	Iout = 0 to Iomax		—	25	—	mV
	Ripple removal ratio	RR1kld2	Vinput = 0.2 Vpp, Vvcc1, Iout = 1 mA to Iomax	f = 1 kHz	—	60	—	dB
		RR10kld2		f = 10 kHz	—	40	—	dB
	Output noise voltage	Vnoiseld2	f = 10 Hz to 100 kHz, Iout = 10 mA to Iomax		—	30	45	µVrms
	Rise time	Trld2	Vvcc1, Iout = 0 mA, Vout = 90%		—	70	—	µs
	Fall time	Tfld2	Vvcc1, Iout = 0 mA, Vout = 10%		—	150	—	µs

(Continued)

Parameter		Symbol	Condition		Value			Unit
					Min	Typ	Max	
LDO3	Output voltage	Voutld3	Iout = 0 to Iomax, VSEL_SYN = “0” (register 02H[0])		1.100	1.200	1.300	V
			Iout = 0 to Iomax, VSEL_SYN = “1” (register 02H[0])		1.200	1.300	1.400	V
	Maximum output current	Ioutld3	—		84	—	—	mA
	Input stability	Vlineld3	Iout = − 10 mA		—	5	—	mV
	Load stability	Vloadld3	Iout = 0 to Iomax		—	20	—	mV
	Ripple removal ratio	RR1kld3	Vinput = 0.2 Vpp, Vvcc1, Iout = 1mA to Iomax	f = 1 kHz	—	60	—	dB
		RR10kld3		f = 10 kHz	—	40	—	dB
	Output noise voltage	Vnoiseld3	f = 10 Hz to 100 kHz, Iout = 10 mA to Iomax		—	30	40	μVrms
	Rise time	Trld3	Vvcc1, Iout = 0 mA, Vout = 90%		—	60	—	μs
	Fall time	Tfld3	Vvcc1, Iout = 0 mA, Vout = 10%		—	150	—	μs
LDO4	Output voltage	Voutld4	Iout = 0 to Iomax		2.850	2.925	3.000	V
	Maximum output current	Ioutld4	—		6.5	—	—	mA
	Input stability	Vlineld4	Iout = − 6.5 mA		—	5	—	mV
	Load stability	Vloadld4	Iout = 0 to Iomax		—	5	—	mV
	Ripple removal ratio	RR1kld4	Vinput = 0.2 Vpp, Vvcc1 = Vvcc3 = 3.3 V, Iout = 1 mA to Iomax	f = 1 kHz	—	60	—	dB
		RR10kld4		f = 10 kHz	—	40	—	dB
	Output noise voltage	Vnoiseld4	f = 10 Hz to 100 kHz, Iout = 1 mA to Iomax		—	30	40	μVrms
	Rise time	Trld4	Vvcc1 = Vvcc3 = 3.3 V, Iout = 0 mA, Vout = 90%		—	130	—	μs
	Fall time	Tfld4	Vvcc1 = Vvcc3 = 3.3 V, Iout = 0 mA, Vout = 10%		—	70	—	μs

(Continued)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
DC/DC1 converter	Output voltage	Voutdd1	Iout = 0 to Iomax	1.100	1.200	1.300	V
	Maximum output current	Ioutdd1	—	800	—	—	mA
	Output ripple voltage	Vrpldd11	Iout = 0 to Iomax	—	15	—	mV
	Input stability	Vlinedd1	Vvcc1 = 2.7 V to 5.5 V	—	10	—	mV
	Load stability	Vloaddd1	Iout = − 1 mA to Iomax	—	—	20	mV
	Oscillation frequency	Fdd1	PWM mode	—	1.7	—	MHz
	Efficiency	ηdd1	Vvcc1 = 3.3 V, Iout = − 200 mA	75	85	—	%
	Rise time	Trdd1	Vvcc1 = 3.3 V, Iout = 0 mA	—	50	—	µs
	Fall time	Tfdd1	Vvcc1 = 3.3 V, Iout = 0 mA	—	200	—	µs
DC/DC2 converter	Output voltage	Voutdd2	Iout = 0 to Iomax	1.750	1.825	1.900	V
	Maximum output current	Ioutdd2	—	600	—	—	mA
	Output ripple voltage	Vrpldd21	Iout = 0 to Iomax	—	15	—	mV
	Input stability	Vlinedd2	Vvcc1 = 2.7 V to 5.5 V	—	10	—	mV
	Load stability	Vloaddd2	Iout = − 1 mA to Iomax	—	—	20	mV
	Oscillation frequency	Fdd2	PWM mode	—	1.7	—	MHz
	efficiency	ηdd2	Vvcc1 = 3.3 V, Iout = − 200 mA	80	90	—	%
	Rise time	Trdd2	Vvcc1 = 3.3 V, Iout = 0 mA	—	50	—	µs
	Fall time	Tfdd2	Vvcc1 = 3.3 V, Iout = 0 mA	—	200	—	µs
DC/DC3 converter	Output voltage	Voutdd3	Iout = 0 to Iomax	3.200	3.300	3.400	V
	Maximum output current	Ioutdd3	—	650	—	—	mA
	Output ripple voltage	Vrpldd31	Iout = 0 to Iomax	—	60	—	mV
	Input stability	Vlinedd3	Vvcc1 = 2.7 V to 5.5 V	—	10	—	mV
	Load stability	Vloaddd3	Iout = − 1 mA to Iomax	—	—	30	mV
	Oscillation frequency	Fdd3	PWM mode	—	1.7	—	MHz
	efficiency	ηdd3	Vvcc1 = 3.3 V, Iout = − 200 mA	80	90	—	%
	Rise time	Trdd3	Vvcc1 = 3.3 V, Iout = 0 mA	—	100	—	µs
	Fall time	Tfdd3	Vvcc1 = 3.3 V, Iout = 0 mA	—	120	—	µs

(Continued)

(Continued)

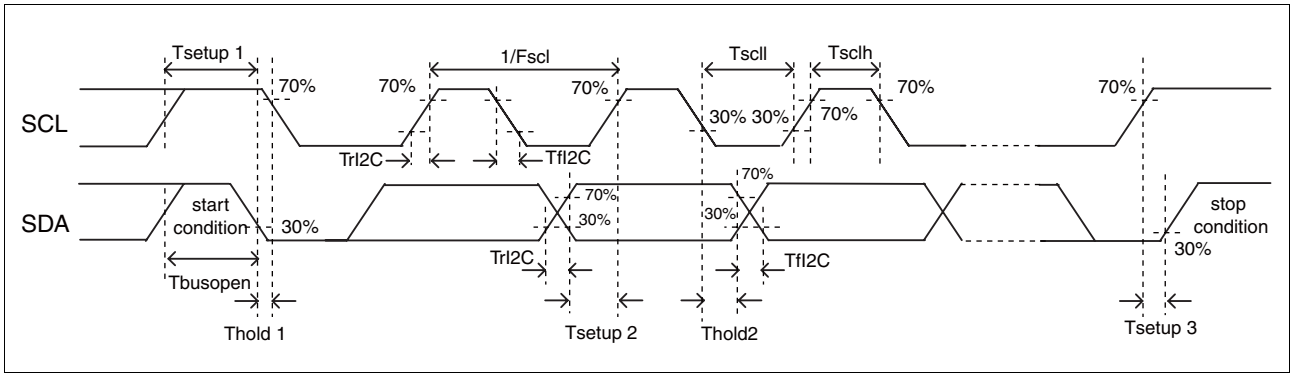
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Start/stop control block	Input voltage	Vil1	ONOFF	0.0	—	0.3 × Vvcc1	V
		Vih1		0.7 × Vvcc1	—	Vvcc1	V
		Vil2	LDOCNT1, LDOCNT2	0.0	—	0.3 × Vvcc3	V
		Vih2		0.7 × Vvcc3	—	Vvcc3	V
	Output voltage	Vol1	XRST1, XRST2, Iout = 1 mA	0.0	—	0.15 × Vvcc3	V
		Voh1	XRST1, XRST2, Iout = − 1 mA	0.85 × Vvcc3	—	Vvcc3	V
	VCC1 power supply detection voltage	Vdetvon	VCC1 rise = 0.1 V/10 µs	2.55	2.6	2.65	V
	VCC1 Voltage for power supply cut-off detection	Vdetvoff	VCC1 fall = 0.3 V/10 µs	2.3	2.4	2.5	V
RTC block	Output voltage	Vol32k	RTC_CLK, Iout = 0.5 mA	0.0	—	0.15 × Vrtc	V
		Voh32k	RTC_CLK, Iout = − 0.5 mA	0.85 × Vrtc	—	Vrtc	V
	Internal oscillation capacitance 1	Cg	OSCIN	—	10	—	pF
	Internal oscillation capacitance 2	Cd	OSCOUT	—	10	—	pF
I²C interface	Input voltage	Vil14	SCL, SDA (for input)	0.0	—	0.3 × Vvcc3	V
		Vih14		0.7 × Vvcc3	—	Vvcc3	V
	Output voltage	Vol18	SDA (for output) Iout = 3 mA	0.0	—	0.4	V
VFIL1, VFIL2	Output voltage	Vovfil1	VFIL1	1.175	1.225	1.275	V
		Vovfil2	VFIL2	0.575	0.60	0.625	V
LDO5	Output voltage	Voutld5	Iout = 0 to Iomax	2.325	2.40	2.475	V
UVLO	UVLO release voltage	Vuvlod	—	2.1	2.2	2.3	V
	UVLO detection voltage	Vuvlor	—	2.0	2.1	2.2	V
Over temperature protection (OTP)	Detection temperature	Totpd	—	+ 135	+ 150	+ 165	°C
	Release temperature	Totpr	—	+ 105	+ 120	+ 135	°C
Output short circuit protection (SCP)	Detection protection time	Tshort	Output = 0.6 V ± 0.2 V or less	75	100	125	ms

2. AC characteristics

(Ta = − 30 °C to + 85 °C, Vvcc1 = 2.7 V to 5.5 V ,Vvcc3 = 3.2 V to 5.5 V, Vvcc2 = 1.75 V to 1.90 V, Vrtc = 2.35 V to 2.475 V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
RTC block	Clock frequency	Fck	When using RTC_CLK, and FC_12M (manufactured by Epson Toyocom Corporation) for external crystal.	—	32.768	—	kHz
	Clock duty	Rck	When using RTC_CLK, and FC_12M (manufactured by Epson Toyocom Corporation) for external crystal.	25	50	75	%
	Margin for oscillation	Rfm	Rmax = 90 kΩ	10 × Rmax	—	—	kΩ
I²C interface	Clock frequency	Fscl	SCL	—	—	400	kHz
	Start condition hold time	Thold1	SCL, SDA	0.6	—	—	µs
	SCL clock L cycle	Tscll	SCL	1.3	—	—	µs
	SCL clock H cycle	Tsclh	SCL	0.6	—	—	µs
	Start condition set up time	Tsetup1	SCL, SDA	0.6	—	—	µs
	Data hold time	Thold2	SCL, SDA	0	—	0.9	µs
	Data set up time	Tsetup2	SCL, SDA	0.1	—	—	µs
	Stop condition set up time	Tsetup3	SCL, SDA	0.6	—	—	µs
	Bus open time between stop condition-start condition	Tbusopen	SDA	1.3	—	—	µs
	Rise time	TrI2C	SCL, SDA	—	—	300	ns
	Fall time	TfI2C	SCL, SDA	—	—	300	ns

• I²C interface



3. Current dissipation

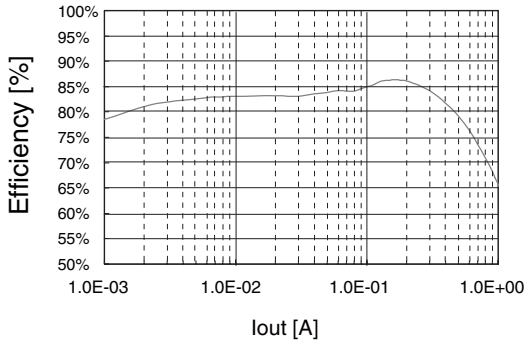
Parameter	Condition	Value		Unit
		Typ	Max	
Standby current	ONOFF : L	150	250	µA
ON current	DC/DC1 converter, DC/DC2 converter : ON (no load) LDO1, LDO2, LDO3, LDO4 : ON (no load)	650	850	µA

■ TYPICAL CHARACTERISTICS

For the reference of design, typical characteristics are shown below.

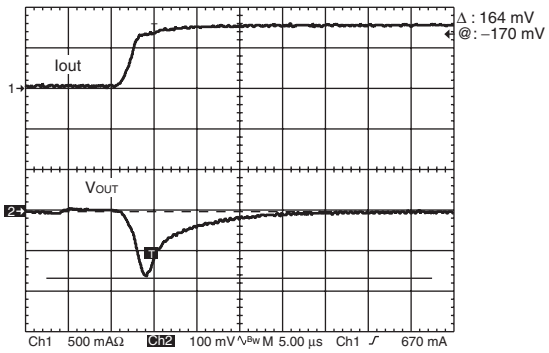
- Characteristics of Voltage step-down DCDC (DCDC1, Vout = 1.200 V)

Efficiency vs. Output current
DCDC1 efficiency (Ta = + 25 °C)
VCC = 3.3 V

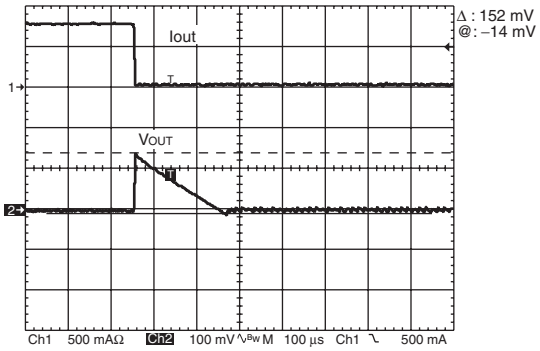


Load changes suddenly characteristics

I_{OUT} = 0 mA → 800 mA

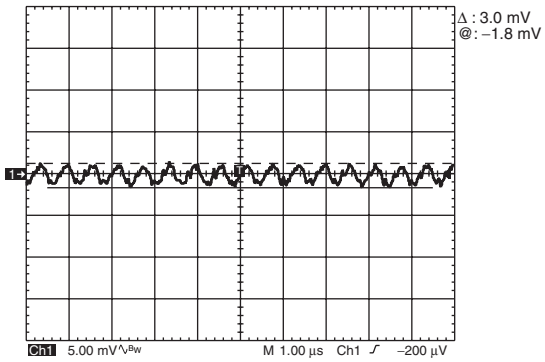


Iout = 800 mA → 0 mA

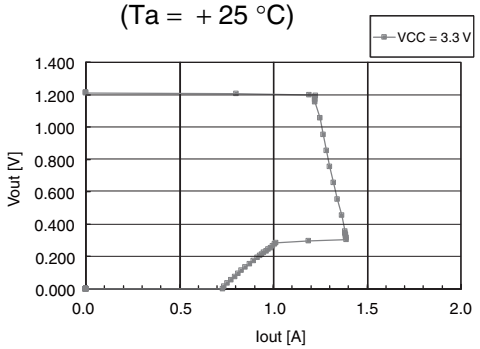


Output ripple voltage

VCC = 3.3 V, Iout = 200 mA

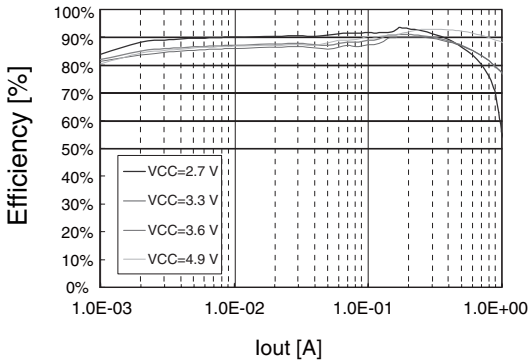


Output voltage vs. Load current characteristics
DCDC1 Output voltage vs. Load current
(Ta = + 25 °C)



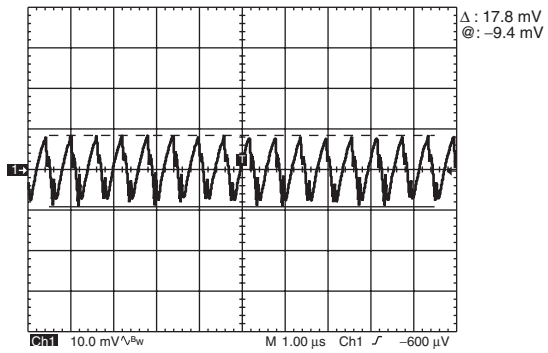
- Characteristics of Voltage step-down/up DCDC (DCDC3, Vout = 3.300 V)

Efficiency vs.Output current
DCDC3 efficiency (Ta = + 25 °C)

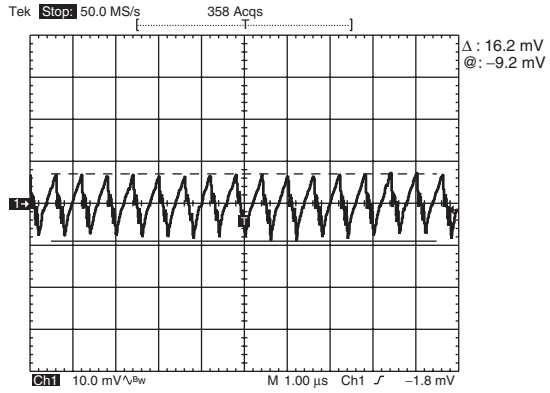


Output ripple voltage

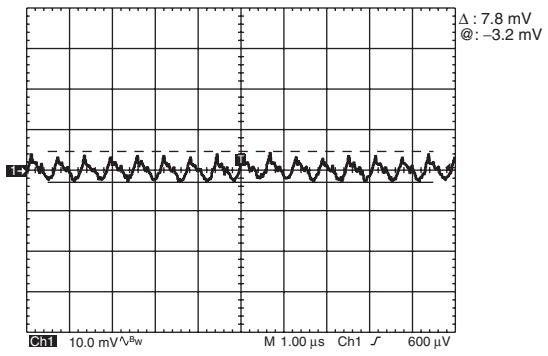
VCC = 2.7 V, Iout = 400 mA



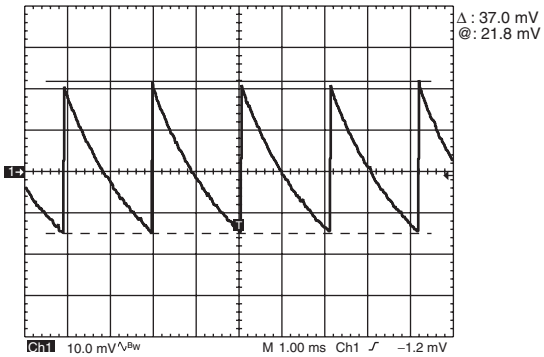
VCC = 3.3 V, Iout = 400 mA



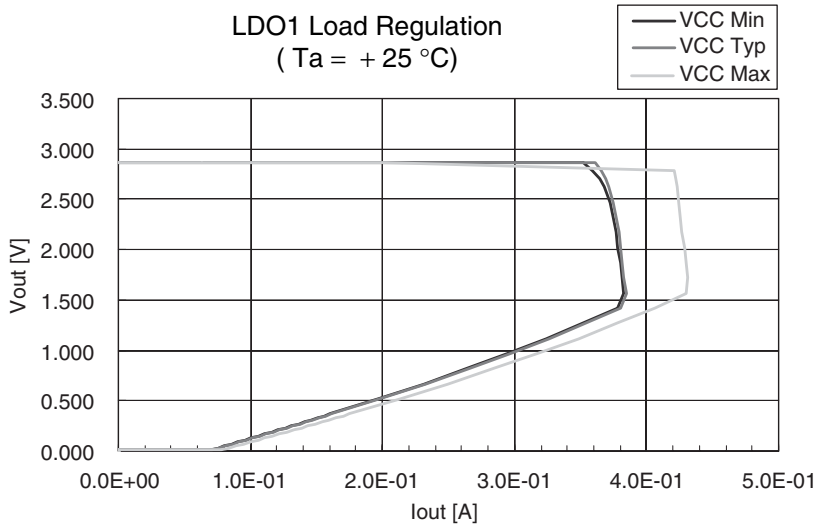
VCC = 4.9 V, Iout = 400 mA

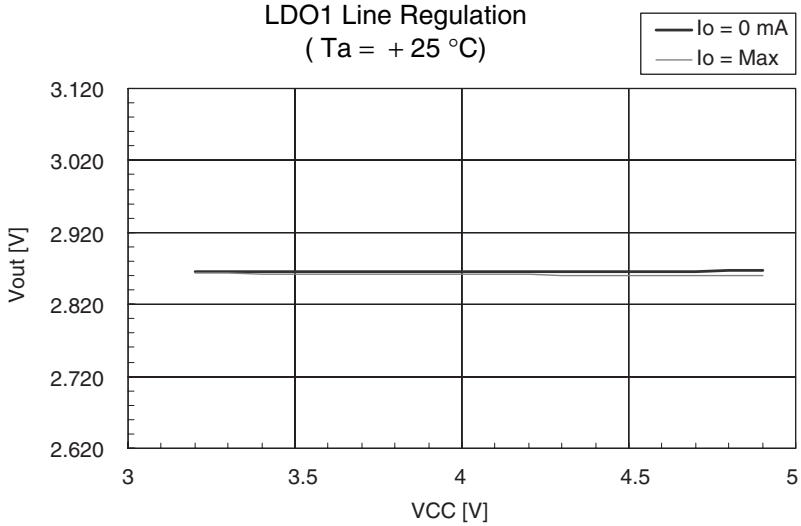


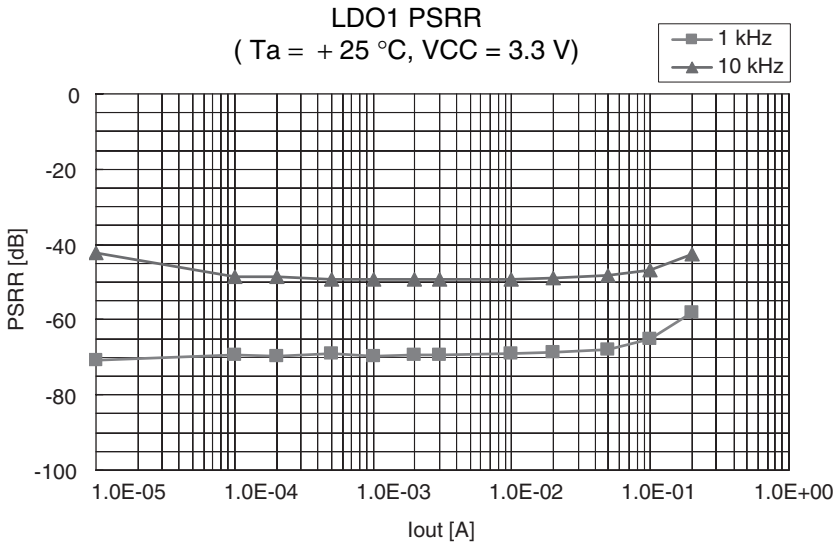
VCC = 4.9 V, Iout = 0 mA



• LDO(LDO1) characteristics







■ START/STOP CONTROL FUNCTION

Conditions of the VCC1 power supply pin and ONOFF, LDOCNT1 and LDOCNT2 pins and the setting of the REON register control the output of the LDO, the DC/DC converter and reset signals (XRST1 and XRST2). Also, the setting of the HRST register controls the output of the reset signal.

1. Conditions for start and stop

• Conditions for start

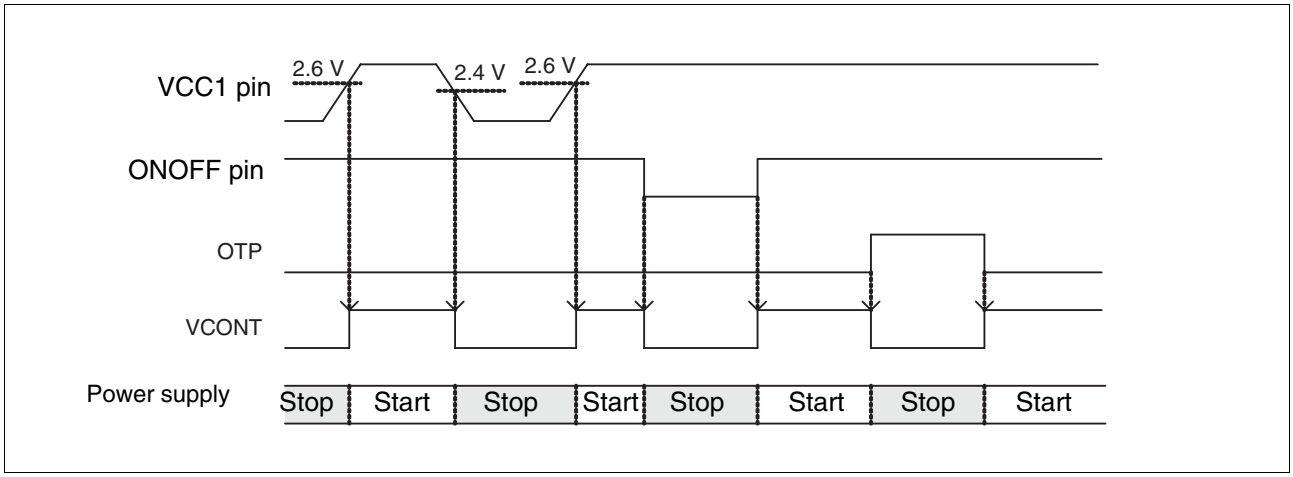
When all conditions mentioned below are completed, the LDO and the DC/DC converter will start.

- VCC1 pin input voltage 2.6 V or more
- ONOFF pin input “H”

• Conditions for stop

When one of conditions mentioned below occurs, the LDO and the DC/DC converter will stop.

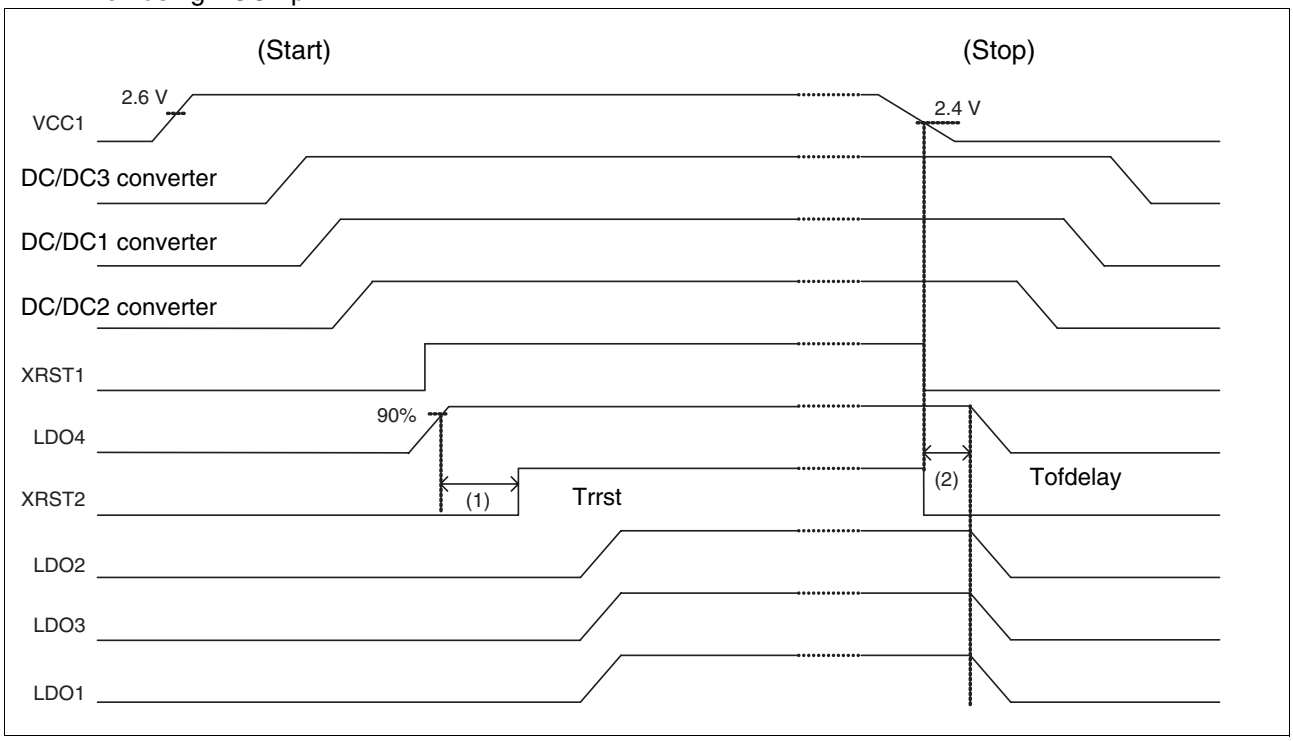
- VCC1 pin input voltage 2.4 V or less
- ONOFF pin input “L”
- When the REON bit in the REON register changes “0” to “1”
- OTP (Over temperature protection) detection



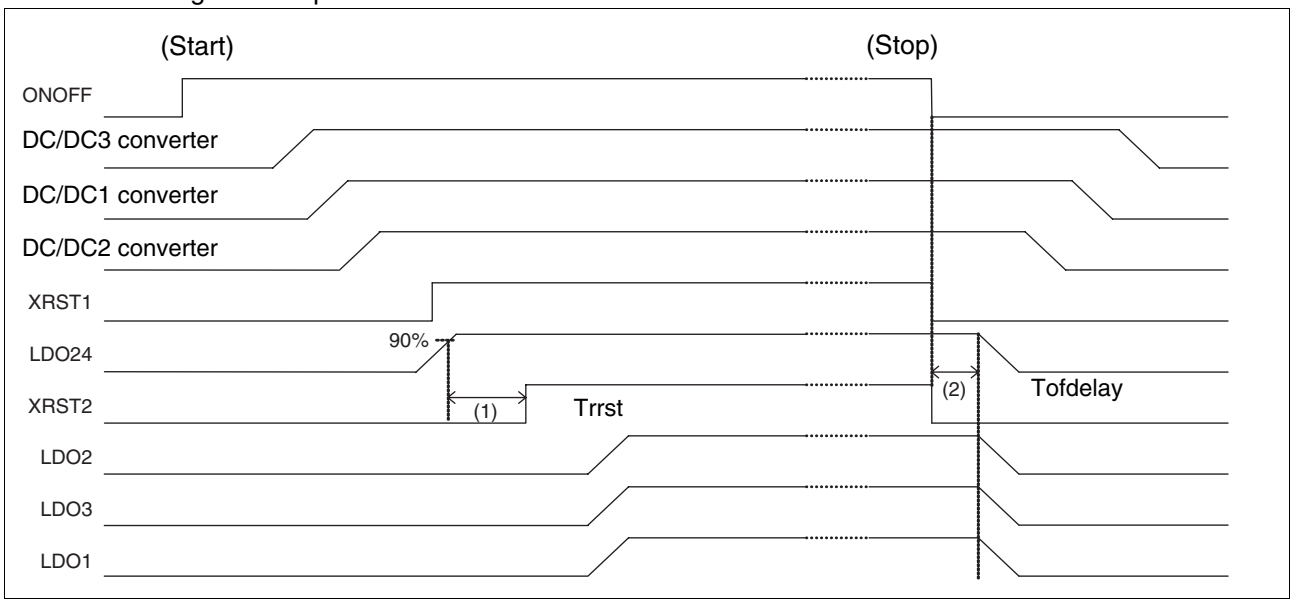
The start and stop status in the constant voltage power supply block by the VCC1 pin input voltage and the ONOFF pin input is reflected to the VCONT bit (address 05_H [0]) in the STATE register.

2. Start/stop sequence by VCC1 power supply pin and ONOFF pin

- When using VCC1 pin



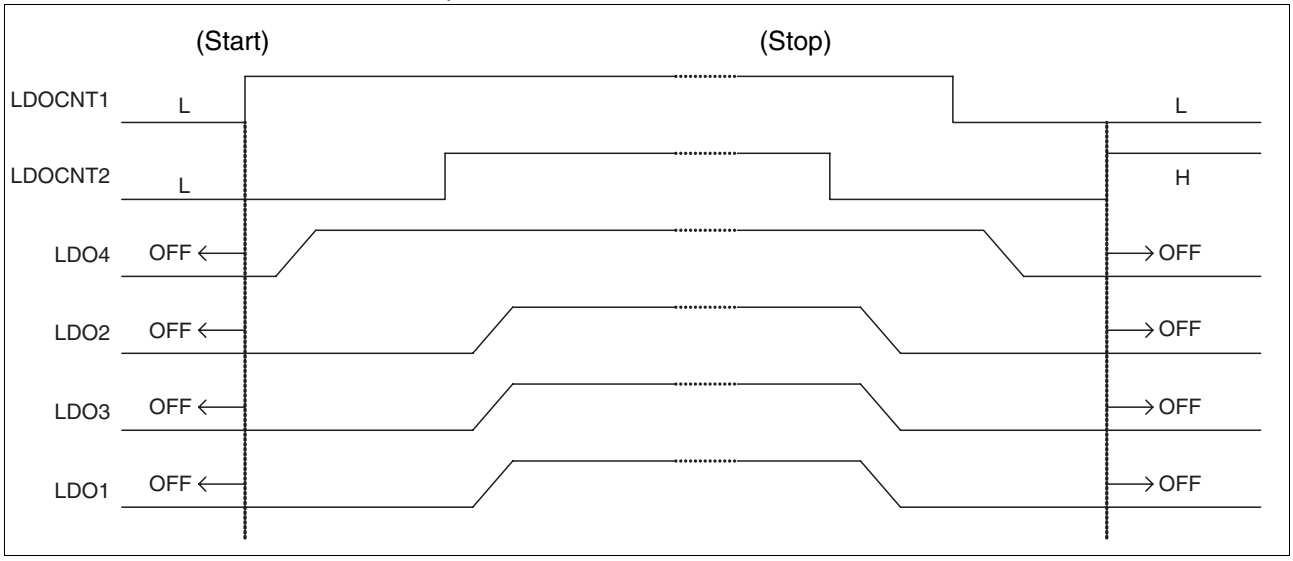
- When using ONOFF pin



Parameter	Symbol	Value			Unit
		Min	Typ	Max	
(1)	Trrst	4	5	6	ms
(2)	Tofdelay	150	200	250	µs

3. Start/stop by LDOCNT1 and LDOCNT2 pins (intermittent control)

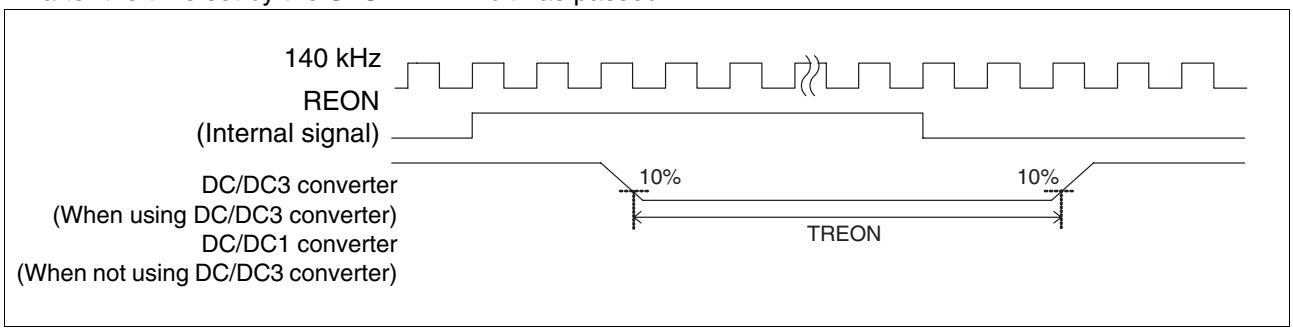
When the XRST1 and the XRST2 pins are in “H”, the LDO starts and stops depending on the conditions of the LDOCNT1 and the LDOCNT2 pins.



Input condition		LDO1	LDO2	LDO3	LDO4
LDOCNT1	LDOCNT2				
H	H	ON	ON	ON	ON
H	L	OFF	OFF	OFF	ON
L	L	OFF	OFF	OFF	OFF
L	H	OFF	OFF	OFF	OFF

4. Start/stop by REON register (Restart power supply)

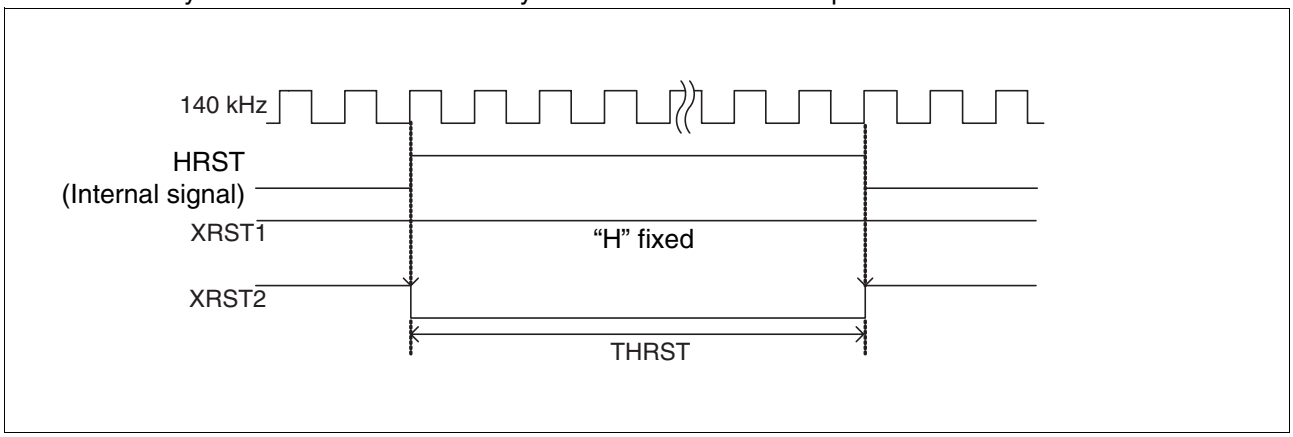
When “1” is written to the REON bit in the REON register (address 04_H [0]), the power supply stops following the sequence and starts again after a fixed period has passed.
The STOPTIMEB bit (address 04_H [5:4]) can set the time between the stop of the power supply and the restart of the power supply (calculated by the 140 kHz internal clock). The REON bit is automatically cleared after the time set by the STOPTIMEB bit has passed.



Parameter	STOPTIMEB bit [1:0]	Value			Unit
		Min	Typ	Max	
TREON	00_B	0.8	1.0	1.2	ms
	01_B	3.4	4.0	5.2	ms
	10_B	6.8	8.0	9.8	ms
	11_B	13.6	16.0	19.0	ms

5. Reset control by HRST register

When “1” is written to the HRST bit in the HRST register (address 03_H [0]), the output of XRST2 remains at “L” level for a fixed period.
The STOPTIMEA bit (address 03_H [5:4]) can set the time for remaining on XRST2 = “L”. The HRST bit is automatically cleared after the time set by the STOPTIMEA bit has passed.



Parameter	STOPTIMEA bit [1:0]	Value			Unit
		Min	Typ	Max	
THRST	00_B	0.8	1.0	1.2	ms
	01_B	3.4	4.0	5.2	ms
	10_B	6.8	8.0	9.8	ms
	11_B	13.6	16.0	19.0	ms

■ 32.768 kHz OUTPUT (CMOS output)

If the crystal oscillator is connected to the OSCIN and the OSCOUT pins, the 32.768 kHz clock can be output from the RTC_CLK pin.

■ I²C INTERFACE

This is the interface which is compliant with the I²C bus standard. The internal register data are read and write to the internal register data via two bidirectional bus lines which are the serial data line (SDA) and the serial clock line (SCL).
The MB39C316 has the following features.

- This LSI is set as slave, so the LSI cannot be set to master.
- The slave address is "2A$_H$".
- Supports high speed mode (Max 400 kbps)

1. Writing flow

(1) Detect start condition

(2) Receive slave address ("2A$_H$") and W/R bit ("0")

(3) Transmit ACK

(4) Receive register address

(5) Transmit ACK

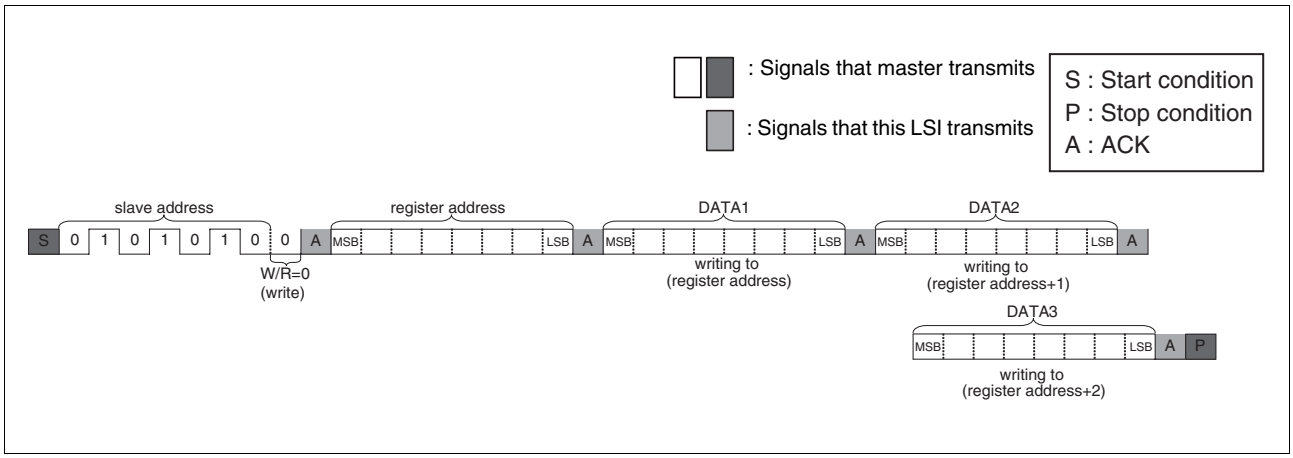
(6) Receive write data

(7) Transmit ACK

(8) Increase the register address and then go back to (6), when a stop condition is not detected.*

(9) Communication stops after detecting a stop condition.

* : Increment stops at address FF$_H$ and keeps at FF$_H$. The flow does not go back to 00$_H$.



Notes : • If the register address which does not exist or the bit which are not assigned is specified, ACK will be returned, but data will not be written.
• If writing is set to the Read Only address, ACK will not be returned, but data will not be written.

2. Reading flow

(1) Detect start condition

(2) Receive slave address (“2A$_H$”) and W/R bit (“0”)

(3) Transmit ACK

(4) Receive register address

(5) Transmit ACK

(6) Detect start condition

(7) Receive slave address (“2A$_H$”) and W/R bit (“1”)

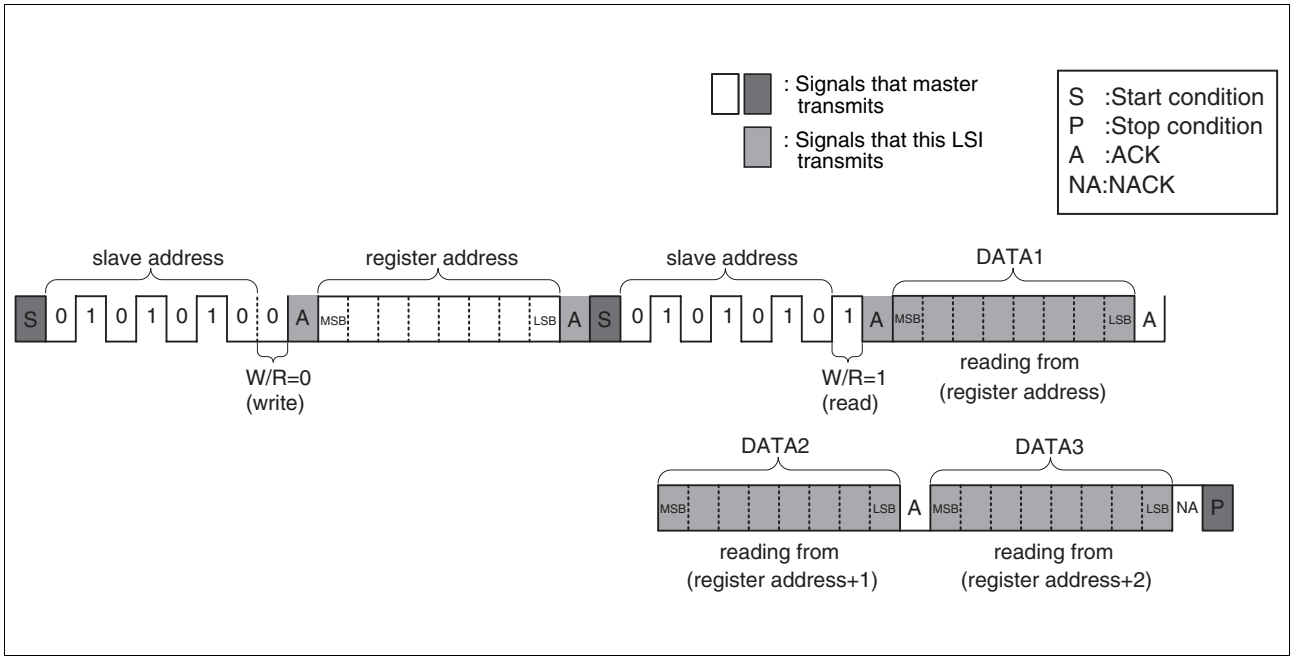
(8) Transmit ACK

(9) Transmission of read data

(10) Increase the register address and then go back to (9).*
If [1] ACK is received. Release the bus if [2] NACK is received.

(11) Communication stops after detecting a stop condition.

* : Increment stops at address FF$_H$ and keeps FF$_H$. Increment does not go back to 00$_H$.



Note : If the register address which does not exist and the bit which does not execute the bit assign are specified, read data becomes “0”.

■ REGISTERS

1. Address allocation

Address (hex)	Type	Register name (function)	W/R	Register Contents								Default value
				D7	D6	D5	D4	D3	D2	D1	D0	
00	Reset	SRST (Soft reset control)	*	RSTDET	—	—	—	—	—	—	SRST	0000 0000
01	Version	VERSION (Information about versions)	R	—	—	—	—	VER3	VER2	VER1	VER0	0000 0011
02	Constant voltage power supply	VSEL_SYN (LDO voltage setting)	WR	—	—	—	—	—	—	—	VSEL_SYN	0000 0000
03	Reset	HRST (Hard reset control)	WR	HRDET	—	STOPTIMEA1	STOPTIMEA0	—	—	—	HRST	0000 0000
04	Power supply control	REON (Control of re-starting power supply)	WR	REDET	—	STOPTIMEB1	STOPTIMEB0	—	—	—	REON	0000 0000
05	Notice of state	STATE (Notice of state)	R	—	—	—	—	CUR_lim	OTP	RTC_OSC	VCONT	0000 0000
06	General	GP (General-purpose register)	WR	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
07-7F	—	—	—	—	—	—	—	—	—	—	—	—
80-8B	TEST	reserved (reserved bytes)	—	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved	—
8C	—	—	—	—	—	—	—	—	—	—	—	—

* : 00_H [D0] is Write only, [D7] is Write/Read.

- Although data which "_" is shown is accessible to read and write, writing is invalid and reading data becomes "0".
- All registers are initialized to the default value by power-on reset.
- Executing the soft reset control initializes all Write registers to the default value. There is a possibility that written data during execution of the soft reset control is not reflected correctly.

Note : Address 80_H to $8B_H$ is mapped on the registers for this LSI test. It is prohibited to write to 80_H to $8B_H$ when using this LSI.

2. Functional description

• Soft reset control (Address 00_H)

	D7	D6	D5	D4	D3	D2	D1	D0
At Write	RSTDET	—	—	—	—	—	—	SRST
At Read	RSTDET	0	0	0	0	0	0	0
Default	0	0	0	0	0	0	0	0

bit [7] RSTDET : Register reset history bit

RSTDET	Operation
0	No execution of soft reset control (Read)/RSTDET clear bits (Write)
1	Execution of register reset by soft reset control (Read)

This bit saves the execution history of the reset operation by the soft reset control. If the reset operation by the soft reset control is executed, this bit is set to “1”.
When clearing this bit, write “00_H” to this register.
Writing RSTDET = “1” is ignored.

bit [0] SRST : Register reset bit

SRST	Operation
0	Normal operation
1	Reset the Write register for other than address 00_H.

If writing “1” to this bit, all Write registers are reset, and the read value for address 00_H is “80_H”.
The reset state will be remained for about 15 µs after writing SRST = “1”.
This bit is for the write only and the read value is always “0”.

Notes : • If RSTDET = “0” and SRST = “1” are written simultaneously, RSTDET = “0” is ignored. The reset operation by SRST = “1” is executed and the RSTDET bit is set to “1”.
• There is a possibility that written data during the soft reset control execution is not written correctly.

• Information about versions (Address 01_H)

	D7	D6	D5	D4	D3	D2	D1	D0
At Write	—	—	—	—	—	—	—	—
At Read	0	0	0	0	VER3	VER2	VER1	VER0
Default	0	0	0	0	Fixed value for each version			

bit [3:0] VER : Version display bit

VER	Operation
0000	—
0001	1
0010	2
0011	3
:	:

This register reads information about device's versions.

• LDO voltage setting (Address 02H)

	D7	D6	D5	D4	D3	D2	D1	D0
At Write	—	—	—	—	—	—	—	VSEL_SYN
At Read	0	0	0	0	0	0	0	VSEL_SYN
Default	0	0	0	0	0	0	0	0

bit [0] VSEL_SYN : Selection bit of LDO3 voltage

VSEL_SYN	Operation
0	1.2 V (Typ)
1	1.3 V (Typ)

This bit switches output voltage of LDO3.

• Hard reset control (Address 03H)

	D7	D6	D5	D4	D3	D2	D1	D0
At Write	HRDET	—	STOPTIMEA1	STOPTIMEA0	—	—	—	HRST
At Read	HRDET	0	STOPTIMEA1	STOPTIMEA0	0	0	0	HRST
Default	0	0	0	0	0	0	0	0

bit [7] HRDET : HRST history bit

HRDET	Operation
0	No execution of hard reset control (Read)/HRDET clear bits (Write)
1	Execution of XRST2 reset by hard reset control (Read)

This bit saves the execution history of the reset operation by the hard reset control. The reset operation by the hard reset control sets this bit to “1” (same time as re-writing of the HRST bit).
Write “00H” to this register when clearing this bit.
Writing HRDET = “1” is ignored.

bit [5:4] STOPTIMEA : XRST2 = “L” time setting bit

STOPTIMEA	Operation
00	1 ms (Typ)
01	4 ms (Typ)
10	8 ms (Typ)
11	16 ms (Typ)

This bit selects the time of XRST2 = “L” by the hard reset control.

bit [0] HRST : HRST Control bit

HRST	Operation
0	Normal operation (Read)
1	Instructions of hard reset control start (Write)

When writing “1” to this bit, the output of the XRST2 pin will remain in “L” for the time set by the STOPTIMEA bit.
This bit is automatically cleared after the time set has passed.

Note : If HRDET = “0” and HRST = “1” are written at the same time, HRDET = “0” is ignored. The reset operation is executed by HRST = “1” and the HRDET bit is set to “1”.