



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

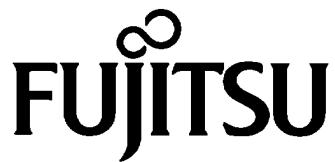
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MB86296S <CORAL PA>

PCI Graphics Controller

Specification

Revision 1.1
25 September, 2007



Copyright © FUJITSU LIMITED 2003-2004

ALL RIGHTS RESERVED

<Notes>

- The specifications in this manual are subject to change without notice. Contact our Sales Department before purchasing the product described in this manual.
- Information and circuit diagrams in this manual are only examples of device applications, they are not intended to be used in actual equipment. Also, Fujitsu accepts no responsibility for infringement of patents or other rights owned by third parties caused by use of the information and circuit diagrams.
- The contents of this manual must not be reprinted or duplicated without permission of Fujitsu.
- Fujitsu's semiconductor devices are intended for standard uses (such as office equipment (computers and OA equipment), industrial/communications/measuring equipment, and personal/home equipment). Customers using semiconductor devices for special applications (including aerospace, nuclear, military and medical applications) in which a failure or malfunction might endanger life or limb and which require extremely high reliability must contact our Sales Department first. If damage is caused by such use of our semiconductor devices without first consulting our Sales Department, Fujitsu will not assume any responsibility for the loss.
- Semiconductor devices fail with a known probability. Customers must use safety design (such as redundant design, fireproof design, over-current prevention design, and malfunction prevention design) so that failures will not cause accidents, injury or death).
- If the products described in this manual fall within the goods or technologies regulated by the Foreign Exchange and Foreign Trade Law, permission must be obtained before exporting the goods or technologies.



Burns There is a danger of burns because the IC surface is heated depending on the IC operating conditions. In this case, take safety measures.

All Rights Reserved

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering. The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams. The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

Update history

Date	Version	Page count	Change
28.2.2005	1.0	346	First edition
25.9.2007	1.1	356	Correct MMR Register (RAW > SAW) and some lingual improvements

CONTENTS

1. GENERAL	1
1.1 Preface	1
1.2 Features	2
1.3 Block Diagram	3
1.4 Functional Overview	4
1.4.1 Host CPU interface	4
1.4.2 External memory interface	5
1.4.3 Display controller.....	6
1.4.4 Video capture function	8
1.4.5 Geometry processing	9
1.4.6 2D Drawing.....	10
1.4.7 3D Drawing.....	12
1.4.8 Special effects	13
1.4.9 Others.....	15
2. PINS	16
2.1 Signals.....	16
2.1.1 Signal lines.....	16
2.2 Pin Assignment.....	17
2.2.1 Pin assignment diagram.....	17
2.2.2 Pin assignment table.....	18
2.3 Pin Function.....	26
2.3.1 Host CPU interface	26
2.3.2 Video output interface	28
2.3.3 Video capture interface	30
2.3.4 I ² C interface.....	31
2.3.5 Graphics memory interface	32
2.3.6 Clock input.....	33
2.3.7 Test pins	34
2.3.8 Reset sequence	34
2.3.9 How to switch internal operating frequency	34
3. PROCEDURE OF THE HARDWARE INITIALIZATION	35
3.1. Hardware reset.....	35
3.2. Re-reset.....	35
3.3. Software reset.....	35
4. HOST INTERFACE	36
4.1 Standard PCI Slave Accesses	36
4.1.1 PCI Slave Write	36
4.1.2 PCI Slave Read.....	36
4.2 Burst Controller Accesses (including PCI Master).....	36
4.2.1 Transfer Modes	37
4.2.2 Burst Controller Control/Status.....	38
4.3 FIFO Transfers.....	39
4.4 GPIO/Serial Interface.....	39
4.4.1 GPIO	39
4.4.2 Serial Interface	39
4.5 Interrupt.....	40
4.5.1 Address Error Interrupt.....	40
4.6 Memory Map	41
5. I²C Interface Controller	43

5.1 Features	43
5.2 Block diagram.....	44
5.2.1 Block Diagram	44
5.2.2 Block Function Overview.....	45
5.3 Example application	46
5.3.1 Connection Diagram	46
5.4 Function overview.....	47
5.4.1 START condition.....	47
5.4.2 STOP condition	47
5.4.3 Addressing.....	48
5.4.4 Synchronization of SCL.....	48
5.4.5 Arbitration	49
5.4.6 Acknowledge	49
5.4.7 Bus error.....	49
5.4.8 Initialize	50
5.4.9 1-byte transfer from master to slave	51
5.4.10 1-byte transfer from slave to master	52
5.4.11 Recovery from bus error.....	53
5.5 Note	54
6. Graphics Memory	55
6.1. Configuration	55
6.1.1. Data type	55
6.1.2. Memory Mapping	56
6.1.3. Data Format	56
6.2. Frame Management	58
6.2.1. Single Buffer.....	58
6.2.2. Double Buffer	58
6.3. Memory Access	58
6.3.1. Memory Access by host CPU.....	58
6.3.2. Priority of memory accessing	58
6.4. Connection with memory	59
6.4.1. Connection with memory.....	59
7. DISPLAY CONTROLLER	60
7.1 Overview.....	60
7.2 Display Function	61
7.2.1 Layer configuration.....	61
7.2.2 Overlay	62
7.2.3 Display parameters	64
7.2.4 Display position control	65
7.3 Display Color	67
7.4 Cursor.....	68
7.4.1 Cursor display function.....	68
7.4.2 Cursor control.....	68
7.5 Display Scan Control	69
7.5.1 Applicable display.....	69
7.5.2 Interlace display	70
7.6 Video Interface, NTSC/PAL Output	71
7.7 Programmable YCbCr/RGB conversion for L1-layer display	72
7.8 DCLKO shift	74
7.9 Syncronous register update of display.....	74

7.10 Dual Display	75
7.10.1 Overview	75
7.10.2 Destination Control.....	75
7.10.3 Output Signal Control.....	76
7.10.4 Output Circuit Example	77
7.10.5 Display Clock and Timing.....	79
7.10.6 Limitation	79
8. Video Capture	80
8.1 Video Capture function	80
8.1.1 Input data Formats	80
8.1.2 Capturing of Video Signal	80
8.1.3 Non-interlace Transformation.....	80
8.2 Video Buffer	81
8.2.1 Data Form	81
8.2.2 Synchronous Control.....	81
8.2.3 Area Allocation.....	81
8.2.4 Window Display.....	82
8.2.5 Interlace Display.....	82
8.2.6 RGB555 Mode.....	82
8.3 Scaling	83
8.3.1 Down-scaling Function.....	83
8.3.2 Up-scaling Function	83
8.3.2 Flow of image processing	85
8.4 External video signal input conditions	88
8.4.1 RTB656 YUV422 input format.....	88
8.4.2 RGB input format.....	90
1) RGB Input Signals	90
2) Captured Range	90
3) Input Operation	92
4) Conversion Operation	94
8.5 Input Video Signal Parameter Setup	95
9. GEOMETRY ENGINE	96
9.1 Geometry Pipeline	96
9.1.1 Processing flow	96
9.1.2 Model-view-projection (MVP) transformation (OC→CC coordinate transformation)	97
9.1.3 3D-2D transformation (CC→NDC coordinate transformation).....	97
9.1.4 View port transformation (NDC→DC coordinate transformation)	98
9.1.5 View volume clipping.....	98
9.1.6 Back face culling	100
9.2 Data Format.....	101
9.2.1 Data format.....	101
9.3 Setup Engine	102
9.3.1 Setup processing	102
9.4 Log Output of Device Coordinates	102
9.4.1 Log output mode	102
9.4.2 Log output destination address	102
9.4.3 Log output format	102
10. DRAWING PROCESSING	103
10.1 Coordinate System	103
10.1.1 Drawing coordinates	103

10.1.2 Texture coordinates	104
10.1.3 Frame buffer.....	104
10.2 Figure Drawing	105
10.2.1 Drawing primitives	105
10.2.2 Polygon drawing function	105
10.2.3 Drawing parameters	106
10.2.4 Anti-aliasing function	107
10.3 Bit Map Processing.....	108
10.3.1 BLT	108
10.3.2 Pattern data format	108
10.4 Texture Mapping	109
10.4.1 Texture size	109
10.4.2 Texture color.....	109
10.4.3 Texture Wrapping	110
10.4.4 Filtering.....	111
10.4.5 Perspective correction.....	111
10.4.6 Texture blending	112
10.4.7 Bi-linear high-speed mode	112
10.5 Rendering	114
10.5.1 Tiling	114
10.5.2 Alpha blending.....	114
10.5.3 Logic operation.....	115
10.5.4 Hidden plane management.....	115
10.6 Drawing Attributes	116
10.6.1 Line drawing attributes	116
10.6.2 Triangle drawing attributes	116
10.6.3 Texture attributes.....	117
10.6.4 BLT attributes	118
10.6.5 Character pattern drawing attributes.....	118
10.7 Bold Line.....	119
10.7.1 Starting and ending points.....	119
10.7.2 Broken line pattern	120
10.7.3 Edging	121
10.7.4 Interpolation of bold line joint	122
10.8 Shadowing	123
10.8.1 Shadowing.....	123
11 DISPLAY LIST	124
11.1 Overview	124
11.1.1 Header format.....	125
11.1.2 Parameter format.....	125
11.2 Geometry Commands.....	126
11.2.1 Geometry command list	126
11.2.2 Explanation of geometry commands	130
11.3 Rendering Command.....	139
11.3.1 Command list.....	139
11.3.2 Details of rendering commands	143
12. PCI Configuration Registers	154
12.1 PCI Configuration register list.....	154
12.2 PCI Configuration Registers Descriptions	155
13 Local Memory Registers	158

13.1 Local memory register list.....	158
13.1.1 Host interface register list.....	158
13.1.2 I ² C interface register list	160
13.1.3 Graphics memory interface register list	160
13.1.4 Display controller register list	161
13.1.5 Video capture register list.....	167
13.1.6 Drawing engine register list.....	169
13.1.7 Geometry engine register list	175
13.2 Explanation of Local Memory Registers.....	176
13.2.1 Host interface registers	177
13.2.2 I ² C Interface Registers	192
13.2.3 Graphics memory interface registers	198
13.2.4 Display control register.....	201
13.2.5 Video capture registers	255
13.2.6 Drawing control registers	271
13.2.7 Drawing mode registers	274
13.2.8 Triangle drawing registers	291
13.2.9 Line drawing registers	294
13.2.10 Pixel drawing registers	295
13.2.11 Rectangle drawing registers	295
13.2.12 Blt registers	296
13.2.13 High-speed 2D line drawing registers	297
13.2.14 High-speed 2D triangle drawing registers.....	298
13.2.15 Geometry control register.....	299
13.2.16 Geometry mode registers.....	301
13.2.17 Display list FIFO registers	308
14. TIMING DIAGRAM	309
14.1 Host Interface	309
14.1.1 PCI Interface	309
14.1.2 EEPROM Timing	310
14.1.3 Serial Interface Timing	311
14.2 I ² C Interface.....	312
14.3 Graphics Memory Interface	313
14.3.1 Timing of read access to same row address.....	313
14.3.2 Timing of read access to different row addresses.....	314
14.3.3 Timing of write access to same row address	315
14.3.4 Timing of write access to different row addresses	316
14.3.5 Timing of read/write access to same row address	317
14.3.6 Delay between ACTV commands	318
14.3.7 Delay between Refresh command and next ACTV command.....	318
14.4 Display Timing	319
14.4.1 Non-interlace mode.....	319
14.4.2 Interlace video mode	320
14.4.3 Composite synchronous signal	321
15. ELECTRICAL CHARACTERISTICS	322
15.1 Introduction.....	322
15.2 Maximum Rating.....	322
15.3 Recommended Operating Conditions	323
15.3.1 Recommended operating conditions	323
15.3.2 Note at power-on.....	324

15.4 DC Characteristics.....	325
15.4.1 DC Characteristics of PCI Buffer.....	325
15.4.2 DC Characteristics of other than PCI buffer.....	327
15.5 AC Characteristics	329
15.5.1 Host interface	329
15.5.2 I ² C Interface	330
15.5.3 Video interface	331
15.5.4 Video capture interface	333
15.5.5 Graphics memory interface	334
15.6 AC Characteristics Measuring Conditions	340
15.7 Timing Diagram	341
15.7.1 Host interface	341
15.7.2 Video interface	342
15.7.3 Video capture interface	344
15.7.4 Graphics memory interface	345

1. GENERAL

1.1 Preface

The MB86296S <CORAL-PA> is a graphics controller with a PCI host interface.

Note:

This device has a I²C interface. Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Right to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

1.2 Features

- Geometry Engine

The Geometry Engine supports the geometry processing that is basically compatible**1 with ORCHID (MB86292). Display lists generated for ORCHID can be processed. Extensive geometric operation processing such as coordinate conversions or clipping which normally load the CPU dramatically can be reduced using the Geometry Engine. **1 (Floating point setup command is changed or deleted. G_BeginCont command is deleted. GMDR0 CF&DF table mapping is changed ... etc)

- 2D and 3D Drawing

MB86296's drawing functionality is compatible to the CREMON (MB86290A). It can draw data using the display lists created for CREMON (however internal texture RAM is deleted).

The MB86296 also supports 3D rendering, such as texture mapping with perspective correction and Gouraud shading, alpha blending and anti-aliasing for drawing smooth lines.

- Digital video capture

The digital video capture function can store digital video data such as TV images in graphics memory; it can display drawn images and video images on the same screen.

- Display controller

The MB86296 has a display controller that is compatible with ORCHID.

In addition to the traditional XGA (1024×768 pixels) display, 4-layer overlay, left/right split display, wrap-around scrolling, double buffers, and translucent display, 6-layer overlay functionality, 4-siding for palette are expanded.

- Host CPU interface

The MB86296 has a 32 bit, 33MHz PCI interface fully compliant to PCI version 2.1.

- External memory interface

SDRAM and FCRAM can be connected.

- Optional function

Final device can be selected from the combination of geometry high-/low-speed version and video capture function provided/ not provided.

- Others

CMOS technology 0.18μm

BGA256 Package

Supply voltage: 1.8 V (internal operation) / 3.3 V (I/O)

Current consumption (TYPICAL)

1.8 V : 500mA

3.3 V : 100mA

1.3 Block Diagram

The CORAL-PA general block diagram is shown below:

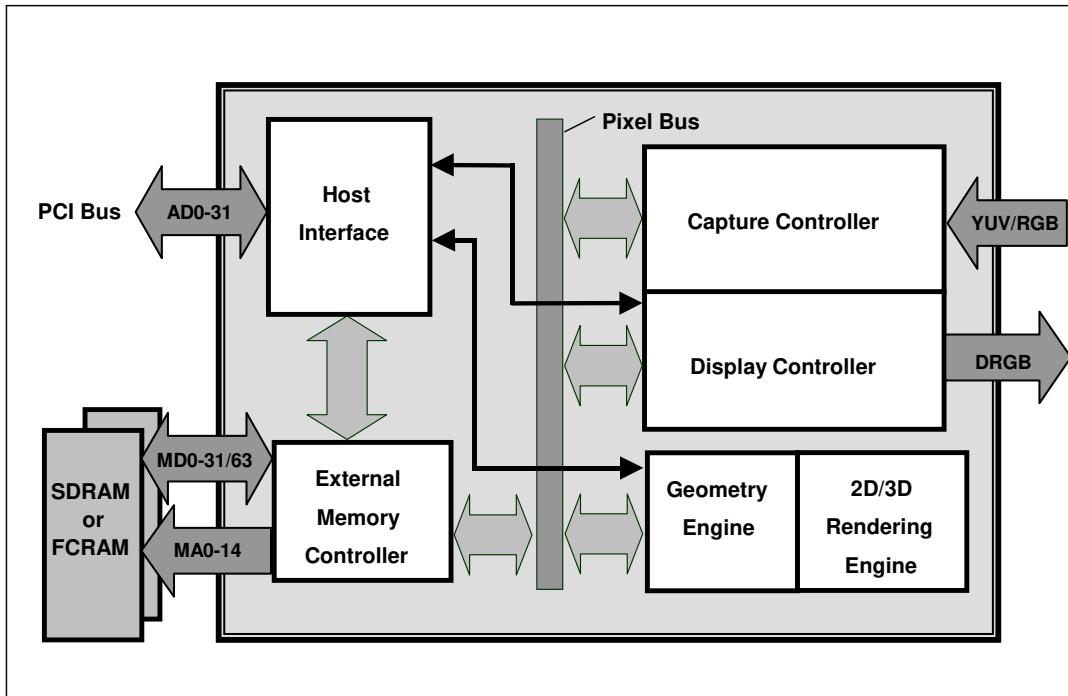


Fig.1.1 CORAL-PA Block Diagram

1.4 Functional Overview

1.4.1 Host CPU interface

Supported CPU

The MB86296 can be connected to any CPU with a 33MHz 32-bit PCI v2.1 host interface.

Configuration

EEPROM configuration supported

Serial interface for external device control through PCI interface

PCI Slave

Supports burst reads/writes of up to 8 double words (32 bytes).

Supports multi-burst transfers with automatic pre-fetch.

PCI Master

Supports transfers of up to $2^{24}-1$ double words in bursts of between 1 and 8 double words.

Supports all combinations of transfer (PCI->PCI, PCI->Internal, Internal->PCI)

Host notification on burst complete and/or transfer complete

Optional external burst initiation control

Internal DMA

Supports transfers of up to $2^{24}-1$ double words in bursts of between 1 and 8 double words.

Interrupt

Vertical (frame) synchronous detection

Field synchronous detection

External synchronous error detection

Register update

Drawing command error

Drawing command execution end

Burst/Transfer complete

1.4.2 External memory interface

SDRAM or FCRAM can be connected.

64 bits or 32 bits can be selected for data bus.

Max. 133 MHz is available for operating frequency.

Connectable memory configuration is as shown below.

External Memory Configuration

Type	Data bus width	Use count	Total capacity
FCRAM 16 Mbits (x16 Bits)	32 Bits	2	4 Mbytes
SDRAM 64 Mbits (x32 Bits)	32 Bits	1	8 Mbytes
SDRAM 64 Mbits (x32 Bits)	64 Bits	2	16 Mbytes
SDRAM 64 Mbits (x16 Bits)	32 Bits	2	16 Mbytes
SDRAM 128 Mbits (x32 Bits)	32 Bits	1	16 Mbytes
SDRAM 128 Mbits (x32 Bits)	64 Bits	2	32 Mbytes
SDRAM 128 Mbits (x16 Bits)	32 Bits	2	32 Mbytes
SDRAM 256 Mbits (x16 Bits)	32 Bits	2	64 Mbytes

1.4.3 Display controller

Video data output

Analog RGB video output is provided as well as 8-bit digital video output is provided. When selecting each 8 bits output, usable external memory bus width is 32 bits only.

Screen resolution

LCD panels with wide range of resolutions are supported by using a programmable timing generator as follows:

Screen Resolutions

Resolutions
1024 × 768
1024 × 600
800 × 600
854 × 480
640 × 480
480 × 234
400 × 234
320 × 234

Hardware cursor

MB86296S supports two hardware cursor functions. Each of these hardware cursors is specified as a 64×64 -pixel area. Each pixel of these hardware cursors is 8 bits and uses the same look-up table as indirect color mode.

Double buffer method

The double buffer method in which drawing window and display window is switched in units of 1 frame enables the smooth animation.

Flipping (switching of display window area) is performed in synchronization with the vertical blanking period using program.

Scroll method

Independent setting of drawing and display windows and their starting position enables the smooth scrolling.

Display colors

- Supports indirect color mode which uses the look-up table (color palette) in 8 bits/pixels.
- Entry for look-up table (color palette) corresponds to color code for 8 bits, in other words, 256. Color data is each 6 bits of RGB. Consequently, 256 colors can be displayed out of 260,000 colors.
- Supports direct color mode which specifies RGB with 16 bits/pixels.
- Supports direct color mode which specifies RGB with 24 bits/pixels.

Overlay

Compatibility mode

Up to four extra layers (C, W, M and B) can be displayed overlaid.

The overlay position for the hardware cursors is above/below the top layer (C).

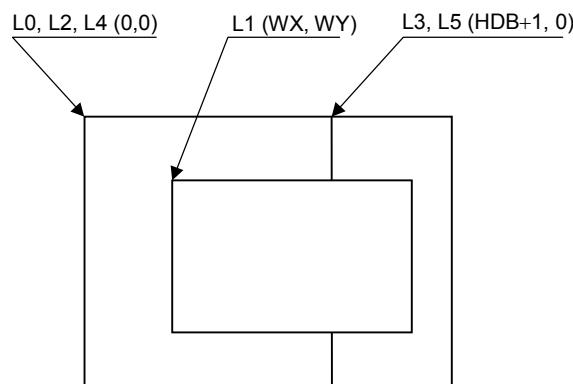
The transparent mode or the blend mode can be selected for overlay.

The M- and B-layers can be split into separate windows.

Window display can be performed for the W-layer.

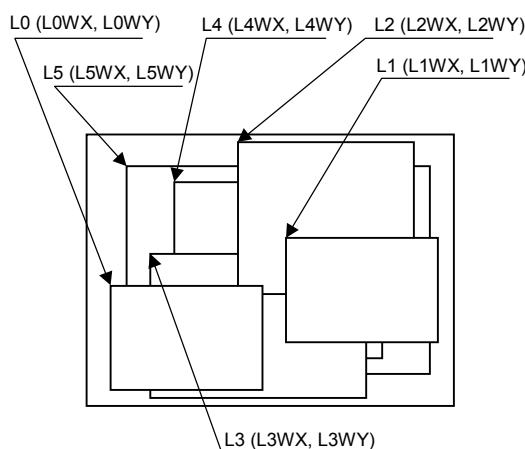
Two palettes are provided: C-layer and M-/B-layer.

The W-layer is used as the video input layer.



Window mode

- Up to six screens (L0 to 5) can be displayed overlaid.
- The overlay sequence of the L0- to L5-layers can be changed arbitrarily.
- The overlay position for the hardware cursors is above/below the L0-layer.
- The transparent mode or the blend mode can be selected for overlay.
- The L5-layer can be used as the blend coefficient plane (8 bits/pixel).
- Window display can be performed for all layers.
- Four palettes corresponded to L0 to 3 are provided.
- The L1-layer is used as the video input layer.
- Background color display is supported in window display for all layers.



1.4.4 Video capture function

Video input

- The input format is either ITU RBT-656 or RGB666.
- Video data is stored in graphics memory once and then displayed on the screen in synchronization with the display scan.

Scaling

- A scale-up factor 1 to 2 can be used. PAL or NTSC images can be displayed on a wide screen.
- A scale-down factor 1 to 1/32 can be used.
- Picture-in-picture can be used to display drawn images and video images on the same screen.

1.4.5 Geometry processing

The MB86296 has a geometry engine for performing the numerical operations required for graphics processing. The geometry engine uses the floating-point format for highly precise operations. It selects the required geometry processing according to the set drawing mode and primitive type and executes processing to the final drawing.

Primitives

Point, line, line strip, independent triangle, triangle strip, triangle fan, and arbitrary polygon are supported.

MVP Transformation

MVP Transformation

Setting a 4×4 transformation matrix enables transformation of a 3D model view projection. Two-dimensional affine transformation is also possible.

Clipping

Clipping stops drawing of figures outside the window (field of view). Polygons (including concave shapes) can also be clipped.

Culling

Backfacing triangles are not drawn.

3D-2D Transformation

This function transforms 3D coordinates (normalization) into 2D coordinates in orthogonal or perspective projections.

View port transformation

This function transforms normalized 2D coordinates into drawing (device) coordinates.

Primitive setup

This function automatically performs a variety of slope computations, etc., based on transforming vertex data into coordinates and prepares for rendering (setup).

Log output of device coordinates

The view port conversion results are output to the local memory.

1.4.6 2D Drawing

2D Primitives

MB86296S can perform 2D drawing for graphics memory (drawing plane) in direct color mode or indirect color mode.

Wide bold lines and broken lines can be drawn. Smooth diagonal lines can also be drawn using anti-aliasing.

A triangle can be tiled in a single color or 2D pattern (tiling) or mapped with a texture pattern by specifying coordinates of the 2D pattern at each vertex (texture mapping). With texture mapping, drawing/non-drawing can be set in pixel units. Moreover, transparent processing can be performed using alpha blending. When drawing in single color or tiling without Gouraud shading or texture mapping, high-speed 2DLine and high-speed 2DTriangle functions can be used. Only vertex coordinates are set for these primitives. High-speed 2DTriangle is also used to draw polygons.

2D Primitives

Primitive type	Description
Point	Plots point
Line	Draws line
Bold line strip (provisional name)	Draws continuous bold line This primitive is used when interpolating the bold line joint.
Triangle	Draws triangle
High-speed 2DLine	Draws lines Compared to line, this reduces the host CPU processing load.
Arbitrary polygon	Draws arbitrary closed polygon containing concave shapes consisting of vertices

Arbitrary polygon drawing

Using this function, arbitrary closed polygons containing concave shapes consisting of vertices can be drawn (there is no restriction on the count of vertices, however, polygons with crossing sides are not supported.) In this case, a polygon drawing flag buffer is used on the graphics memory, as a work area for drawing. When drawing polygons, draw the triangles for the polygon drawing flag buffer using high-speed 2DTriangle. Decide on any vertex as a starting point to draw the triangle along the edge. You can draw the final polygon form in a single color or with tiling or with texture mapping in a drawing frame.

BLT/Rectangle drawing

This function draws a rectangle using logic operations. It is used to draw pattern and copy the image pattern within the drawing frame. It is also used for clearing drawing frame and Z buffer.

BLT Attributes

Attribute	Description
Raster operation	Selects two source logical operation mode
Transparent processing	Performs BLT without drawing pixel consistent with the transparent color.
Alpha blending	The alpha map and source in the memory is subjected to alpha blending and then copied to the destination.

Pattern (Text) drawing

This function draws a binary pattern (text) in a specified color.

Pattern (Text) Drawing Attributes

Attribute	Description
Enlarge	Vertically $\times 2$ Horizontally $\times 2$ Vertically and Horizontally $\times 2$
Shrink	Vertically $\times 1/2$ Horizontally $1/2$ Vertically and Horizontally $1/2$

Drawing clipping

This function sets a rectangle frame in drawing frame to prohibit the drawing of the outside the frame.

1.4.7 3D Drawing

3D Primitives

This function draws 3D objects in drawing memory in the direct color mode.

3D Primitives

Primitive	Description
Point	Plots 3D point
Line	Draws 3D line
Triangle	Draws 3D triangle
Arbitrary polygon	Draws arbitrary closed polygon containing concave shapes consisting of vertexes

3D Drawing attributes

Texture mapping with bi-linear filtering/automatic perspective correction and Gouraud shading provides high-quality realistic 3D drawing. A built-in texture mapping unit performs fast pixel calculations. This unit also delivers color blending between the shading color and texture color.

Hidden plane management

MB86296S supports the Z buffer for hidden plane management.

1.4.8 Special effects

Anti-aliasing

Anti-aliasing manipulates line borders of polygons in sub-pixel units and blend the pre-drawing pixel color with color to make the jaggies be seen smooth. It is used as a functional option for 2D drawing (in direct color mode only).

Bold line and broken line drawing

This function draws lines of a specific width and a broken line.

Line Drawing Attributes

Attribute	Description
Line width	Selectable from 1 to 32 pixels
Broken line	Set by 32 bit or 24 bit of broken line pattern

- Supports the verticality of starting and ending points.
- Supports the verticality of broken line pattern.
- Interpolation of bold line joint supports the following modes:
 - (1) Broken line pattern reference address fix mode
 - The same broken line pattern is kept referencing for the period of some pixels starting from the joint and the starting point for the next line.
 - (2) No interpolation
- Supports the equalization of the width of bold lines.
- Supports the bold line edging.
- Not support the Anti-aliasing of dashed line patterns.
- For a part overlaid due to connection of bold lines, natural overlay can be represented by providing depth information. (Z value).

Shading

Supports the shading primitive.

Drawing is performed to the body primitive coordinates (X, Y) with an offset as a shade. At this drawing, the Z buffer is used in order to differentiate between the body and shade.

Alpha blending

Alpha blending blends two image colors to provide a transparent effect. CORAL supports two types of blending; blending two different colors at drawing, and blending overlay planes at display. Transparent color is not used for these blending options.

There are two ways of specifying alpha blending for drawing:

- (1) Set a transparent coefficient to the register; the transparent coefficient is applied for transparency processing of one plane.
- (2) Set a transparent coefficient for each vertex of the plane; as with Gouraud shading, the transparent coefficient is linear-interpolated to perform transparent processing in pixel units.

In addition to the above, the following settings can be performed at texture mapping. When the most significant bit of each texture cell is 1, drawing or transparency can be set. When the most significant bit of each texture cell is 0, non-drawing can be set.

Alpha Blending

Type	Description
Drawing	<p>Transparent ratio set in particular register</p> <p>While one primitive (polygon, pattern, etc.), being drawn, registered transparent ratio applied</p> <p>A transparent coefficient set for each vertex. A linear-interpolated transparent coefficient applied.</p> <p>This is possible only in direct color mode.</p>
Overlay display	<p>Blends top layer pixel color with lower layer pixel color</p> <p>Transparent coefficient set in particular register</p> <p>Registered transparent coefficient applied during one frame scan</p>

Gouraud Shading

Gouraud shading can be used in the direct color mode to provide 3D object real shading and color gradation.

Gray Scale Gouraud Shading

Gray scale gouraud shading can be used in the in-direct color mode to draw a blend coefficient layer.

Texture mapping

MB86296 supports texture mapping to map a image pattern onto the surface of plane. For 2D pattern texture mapping, MB86296 has a built-in pattern memory for a field of up to 64×64 pixels (at 16-bit color), which performs high-speed texture mapping. The texture pattern can also be laid out in the graphics memory. In this case, max. 4096×4096 pixels can be used.

Drawing of 8-/16-bit direct color is supported for the texture pattern. For drawing 8-bit direct color, only point sampling can be specified for texture interpolation; only decal can be specified for the blend mode.

Texture Mapping

Function	Description
Filtering	Point sample Bi-linear filter
Coordinates correction	Linear Perspective
Blend	Decal Modulate Stencil
Alpha blend	Normal Stencil Stencil alpha
Wrap	Repeat Clamp Border

1.4.9 Others

Top-left rule non-applicable mode

In addition to the top-left rule applicable mode in which the triangle borders are compatible with CREMSON, the top-left rule non-applicable mode can be used.

Caution: Use perspective correct mode when use texture at the top-left rule non-applicable mode.

Top-left rule non-applicable primitives cannot use Geometry clip function.

Non-top-left-part's pixel quality is less than body. (using approximate calculation)