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MB86R01

DATA SHEET

July, 2009 the 1.4 edition

FUJITSU

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Revision History

Date	Ver.	Contents
2007/07/12	1.0	Newly issued
2007/08/20	1.1	8.3.1. Recommended Power On/Off Sequence • Revised the last line of description (PLL reference clock part) 8.4.3. ADC • Revised value of table 8-16 • Revised and deleted descriptive content of note • Revised footnote (*2) of table 8-17 8.4.4. I^2C Bus Fast Mode I/O • Revised table 8-18 and footnote • Deleted footnote (*3) 8.5.9. I^2C Bus Timing • Revised footnote (*2) of table 8-37 8.5.12. MLB Signal Timing • Revised MLB to MediaLB • Revised footnote of table 8-42, 8-45
2007/11/09	1.2	4. Function list • Revised contents of the list 6. Pin assignment • Revised figures in 1-8/1-9 pages • Added "top view" statement 7.1. Pin Multiplex • Revised description of note • Added mode setting description to pin multiplex group #1 ~ #5 • Revised table of pin multiplex group #2 and #4 7.2.4. USB 2.0 Host/Function related pin • Revised description of USB_EXT12K pin 7.2.5. External interrupt controller related pin • Revised title 7.2.12. A/D converter related pin • Revised pin name: AD_AVD0 → AD_AVD, AD_AVS1 → AD_AVS 7.2.24. Unused pin • Added this section 7.2.25. Unused pin with pin multiplex function in the duplex case • Added this section 8.4.2. DDR2SDRAM IF I/O (SSTL_18) • Revised table 8-12 8.5.1. Memory Controller Signal Timing • Revised table 8-21 • Revised figure 8-8 and 8-9 • Added figure 8-10, 8-11, and 8-12 8.5.6.2. Input Signal • Revised figure 8-23
2008/02/07	1.3	6. Pin assignment • Revised figure and table 7.2.2. IDE66 related pin • Revised type • Revised status pin after reset 7.2.3. SD memory controller related pin • Unified SD_DAT[0] and SD_DAT[3:1] 7.2.7. CAN related pin • Revised type

Date	Ver.	Contents
2008/02/07	1.3	7.2.8. I2S related pin • Revised type • Revised status pin after reset 7.2.10. SPI related pin • Revised type 7.2.11. PWM related pin • Revised type • Added comment 7.2.13. DDR2 related pin • Revised resistance value of *2 7.2.15. Video captured related pin • Revised type • Added comment 7.2.18. ICE related pin • Revised status pin after reset of XSRST 7.2.20. ETM related pin • Revised pin name in description column of TRACECLK 7.2.22. MediaLB related pin • Revised pin name • Revised type 7.2.24. Unused pin • Revised process • Deleted BIGEND • Revised pin name of B17, B16, C17, C16, and D16 7.2.25. Unused pin with pin multiplex function in the duplex case • Revised process 8.1. Maximum Ratings • Revised table 8-1
2009/07/07	1.4	7.2.14. DISPLAY related pin • Added note 8.1. Maximum Ratings • Revised table 8-1 8.3.2. Power On Reset • Revised figure 8-3 • Revised description 8.5.5.1. Clock • Revised table 8-28 8.5.7. I2S Signal Timing • Revised table 8-34 and 8-35 8.5.10. SPI Signal Timing • Revised table 8-38

Contents

1. Outline

MB86R01 is LSI product for the graphics applications with ARM Limited's CPU ARM926EJ-S and Fujitsu's GDC MB86296 as its core. This product contains peripheral I/O resources, such as in-vehicle LAN, HDD, and USB; therefore only a single chip of MB86R01 controls main graphics application system which usually requires 2 chips (CPU and GDC.)

2. Feature

- CMOS 90nm technology
- Package: PBGA484
- Power-supply voltage: (IO: 3.3 ± 0.3V, core: 1.2 ± 0.1V, DDR2: 1.8 ± 0.1V)
- Operation frequency: 333MHz (CPU), 83MHz (AHB), 41.5MHz (APB)
- CPU core
  - ARM926EJ-S
  - 16KB instruction cache/16KB data cache
  - 16KB ITCM/16KB DTCM
  - ETM9CS Single and JTAG ICE interface
  - Java acceleration (Jazelle technology)
- Bus architecture
  - Multi-layer AHB bus architecture
- Interrupt
- Built-in SRAM
- Clock/Reset control function
- Remap/Boot control function
- 16 bit external bus interface with decoding engine
- 32 bit DDR2 memory interface (target: 166MHz: 333Mbps)
- Graphics display controller
  - 2D/3D rendering engine of Fujitsu MB86296
  - RGB66 video output × 1ch (extensible to RGB888 with using option I/O)
  - ITU RBT-656 video capture × 1ch (extensible to RGB666 with using option I/O)
- USB 2.0 host (HS/FS protocols) × 1ch
- IDE66 (ATA/ATAPI-5) × 1ch
- SD memory interface (SDIO/CPRM: unsupported) × 1ch
- 10 bit A/D converter (1MS/s) × 2ch
- I^2C (I/O voltage: 3.3V) × 2ch
- UART × 3ch (extensible up to 6ch with using option I/O)
- 32/16 bit timer × 2ch
- DMAC × 8ch

Option I/O (with pin multiplex)

- RGB666 video output is extensible to 2ch
- Video capture is extensible to 2ch
- MediaLB (MOST50) × 1ch is addable
- CAN (I/O voltage: 3.3V) × 2ch is addable
- USB 2.0 function (HS/FS protocols) is switchable (USB 2.0 function and USB 2.0 host are accessed exclusively)
- GPIO is addable up to 24
- SPI × 1ch is addable
- PWM × 2ch is addable

- I2S is addable up to 3ch
- The number of UART channel is extensible up to 6ch
- The data width in the external bus interface is extensible to 32 bit

3. Block diagram

Figure 3-1 shows block diagram of MB86R01.

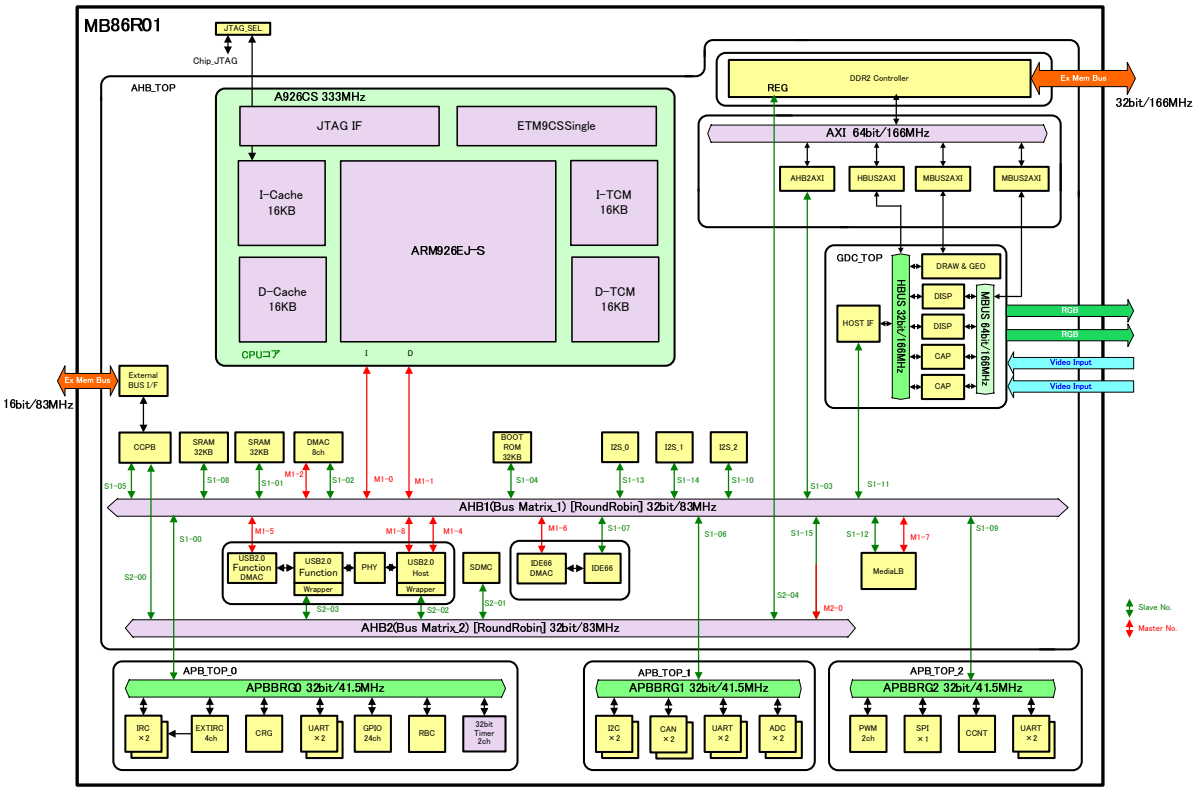


Figure 3-1 Block diagram of MB86R01

CPU core

This is CPU core block of ARM926EJ-S which is connected to each I/O through AHB bus in LSI. Instruction (I)/Data (D) function as a separate bus master for Harvard architecture.

GDC_TOP

This is MB86296 compatible GDC which has 2 functions: AHB slave function writes required display list for drawing to GDC with having CPU or DMA controller as master, and AXI master function reads display list arranged in DDR2 memory with having GDC as master.

AXI bus

This bus bridges main memory and internal resource. Following four bus masters are connected.

- AHB1: Each bus master of AHB bus such as CPU and DMA controller
- HBUS: HOST IF on GDC
- DRAW & GEO: Draw (2D/3D drawing) and GEO (geometry engine) on GDC
- MBUS: DISP (display controller) and CAP (Video capture) on GDC

AHB1 bus

Following resources are connected.

- CPU core: Bus masters of instruction (I)/data (D)
- GDC: GDC register part
- AHB2AXI: AXI port for main memory access
- CCPB: Encrypted ROM decoding block
- External BUS I/F: External bus interface (connected through CCPB)
- SRAM: General purpose internal SRAM 32KB × 2
- DMAC: General purpose DMA × 8ch
  It operates as bus master at data transfer
- Boot ROM: Built-in boot ROM
- I2S_0/1/2: Serial audio controller × 3ch
- USB 2.0 Function DMAC: USB function DMAC
  It operates as bus master at data transfer
- USB2.0 Host: It operates as USB2.0 EHCI, USB1.1 OHCI bus masters
- IDE66/IDE66DMAC: Register part of IDE host controller and built-in DMAC
  The DMAC part operates as bus master at data transfer
- MLB: MediaLB controller
- AHB2
- APBBRG0/1/2: AHB-APB bridge circuit × 3ch

AHB2 bus

- CCPB: Encrypted ROM decoding block
- USB 2.0 Function: USB 2.0 function controller's register part
- USB 2.0 Host: USB 2.0 host controller's register part
- SDMC: SD memory controller
- DDR2 controller: DDR2 controller's register part

APB_TOP_0

This block bridges between APBBRG0 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- Interrupt controller (IRC) × 2ch
- External interrupt controller (EXTIRC)
- Clock reset generator (CRG)
- UART (ch0 and ch1) × 2ch
- Remap boot controller (RBC)
- 32 bit general-purpose timer (32 bit timer) × 2ch

APB_TOP_1

This block bridges between APBBRG1 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- I^2C controller × 2ch
- CAN controller × 2ch
- UART (ch2 and ch3) × 2ch
- A/D converter (ADC) × 2ch

APB_TOP_2

This block bridges between APBBRG2 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- PWM controller (PWM)
- SPI controller (SPI)
- CCNT
- UART (ch4 and ch5) × 2ch

4. Function list

Function list of MB86R01 is shown below.

Function	Outline
CPU core	• ARM926EJ-S™ processor core • Core operation frequency: 333MHz • 16KB instruction cache • 16KB data cache • Tightly-Coupled memory for 16KB instruction (ITCM) • Tightly-Coupled memory for 16KB data (DTCM) • ETM9CS Single and JTAG ICE debugging interface • Java acceleration (Jazelle technology)
Bus architecture	• Multilayer AHB bus architecture (software interrupt) • Speeding up data transfer between main memory and each bus master with 64 bit AXI bus
Interrupt	• High-speed interrupt × 1ch h (soft interrupt) • Normal interrupt × 64ch (external interrupt × 4ch + built-in internal interrupt × 60ch) • Up to 16 interrupt levels are settable by channel
Clock	• PLL multiplication: selectable from ×15 ~ 49 • Operation frequency: 333MHz (CPU), 83MHz (AHB), 41.5MHz (APB) • Low power consumption mode (clock to ARM and module is stoppable)
Reset	• Hardware reset, software reset, and watchdog reset
Remap	• ROM area is able to be mapping to built-in SRAM area
External bus interface	• Three chip select signals • Provided 32M byte address space in each chip select • Supported 16/32 bit width SRAM/Flash ROM connection • Programmable weight controller • Encrypted ROM compound engine
DDR2 controller	• Supported DDR2SDRAM (DDR2-400) • Connectable capacity: 256 ~ 512M bit × 2 or 256 ~ 512M bit × 1 • I/O width: Selectable from ×16/×32 bit • Max. transfer rate: 166MHz/333Mbps
Built-in SRAM	• Mounted general purpose SRAM of 32KB × 2 (32 bit bus)
DMAC	• AHB connection × 8ch • Transfer mode: Block, burst, and demand
Timer	• 32/16 bit programmable × 2 channels
GPIO (*2)	• Max. 24 is usable • Interrupt function
PWM (*2)	• Built-in 2 channels • Duty ratio and phase are configurable
A/D converter	• 10 bit successive approximation type A/D converter × 2ch • Sampling rate: 648KS/s (max. sampling plate) • Nonlinearity error: ± 2.0LSB (max.)

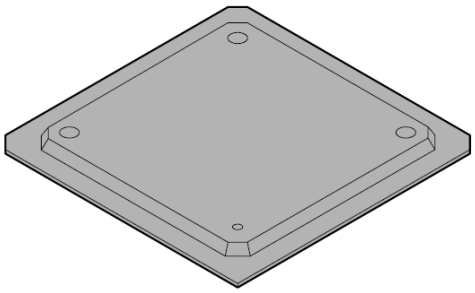
Function	Outline
GDC (*1)	• Display controller RGB666 or RGB888 output Max. resolution is 1024 × 768 Max. 6 layered display Max. 2 screen output • Digital video capture function BT.601, BT.656, and RGB666 Max. 2 inputs • Geometry engine (MB86296 compatible display list is usable) • 2D/3D drawing function (MB86296 compatible display list is usable)
I2S (*2)	• Audio output × 3ch (L/R)/Audio input × 3ch (L/R) • Supported three-wire serial (I2S, MSB-Justified) and serial PCM data transfer interface • Master/Slave operations are selectable • Resolution capability: Max. 32 bit/sample
UART (*2)	• Max. 6 channels (dedicated channel: 3ch, option: 3ch) • 1 channel: capable of input/output CTS/RTS signals • 8 bit pre-scaler for baud rate clock generation • Enabled DMA transfer
I^2C	• 3.3V pin × 2ch • Supported standard mode (max. 100kbps)/high-speed mode (max. 400kbps)
SPI (*2)	• Full duplex/Synchronous transmission • Transfer data length: 1 bit unit (max. 32 bit) (programmable setting)
CAN (*2)	• Mounted BOSCH C_CAN module × 2ch • Conformed to CAN protocol version 2.0 part A and B • I/O voltage: 3.3V
MediaLB (*2)	• 16 channels • MediaLB clock speed: 256Fs/512Fs/1024Fs • Built-in 9K bit channel buffer
USB (*2)	• USB 2.0 compliant Host/Function controller × 1ch (pin multiplex) • HS/FS protocol support (supported VBus and isochronous transfer)
IDE (*2)	• Supported ATA/ATAPI-5 • Equipped 1 channel • Supported primary IDE channel • Equipped transmission FIFO buffer (512 byte × 2) and reception FIFO buffer (512 byte × 2) for the ultra DMA transfer • Unsupported single word DMA and multiword DMA
SDMC	• Conformed to SD memory card physical layer specification 1.0 • Equipped 1 channel • Supported SD memory card and multimedia card • Unsupported SPI mode, SDIO mode, and CPRM
CCNT	• Mode selection of multiplex pin group 2 and 4 • Software reset control • AXI interconnection control (priority and WAIT setting)
JTAG	• Conformed to IEIEEE1149.1 (IEEE Standard Test Access Port and Boundary-Scan Architecture) • Supported JTAG ICE connection

*1: Number of layer of simultaneous display and number of output display as well as capture input for displaying in high resolution may be restricted due to data supply capacity of graphics memory (DDR2 controller).
*2: A part of external pin functions of this LSI is multiplexed. Max. number of usable channel is limited by pin multiplex function setting.

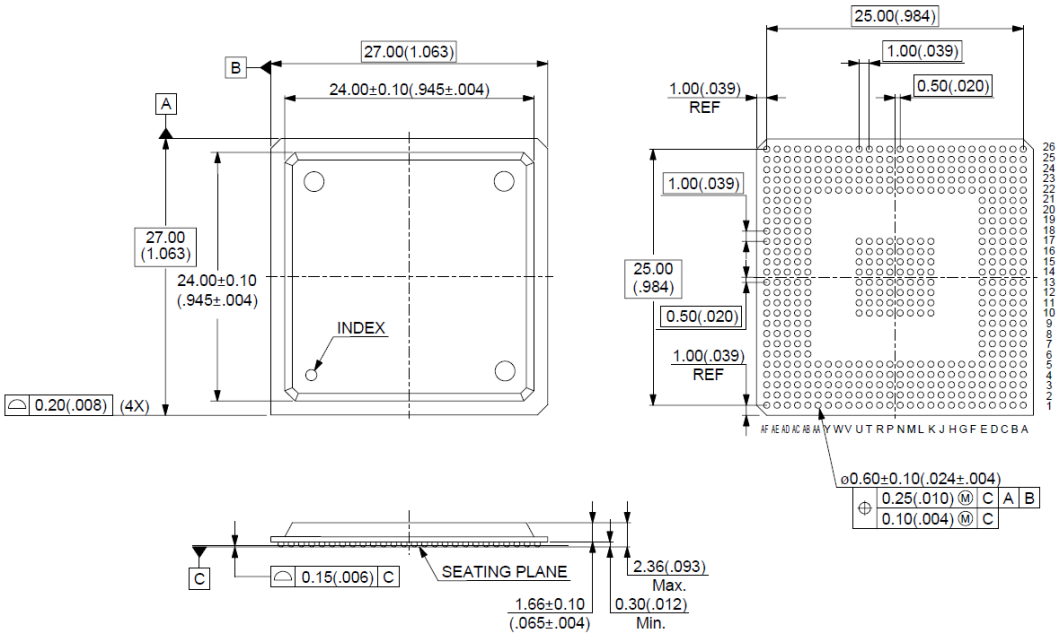
5. Package dimension

Package dimension of MB86R01 is shown below.

BGA-484P-M07

484-pin plastic PBGA		
 (BGA-484P-M07)	Ball pitch	1.00 mm
	Package width × package length	27.00 mm × 27.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	2.36 mm Max

484-pin plastic PBGA
(BGA-484P-M07)

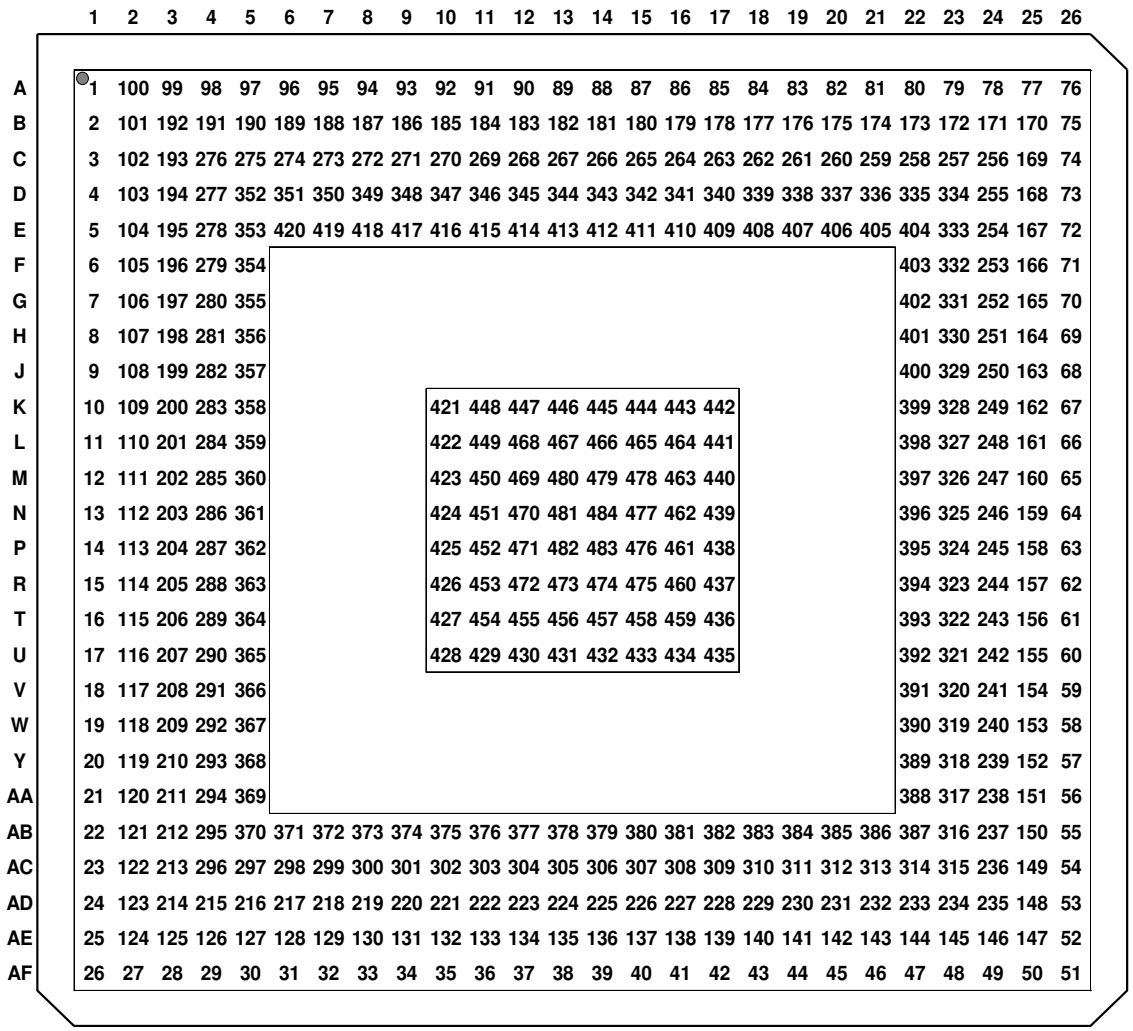


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

6. Pin assignment

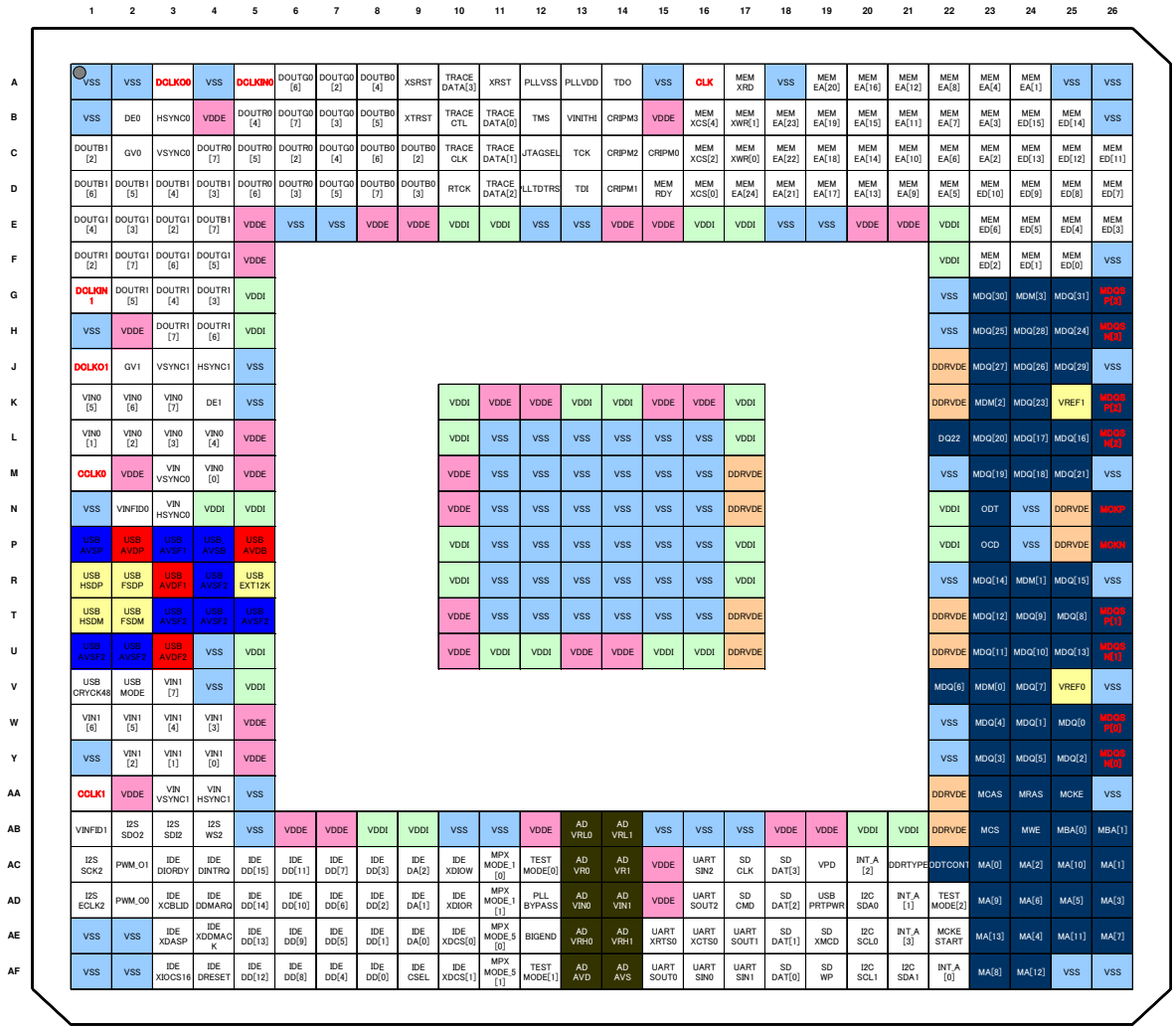
Pin assignment of MB86R01 is shown below.

(Top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	1	100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76
B	2	101	192	191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	174	173	172	171	170	75
C	3	102	193	276	275	274	273	272	271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256	169	74
D	4	103	194	277	352	351	350	349	348	347	346	345	344	343	342	341	340	339	338	337	336	335	334	255	168	73
E	5	104	195	278	353	420	419	418	417	416	415	414	413	412	411	410	409	408	407	406	405	404	333	254	167	72
F	6	105	196	279	354																	403	332	253	166	71
G	7	106	197	280	355																	402	331	252	165	70
H	8	107	198	281	356																	401	330	251	164	69
J	9	108	199	282	357																	400	329	250	163	68
K	10	109	200	283	358						421	448	447	446	445	444	443	442				399	328	249	162	67
L	11	110	201	284	359						422	449	468	467	466	465	464	441				398	327	248	161	66
M	12	111	202	285	360						423	450	469	480	479	478	463	440				397	326	247	160	65
N	13	112	203	286	361						424	451	470	481	484	477	462	439				396	325	246	159	64
P	14	113	204	287	362						425	452	471	482	483	476	461	438				395	324	245	158	63
R	15	114	205	288	363						426	453	472	473	474	475	460	437				394	323	244	157	62
T	16	115	206	289	364						427	454	455	456	457	458	459	436				393	322	243	156	61
U	17	116	207	290	365						428	429	430	431	432	433	434	435				392	321	242	155	60
V	18	117	208	291	366																	391	320	241	154	59
W	19	118	209	292	367																	390	319	240	153	58
Y	20	119	210	293	368																	389	318	239	152	57
AA	21	120	211	294	369																	388	317	238	151	56
AB	22	121	212	295	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	316	237	150	55
AC	23	122	213	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	236	149	54
AD	24	123	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	148	53
AE	25	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	52
AF	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51

(Top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSS	VSS	DCLKO0	VSS	DCLKIN0	DOUTG0 [6]	DOUTG0 [2]	DOUTB0 [4]	XSRST	TRACE DATA[3]	XRST	PLLVSS	PLLVDD	TDO	VSS	CLK	MEM XRD	VSS	MEM EA[20]	MEM EA[16]	MEM EA[12]	MEM EA[8]	MEM EA[4]	MEM EA[1]	VSS	VSS
B	VSS	DE0	HSYNC0	VDDE	DOUTR0 [4]	DOUTG0 [7]	DOUTG0 [3]	DOUTB0 [5]	XTRST	TRACE CTL	TRACE DATA[0]	TMS	VINITHI	CRIPM3	VDDE	MEM XCS[4]	MEM XWR[1]	MEM EA[23]	MEM EA[19]	MEM EA[15]	MEM EA[11]	MEM EA[7]	MEM EA[3]	MEM ED[15]	MEM ED[14]	VSS
C	DOUTB1 [2]	GV0	VSYNC0	DOUTR0 [7]	DOUTR0 [5]	DOUTR0 [2]	DOUTG0 [4]	DOUTB0 [6]	DOUTB0 [2]	TRACE CLK	TRACE DATA[1]	JTAGSEL	TCK	CRIPM2	CRIPM0	MEM XCS[2]	MEM XWR[0]	MEM EA[22]	MEM EA[18]	MEM EA[14]	MEM EA[10]	MEM EA[6]	MEM EA[2]	MEM ED[13]	MEM ED[12]	MEM ED[11]
D	DOUTB1 [6]	DOUTB1 [5]	DOUTB1 [4]	DOUTB1 [3]	DOUTR0 [6]	DOUTR0 [3]	DOUTG0 [5]	DOUTB0 [7]	DOUTB0 [3]	RTCK	TRACE DATA[2]	TLLTDTRS	TDI	CRIPM1	MEM RDY	MEM XCS[0]	MEM EA[24]	MEM EA[21]	MEM EA[17]	MEM EA[13]	MEM EA[9]	MEM EA[5]	MEM ED[10]	MEM ED[9]	MEM ED[8]	MEM ED[7]
E	DOUTG1 [4]	DOUTG1 [3]	DOUTG1 [2]	DOUTB1 [7]	VDDE	VSS	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	VDDE	VDDI	MEM ED[6]	MEM ED[5]	MEM ED[4]	MEM ED[3]
F	DOUTR1 [2]	DOUTG1 [7]	DOUTG1 [6]	DOUTG1 [5]	VDDE																	VDDI	MEM ED[2]	MEM ED[1]	MEM ED[0]	VSS
G	DCLKIN 1	DOUTR1 [5]	DOUTR1 [4]	DOUTR1 [3]	VDDI																	VSS	MDQ[30]	MDM[3]	MDQ[31]	MDQS P[3]
H	VSS	VDDE	DOUTR1 [7]	DOUTR1 [6]	VDDI																	VSS	MDQ[25]	MDQ[28]	MDQ[24]	MDQS N[3]
J	DCLKO1	GV1	VSYNC1	HSYNC1	VSS																	DDRVDE	MDQ[27]	MDQ[26]	MDQ[29]	VSS
K	VIN0 [5]	VIN0 [6]	VIN0 [7]	DE1	VSS					VDDI	VDDE	VDDE	VDDI	VDDI	VDDE	VDDE	VDDI					DDRVDE	MDM[2]	MDQ[23]	VREF1	MDQS P[2]
L	VIN0 [1]	VIN0 [2]	VIN0 [3]	VIN0 [4]	VDDE					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					DQ22	MDQ[20]	MDQ[17]	MDQ[16]	MDQS N[2]
M	CCLK0	VDDE	VIN VSYNC0	VIN0 [0]	VDDE					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					VSS	MDQ[19]	MDQ[18]	MDQ[21]	VSS
N	VSS	VINFID0	VIN HSYNC0	VDDI	VDDI					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					VDDI	ODT	VSS	DDRVDE	MCKP
P	USB AVSP	USB AVDP	USB AVSF1	USB AVSF	USB AVDB					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					VDDI	OCD	VSS	DDRVDE	MCKN
R	USB HSDP	USB FSDP	USB AVDF1	USB AVSF3	USB EXT12K					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					VSS	MDQ[14]	MDM[1]	MDQ[15]	VSS
T	USB HSDM	USB FSDM	USB AVSF2	USB AVSF2	USB AVSF2					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					DDRVDE	MDQ[12]	MDQ[9]	MDQ[8]	MDQS P[1]
U	USB AVSF2	USB AVSF2	USB AVDF2	VSS	VDDI					VDDE	VDDI	VDDI	VDDE	VDDE	VDDI	VDDI	DDRVDE					DDRVDE	MDQ[11]	MDQ[10]	MDQ[13]	MDQS N[1]
V	USB CRYCK48	USB MODE	VIN1 [7]	VSS	VDDI																	MDQ[6]	MDM[0]	MDQ[7]	VREF0	VSS
W	VIN1 [6]	VIN1 [5]	VIN1 [4]	VIN1 [3]	VDDE																	VSS	MDQ[4]	MDQ[1]	MDQ[0	MDQS P[0]
Y	VSS	VIN1 [2]	VIN1 [1]	VIN1 [0]	VDDE																	VSS	MDQ[3]	MDQ[5]	MDQ[2]	MDQS N[0]
AA	CCLK1	VDDE	VIN VSYNC1	VIN HSYNC1	VSS																	DDRVDE	MCAS	MRAS	MCKE	VSS
AB	VINFID1	I2S SDO2	I2S SDI2	I2S WS2	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	AD VRL0	AD VRL1	VSS	VSS	VSS	VDDE	VDDE	VDDI	VDDI	DDRVDE	MCS	MWE	MBA[0]	MBA[1]
AC	I2S SCK2	PWM_O1	IDE DIORDY	IDE DINTRQ	IDE DD[15]	IDE DD[11]	IDE DD[7]	IDE DD[3]	IDE DA[2]	IDE XDIOW	MPX MODE_1 [0]	TEST MODE[0]	AD VR0	AD VR1	VDDE	UART SIN2	SD CLK	SD DAT[3]	VPD	INT_A [2]	DDRTYPE	ODTCONT	MA[0]	MA[2]	MA[10]	MA[1]
AD	I2S ECLK2	PWM_O0	IDE XCBLID	IDE DDMARQ	IDE DD[14]	IDE DD[10]	IDE DD[6]	IDE DD[2]	IDE DA[1]	IDE XDIOR	MPX MODE_1 [1]	PLL BYPASS	AD VIN0	AD VIN1	VDDE	UART SOUT2	SD CMD	SD DAT[2]	USB PRTPWR	I2C SDA0	INT_A [1]	TEST MODE[2]	MA[9]	MA[6]	MA[5]	MA[3]
AE	VSS	VSS	IDE XDASP	IDE XDDMACK	IDE DD[13]	IDE DD[9]	IDE DD[5]	IDE DD[1]	IDE DA[0]	IDE XDCS[0]	MPX MODE_5 [0]	BIGEND	AD VRH0	AD VRH1	UART XRTS0	UART XCTS0	UART SOUT1	SD DAT[1]	SD XMCD	I2C SCL0	INT_A [3]	MCKE START	MA[13]	MA[4]	MA[11]	MA[7]
AF	VSS	VSS	IDE XIOCS16	IDE DRESET	IDE DD[12]	IDE DD[8]	IDE DD[4]	IDE DD[0]	IDE CSEL	IDE XDCS[1]	MPX MODE_5 [1]	TEST MODE[1]	AD AVD	AD AVS	UART SOUT0	UART SIN0	UART SIN1	SD DAT[0]	SD WP	I2C SCL1	I2C SDA1	INT_A [0]	MA[8]	MA[12]	VSS	VSS

Pin assignment table

Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME
1	A1	VSS	101	B2	DE0	201	L3	VIN0[3]	301	AC9	IDE_DA[2]	401	H22	VSS
2	B1	VSS	102	C2	GV0	202	M3	VINVSYNC0	302	AC10	IDE_XDIOW	402	G22	VSS
3	C1	DOUTB1[2]	103	D2	DOUTB1[5]	203	N3	VINHSYNC0	303	AC11	MPX_MODE_1[0]	403	F22	VDDI
4	D1	DOUTB1[6]	104	E2	DOUTG1[3]	204	P3	USB_AVSF1	304	AC12	TESTMODE[0]	404	E22	VDDI
5	E1	DOUTG1[4]	105	F2	DOUTG1[7]	205	R3	USB_AVDF1	305	AC13	AD_VR0	405	E21	VDDE
6	F1	DOUTR1[2]	106	G2	DOUTR1[5]	206	T3	USB_AVSF2	306	AC14	AD_VR1	406	E20	VDDE
7	G1	DCLKIN1	107	H2	VDDE	207	U3	USB_AVDF2	307	AC15	VDDE	407	E19	VSS
8	H1	VSS	108	J2	GV1	208	V3	VIN1[7]	308	AC16	UART_SIN2	408	E18	VSS
9	J1	DCLKO1	109	K2	VIN0[6]	209	W3	VIN1[4]	309	AC17	SD_CLK	409	E17	VDDI
10	K1	VIN0[5]	110	L2	VIN0[2]	210	Y3	VIN1[1]	310	AC18	SD_DAT[3]	410	E16	VDDI
11	L1	VIN0[1]	111	M2	VDDE	211	AA3	VINVSYNC1	311	AC19	VPD	411	E15	VDDE
12	M1	CCLK0	112	N2	VINFID0	212	AB3	I2S_SDI2	312	AC20	INT_A[2]	412	E14	VDDE
13	N1	VSS	113	P2	USB_AVDP	213	AC3	IDE_DIORDY	313	AC21	DDRTYPE	413	E13	VSS
14	P1	USB_AVSP	114	R2	USB_FSDP	214	AD3	IDE_XCBLID	314	AC22	ODTCONT	414	E12	VSS
15	R1	USB_HSDP	115	T2	USB_FSDM	215	AD4	IDE_DDMARQ	315	AC23	MA[0]	415	E11	VDDI
16	T1	USB_HSDM	116	U2	USB_AVSF2	216	AD5	IDE_DD[14]	316	AB23	MCS	416	E10	VDDI
17	U1	USB_AVSF2	117	V2	USB_MODE	217	AD6	IDE_DD[10]	317	AA23	MCAS	417	E9	VDDE
18	V1	USB_CRYCK48	118	W2	VIN1[5]	218	AD7	IDE_DD[6]	318	Y23	MDQ[3]	418	E8	VDDE
19	W1	VIN1[6]	119	Y2	VIN1[2]	219	AD8	IDE_DD[2]	319	W23	MDQ[4]	419	E7	VSS
20	Y1	VSS	120	AA2	VDDE	220	AD9	IDE_DA[1]	320	V23	MDM[0]	420	E6	VSS
21	AA1	CCLK1	121	AB2	I2S_SDO2	221	AD10	IDE_XDIOR	321	U23	MDQ[11]	421	K10	VDDI
22	AB1	VINFID1	122	AC2	PWM_O1	222	AD11	MPX_MODE_1[1]	322	T23	MDQ[12]	422	L10	VDDI
23	AC1	I2S_SCK2	123	AD2	PWM_O0	223	AD12	PLLBYPASS	323	R23	MDQ[14]	423	M10	VDDE
24	AD1	I2S_ECLK2	124	AE2	VSS	224	AD13	AD_VIN0	324	P23	OCD	424	N10	VDDE
25	AE1	VSS	125	AE3	IDE_XDASP	225	AD14	AD_VIN1	325	N23	ODT	425	P10	VDDI
26	AF1	VSS	126	AE4	IDE_XDDMACK	226	AD15	VDDE	326	M23	MDQ[19]	426	R10	VDDI
27	AF2	VSS	127	AE5	IDE_DD[13]	227	AD16	UART_SOUT2	327	L23	MDQ[20]	427	T10	VDDE
28	AF3	IDE_XIOCS16	128	AE6	IDE_DD[9]	228	AD17	SD_CMD	328	K23	MDM[2]	428	U10	VDDE
29	AF4	IDE_XDRESET	129	AE7	IDE_DD[5]	229	AD18	SD_DAT[2]	329	J23	MDQ[27]	429	U11	VDDI
30	AF5	IDE_DD[12]	130	AE8	IDE_DD[1]	230	AD19	USB_PRTPWR	330	H23	MDQ[25]	430	U12	VDDI
31	AF6	IDE_DD[8]	131	AE9	IDE_DA[0]	231	AD20	I2C_SDA0	331	G23	MDQ[30]	431	U13	VDDE
32	AF7	IDE_DD[4]	132	AE10	IDE_XDCS[0]	232	AD21	INT_A[1]	332	F23	MEM_ED[2]	432	U14	VDDE
33	AF8	IDE_DD[0]	133	AE11	MPX_MODE_5[0]	233	AD22	TESTMODE[2]	333	E23	MEM_ED[6]	433	U15	VDDI
34	AF9	IDE_CSEL	134	AE12	BIGEND	234	AD23	MA[9]	334	D23	MEM_ED[10]	434	U16	VDDI
35	AF10	IDE_XDCS[1]	135	AE13	AD_VRH0	235	AD24	MA[6]	335	D22	MEM_EA[5]	435	U17	DDRVDE
36	AF11	MPX_MODE_5[1]	136	AE14	AD_VRH1	236	AC24	MA[2]	336	D21	MEM_EA[9]	436	T17	DDRVDE
37	AF12	TESTMODE[1]	137	AE15	UART_XRTS0	237	AB24	MWE	337	D20	MEM_EA[13]	437	R17	VDDI
38	AF13	AD_AVD	138	AE16	UART_XCTS0	238	AA24	MRAS	338	D19	MEM_EA[17]	438	P17	VDDI
39	AF14	AD_AVS	139	AE17	UART_SOUT1	239	Y24	MDQ[5]	339	D18	MEM_EA[21]	439	N17	DDRVDE
40	AF15	UART_SOUT0	140	AE18	SD_DAT[1]	240	W24	MDQ[1]	340	D17	MEM_EA[24]	440	M17	DDRVDE
41	AF16	UART_SIN0	141	AE19	SD_XMCD	241	V24	MDQ[7]	341	D16	MEM_XCS[0]	441	L17	VDDI
42	AF17	UART_SIN1	142	AE20	I2C_SCL0	242	U24	MDQ[10]	342	D15	MEM_RDY	442	K17	VDDI
43	AF18	SD_DAT[0]	143	AE21	INT_A[3]	243	T24	MDQ[9]	343	D14	CRIPM1	443	K16	VDDE
44	AF19	SD_WP	144	AE22	MCKE_START	244	R24	MDM[1]	344	D13	TDI	444	K15	VDDE
45	AF20	I2C_SCL1	145	AE23	MA[13]	245	P24	VSS	345	D12	PLLTDTRST	445	K14	VDDI
46	AF21	I2C_SDA1	146	AE24	MA[4]	246	N24	VSS	346	D11	TRACEDATA[2]	446	K13	VDDI
47	AF22	INT_A[0]	147	AE25	MA[11]	247	M24	MDQ[18]	347	D10	RTCK	447	K12	VDDE
48	AF23	MA[8]	148	AD25	MA[5]	248	L24	MDQ[17]	348	D9	DOUTB0[3]	448	K11	VDDE
49	AF24	MA[12]	149	AC25	MA[10]	249	K24	MDQ[23]	349	D8	DOUTB0[7]	449	L11	VSS
50	AF25	VSS	150	AB25	MBA[0]	250	J24	MDQ[26]	350	D7	DOUTG0[5]	450	M11	VSS
51	AF26	VSS	151	AA25	MCKE	251	H24	MDQ[28]	351	D6	DOUTR0[3]	451	N11	VSS
52	AE26	MA[7]	152	Y25	MDQ[2]	252	G24	MDM[3]	352	D5	DOUTR0[6]	452	P11	VSS
53	AD26	MA[3]	153	W25	MDQ[0]	253	F24	MEM_ED[1]	353	E5	VDDE	453	R11	VSS
54	AC26	MA[1]	154	V25	VREF0	254	E24	MEM_ED[5]	354	F5	VDDE	454	T11	VSS
55	AB26	MBA[1]	155	U25	MDQ[13]	255	D24	MEM_ED[9]	355	G5	VDDI	455	T12	VSS
56	AA26	VSS	156	T25	MDQ[8]	256	C24	MEM_ED[13]	356	H5	VDDI	456	T13	VSS
57	Y26	MDQSN[0]	157	R25	MDQ[15]	257	C23	MEM_EA[2]	357	J5	VSS	457	T14	VSS
58	W26	MDQSP[0]	158	P25	DDRVDE	258	C22	MEM_EA[6]	358	K5	VSS	458	T15	VSS
59	V26	VSS	159	N25	DDRVDE	259	C21	MEM_EA[10]	359	L5	VDDE	459	T16	VSS
60	U26	MDQSN[1]	160	M25	MDQ[21]	260	C20	MEM_EA[14]	360	M5	VDDE	460	R16	VSS
61	T26	MDQSP[1]	161	L25	MDQ[16]	261	C19	MEM_EA[18]	361	N5	VDDI	461	P16	VSS
62	R26	VSS	162	K25	VREF1	262	C18	MEM_EA[22]	362	P5	USB_AVDB	462	N16	VSS
63	P26	MCKN	163	J25	MDQ[29]	263	C17	MEM_XWR[0]	363	R5	USB_EXT12K	463	M16	VSS
64	N26	MCKP	164	H25	MDQ[24]	264	C16	MEM_XCS[2]	364	T5	USB_AVSF2	464	L16	VSS
65	M26	VSS	165	G25	MDQ[31]	265	C15	CRIPM0	365	U5	VDDI	465	L15	VSS
66	L26	MDQSN[2]	166	F25	MEM_ED[0]	266	C14	CRIPM2	366	V5	VDDI	466	L14	VSS
67	K26	MDQSP[2]	167	E25	MEM_ED[4]	267	C13	TCK	367	W5	VDDE	467	L13	VSS
68	J26	VSS	168	D25	MEM_ED[8]	268	C12	JTAGSEL	368	Y5	VDDE	468	L12	VSS
69	H26	MDQSN[3]	169	C25	MEM_ED[12]	269	C11	TRACEDATA[1]	369	AA5	VSS	469	M12	VSS
70	G26	MDQSP[3]	170	B25	MEM_ED[14]	270	C10	TRACECLK	370	AB5	VSS	470	N12	VSS
71	F26	VSS	171	B24	MEM_ED[15]	271	C9	DOUTB0[2]	371	AB6	VDDE	471	P12	VSS
72	E26	MEM_ED[3]	172	B23	MEM_EA[3]	272	C8	DOUTB0[6]	372	AB7	VDDE	472	R12	VSS
73	D26	MEM_ED[7]	173	B22	MEM_EA[7]	273	C7	DOUTG0[4]	373	AB8	VDDI	473	R13	VSS
74	C26	MEM_ED[11]	174	B21	MEM_EA[11]	274	C6	DOUTR0[2]	374	AB9	VDDI	474	R14	VSS
75	B26	VSS	175	B20	MEM_EA[15]	275	C5	DOUTR0[5]	375	AB10	VSS	475	R15	VSS
76	A26	VSS	176	B19	MEM_EA[19]	276	C4	DOUTR0[7]	376	AB11	VSS	476	P15	VSS
77	A25	VSS	177	B18	MEM_EA[23]	277	D4	DOUTB1[3]	377	AB12	VDDE	477	N15	VSS
78	A24	MEM_EA[1]	178	B17	MEM_XWR[1]	278	E4	DOUTB1[7]	378	AB13	AD_VRL0	478	M15	VSS
79	A23	MEM_EA[4]	179	B16	MEM_XCS[4]	279	F4	DOUTG1[5]	379	AB14	AD_VRL1	479	M14	VSS
80	A22	MEM_EA[8]	180	B15	VDDE	280	G4	DOUTR1[3]	380	AB15	VSS	480	M13	VSS
81	A21	MEM_EA[12]	181	B14	CRIPM3	281	H4	DOUTR1[6]	381	AB16	VSS	481	N13	VSS
82	A20	MEM_EA[16]	182	B13	VINITHI	282	J4	HSYNC1	382	AB17	VSS	482	P13	VSS
83	A19	MEM_EA[20]	183	B12	TMS	283	K4	DE1	383	AB18	VDDE	483	P14	VSS
84	A18	VSS	184	B11	TRACEDATA[0]	284	L4	VIN0[4]	384	AB19	VDDE	484	N14	VSS
85	A17	MEM_XRD	185	B10	TRACECTL	285	M4	VIN0[0]	385	AB20	VDDI			
86	A16	CLK	186	B9	XTRST	286	N4	VDDI	386	AB21	VDDI			
87	A15	VSS	187	B8	DOUTB0[5]	287	P4	USB_AVSB	387	AB22	DDRVDE			
88	A14	TDO	188	B7	DOUTG0[3]	288	R4	USB_AVSF2	388	AA22	DDRVDE			
89	A13	PLLVDD	189	B6	DOUTG0[7]	289	T4	USB_AVSF2	389	Y22	VSS			
90	A12	PLLVSS	190	B5	DOUTR0[4]	290	U4	VSS	390	W22	VSS			
91	A11	XRST	191	B4	VDDE	291	V4	VSS	391	V22	MDQ[6]			
92	A10	TRACEDATA[3]	192	B3	HSYNC0	292	W4	VIN1[3]	392	U22	DDRVDE			
93	A9	XSRST	193	C3	VSYNC0	293	Y4	VIN1[0]	393	T22	DDRVDE			
94	A8	DOUTB0[4]	194	D3	DOUTB1[4]	294	AA4	VINHSYNC1	394	R22	VSS			
95	A7	DOUTG0[2]	195	E3	DOUTG1[2]	295	AB4	I2S_WS2	395	P22	VDDI			
96	A6	DOUTG0[6]	196	F3	DOUTG1[6]	296	AC4	IDE_DINTRQ	396	N22	VDDI			
97	A5	DCLKIN0	197	G3	DOUTR1[4]	297	AC5	IDE_DD[15]	397	M22	VSS			
98	A4	VSS	198	H3	DOUTR1[7]	298	AC6	IDE_DD[11]	398	L22	MDQ[22]			
99	A3	DCLKO0	199	J3	VSYNC1	299	AC7	IDE_DD[7]	399	K22	DDRVDE			
100	A2	VSS	200	K3	VIN0[7]	300	AC8	IDE_DD[3]	400	J22	DDRVDE			

7. Pin function

External pin function of MB86R01 is described below.

7.1. Pin Multiplex

This LSI adopts pin multiplex function, and a part of external pin function is multiplexed.
The external pin function is categorized into following five groups. Each group is able to set the external pin function individually; therefore, the function can be flexibly set depending on the peripheral I/O resource to be used.

1. Pin multiplex group #1 (setting pin: MPX_MODE_1[1:0])
   - Mode 0: Pin related to DISPLAY1
   - Mode 1: Pin related to external bus interface
   - Mode 2: Pin related to I2S0, GPIO, and DISPLAY0 data width extension
2. Pin multiplex group #2 (setting register: CMUX_MD.MPX_MODE_2[2:0])
   - Mode 0: Pin related to CAP1, CAP0 synchronizing signal, PWM, and I2S2
   - Mode 1: Pin related to CAP1 (NRGB666)
   - Mode 2: Pin related to GPIO, CAN, I2S1, MediaLB, and I2S2
   - Mode 3: Pin related to GPIO, CAN, I2S1, MediaLB, and SPI
   - Mode 4: Pin related to GPIO, CAN, I2S1, MediaLB, and I2S2 (input)
3. Pin multiplex group #3 (setting pin: USB_MODE)
   - Mode 0: Pin related to USB 2.0 host
   - Mode 1: Pin related to USB 2.0 function
4. Pin multiplex group #4 (setting register: CMUX_MD.MPX_MODE_4[1:0])
   - Mode 0: Pin related to IDE
   - Mode 1: Pin related to I2S1, CAN, GPIO, and PWM
5. Pin multiplex group #5 (setting pin: MPX_MODE_5[1:0])
   - Mode 0: Pin related to ETM
   - Mode 1: Pin related to UART3, UART4, and UART5
   - Mode 2: Pin related to UART3, UART4, and PWM

Note:
Mode should be changed when each pin is not in operation.
PWM, I2S1, and CAN pins may be duplicated and allocated to external pin depending on group combination; in this case, use either of them. For unused pin, follow the procedure in 1.6.27, unused pin with pin multiplex function in the duplex case.

Pin multiplex group #1 (setting pin: MPX_MODE_1 [1:0])

Pin No.	JEDEC	Mode 0	Mode 1	Mode 2			
		Pin related to DISPLAY1	Pin related to external bus interface	Pin related to I2S0	Pin related to GPIO	Pin related to DISPLAY0	Pin related to external bus interface
198	H3	DOUTR1[7]	MEM_ED[31]	I2S_ECLK0	-	-	-
281	H4	DOUTR1[6]	MEM_ED[30]	I2S_SCK0	-	-	-
106	G2	DOUTR1[5]	MEM_ED[29]	I2S_WS0	-	-	-
197	G3	DOUTR1[4]	MEM_ED[28]	I2S_SDI0	-	-	-
280	G4	DOUTR1[3]	MEM_ED[27]	I2S_SDO0	-	-	-
6	F1	DOUTR1[2]	MEM_ED[26]	-	GPIO_PD[12]	-	-
105	F2	DOUTG1[7]	MEM_ED[25]	-	GPIO_PD[11]	-	-
196	F3	DOUTG1[6]	MEM_ED[24]	-	GPIO_PD[10]	-	-
279	F4	DOUTG1[5]	MEM_ED[23]	-	GPIO_PD[9]	-	-
5	E1	DOUTG1[4]	MEM_ED[22]	-	GPIO_PD[8]	-	-
104	E2	DOUTG1[3]	MEM_ED[21]	-	GPIO_PD[7]	-	-
195	E3	DOUTG1[2]	MEM_ED[20]	-	GPIO_PD[6]	-	-
278	E4	DOUTB1[7]	MEM_ED[19]	-	-	DOUTR0[1]	-
4	D1	DOUTB1[6]	MEM_ED[18]	-	-	DOUTR0[0]	-
103	D2	DOUTB1[5]	MEM_ED[17]	-	-	DOUTG0[1]	-
194	D3	DOUTB1[4]	MEM_ED[16]	-	-	DOUTG0[0]	-
277	D4	DOUTB1[3]	MEM_XWR[3]	-	-	DOUTB0[1]	-
3	C1	DOUTB1[2]	MEM_XWR[2]	-	-	DOUTB0[0]	-
283	K4	DE1	XDACK[7]	-	-	-	XDACK[7]
282	J4	HSYNC1	DREQ[6]	-	-	-	DREQ[6]
199	J3	VSYNC1	XDACK[6]	-	-	-	XDACK[6]
108	J2	GV1	DREQ[7]	-	-	-	DREQ[7]

Pin multiplex group #1 mode setting

This mode is set with external pin, MPX_MODE_1[1:0].

MPX_MODE_1[1] pin	MPX_MODE_1[0] pin	Pin multiplex group #1 mode
"L"	"L"	Mode 0
"L"	"H"	Mode 1
"H"	"L"	Mode 2
"H"	"H"	Mode 0

Pin multiplex group #2 (setting register: PIN MPX Select.MPX_MODE_2 [2:0])

Pin No.	JEDEC	Mode0			Mode1	Mode2				Mode3					Mode4			
		Pin related to CAP0/1	Pin related to PWM	Pin related to I2S2	Pin related to CAP1 (NRGB666)	Pin related to GPIO	Pin related to CAN	Pin related to I2S1/2	Pin related to MediaLB	Pin related to GPIO	Pin related to CAN	Pin related to I2S1	Pin related to MediaLB	Pin related to SPI	Pin related to GPIO	Pin related to CAN	Pin related to I2S1/2	Pin related to MediaLB
208	V3	VIN1[7]	-	-	RI1[7]	GPIO_PD[5]	-	-	-	GPIO_PD[5]	-	-	-	-	GPIO_PD[5]	-	-	-
19	W1	VIN1[6]	-	-	RI1[6]	GPIO_PD[4]	-	-	-	GPIO_PD[4]	-	-	-	-	GPIO_PD[4]	-	-	-
118	W2	VIN1[5]	-	-	RI1[5]	-	CAN_TX0	-	-	-	CAN_TX0	-	-	-	-	CAN_TX0	-	-
209	W3	VIN1[4]	-	-	RI1[4]	-	CAN_RX0	-	-	-	CAN_RX0	-	-	-	-	CAN_RX0	-	-
292	W4	VIN1[3]	-	-	RI1[3]	-	CAN_TX1	-	-	-	CAN_TX1	-	-	-	-	CAN_TX1	-	-
119	Y2	VIN1[2]	-	-	RI1[2]	-	CAN_RX1	-	-	-	CAN_RX1	-	-	-	-	CAN_RX1	-	-
210	Y3	VIN1[1]	-	-	GI1[7]	-	-	I2S_SCK1	-	-	-	I2S_SCK1	-	-	-	-	I2S_SCK1	-
293	Y4	VIN1[0]	-	-	GI1[6]	-	-	I2S_WS1	-	-	-	I2S_WS1	-	-	-	-	I2S_WS1	-
211	AA3	VINVSYNC1	-	-	VINVSYNC1	-	-	I2S_ECLK1	-	-	-	I2S_ECLK1	-	-	-	-	I2S_ECLK1	-
294	AA4	VINHSYNC1	-	-	VINHSYNC1	-	-	I2S_SDI1	-	-	-	I2S_SDI1	-	-	-	-	I2S_SDI1	-
22	AB1	VINFID1	-	-	VINFID1	-	-	I2S_SDO1	-	-	-	I2S_SDO1	-	-	-	-	I2S_SDO1	-
202	M3	VINVSYNC0	-	-	GI1[5]	-	-	-	MLB_DATA	-	-	-	MLB_DATA	-	-	-	-	MLB_DATA
203	N3	VINHSYNC0	-	-	GI1[4]	-	-	-	MLB_SIG	-	-	-	MLB_SIG	-	-	-	-	MLB_SIG
112	N2	VINFID0	-	-	GI1[3]	-	-	-	MLB_CLK	-	-	-	MLB_CLK	-	-	-	-	MLB_CLK
123	AD2	-	PWM_O0	-	GI1[2]	GPIO_PD[3]	-	-	-	GPIO_PD[3]	-	-	-	-	GPIO_PD[3]	-	-	-
122	AC2	-	PWM_O1	-	BI1[7]	GPIO_PD[2]	-	-	-	GPIO_PD[2]	-	-	-	-	GPIO_PD[2]	-	-	-
121	AB2	-	-	I2S_SDO2	BI1[6]	-	-	I2S_SDO2	-	-	-	-	-	SPI_DO	GPIO_PD[1]	-	-	-
24	AD1	-	-	I2S_ECLK2	BI1[5]	-	-	I2S_ECLK2	-	-	-	-	-	Reserved (Input/Output)	GPIO_PD[0]	-	-	-
23	AC1	-	-	I2S_SCK2	BI1[4]	-	-	I2S_SCK2	-	-	-	-	-	SPI_SCK	-	-	I2S_SCK2	-
295	AB4	-	-	I2S_WS2	BI1[3]	-	-	I2S_WS2	-	-	-	-	-	SPI_SS	-	-	I2S_WS2	-
212	AB3	-	-	I2S_SDI2	BI1[2]	-	-	I2S_SDI2	-	-	-	-	-	SPI_DI	-	-	I2S_SDI2	-

Pin multiplex group #2 mode setting

This mode is set with MPX_MODE_2 bit (bit 2-0) in the multiplex mode setting register (CMUX_MD.)

MPX_MODE_2 (bit 2-0) of the CMUX_MD register	Pin multiplex group #2 mode
000	Mode 0
001	Mode 1
010	Mode 2
011	Mode 3
100	Mode 4
101 – 0110	Reserved
111	(Initial value)

Pin multiplex group #3 (setting pin: USB_MODE)

Pin No.	JEDEC	Mode 0	Mode 1
		Pin related to USB 2.0 host	Pin related to USB 2.0 function
114	R2	USB_FSDP	USB_FSDP
115	T2	USB_FSDM	USB_FSDM
15	R1	USB_HSDP	USB_HSDP
16	T1	USB_HSDM	USB_HSDM
18	V1	USB_CRYCK48	USB_CRYCK48
230	AD19	USB_PRTPWR	USB_PRTPWR

Pin multiplex group #3 mode setting

This mode is set with external pin, USB_MODE.

USB_MODE pin	Pin multiplex group #3 mode
"L"	Mode 0
"H"	Mode 1

Pin multiplex group #4 (setting register: PIN_MPX_Select.MPX_MODE_4 [1:0])

Pin No.	JEDEC	Mode 0	Mode 1				
		Pin related to IDE	Pin related to I2S1	Pin related to CAN	Pin related to GPIO	Pin related to PWM	Unused pin (input/output)
29	AF4	IDE_XDRESET	-	-	-	-	Reserved (output)
28	AF3	IDE_XIOCS16	I2S_SDI1	-	-	-	-
125	AE3	IDE_XDASP	I2S_WS1	-	-	-	-
215	AD4	IDE_DDMARQ	I2S_ECLK1	-	-	-	-
296	AC4	IDE_DINTRQ	I2S_SDO1	-	-	-	-
214	AD3	IDE_XCBLID	I2S_SCK1	-	-	-	-
297	AC5	IDE_DD[15]	-	CAN_TX0	-	-	-
216	AD5	IDE_DD[14]	-	CAN_RX0	-	-	-
127	AE5	IDE_DD[13]	-	CAN_TX1	-	-	-
30	AF5	IDE_DD[12]	-	CAN_RX1	-	-	-
298	AC6	IDE_DD[11]	-	-	GPIO_PD[23]	-	-
217	AD6	IDE_DD[10]	-	-	GPIO_PD[22]	-	-
128	AE6	IDE_DD[9]	-	-	GPIO_PD[21]	-	-
31	AF6	IDE_DD[8]	-	-	GPIO_PD[20]	-	-
299	AC7	IDE_DD[7]	-	-	GPIO_PD[19]	-	-
218	AD7	IDE_DD[6]	-	-	GPIO_PD[18]	-	-
129	AE7	IDE_DD[5]	-	-	GPIO_PD[17]	-	-
32	AF7	IDE_DD[4]	-	-	GPIO_PD[16]	-	-
300	AC8	IDE_DD[3]	-	-	GPIO_PD[15]	-	-
219	AD8	IDE_DD[2]	-	-	GPIO_PD[14]	-	-
130	AE8	IDE_DD[1]	-	-	GPIO_PD[13]	-	-
33	AF8	IDE_DD[0]	-	-	-	-	Reserved (input/output)
213	AC3	IDE_DIORDY	-	-	-	-	Reserved (input)
301	AC9	IDE_DA[2]	-	-	-	-	Reserved (output)
220	AD9	IDE_DA[1]	-	-	-	PWM_O1	-
131	AE9	IDE_DA[0]	-	-	-	PWM_O0	-
35	AF10	IDE_XDCS[1]	-	-	-	-	Reserved (output)
132	AE10	IDE_XDCS[0]	-	-	-	-	Reserved (output)
221	AD10	IDE_XDIOR	-	-	-	-	Reserved (output)
302	AC10	IDE_XDIOW	-	-	-	-	Reserved (output)
34	AF9	IDE_CSEL	-	-	-	-	Reserved (output)
126	AE4	IDE_XDDMACK	-	-	-	-	Reserved (output)

Pin multiplex group #4 mode setting

This mode is set with MPX_MODE_4 bit (bit 5-4) in the multiplex mode setting register (CMUX_MD.)

MPX_MODE_4 (Bit 5-4) of the CMUX_MD register	Pin multiplex group #4 mode
00	Mode 0
01	Mode 1
10	Reserved
11	(Initial value)

Pin multiplex group #5 (setting pin: MPX_MODE_5 [1:0])

Pin No.	JEDEC	Mode 0	Mode 1	Mode 2	
		Pin related to ETM	Pin related to UART3/4/5	Pin related to UART3/4	Pin related to PWM
270	C10	TRACECLK	UART_SIN3	UART_SIN3	-
185	B10	TRACECTL	UART_SOUT3	UART_SOUT3	-
92	A10	TRACEDATA[3]	UART_SIN4	UART_SIN4	-
346	D11	TRACEDATA[2]	UART_SOUT4	UART_SOUT4	-
269	C11	TRACEDATA[1]	UART_SIN5	-	PWM_O1
184	B11	TRACEDATA[0]	UART_SOUT5	-	PWM_O0

Pin multiplex group #5 mode setting

This mode is set with external pin, MPX_MODE_5[1:0].

MPX_MODE_5[1] pin	MPX_MODE_5[0] pin	Pin multiplex group #5 mode
"L"	"L"	Mode 0
"L"	"H"	Mode 1
"H"	"L"	Mode 2
"H"	"H"	Mode 0

7.2. Pin Function

Format

Pin function list is shown in the following format.

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description

Meaning of item and sign

Pin name

Name of external pin.

I/O

Input/Output signal's distinction based on this LSI.

- I: Pin that can be used as input
- O: Pin that can be used as output
- IO: Pin that can be used as input and output (interactive pin)

Polarity

Active polarity of external pin's input/output signals

- P: "H" active pin (positive logic)
- N: "L" active pin (negative logic)
- PN: "H" and "L" active pins

Analog/Digital

Signal type of external pin

- A: Analog signal
- D: Digital signal

Type

Input/Output circuit type of external pin.

- CLK:
- POD: Pseudo Open Drain
- PU: Pull Up
- PD: Pull Down
- ST: Schmitt Type
- Tri: Tri-state

Pin status after reset

Pin status after external pin reset

- H: "H" level
- L: "L" level
- HiZ: High impedance
- X: "H" level or "L" level
- A: Clock output

Description

Outline of external pin function

7.2.1. External bus interface related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
MEM_XCS[4]	O	N	D	-	H	Chip select 4
MEM_XCS[2]	O	N	D	-	H	Chip select 2
MEM_XCS[0]	O	N	D	-	H	Chip select 0
MEM_XRD	O	N	D	-	H	Read strobe
MEM_XWR[3:2]	O	N	D	-	H	Write strobe MEM_XWR[3] -> MEM_ED[31:24], MEM_XWR[2] -> MEM_ED[23:16] (optional pin)
MEM_XWR[1:0]	O	N	D	-	H	Write strobe MEM_XWR[1] -> MEM_ED[15:8], MEM_XWR[0] -> MEM_ED[7:0]
MEM_RDY	I	P	D	-	-	Ready input for slow device
MEM_EA[24:1]	O	-	D	-	L	Address bus
MEM_ED[31:16]	IO	-	D	-	HiZ	Bi-directional data bus (optional pin)
MEM_ED[15:0]	IO	-	D	-	HiZ	Bi-directional data Bus
DREQ[7:6]	I	-	D	-	-	External DMA request
XDACK[7:6]	O	P	D	-	L	External DMA acknowledge

7.2.2. IDE66 related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
IDE_XDRESET	O	N	D	-	H	IDE reset
IDE_DD[15:0]	IO	-	D	PD	L	IDE device data
IDE_XDCS[1:0]	O	N	D	-	H	IDE chip select
IDE_DA[2:0]	O	P	D	-	L	IDE device address
IDE_XDIOR	O	N	D	-	H	IDE device I/O read
IDE_XDIOW	O	N	D	-	H	IDE device I/O write
IDE_DIORDY	I	P	D	-	-	IDE I/O channel ready
IDE_DDMARQ	I	P	D	-	-	IDE device DMA request
IDE_XDDMACK	O	N	D	-	H	IDE device DMA acknowledge
IDE_CSEL	O	P	D	-	L	IDE cable select
IDE_XIOCS16	I	N	D	-	-	IDE 16 bit I/O
IDE_XDASP	I	N	D	PD	-	IDE device active
IDE_DINTRQ	I	P	D	PD	-	IDE Interrupt
IDE_XCBLID	I	N	D	PD	-	IDE cable ID

7.2.3. SD Memory controller related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
SD_CLK	O	N	D	-	L	Media clock
SD_CMD	IO	-	D	-	HiZ	Media command
SD_DAT[3:0]	IO	-	D	-	HiZ	Media data
SD_WP	I	P	D	-	-	Media write protection
SD_XMCD	I	N	D	-	-	Media card detection

7.2.4. USB 2.0 Host/Function related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
USB_FSDP	IO	-	A	-	-	D+ for FS
USB_FSDM	IO	-	A	-	-	D- for FS
USB_HSDP	IO	-	A	-	-	D+ for HS
USB_HSDM	IO	-	A	-	-	D- for HS
USB_CRYCK48	I	-	D	CLK	-	Clock used for USB communication
USB_PRTPWR	O	-	D	-	L	USB port power control
USB_EXT12K	O	-	A	-	-	External resistance pin This should be connected to USB_AVDB through 12kΩ resistance.
USB_AVSP	I	-	A	-	-	PLL ground
USB_AVSB	I	-	A	-	-	Reference voltage ground
USB_AVDP	I	-	A	-	-	PLL power supply
USB_AVDB	I	-	A	-	-	Reference voltage power supply
USB_AVSF1	I	-	A	-	-	Driver/Receiver ground 1
USB_AVDF1	I	-	A	-	-	Driver/Receiver power supply 1
USB_AVSF2	I	-	A	-	-	Driver/Receiver ground 2
USB_AVDF2	I	-	A	-	-	Driver/Receiver power supply 2

7.2.5. External interrupt controller related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
INT_A[3:0]	I	PN	D	-	-	Asynchronous external interrupt requests

7.2.6. UART related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
UART_SIN0	I	P	D	-	-	Input data signal
UART_SOUT0	O	P	D	-	H	Output data signal
UART_XCTS0	I	N	D	-	-	Clear to send
UART_XRTS0	O	N	D	-	H	Request to send
UART_SIN1	I	P	D	-	-	Input data signal
UART_SOUT1	O	P	D	-	H	Output data signal
UART_SIN2	I	P	D	-	-	Input data signal
UART_SOUT2	O	P	D	-	H	Output data signal
UART_SIN3	I	P	D	-	-	Input data signal (optional)
UART_SOUT3	O	P	D	-	H	Output data signal (optional)
UART_SIN4	I	P	D	-	-	Input data signal (optional)
UART_SOUT4	O	P	D	-	H	Output data signal (optional)
UART_SIN5	I	P	D	-	-	Input data signal (optional)
UART_SOUT5	O	P	D	-	H	Output data signal (optional)

7.2.7. CAN related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
CAN_TX0	O	-	D	PD	H	Transmission (optional)
CAN_RX0	I	-	D	PD	-	Reception (optional)
CAN_TX1	O	-	D	PD	H	Transmission (optional)
CAN_RX1	I	-	D	PD	-	Reception (optional)

7.2.8. I2S related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
I2S_ECLK0	I	-	D	-	-	External clock (optional)
I2S_SCK0	IO	-	D	-	HiZ	Clock (optional)
I2S_WS0	IO	PN	D	-	HiZ	Sync (optional)
I2S_SDI0	I	P	D	-	-	Input data signal (optional)
I2S_SDO0	O	P	D	-	Hiz	Output data signal (optional)
I2S_ECLK1	I	-	D	-	-	External clock (optional)
I2S_SCK1	IO	-	D	PD	L	Clock (optional)
I2S_WS1	IO	PN	D	PD	L	Sync(optional)
I2S_SDI1	I	P	D	-	-	Input data signal (optional)
I2S_SDO1	O	P	D	PD	L	Output data signal (optional)
I2S_ECLK2	I	-	D	PD	-	External clock (optional)
I2S_SCK2	IO	-	D	PD	L	Clock (optional)
I2S_WS2	IO	PN	D	PD	L	Sync (optional)
I2S_SDI2	I	P	D	-	-	Input data signal (optional)
I2S_SDO2	O	P	D	PD	L	Output data signal (optional)