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Automotive Solutions

CMOS

FlexRay ASSP

MB88121/MB88121A/MB88121B/MB88121C

■ DESCRIPTION

The MB88121 Series FlexRay ASSP (application specific standard product) facilitates to add FlexRay connectivity to 8-bit, 16-bit and 32-bit microcontrollers that do not comprise embedded FlexRay protocol cores. The device features a FlexRay communication controller based on the ERAY[*1] IP core provided by Bosch. The most recent FlexRay communication controller complies to the protocol definition 2.1 of the FlexRay consortium. Fujitsu intends to update the communications controller when new protocol definitions are released. Please, refer to the chapter 'product lineup' for a cross reference between device version and protocol version supported. Several parallel and serial interfaces provide connectivity to a vast number of host processors.

All types of host interfaces are selectable by mode pins that supersede any programming by the user. The configurable parallel host interface connects to most 16-bit and 32-bit microcontrollers while SPI offers serial interfacing options. A DMA support unit avoids that the application on the host processor has to wait until the input buffer becomes available for writing.

The version suffix 'B/C' of the ASSP is operated from a single 3.3V or 5.0 V supply and includes an on board voltage regulator that provides 1.8 V to the internal core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 80 MHz clock from an external 4 MHz, 5 MHz, 8 MHz, 10 MHz, 16 MHz[*2] or 20 MHz[*2] clock. Alternatively the user may choose to drive the clock input with a square wave signal from the host processor.

*1 : License of Robert Bosch GmbH

*2 : MB88121C only

FUJITSU

■ PACKAGE

64-pin Plastic LQFP

(FPT-64P-M03/M24)
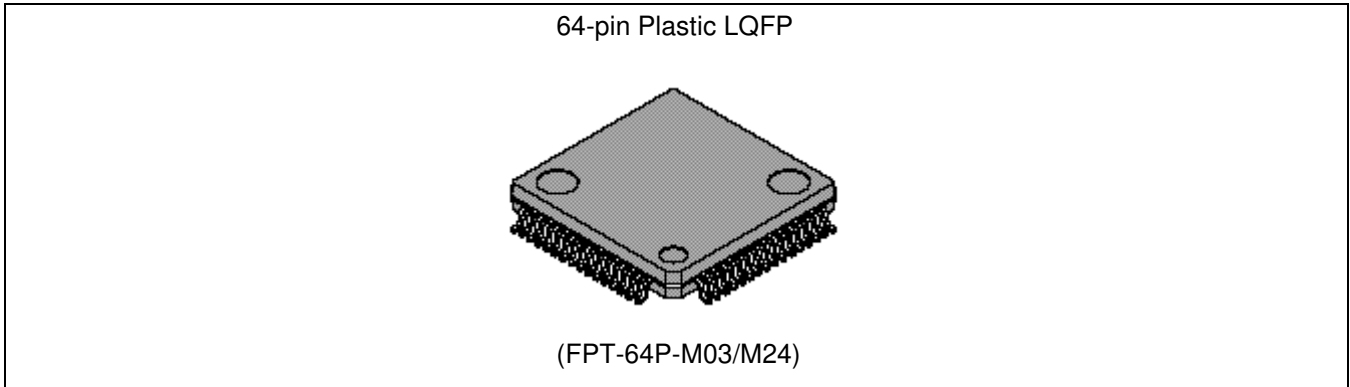
The device is offered in a standard 64-pin quad flatpack package with a pin pitch of 0.5 mm.

■ FEATURES

- FlexRay communication controller based on ERAY[*1] IP core from Bosch
    - Data rates of up to 10 Mbit/s on each channel
    - Up to 128 message buffers configurable
    - 8 Kbyte of Message RAM for storage of e.g. 128 message buffers with max. 48 byte data section or up to 30 message buffers with 254 byte data section
    - Configuration of message buffers with different payload lengths possible
    - One configurable receive FIFO
    - Each message buffer can be configured as receive buffer, as transmit buffer or as part of the receive FIFO
    - Host access to message buffers via Input and Output Buffer
        Input Buffer: Holds message to be transferred to the Message RAM
        Output Buffer: Holds message read from the Message RAM
    - Filtering for slot counter, cycle counter, and channel
    - Maskable module interrupts
    - Network Management supported
- Configurable parallel host interface
- SPI interface (8 Mbit/s) (MB88121B/C only)
- DMA support unit (MB88121A/B/C only)
- 0.18μm CMOS Process Technology
- Single voltage supply (5.0 V / 3.3 V), internal voltage regulator for 1.9 V core voltage offering low EMI and low power consumption (MB88121B/C only)
- Package : 64-pin[*2] plastic LQFP;

*1 : License of Robert Bosch GmbH

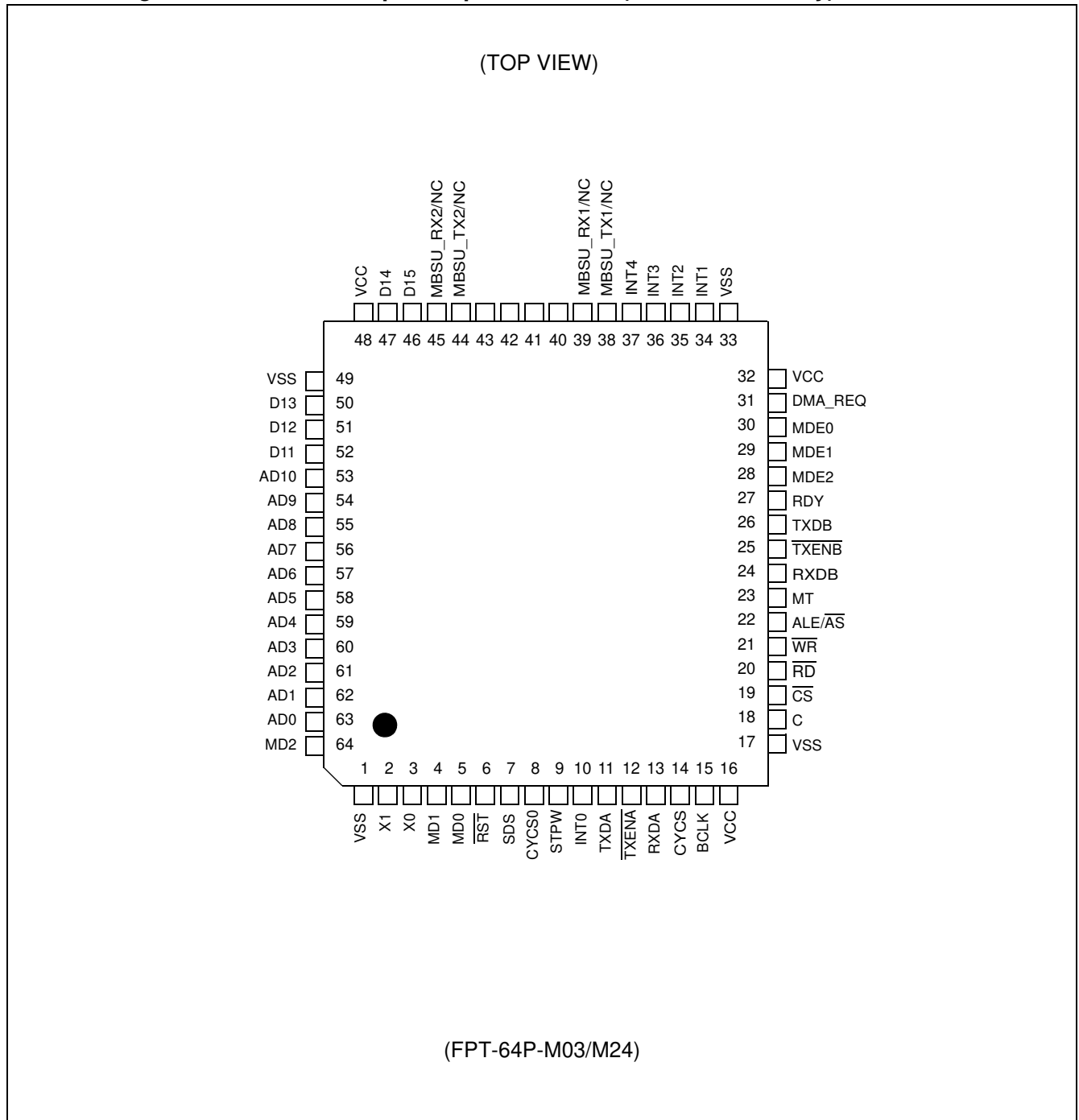*2: Other packages such as 48-pin plastic LQFP featuring only SPI host interface are under consideration.
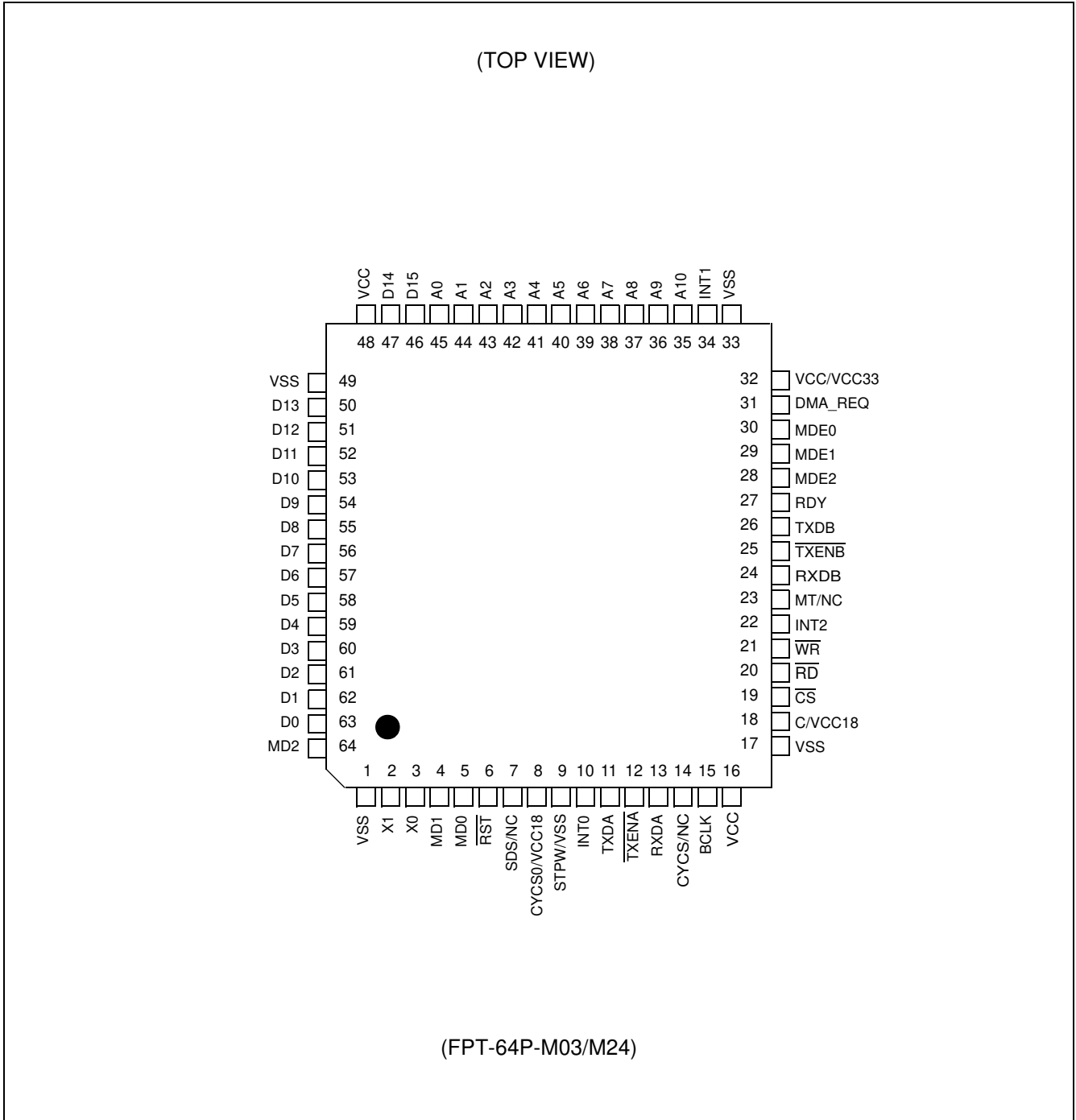
■ PRODUCT LINEUP

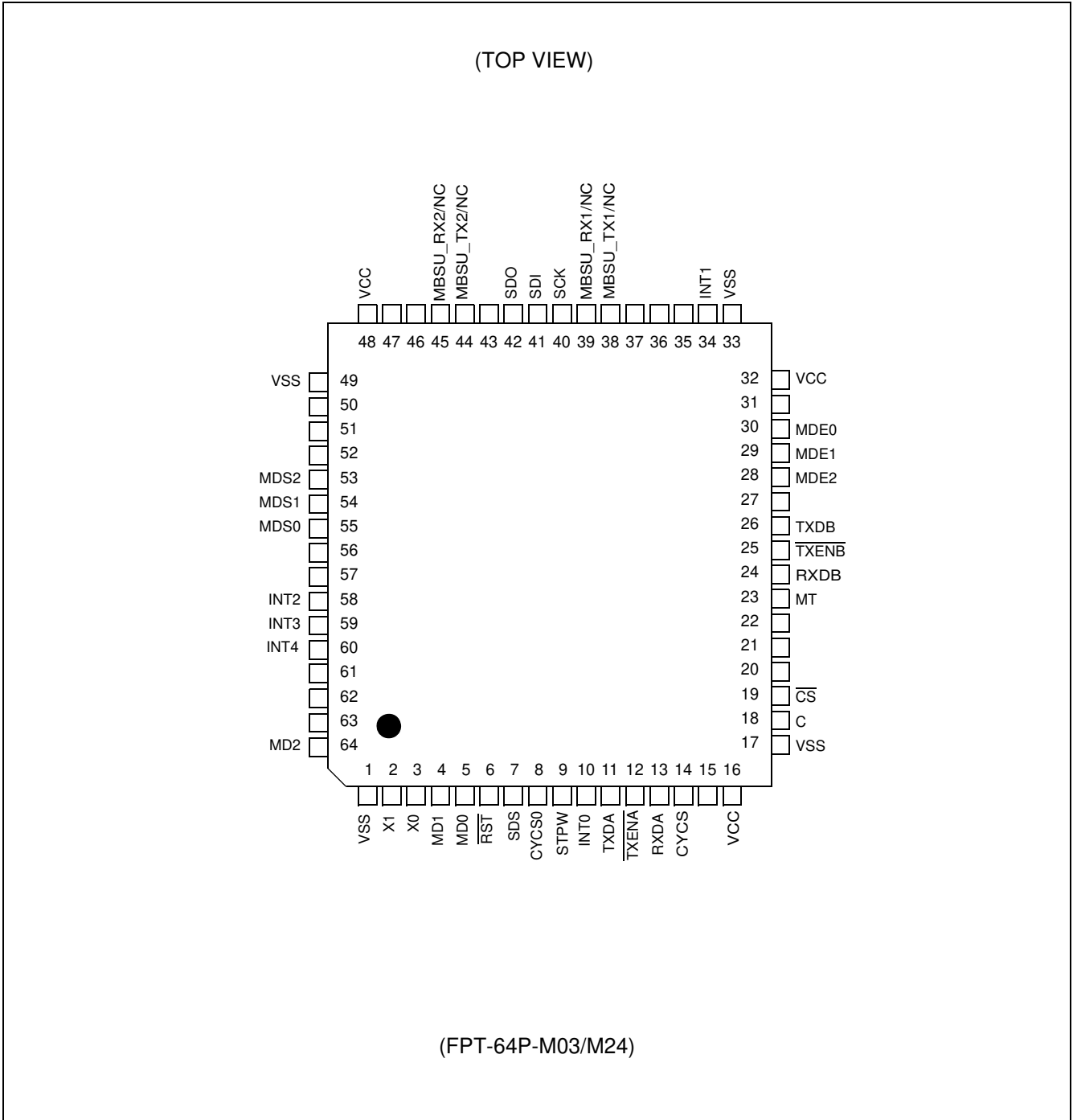| Part Number Parameter	MB88121	MB88121A	MB88121B	MB88121C
System clock	Direct clock input: 80MHz (or 40MHz for 5Mbit/s). On-chip PLL (evaluation pending): External clock 10 MHz, internal clock 80 MHz (50% duty cycle).		On-chip PLL (jitter evaluation pending) External clock input 4/5/8/10 MHz	Direct clock input: 80MHz. On-chip PLL (jitter evaluation pending) External clock input 4/5/8/10/16/20 MHz
Technology	0.18μm CMOS with triple voltage supply (5.0V, 3.3V, 1,8V).		0.18μm CMOS with on-chip voltage regulator for internal power supply.	
Operating voltage range	5.0V±0.5V, 3.3V±0.3V, 1.8V±0.15V		3.0 V - 5.5 V	
Temperature range	$T_A = -40 \,^\circ C$ to $+85 \,^\circ C$		$T_A = -40 \,^\circ C$ to $+105 \,^\circ C$	$T_A = -40 \,^\circ C$ to $+125 \,^\circ C$
Package	LQFP-64			
FlexRay Protocol version	2.0	2.1	V2.1	
Parallel host interface	Configurable parallel host interface compatible with Fujitsu 32-bit FR microcontrollers. Maximum frequency 33MHz (target)		Configurable parallel host interface compatible with Fujitsu 16-bit 16FX and 32-bit FR microcontrollers.	
SPI interface	-		Configurable clocking schemes and bit direction.	
DMA support unit	-	Generates DMA request signal for host processor for writing the input buffer. Thus the possibility that the input buffer is busy does not produce any waiting time at the host that can issue other tasks during the buffer writing.		
Low voltage interrupt (tbd)	-		Generates an interrupt when internal or external operating voltage drops below certain limits.	

.

■ **PIN ASSIGNMENTS**

1. **Pin assignment in 16 bit multiplexed parallel mode (MB88121B/C only)**

(TOP VIEW)

(FPT-64P-M03/M24)

2. Pin assignment in 16 bit non-multiplexed parallel mode

(TOP VIEW)

Top pins (left to right, 48–33): VCC, D14, D15, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, INT1, VSS

Pin	Left side		Pin	Right side
49	VSS		32	VCC/VCC33
50	D13		31	DMA_REQ
51	D12		30	MDE0
52	D11		29	MDE1
53	D10		28	MDE2
54	D9		27	RDY
55	D8		26	TXDB
56	D7		25	$\overline{\text{TXENB}}$
57	D6		24	RXDB
58	D5		23	MT/NC
59	D4		22	INT2
60	D3		21	$\overline{\text{WR}}$
61	D2		20	$\overline{\text{RD}}$
62	D1		19	$\overline{\text{CS}}$
63	D0		18	C/VCC18
64	MD2		17	VSS

Bottom pins (left to right, 1–16): VSS, X1, X0, MD1, MD0, $\overline{\text{RST}}$, SDS/NC, CYCS0/VCC18, STPW/VSS, INT0, TXDA, $\overline{\text{TXENA}}$, RXDA, CYCS/NC, BCLK, VCC

(FPT-64P-M03/M24)

3. Pin assignment in SPI mode (MB88121B/C only)

(TOP VIEW)

(FPT-64P-M03/M24)

■ PIN DESCRIPTION
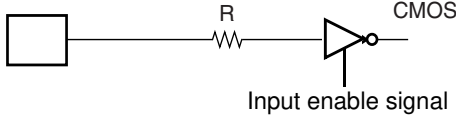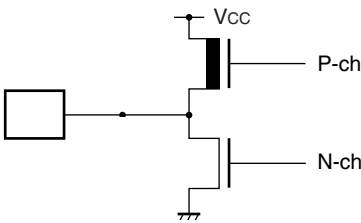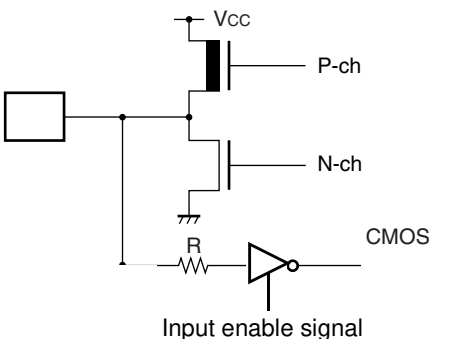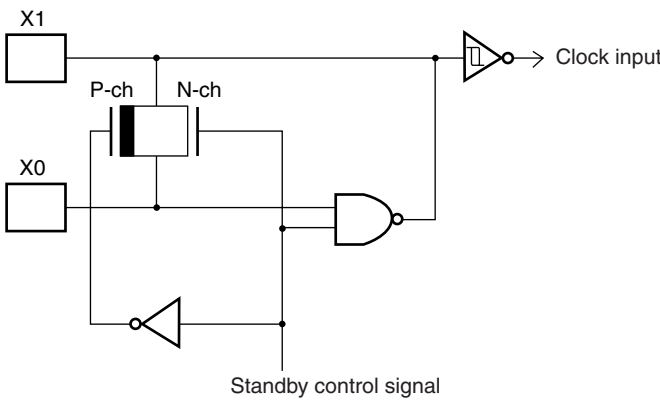
Pin No.	Pin name	Circuit type	Function
1, 17, 33, 49	VSS	—	These are power supply ground (0 V) input pins
16, 48	VCC	—	MB88121B/C: These are power supply (3.3 - 5.0 V) input pins. MB88121(A): These are power supply (5.0 V) input pins
32	VCC/VCC33	—	MB88121B/C: This is a power supply (3.3 - 5.0 V) input pin. MB88121(A): 3.3V supply voltage for the level converters.
18	C/VCC18	—	MB88121B/C: This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 μF ceramic capacitor. MB88121(A): 1.8V core supply input pin.
2	X1	D	Oscillation output pin.
3	X0		Oscillation input pin. If external clock is used, it is connected here.
4 - 5	MD1 - MD0	A	Input pins for the mode selection.
6	$\overline{\text{RST}}$	A	Reset input pin.
7	SDS/NC	B/-	MB88121B/C: Debug pin: Start of dynamic segment, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
8	CYCS0/VCC18	B/-	MB88121B/C: Debug pin: Cycle 0 start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): 1.8V core supply input pin.
9	STPWT/VSS	C/-	MB88121B/C: Stop Watch Trigger Input pin MB88121(A): Power supply ground (0 V) input pin.
10	INT0	B	Output pin for the Interrupt 0 output.
11	TXDA	B	Output pin for the data transmitter output channel A.
12	$\overline{\text{TXENA}}$	B	Output pin for the transmission enable output channel A.
13	RXDA	A	Input pin for the data receiver input channel A.
14	CYCS/NC	B/-	MB88121B/C: Debug pin: Cycle start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
15	BCLK	A	Input pin for the Bus Clock input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.
19	$\overline{\text{CS}}$	A	Input pin for the chip select input.
20	$\overline{\text{RD}}$	A	Input pin for the read enable input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.
21	$\overline{\text{WR}}$	A	Input pin for the write enable input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.

Pin No.	Pin name	Circuit type	Function
22	ALE	C	Input pin for the address latch enable input (high active). This function is enabled in the multiplexed parallel modes for 16FX and for other devices to be defined later.
	$\overline{AS}$		Input pin for the address strobe input (low active). This function is enabled in the multiplexed parallel modes. Timing meets FR core devices (460 series) and other devices.
	INT2		Output pin for the Interrupt 2 output. This function is enabled in 16-bit non-multiplexed parallel mode.
	-		This pin is Hi-Z in in SPI mode.
23	MT/NC	B/-	MB88121B/C: Debug pin; Macrotick start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
24	RXDB	A	Input pin for the data receiver input channel B.
25	$\overline{TXENB}$	B	Output pin for the transmission enable output channel B.
26	TXDB	B	Output pin for the data transmitter output channel B.
27	RDY	B	Output pin for the ready output. This function is enabled in all parallel modes.
	-		This pin is Hi-Z in SPI mode.
28-30	MDE2 - MDE0	A	Input pins for the extended mode selection.
31	DMA_REQ	B	Output pin for the DMA request output (MB88121A/B/C only). On MB88121, this pin outputs "L" level. This function is enabled in all parallel modes
	-	B	This pin is Hi-Z in SPI mode.
34	INT1	B	Output pin for the Interrupt 1 output.
35	A10	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT2		Output pin for the Interrupt 2 output. This function is enabled in 16-bit multiplexed parallel mode.
	-		This pin is Hi-Z in SPI mode.
36	A9	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT3		Output pin for the Interrupt 3 output. This function is enabled in 16-bit multiplexed parallel mode.
	-		This pin is Hi-Z in SPI mode.
37	A8	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed multiplexed parallel mode.
	INT4		Output pin for the Interrupt 4 output This function is enabled in 16-bit multiplexed parallel mode
	-		This pin is Hi-Z inSPI mode.

Pin No.	Pin name	Circuit type	Function
38	A7	C	Input pins for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MBSU_TX1		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
39	A6	C	Input pins for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MBSU_RX1		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
40	A5	A	Input pin for the address bus. This function is enabled 16-bit non-multiplexed parallel modes.
	SCK		Input pin for the serial clock input. This function is enabled in SPI mode.
	-		This pin is unused in 16-bit multiplexed parallel modes.
41	A4	A	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	SDI		Input pin for the serial data input. This function is enabled in SPI mode.
	-		This pin is unused in 16-bit multiplexed parallel modes.
42	A3	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	SDO		Output pin for the serial data output. When CS is "H" SDO is High-Z. This function is enabled in SPI mode.
	-		This pin is Hi-Z in 16-bit multiplexed parallel modes.
43	A2	A	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	-		This pin is unused in 16-bit multiplexed parallel mode and in SPI mode.
44	A1	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	MBSU_TX2		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.

Pin No.	Pin name	Circuit type	Function
45	A0	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	MBSU_RX2		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
46 - 47	D15 - D14	C	I/O pins for the data bus. This function is enabled in 16-bit multiplexed and non-multiplexed parallel modes.
	-		These pins are Hi-Z in SPI mode.
50 - 52	D13 - D11	C	I/O pins for the data bus. This function is enabled in 16-bit multiplexed and non-multiplexed parallel modes.
	-		These pins are Hi-Z in SPI mode.
53 - 55	AD10 - AD8	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D10 - D8		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MDS2 - MDS0		Input pins for specific settings of serial interfaces. This function is only enabled when serial mode was selected by MD / MDE.
56 - 57	AD7 - AD6	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D7 - D6		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	-		These pins are Hi-Z in SPI mode.
58 - 60	AD5 - AD3	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D5 - D3		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT2 - INT4		Output pins for the Interrupt 2 - 4 outputs. This function is enabled in SPI mode.
61 - 63	AD3 - AD0	C	I/O pins for the address/data bus. This function is enabled in 16-bit multiplexed parallel mode.
	D2 - D0		I/O pins for the data bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	-		These pins are Hi-Z in SPI mode.
64	MD2	A	Input pin for the mode selection.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	R CMOS Input enable signal	• CMOS hysteresis input
B	Vcc P-ch N-ch	• CMOS output
C	Vcc P-ch N-ch R CMOS Input enable signal	• CMOS output • CMOS hysteresis input with input enable signal
D	X1 P-ch N-ch X0 Standby control signal Clock input	• Oscillation feedback resistor : 1 MΩ approx.

■ **PIN FUNCTIONS VS. MODES**

Pin No.	16bit mux mode (MB88121B/C only)	16bit non mux mode	SPI mode (MB88121B/C only)
1	VSS		
2	X1		
3	X0		
4	MD1		
5	MD0		
6	$\overline{\text{RST}}$		
7	MB88121B/C: SDS; MB88121(A):NC		
8	MB88121B/C: CYCS0 ; MB88121(A): VCC18		
9	MB88121B/C: STPWT; MB88121(A): VSS		
10	INT0		
11	TXDA		
12	$\overline{\text{TXENA}}$		
13	RXDA		
14	MB88121B/C: CYCS; MB88121(A): NC		
15	BCLK		-
16	VCC		
17	VSS		
18	MB88121B/C: C; MB88121(A): VCC18		
19	$\overline{\text{CS}}$		
20	$\overline{\text{RD}}$		-
21	$\overline{\text{WR}}$		-
22	ALE/$\overline{\text{AS}}$	INT2	-
23	MB88121B/C: MT; MB88121(A): NC		
24	RXDB		
25	$\overline{\text{TXENB}}$		
26	TXDB		
27	RDY		-
28	MDE2		
29	MDE1		
30	MDE0		
31	DMA_REQ		-
32	MB88121B/C: VCC; MB88121(A): VCC33		
33	VSS		

Pin No.	16bit mux mode (MB88121B/C only)	16bit non mux mode	SPI mode (MB88121B/C only)
34	INT1		
35	INT2	A10	-
36	INT3	A9	-
37	INT4	A8	-
38	MBSU_TX1	A7	MBSU_TX1;
39	MBSU_RX1;	A6	MBSU_RX1;
40	-	A5	SCK
41	-	A4	SDI
42	-	A3	SDO
43	-	A2	-
44	MBSU_TX2;	A1	MBSU_TX2
45	MBSU_RX2;	A0	MBSU_RX2
46	D15		-
47	D14		-
48	VCC		
49	VSS		
50	D13		-
51	D12		-
52	D11		-
53	AD10	D10	MDS2
54	AD9	D9	MDS1
55	AD8	D8	MDS0
56	AD7	D7	-
57	AD6	D6	-
58	AD5	D5	INT2
59	AD4	D4	INT3
60	AD3	D3	INT4
61	AD2	D2	-
62	AD1	D1	-
63	AD0	D0	-
64	MD2		

■ **MODE SELECTION**

MD2	MD1	MD0	Mode	MDE2	MDE1	MDE0	Mode Expansion	
0	X	X	Reserved(Set-prohibitd)					
1	0	0	16-bit (Oscillator)	0	0	0	FR (460)[*1]	mux
				0	0	1	16FX[*1]	
				0	1	0	reserved (Set-prohibitd)	
				0	1	1	reserved (Set-prohibitd)	
				1	0	0	FR (460)	non mux
				1	0	1	16FX[*2]	
				1	1	0	FR (360)	
				1	1	1	reserved (Set-prohibitd)	
1	0	1	16-bit[*2] (External Clock Input)	0	0	0	FR (460)	mux
				0	0	1	16FX	
				0	1	0	reserved (Set-prohibitd)	
				0	1	1	reserved (Set-prohibitd)	
				1	0	0	FR (460)	non mux
				1	0	1	16FX	
				1	1	0	FR (360)	
				1	1	1	reserved (Set-prohibitd)	
1	1	0	Serial[*1]	Refer to tables for - frequency selection - serial type selection				
1	1	1	Reserved(Set-prohibitd)	X	X	X		

The table above describes the encoding of host interface options by mode pins. Basically these mode pins (MD[2:0]) select between the different bus types, parallel or serial, and in case of parallel type, their width. For 32-bit modes, the swapping of low word with high word for non-Intel style access is implicit part of the selected mode. The multiplex style for 16-bit modes is encoded in the mode expansion bits MDE[2:0].

The selection of the serial interface is encoded in MDE[2:0]. Implicitly type and operating frequency are encoded as well here. The specific settings of the selected serial interface are encasuplated in the special mode expansion pins MDS[2:0], that become available for MD[2:0] = 110B (select serial) only.

*1: MB88121B/C only

*2: MB88121C only

■ **Used Clock for X0/X1**

Input frequency of X0 and X1 is described Table below.

	MD[2:0]		
	100	101	110
Oscillator	4MHz/5MHz/8MHz	-	4MHz/5MHz/8MHz
External Clock	-	4MHz/5MHz/8MHz/ 10MHz/16MHz/20MHz/ 80MHz	4MHz/5MHz/8MHz/ 10MHz

■ **FREQUENCY SELECTION IN SERIAL MODE**

When operating the device via serial interface, the frequency set up according the table below needs to match the externally supplied clock.

MDE2	MDE1	Frequency
0	0	4 MHz
0	1	5 MHz
1	0	8 MHz
1	1	10 MHz

■ **SERIAL INTERFACE TYPE SELECTION**

The table below applies when MD[2:0] = 110B.

MDE0	Serial interface type
0	SPI (tbd)
1	Reserved

■ **SPI SETTINGS**

The table below applies when MD[2:0] = 110B and MDE0 = 0.

MDS2	MDS1	MDS0	Specific SPI Mode Settings
0	0	0	
0	0	1	MDS2=LSBFE: Bit Direction
0	1	0	1: Data is transferred least significant bit first. 0: Data is transferred most significant bit first.
0	1	1	MDS1=CPOL: Clock Polarity
1	0	0	1: Active-low clock. In idle state SCK is high. 0: Active-high clock. In idle state SCK is low.
1	0	1	MDS0=CPHA: Clock Phase
1	1	0	1: Sampling of data occurs at even edges of SCK. 0: Sampling of data occurs at odd edges of SCK.
1	1	1	

■ HANDLING DEVICES

Special care is required for the following when handling the device :
- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins (V$_{CC}$/V$_{SS}$)
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Notes on Energization
- Caution on Operation with PLL

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :
- A voltage higher than V$_{CC}$ or lower than V$_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V$_{CC}$ and V$_{SS}$.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V$_{CC}$ supply voltage operating range. Therefore, the V$_{CC}$ supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that V$_{CC}$ ripple variations (peak-to-peak values) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard V$_{CC}$ supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

Unused inputs that feature an internal pull up resistor, or unused inputs that have been disabled by a particular operational mode can be left open. Make sure that at least one condition is explicitly mentioned for the respective pin.

4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.
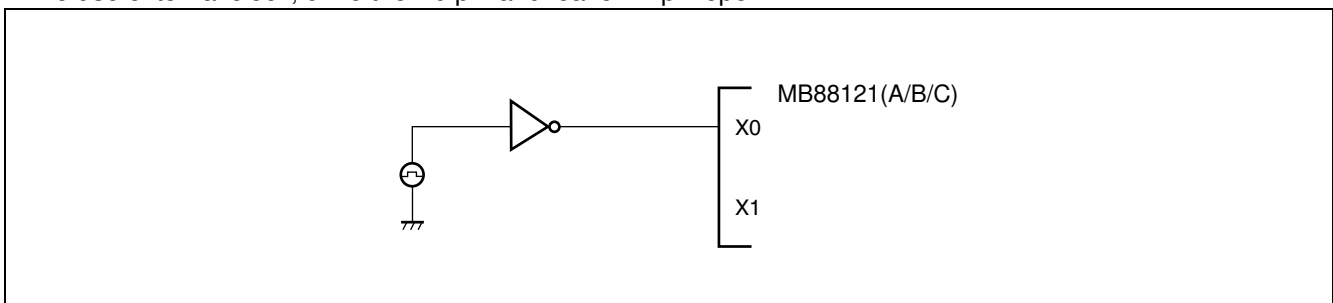
5. Power supply pins (V$_{CC}$/V$_{SS}$)
- If there are multiple V$_{CC}$ and V$_{SS}$ pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the Vcc and Vss pins to the power supply and ground externally.

- Connect Vcc and Vss to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 μF as a bypass capacitor between Vcc and Vss in the vicinity of Vcc and Vss pins of the device.
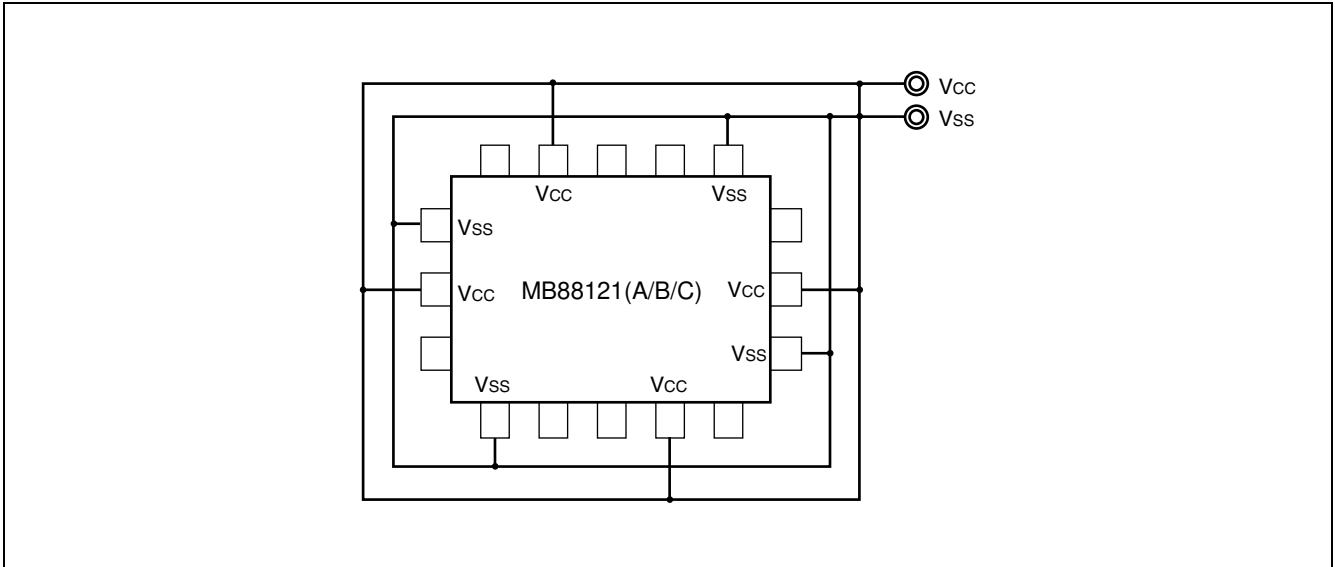
6.   Pull-up/down resistors

MB88121(A/B/C) does not provide internal pull-up/down resistors unless explicitly mentioned in the pin list. Use external components where needed.

7.   Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

8.   Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V) .

9.   Caution on Operation with PLL

As the device operates with an internal PLL clock, it attempts to be working with the self-oscillating circuit even when there is no external oscillator present or when the external clock input stopped. Performance of this operation, however, cannot be guaranteed.

10. Interrupt pin Assignment

The MB88121/A/B/C series supports interrupt pins. In the differrent operation interface modes the interrupt pin assignment is different.

For 16-bit none multiplexed mode (MD[2:0] = 1,0,0; MDE[2:0] = 1,x,x) the interrupt pin assignment is:

-

Pin name	Internal E-Ray signal	Description
INT0	eray_int0	Signal is activate if Interrupt line 0 is activated via ILE Register (ILE.0 = 1). All E-Ray interrupts set to Interrupt line0 and activated will be signaled via this pin (EILS, SILS EIES, SIES Register).
INT1	eray_int1	Signal is activate if Interrupt line 1 is activated via ILE Register(ILE.1 = 1) All E-Ray interrupts set to Interrupt line1 and activated will be signaled via this pin. (EILS, SILS EIES, SIES Register).
INT2	Timer 0 or Timer 1 interrupt, Low voltage detection	Timer0 and Timer 1 interrupts are signaled via this pins. They are logical or combined In case of low voltage detection it is indicated by INT2

For 16-bit multiplexed mode (MD[2:0] = 1,0,0; MDE[2:0] = 0,x,x) and SPI mode (MD[2:0] = 1,1,0) the interrupt pin assignment is:

Pin name	Internal E-Ray signal	Description
INT0	eray_int0	Signal is activate if Interrupt line is activated via ILE Register (ILE.0 = 1). All E-Ray interrupts set to Interrupt line0 and activated will be signaled via this pin (EILS, SILS EIES, SIES Register).
INT1	eray_int1	Signal is activate if Interrupt line is activated via ILE Register(ILE.1 = 1) All E-Ray interrupts set to Interrupt line1 and activated will be signaled via this pin. (EILS, SILS EIES, SIES Register).
INT2	Timer Interrupt 0	Timer0 Interrupt is signaled via this pins.
INT3	Timer interrupt 1	Timer1 Interrupt is signaled via this pins.
INT4	Low voltage detection	In case of low voltage detection it is indicated by INT4 pin.

11. Pin level at interrupt pins

In case that the interrupt pin is enabled following level is output

Level	Description
0	default value, no interrupt request is pending
1	Interrupt request is pending

The output changes to Low-Level when the corresponding flag in the E-Reay register is cleared.

For timer0 and timer1 interrupt pin(s) the High level is output only a dedicated time and set back to Low-Level.

See E-Ray User Manual for details. It is recommended to use egde detection at host side for these pins.

12. Data Accessing of MB88121 series

The MB88121 series includes a parallel bus Interface using 16-bit data width. However the internal Communication Controller requires a 32-bit data access. Therefore always access the MB88121 using 32-bit data access. The Bus Interface expect two 16-bit data transfer from the Host MCU.

The order of the transfer is important, otherwise data can be lost.

First 16-bit write cycle must be the lower, the second 16-bit write cycle the higher 16-bit address of the 32-bit address. As soon as data is written to the higher 16-bit Address, the Communication Controller is writing the 32-bit value to the address.

Example:

Write access to Input buffer: First 32-bit register WRDS1: (Address: 0x400 - 0x403)

Value of WRDS1 register: 0x0000 0000

First 16-bit write cycle via Bus interface to address 0x400-401: Value: 1234

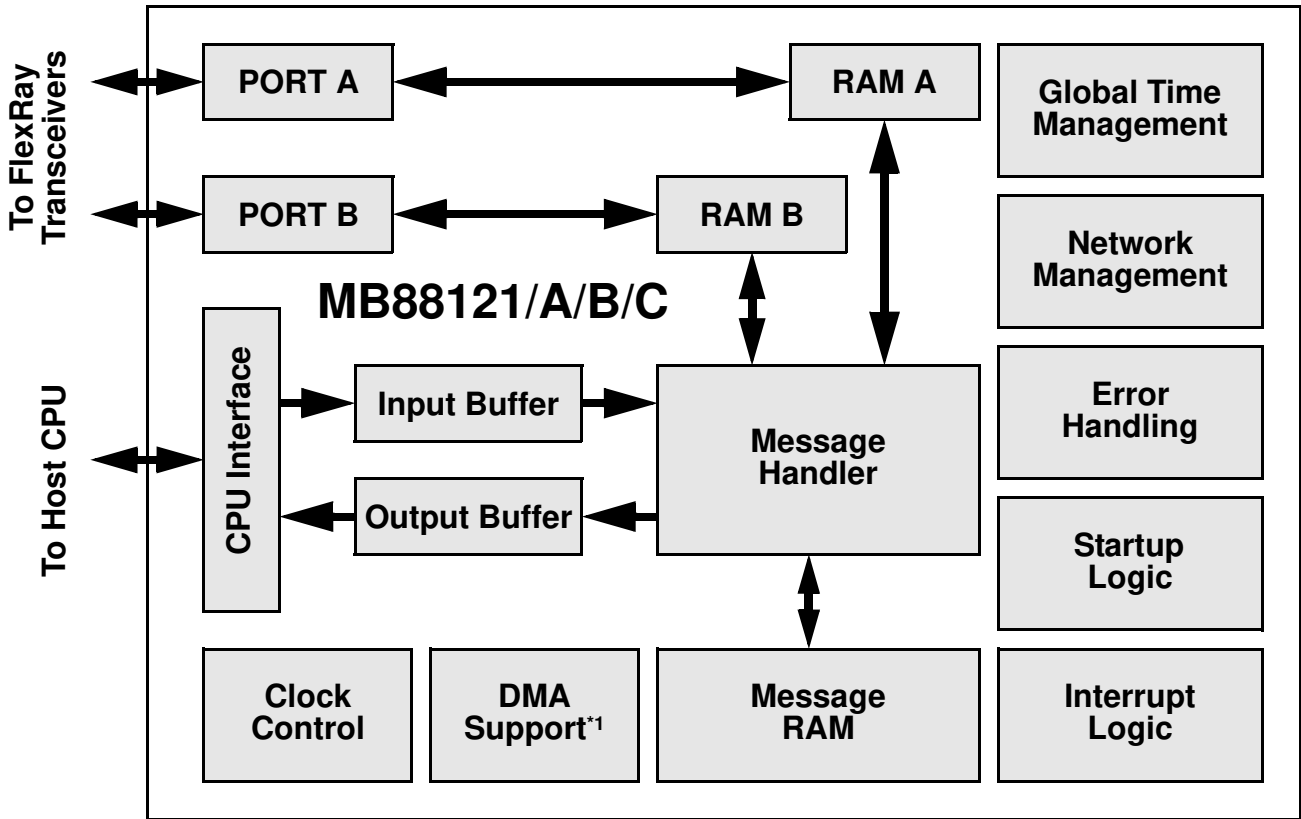Value of WRDS1 register: 0x0000 0000

Second 16 bit write cycle via Bus Interface to address 0x402 - 0x403: Value 5678

32-bit data written to WRDS1 address.
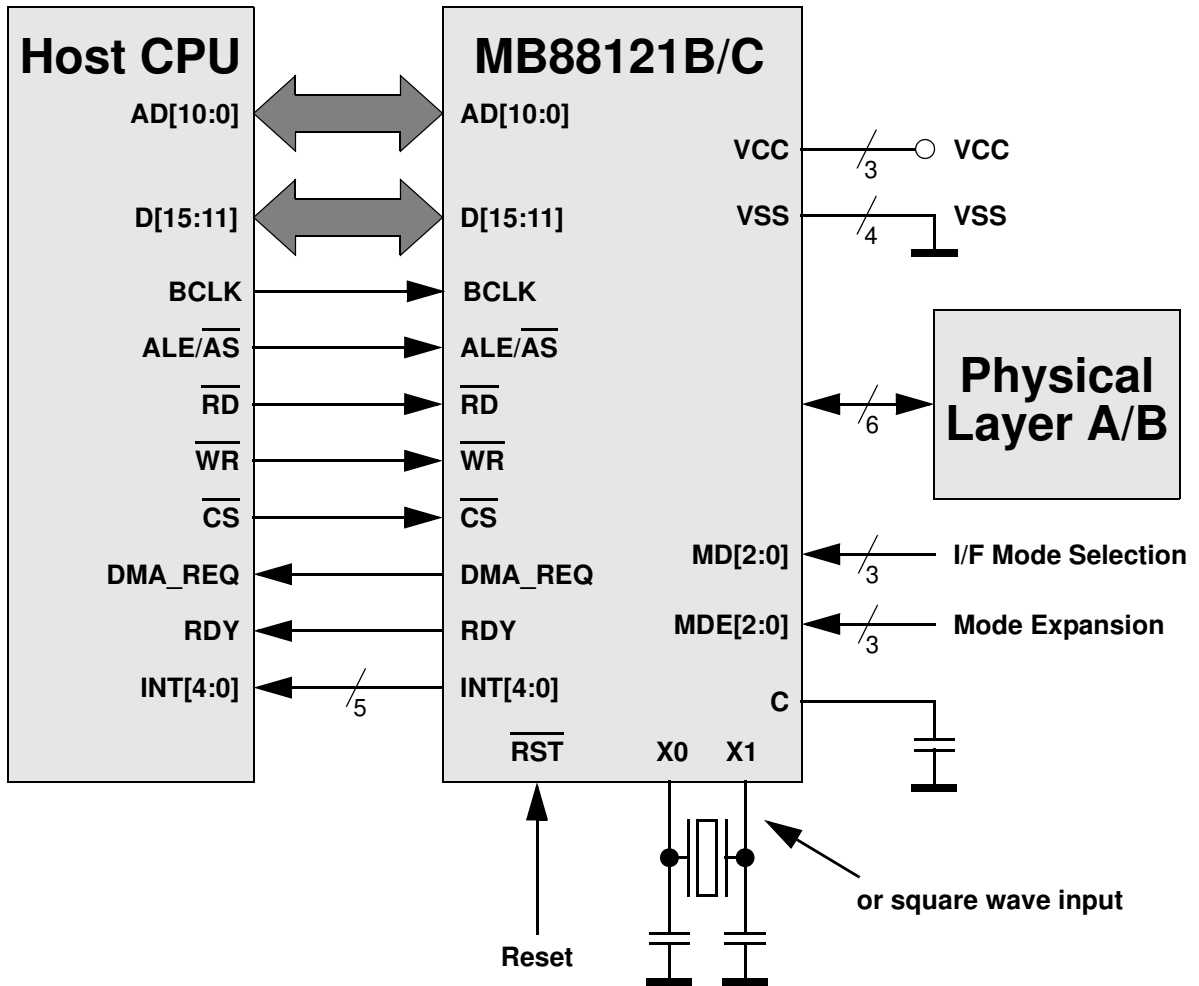
Value of WRDS1 register: 0x1234 5678

■ BLOCK DIAGRAM

MB88121/MB88121A/MB88121B/MB88121C

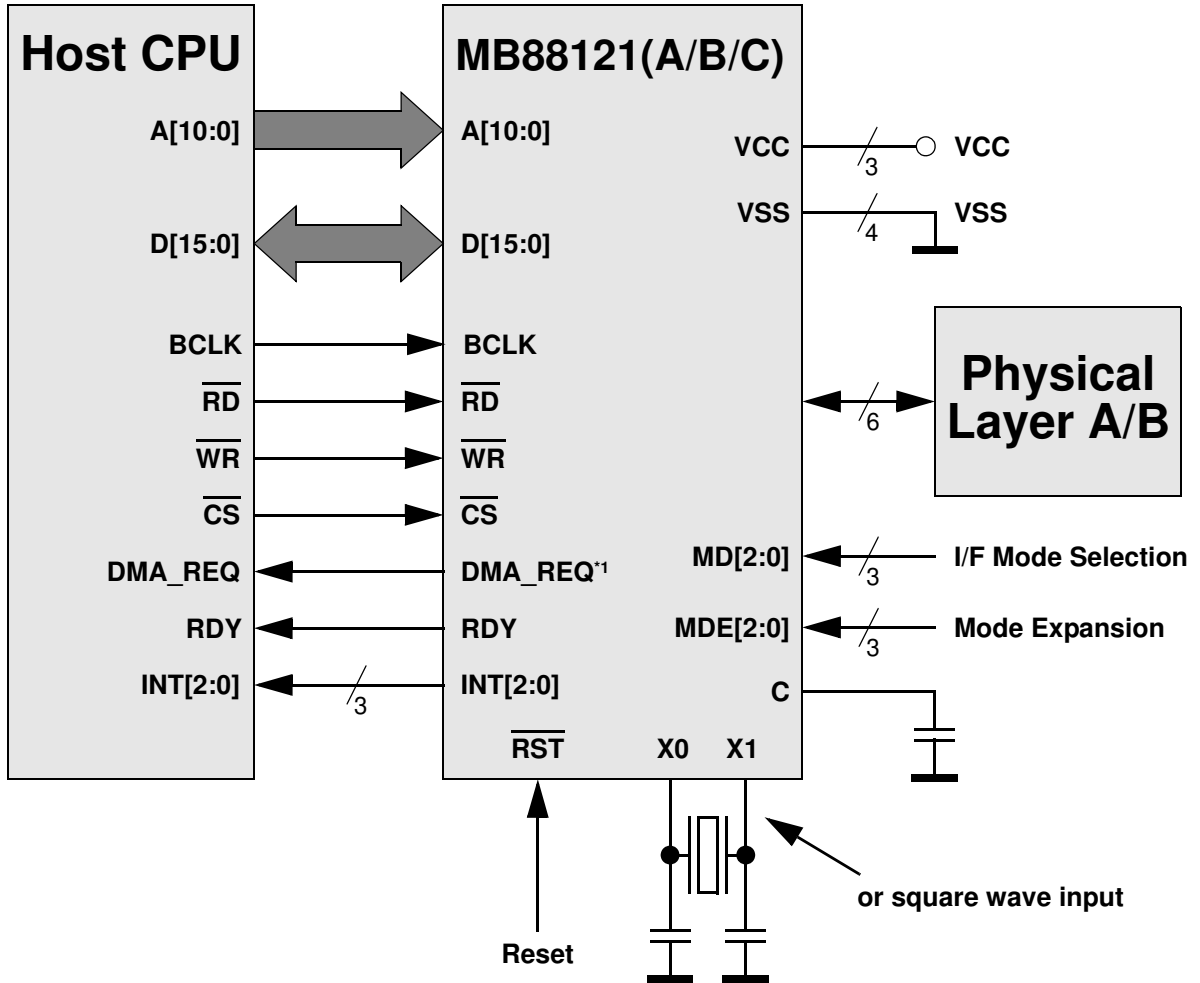*1: DMA support is only available on MB88121A/B/C

■ **HOST INTERFACES**

Connection to Host CPU in 16-bit multiplexed Mode (MB88121B/C only)

*1: DMA_REQ can only be used if RDY is not used, e.g. with automatic wait states.
   The initial function of the RDY/DMA_REQ pin is RDY.

Connection to Host CPU in 16-bit non-multiplexed Mode

*1: MB88121A/B/C only

Connection to Host CPU in SPI Mode (MB88121B/C only)