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CY88152A

Spread Spectrum Clock Generator

CY88152A is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates input frequency as Middle Centered and down spread which modulates so as not to exceed input frequency.

Features

- Input frequency : 16.6 MHz to 134 MHz
- Output frequency : 16.6 MHz to 134 MHz
- Modulation rate : ±0.5%, ±1.5% (Center spread), −1.0%, −3.0% (Down spread)
- Equipped with oscillation circuit: Range of oscillation 16.6 MHz to 48 MHz
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Less than 100 ps
- Low current consumption by CMOS process : 5.0 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature : −40° to +85 °C
- Package : SOP 8-pin

Contents

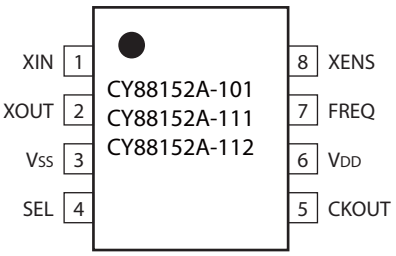
1. Product Line-up

CY88152A has three kinds of input frequency, and two kinds of modulation type (center/down spread), total six line-ups.

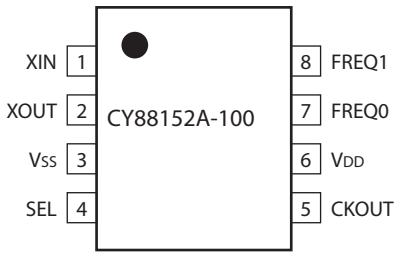
Product	Input/Output Frequency	Modulation Type	Modulation Enable Pin
CY88152A-100	16.6 MHz to 134 MHz	Down spread	No
CY88152A-101	16.6 MHz to 67 MHz		Yes
CY88152A-111	16.6 MHz to 67 MHz	Center spread	Yes
CY88152A-112	40 MHz to 134 MHz		

2. Pin Assignment

TOP VIEW



SOB008

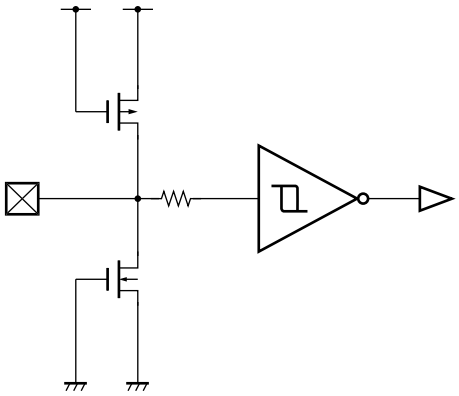
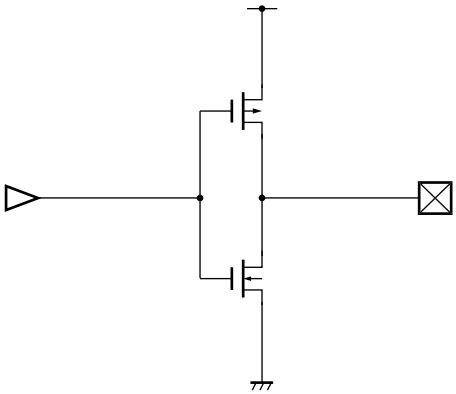


SOB008

3. Pin Description

Pin Name	I/O	Pin No.	Description
XIN	I	1	Crystal resonator connection pin/clock input pin
XOUT	O	2	Crystal resonator connection pin
V_{SS}	–	3	GND pin
SEL	I	4	Modulation rate setting pin
CKOUT	O	5	Modulated clock output pin
V_{DD}	–	6	Power supply voltage pin
FREQ/FREQ0	I	7	Frequency setting pin
XENS/FREQ1	I	8	Modulation enable setting pin/frequency setting pin

4. I/O Circuit Type

Pin	Circuit Type	Remarks
SEL FREQ FREQ0 FREQ1 XENS		CMOS hysteresis input
CKOUT		■ CMOS output ■ I_{OL} = 4 mA

Note: For XIN and XOUT pins, refer to “Oscillation Circuit”.

5. Handling Devices

Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} and V_{SS} pins. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

Handling Unused Pins

- Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.
- Unused output pin should be opened.

The Attention when the External Clock is Used

- Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.
- Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

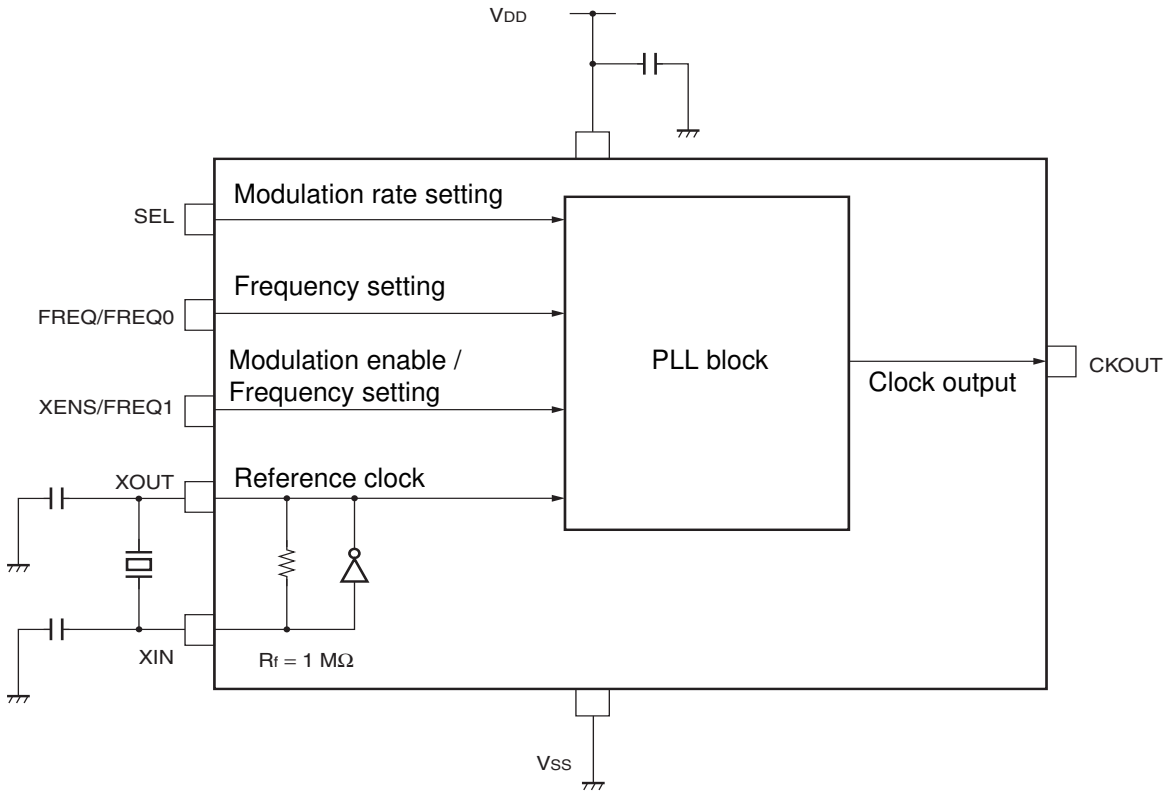
Power Supply Pins

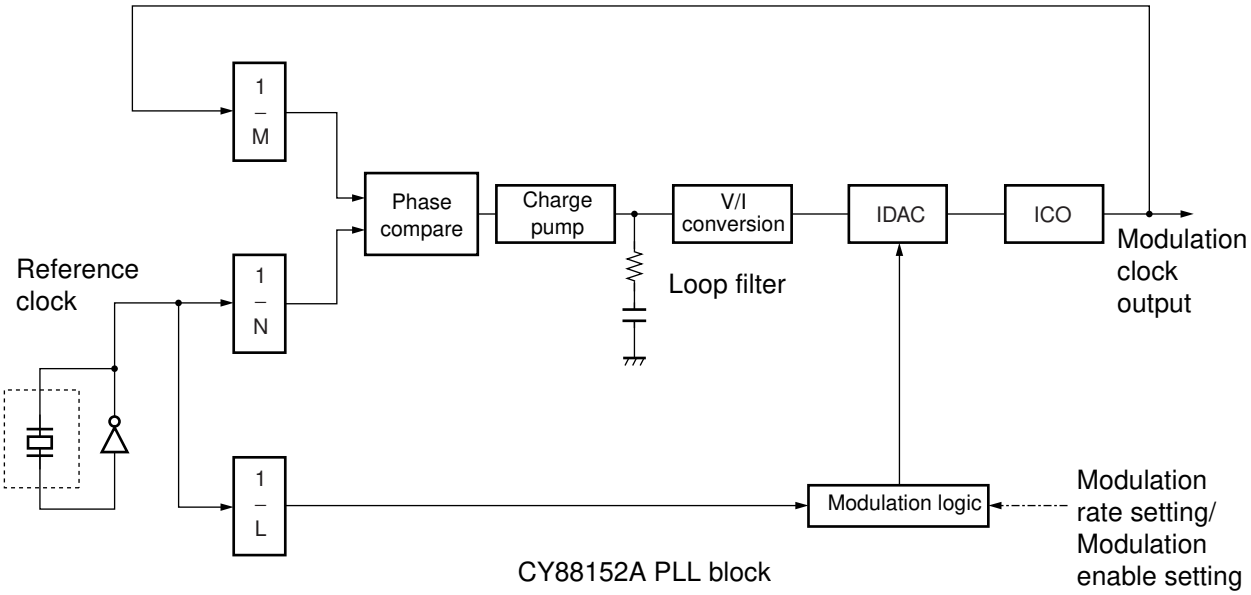
- Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.
- We recommend connecting electrolytic capacitor (about 10 µF) and the ceramic capacitor (about 0.01 µF) in parallel between V_{SS} and V_{DD} pins near the device, as a bypass capacitor.

Oscillation Circuit

- Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and resonator (or ceramic oscillator) do not intersect other wiring.
- Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

6. Block Diagram





CY88152A PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

7. Pin Setting

When changing the pin setting, the stabilization wait time for the modulation clock is required. The stabilization wait time for the modulation clock takes the maximum value of Lock-Up time in “AC Characteristics of Electrical Characteristics”.

7.1 Modulation Enable Setting

XENS	Modulation	
L	Modulation	CY88152A-101, CY88152A-111, CY88152A-112
H	No modulation	

Note: CY88152A-100 and CY88152A-110 do not have XENS pin.

7.2 SEL Modulation Rate Setting

SEL	Modulation Rate		Remarks
L	±0.5%	CY88152A-111, CY88152A-112	Center spread
	−1.0%	CY88152A-100, CY88152A-101	Down spread
H	±1.5%	CY88152A-111, CY88152A-112	Center spread
	−3.0%	CY88152A-100, CY88152A-101	Down spread

Note: The modulation rate can be changed at the level of the terminal.

7.3 Frequency Setting

FREQ	Frequency	
L	16.6 MHz to 40 MHz	CY88152A-101, CY88152A-111
	40 MHz to 80 MHz	CY88152A-112
H	33 MHz to 67 MHz	CY88152A-101, CY88152A-111
	66 MHz to 134 MHz	CY88152A-112

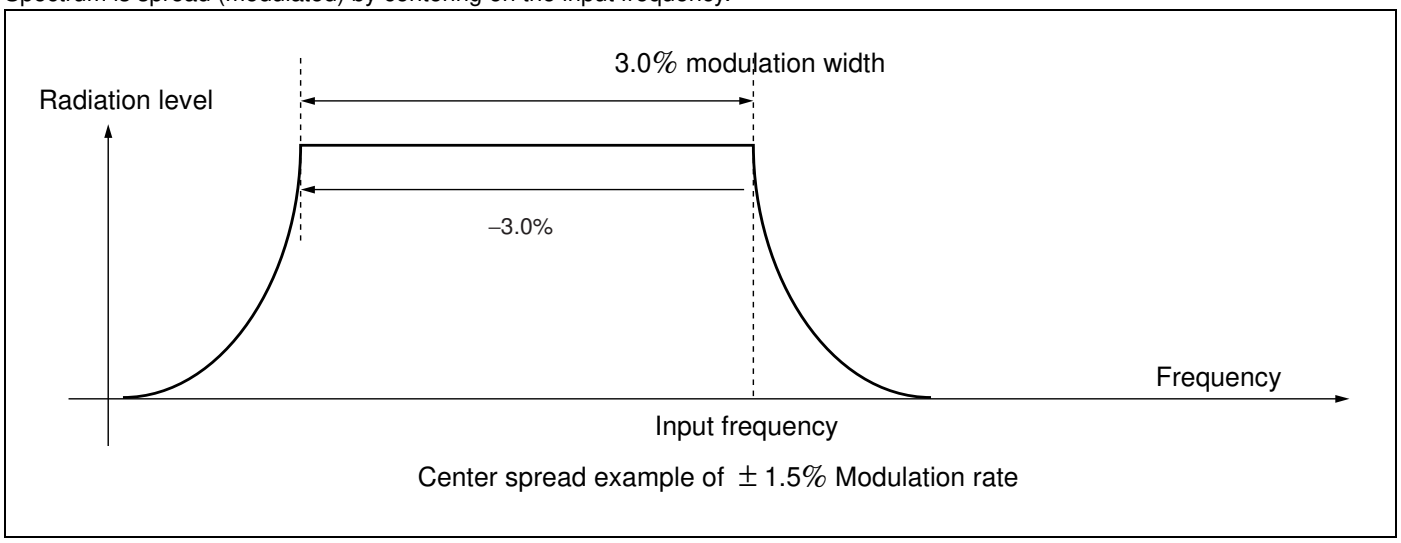
Note: CY88152A-100 and CY88152A-110 do not have FREQ pin.

FREQ1	FREQ0	Frequency	
L	L	16.6 MHz to 40 MHz	CY88152A-100
L	H	33 MHz to 67 MHz	
H	L	40 MHz to 80 MHz	
H	H	66 MHz to 134 MHz	

Note: CY88152A-101, CY88152A-111 and CY88152A-112 have neither FREQ0 pin nor FREQ1 pin.

7.3.1 Center Spread

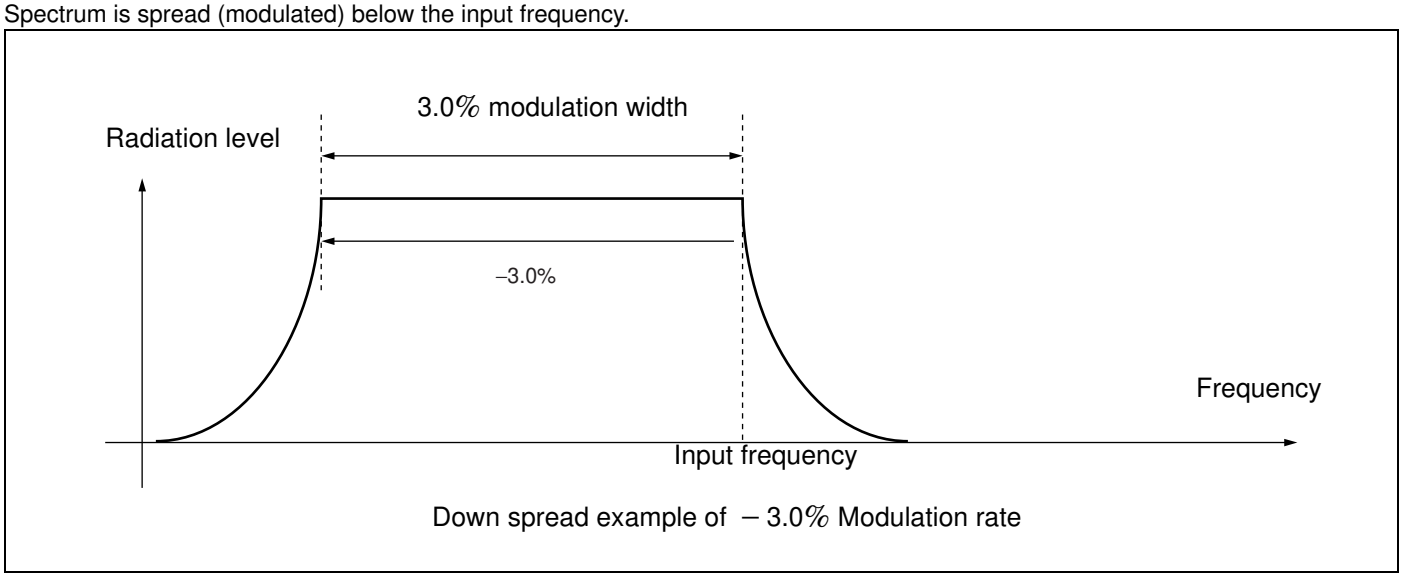
Spectrum is spread (modulated) by centering on the input frequency.



Center spread example of ± 1.5% Modulation rate

7.3.2 Down Spread

Spectrum is spread (modulated) below the input frequency.



Down spread example of – 3.0% Modulation rate

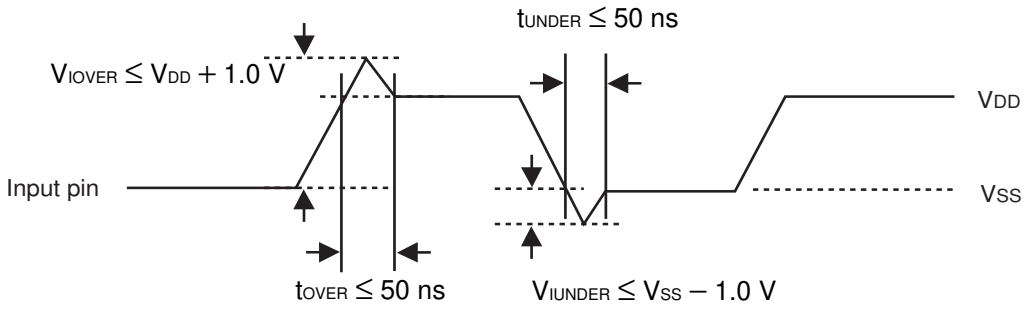
8. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage[a]	V_{DD}	− 0.5	+ 4.0	V
Input voltage[a]	V_I	V_{SS} − 0.5	V_{DD} + 0.5	V
Output voltage[a]	V_O	V_{SS} − 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	− 55	+ 125	°C
Operation junction temperature	T_J	− 40	+ 125	°C
Output current	I_O	− 14	+ 14	mA
Overshoot	V_{IOVER}	–	V_{DD} + 1.0 ($t_{OVER} \leq$ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} − 1.0 ($t_{UNDER} \leq$ 50 ns)	–	V

a. The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



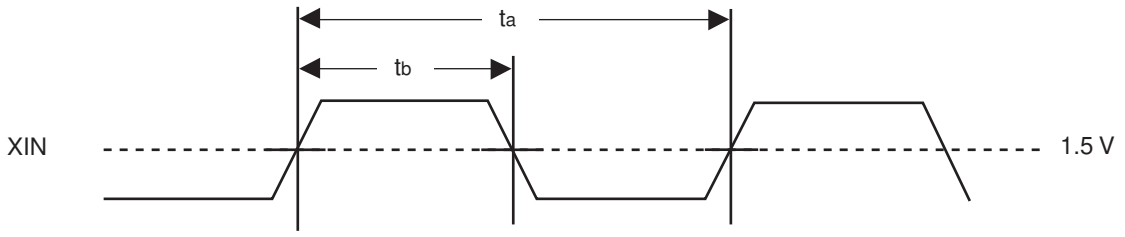
9. Recommended Operating Conditions

(V_{SS} = 0.0 V)

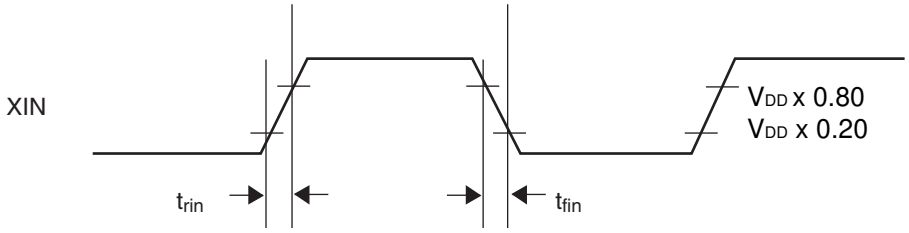
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	–	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	SEL, FREQ/FREQ0, XENS/FREQ1	–	V_{DD} x 0.8	–	V_{DD} + 0.3	V
		XIN	16.6 MHz to 100 MHz	V_{DD} x 0.8	–	V_{DD} + 0.3	V
			100 MHz to 134 MHz	V_{DD} x 0.9	–	V_{DD} + 0.3	V
"L" level input voltage	V_{IL}	SEL, FREQ/FREQ0, XENS/FREQ1	–	V_{SS}	–	V_{DD} x 0.2	V
		XIN	16.6 MHz to 100 MHz	V_{SS}	–	V_{DD} x 0.2	V
			100 MHz to 134 MHz	V_{SS}	–	V_{DD} x 0.1	V
Input clock duty cycle	t_{DCI}	XIN	16.6 MHz to 100 MHz	40	50	60	%
			100 MHz to 134 MHz	45	50	55	
Input clock slew rate	SR_{IN}	XIN	Input frequency 40 MHz to 100 MHz	0.0475 x fin – 1.75	–	–	V/ns
			Input frequency 100 MHz to 134 MHz	3	–	–	
Operating temperature	Ta	–	–	–40	–	+ 85	·C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



Input clock slew rate (SR_{IN})



Note: $SR_{IN} = (V_{DD} \times 0.80 - V_{DD} \times 0.20) / t_{rin}$, $SR_{IN} = (V_{DD} \times 0.80 - V_{DD} \times 0.20) / t_{fin}$

10. Electrical Characteristics

10.1 DC Characteristics

(Ta = −40°C to + 85°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

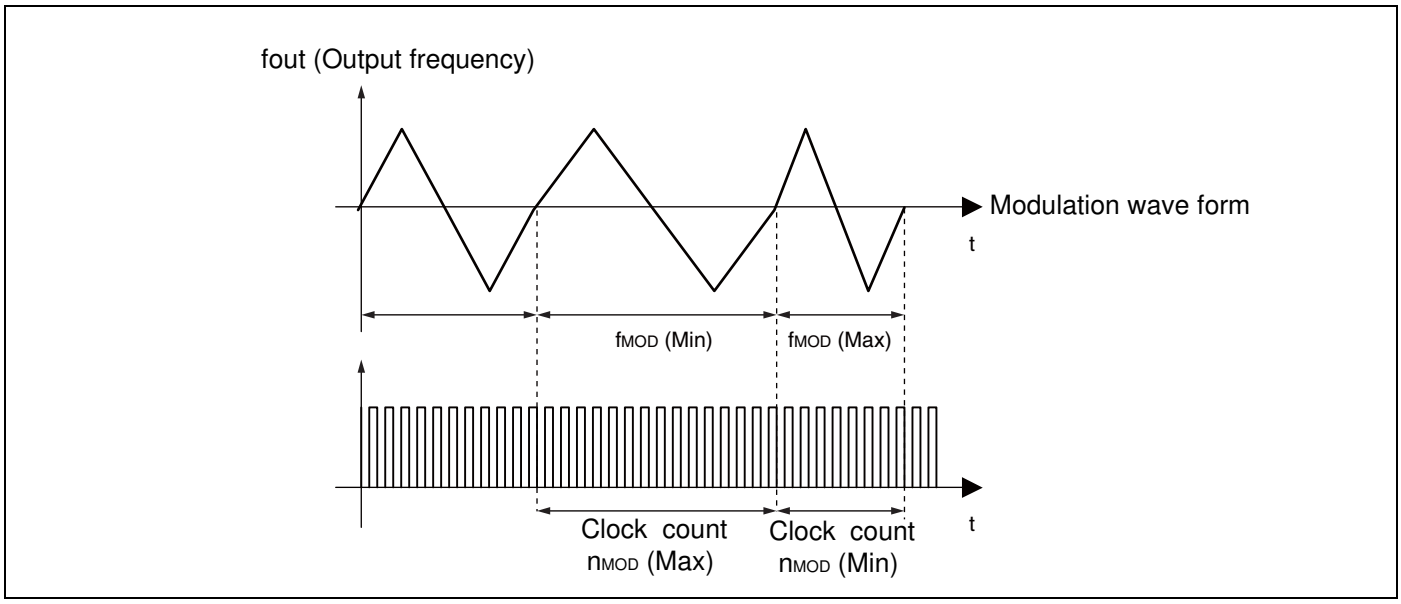
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	V_{DD}	24 MHz output No load capacitance	–	5.0	7.0	mA
Output voltage	V_{OH}	CKOUT	“H” level output I_{OH} = − 4 mA	V_{DD} − 0.5	–	V_{DD}	V
	V_{OL}		“L” level output I_{OL} = 4 mA	V_{SS}	–	0.4	V
Output impedance	Z_O	CKOUT	16.6 MHz to 134 MHz	–	45	–	Ω
Input capacitance	C_{IN}	XIN, SEL, FREQ/ FREQ0, XENS/ FREQ1	Ta = + 25 °C V_{DD} = V_I = 0.0 V f = 1 MHz	–	–	16	pF
Load capacitance	C_L	CKOUT	16.6 MHz to 67 MHz	–	–	15	pF
			67 MHz to 100 MHz	–	–	10	
			100 MHz to 134 MHz	–	–	7	

10.2 AC Characteristics

(Ta = −40°C to + 85°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation	16.6	–	40	MHz
			3rd over tone	40	–	48	
Input frequency	f_{in}	XIN	CY88152A-100	16.6	–	134	MHz
			CY88152A-101/111	16.6	–	67	
			CY88152A-112	40	–	134	
Output frequency	f_{OUT}	CKOUT	CY88152A-100	16.6	–	134	MHz
			CY88152A-101/111	16.6	–	67	
			CY88152A-112	40	–	134	
Output slew rate	SR	CKOUT	0.4 V to 2.4 V Load capacitance 15 pF	0.4	–	4.0	V/ns
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V	40	–	60	%
Modulation frequency (Number of input clocks per modulation)	f_{MOD} (n_{MOD})	CKOUT	CY88152A-100 FREQ[1 : 0] = (00)	fin/2640 (2640)	fin/2280 (2280)	fin/1920 (1920)	kHz (clks)
			CY88152A-100 FREQ[1 : 0] = (01)	fin/4400 (4400)	fin/3800 (3800)	fin/3200 (3200)	
			CY88152A-100 FREQ[1 : 0] = (10)	fin/5280 (5280)	fin/4560 (4560)	fin/3840 (3840)	
			CY88152A-100 FREQ[1 : 0] = (11)	fin/8800 (8800)	fin/7600 (7600)	fin/6400 (6400)	
			CY88152A-101/111 FREQ = 0	fin/2640 (2640)	fin/2280 (2280)	fin/1920 (1920)	
			CY88152A-101/111 FREQ = 1	fin/4400 (4400)	fin/3800 (3800)	fin/3200 (3200)	
			CY88152A-112 FREQ = 0	fin/5280 (5280)	fin/4560 (4560)	fin/3840 (3840)	
			CY88152A-112 FREQ = 1	fin/8800 (8800)	fin/7600 (7600)	fin/6400 (6400)	
Lock-Up time	t_{LK}	CKOUT	16.6 MHz to 80 MHz	–	2	5	ms
			80 MHz to 134 MHz	–	3	8	
Cycle-cycle jitter	t_{JC}	CKOUT	No load capacitance, Ta = + 25 °C, V_{DD} = 3.3 V	–	–	100	ps-rms

<Definition of modulation frequency and number of input clocks per modulation>

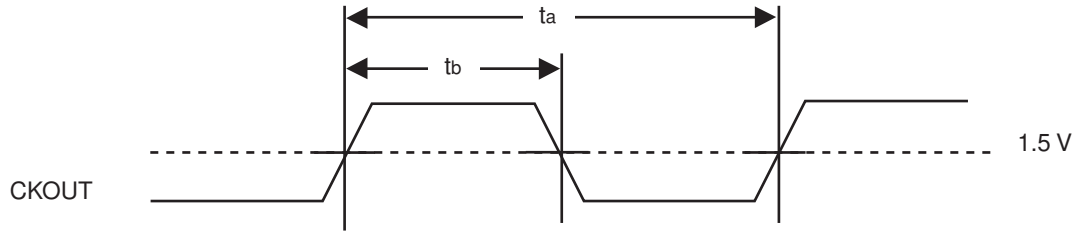


■ CY88152A contains the modulation period to realize the efficient EMI reduction.

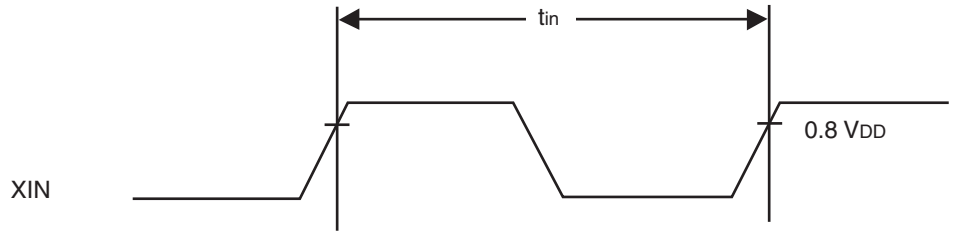
■ The modulation period f_{MOD} depends on the input frequency and changes between f_{MOD} (Min) and f_{MOD} (Max) .

■ Furthermore, the average value of f_{MOD} equals the typical value of the electrical characteristics.

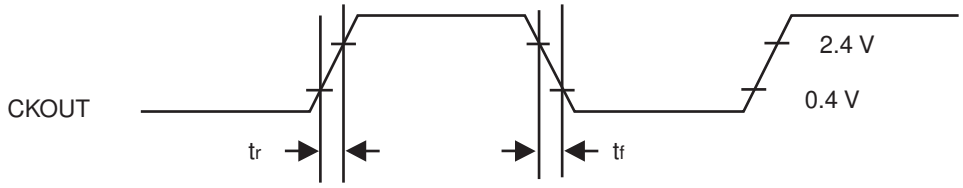
11. Output Clock Duty Cycle ($t_{DCC} = t_b/t_a$)



12. Input Frequency ($f_{in} = 1/t_{in}$)

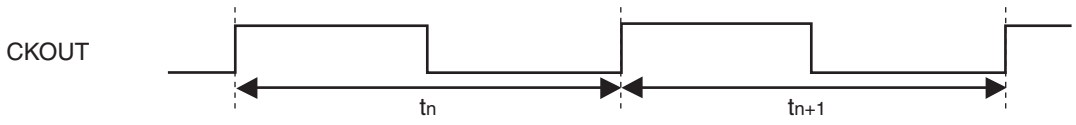


13. Output Slew Rate (SR)



Note: SR = (2.4–0.4) /t_r, SR = (2.4–0.4) /t_f

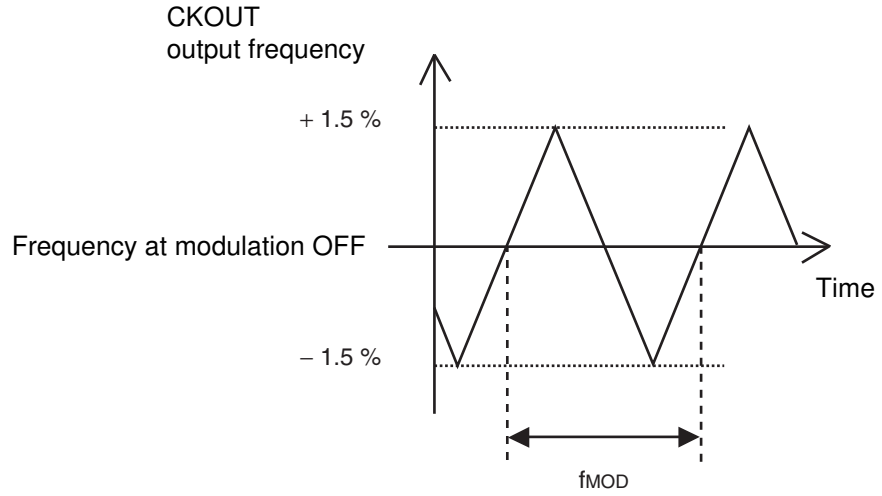
14. Cycle-cycle Jitter ($t_{JC} = | t_n - t_{n+1} |$)



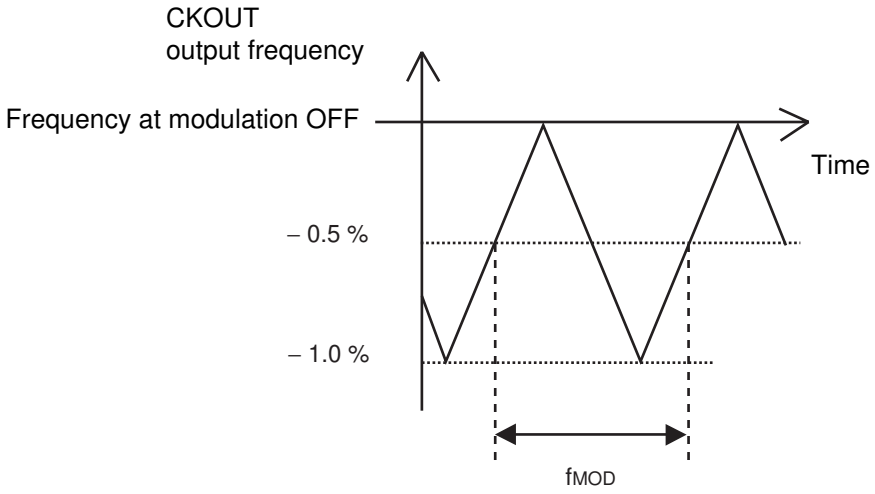
Note: Cycle-cycle jitter is defined the difference between a certain cycle and immediately after (or, immediately before) .

15. Modulation Waveform

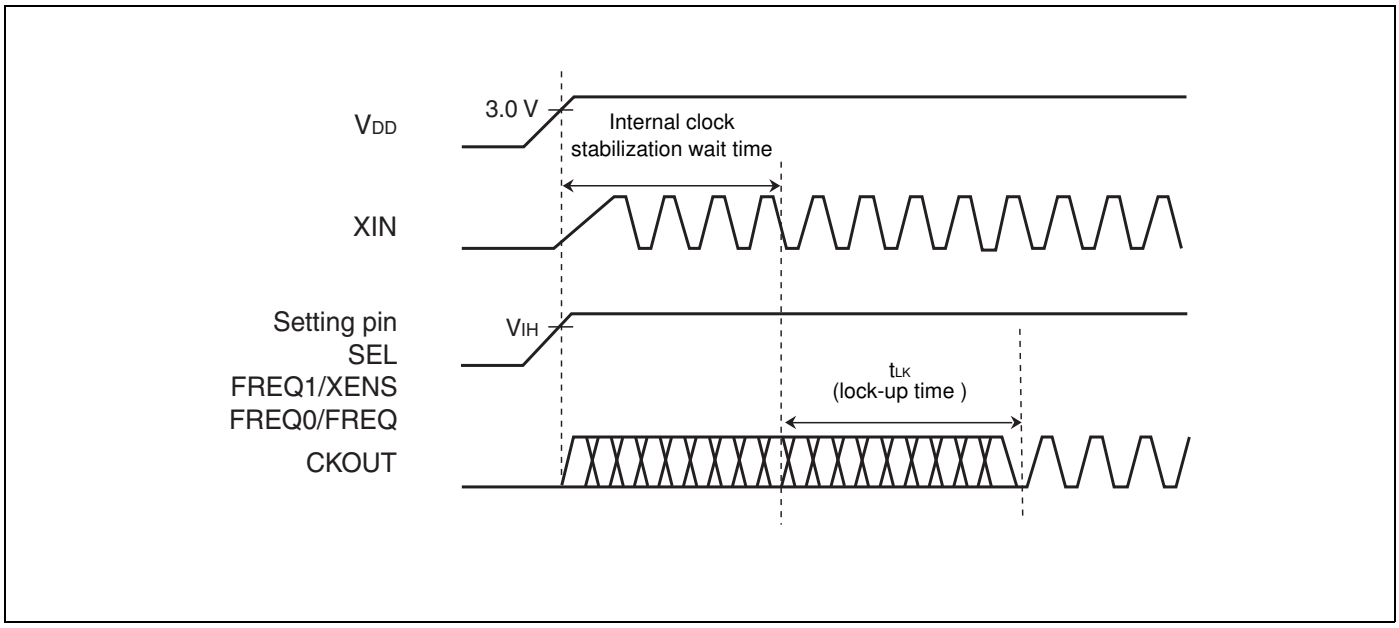
±1.5% modulation rate, Example of center spread



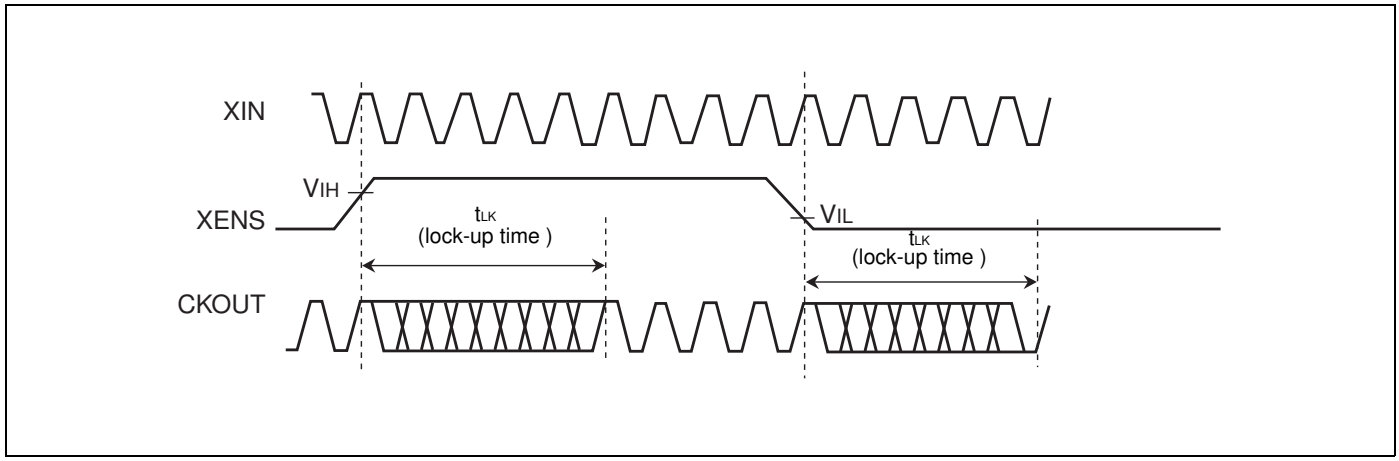
–1.0% modulation rate, Example of down spread



16. Lock-up Time



If the setting pin is fixed at the “H” or “L” level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) + (the lock-up time “t_{LK}”). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.



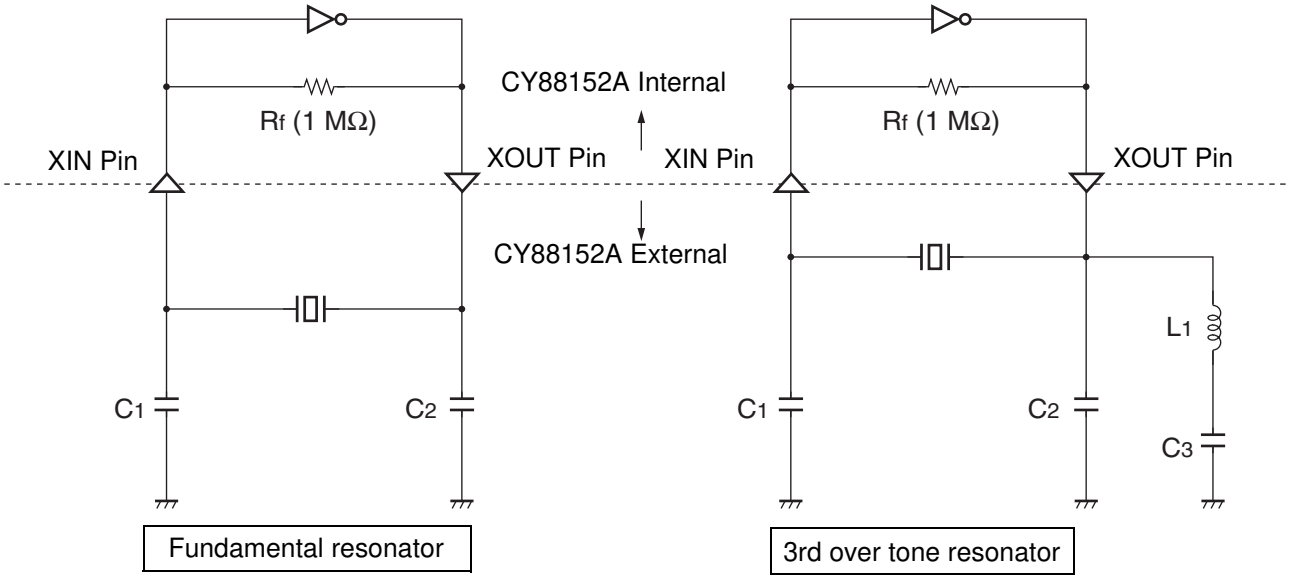
For modulation enable control using the XENS pin during normal operation, the set clock signal is output from CKOUT pin at most the lock-up time (t_{LK}) after the level at the XENS pin is determined.

Note: When the pin setting is changed, the CKOUT pin output clock stabilization time is required. Until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.

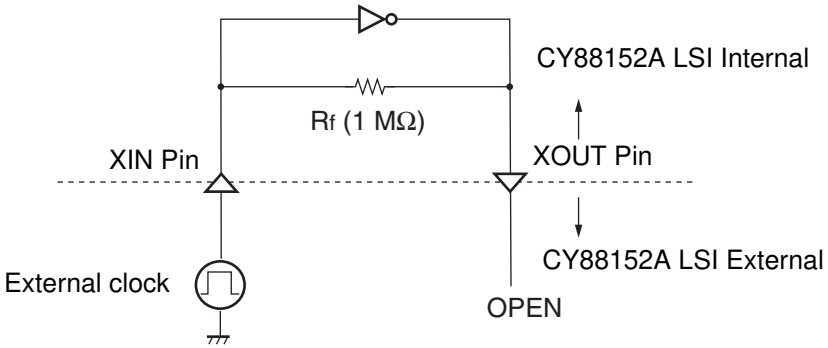
17. Oscillation Circuit

The left side of figures below shows the connection example about general resonator. The oscillation circuit has the built-in feedback resistance (R_f). The value of capacity (C_1 and C_2) is required adjusting to the most suitable value of an individual resonator.
The right side of figures below shows the example of connecting for the 3rd over-tone resonator. The value of capacity (C_1, C_2 and C_3) and inductance (L_1) is needed adjusting to the most suitable value of an individual resonator. The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which you use for the most suitable value. When an external clock is used (the resonator is not used), input the clock to XIN pin and do not connect anything with XOUT pin.

When using the resonator

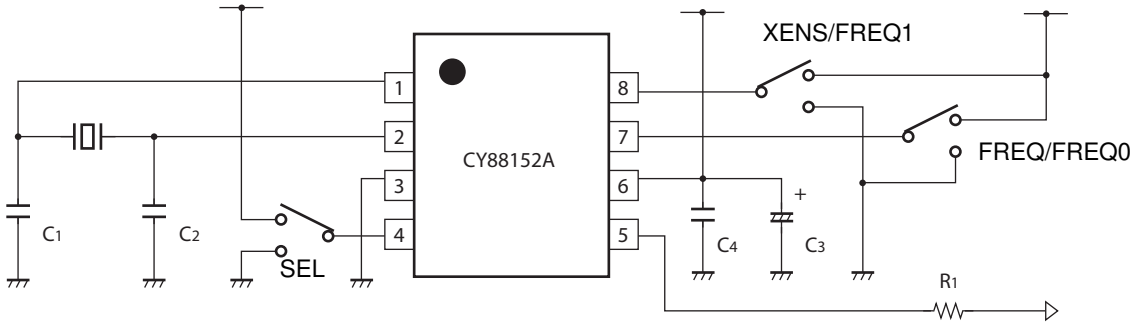


When using an external clock



Note: A jitter characteristic of an input clock may cause an affect to a cycle-cycle jitter characteristic.

18. Interconnection Circuit Example



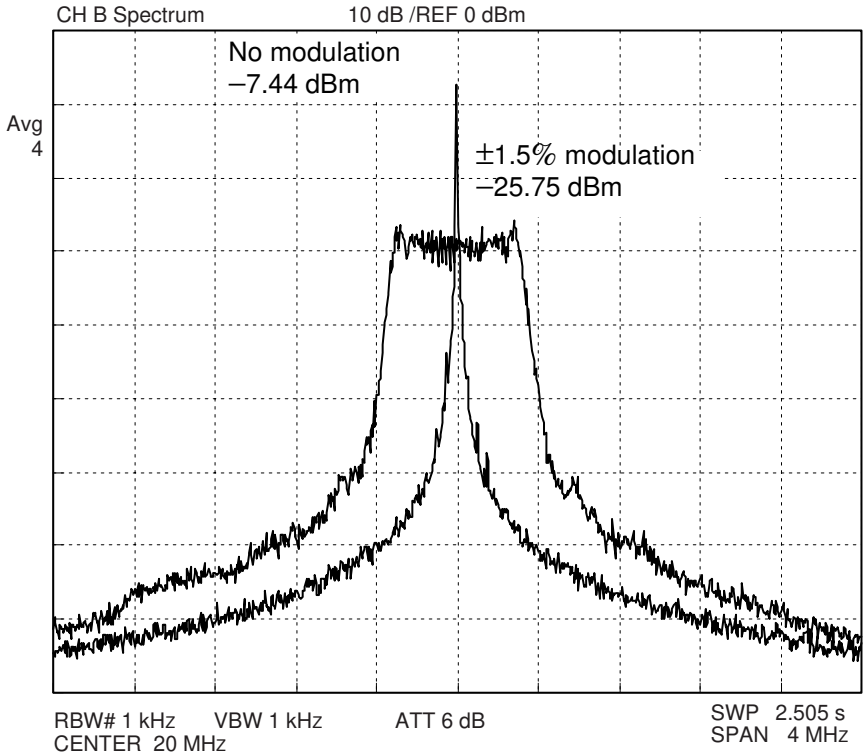
C_1, C_2 : Oscillation stabilization capacitance (refer to "Oscillation Circuit".)
C_3 : Capacitor of 10 µF or higher
C_4 : Capacitor about 0.01 µF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device.)
R_1 : Impedance matching resistor for board pattern

19. Example Characteristics

The condition of the examples of the characteristics is shown as follows : Input frequency = 20 MHz (Output frequency = 20 MHz : Use for CY88152A-111)

Power-supply voltage = 3.3 V, None load capacity, Modulation rate = ±1.5% (center spread) .

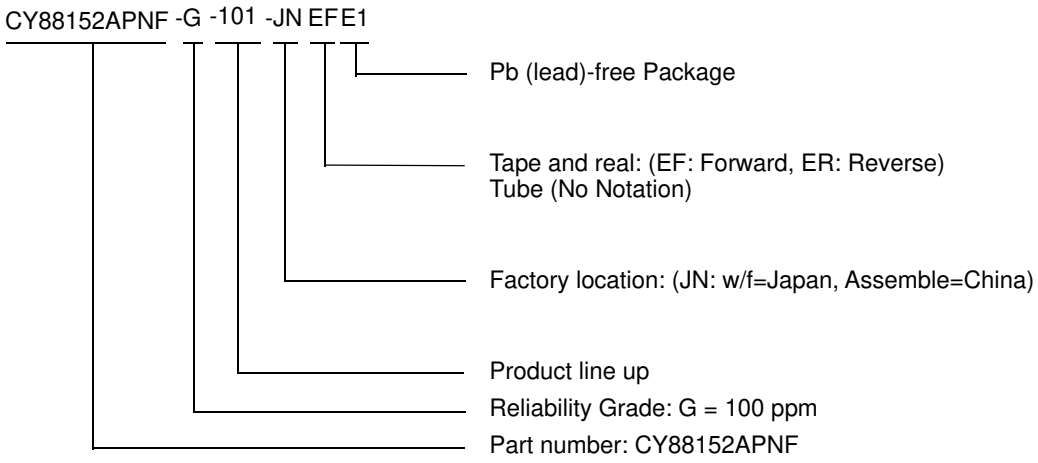
Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with, RBW = 1 kHz (ATT use for −6 dB) .



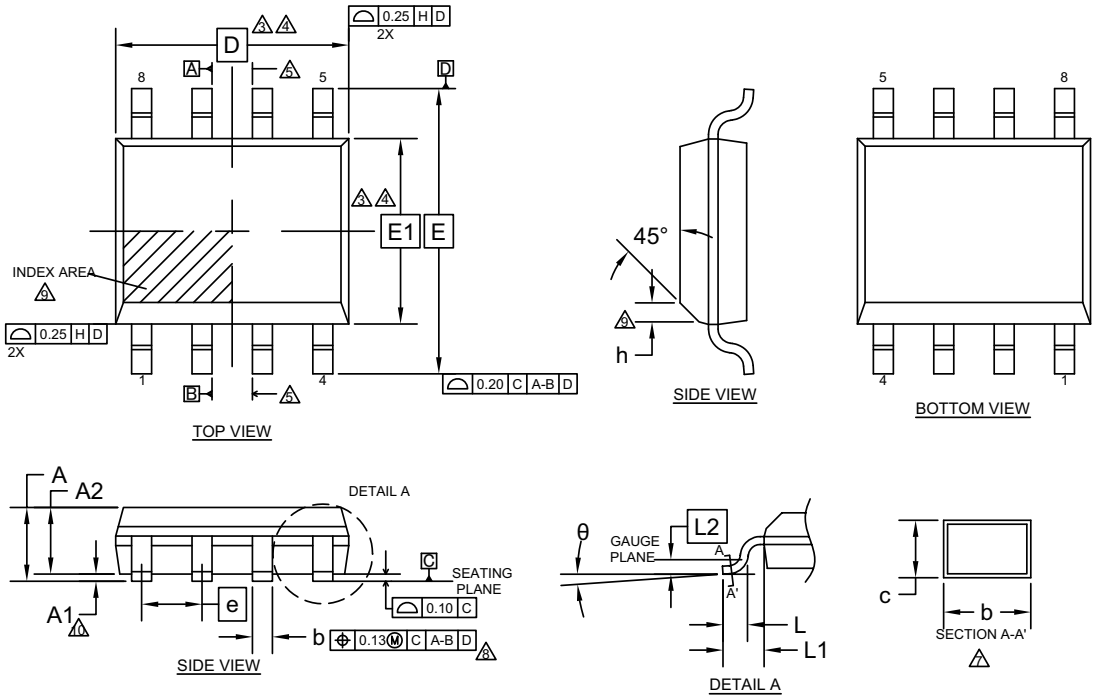
20. Ordering Information

Part Number	Input/Output Frequency	Modulation Type	Modulation Enable pin	Package	Remarks
CY88152APNF-G-100-JNE1	16.6 MHz to 134 MHz	Down spread	No	8-pin plastic SOP (SOB008)	
CY88152APNF-G-101-JNE1	16.6 MHz to 67 MHz	Down spread	Yes		
CY88152APNF-G-111-JNE1	16.6 MHz to 67 MHz	Center spread	Yes		
CY88152APNF-G-112-JNE1	40 MHz to 134 MHz	Center spread	Yes		
CY88152APNF-G-100-JNEFE1	16.6 MHz to 134 MHz	Down spread	No	8-pin plastic SOP (SOB008)	Emboss taping (EF type)
CY88152APNF-G-101-JNEFE1	16.6 MHz to 67 MHz	Down spread	Yes		
CY88152APNF-G-111-JNEFE1	16.6 MHz to 67 MHz	Center spread	Yes		
CY88152APNF-G-112-JNEFE1	40 MHz to 134 MHz	Center spread	Yes		
CY88152APNF-G-100-JNERE1	16.6 MHz to 134 MHz	Down spread	No	8-pin plastic SOP (SOB008)	Emboss taping (ER type)
CY88152APNF-G-101-JNERE1	16.6 MHz to 67 MHz	Down spread	Yes		
CY88152APNF-G-111-JNERE1	16.6 MHz to 67 MHz	Center spread	Yes		
CY88152APNF-G-112-JNERE1	40 MHz to 134 MHz	Center spread	Yes		

Ordering Code Definitions



21. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.75
A1	0.05	——	0.25
A2	1.30	1.40	1.50
D	5.05 BSC.		
E	6.00 BSC.		
E1	3.90 BSC		
θ	0°	——	8°
c	0.15	——	0.25
b	0.36	0.44	0.52
L	0.45	0.60	0.75
L 1	1.05 REF		
L 2	0.25 BSC		
e	1.27 BSC.		
h	0.40 BSC.		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15856 Rev.**

Document History

Document Title: CY88152A Spread Spectrum Clock Generator Document Number: 002-08308				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	TAOA	06/29/2009	Initial release.
*A	5560671	TAOA	12/28/2016	Migrated Spansion datasheet “DS04-29125-3E” into Cypress Template.
*B	6003426	TAOA	12/25/2017	Deleated EOL part number: MB88152A-102/110 Updated Package Dimensions: Updated to Cypress format Changed the package name from FPT-8P-M02 to SOB008
*C	6268353	ATTS	07/31/2018	Updated part number: MB88152A to CY88152A Added Ordering Code Definitions

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