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FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13502-5E

16-bit Proprietary Microcontroller

CMOS

F²MC-16F MB90220 Series

MB90223/224/P224A/W224A
MB90P224B/W224B/V220

■ OUTLINE

The MB90220 series of general-purpose high-performance 16-bit microcontrollers has been developed primarily for applications that demand high-speed real-time processing and is suited for industrial applications, office automation equipment, process control, and other applications. The F²MC-16F CPU is based on the F²MC*-16 Family with improved high-level language support functions and task switching functions, as well as additional addressing modes.

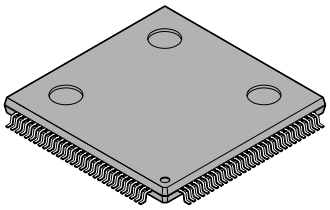
On-chip peripheral resources include a 4-channel PWC timer, a 4-channel ICU (Input Capture Unit), a 1-channel 24-bit timer counter, an 8-channel OCU (Output Compare Unit), a 6-channel 16-bit reload timer, a 2-channel 16-bit PPG timer, a 10-bit A/D converter with 16 inputs, and a 4-channel serial port with a UART function (one channel includes the CTS function).

The MB90P224B, MB90W224B, MB90224 is under development.

*: F²MC stands for FUJITSU Flexible Microcontroller.

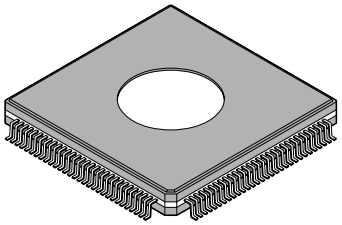
■ PACKAGE

120-pin Plastic QFP



(FPT-120P-M03)

120-pin Ceramic QFP



(FPT-120C-C02)

■ FEATURES

F²MC-16F CPU

- Minimum execution time: 62.5 ns/16 MHz oscillation (using a duty control system)
- Instruction sets optimized for controllers
  Upward object-compatible with the F²MC-16(H)
  Various data types (bit, byte, word, and long-word)
  Instruction cycle improved to speed up operation
  Extended addressing modes: 25 types
  High coding efficiency
  Access method (bank access with linear pointer)
  Enhanced multiplication and division instructions (with signed instructions added)
  Higher-precision operation using a 32-bit accumulator
- Extended intelligent I/O service (automatic transfer function independent of instructions)
  Access area expanded to 64 Kbytes
- Enhanced instruction set applicable to high-level language (C) and multitasking
  System stack pointer
  Enhanced pointer-indirect instructions
  Barrel shift instruction
  Stack check function
- Increased execution speed: 8-byte instruction queue
- Powerful interrupt functions: 8 levels and 28 sources

Peripheral resources

- Mask ROM : 64 Kbytes (MB90223)
  96 Kbytes (MB90224)
  EPROM : 96 Kbytes (MB90W224A/W224B)
- One-time PROM : 96 Kbytes (MB90P224A/P224B)
- RAM: 3 Kbytes (MB90223)
  4.5 Kbytes (MB90224/MB90W224A/P224A/W224B/P224B)
  5 Kbytes (MB90V220)
- General-purpose ports: max. 102 channels
- ICU (Input Capture Unit): 4 channels
- 24-bit timer counter: 1 channel
- OCU (Output Compare Unit): 8 channels
- PWC timer with time measurement function: 4 channels
- 10-bit A/D converter: 16 channels
- UART: 4 channels (one channel includes CTS function)
- 16-bit reload timer
  Toggled output, external clock, and gate functions: 6 channels
- 16-bit PPG timer: 2 channels
- DTP/External-interrupt inputs: 8 channels (of which five have edge detection function only)
- Write-inhibit RAM: 0.5 Kbytes (1 Kbyte for MB90V220)
- Timebase counter: 18 bits
- Clock gear function
- Low-power consumption mode
  Sleep mode
  Stop mode
  Hardware standby mode

Product description

- MB90223/224 are mask ROM product.
- MB90P224A/P224B are one-time PROM products.
- MB90W224A/W224B are EPROM products. ES only.
- Operating temperature of MB90P224A/W224A is –40°C to +85°C.
  (However, the AC characteristics is assured in –40°C to +70°C)
- Operation clock cycle of MB90223 is 10 MHz to 12 MHz.
- MB90V220 is a evaluation device for the program development. ES only.

■ PRODUCT LINEUP

Part number / Item	MB90223	MB90224	MB90P224A MB90P224B	MB90W224A MB90W224B	MB90V220
Classification	Mask ROM product	Mask ROM product	One-time PROM product	EPROM product	Evaluation device
ROM size	64 Kbytes	96 Kbytes	96 Kbytes	96 Kbytes	None
RAM size	3 Kbytes	4.5 Kbytes	4.5 Kbytes	4.5 Kbytes	5 Kbytes
CPU functions	The number of instructions: 412 Instruction bit length: 8 or 16 bits Instruction length: 1 to 7 bytes Data bit length: 1, 4, 8, 16, or 32 bits Minimum execution time: 62.5 ns/16 MHz Interrupt processing time: 1.0 µs/16 MHz (min.)				
Ports	I/O ports (N-ch open-drain): 16 I/O ports (CMOS): 86 Total: 102				
ICU (Input Capture Unit)	Number of channels: 4 Rising edge/falling edge/both edges selectable				
24-bit timer counter	Number of channels: 1 Overflow interrupt, intermediate bit interrupt				
OCU (Output Compare Unit)	Number of channels: 8 Pin change source (match signal causes register value transfer/general-purpose port)				
PWC timer	Number of channels: 4 16-bit reload timer operation (operation clock cycle: 0.25 µs to 1.31 ms) 16-bit pulse-width count operation (Allowing continuous/one-shot measurement, H/L width measurement, inter-edge measurement, and divided-frequency measurement)				
10-bit A/D converter	Resolution: 10 bits Number of inputs: 16 Single conversion mode (conversion of each channel) Scan conversion mode (continuous conversion for up to 16 consecutive channels) Continuous conversion mode (repeated conversion of specified channel) Stop conversion mode (conversion every fixed cycle)				
UART	Number of channels: 4 (1 channel with CTS function) Clock-synchronous transfer mode (full-duplex double buffering, 7 to 9-bit data length, 2400 to 62500 bps) Asynchronous transfer mode (full-duplex double buffering, 7 to 9-bit data length, 2400 to 62500 bps)				
16-bit reload timer	Number of channels: 6 16-bit reload timer operation (operation clock cycle: 0.25 µs to 1.05 s)				

(Continued)

(Continued)

Item \ Part number	MB90223	MB90224	MB90P224A MB90P224B	MB90W224A MB90W224B	MB90V220
16-bit PPG timer	Number of channels: 2 16-bit PPG operation (operation clock cycle: 0.25 μs to 6 s)				
DTP/External interrupts	Number of inputs: 8 (of which five have edge detection function only) External interrupt mode (allowing interrupts to activate at four different request levels) Simple DMA transfer mode (allowing extended I^2OS to activate at two different request levels)				
Write-inhibited RAM	RAM size: 512 bytes (1 Kbyte for MB90V220) RAM write-protectable with $\overline{WI}$ pin				
Standby mode	stop mode (activated by software or hardware) and sleep mode				
Gear function	Machine clock operation frequency switching: 16 MHz, 8 MHz, 4 MHz, 1 MHz (at 16-MHz oscillation)				
Package	FPT-120P-M03			FPT-120C-C02	PGA-256C-A02

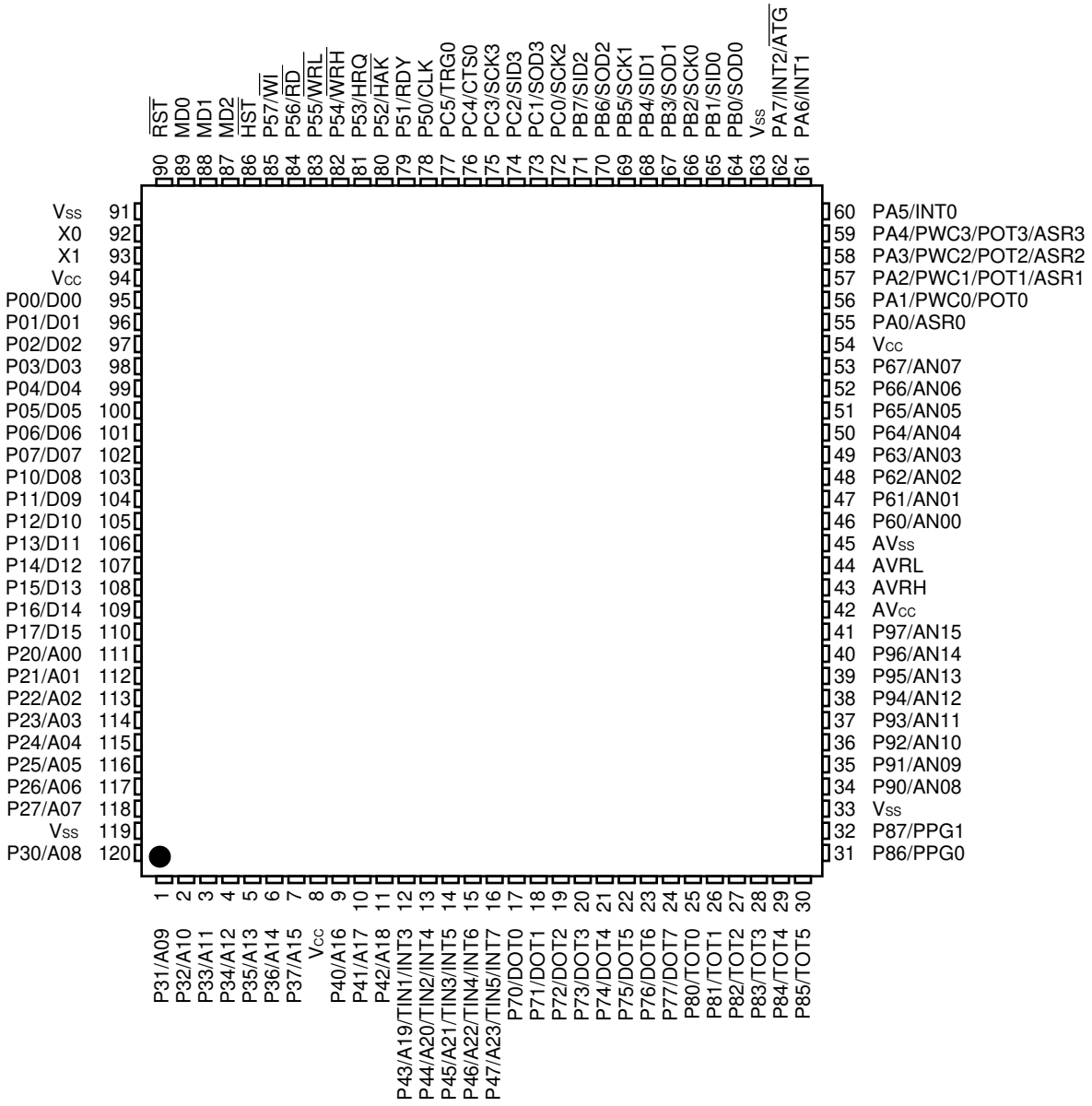
Note: MB90V220 is a evaluation device, therefore, the electrical characteristics are not assured.

■ DIFFERENCES BETWEEN MB90223/224 (MASK ROM PRODUCT) AND MB90P224A/W224A/P224B/W224B

Item \ Part number	MB90223	MB90224	MB90P224A MB90P224B	MB90W224A MB90W224B
ROM	Mask ROM 64 Kbytes	Mask ROM 96 Kbytes	OTPROM 96 Kbytes	EPROM 96 Kbytes
Pin functions: pin 87	MD2 pin		MD2/V_{PP} pin	

■ PIN ASSIGNMENT

(Top view)



(FPT-120P-M03)
(FPT-120C-C02)

■ PIN DESCRIPTION

Pin no. QFP*	Pin name	Circuit type	Function
92, 93	X0, X1	A	Crystal oscillation pins (16 MHz)
89 to 87	MD0 to MD2	D	Operation mode specification input pins Connect directly to V_{CC} or V_{SS}.
90	$\overline{RST}$	G	External reset request input
86	$\overline{HST}$	E	Hardware standby input pin
95 to 102	P00 to P07	C	General-purpose I/O ports This function is valid only in single-chip mode.
	D00 to D07		Output pins for low-order 8 bits of the external address bus. This function is valid only in modes where the external bus is enabled.
103 to 110	P10 to P17	C	General-purpose I/O ports This function is valid only in single-chip mode or when the external bus is enabled and the 8-bit data bus specification has been made.
	D08 to D15		I/O pins for higher-order 8 bits of the external data bus This function is valid only when the external bus is enabled and the 16-bit bus specification has been made.
111 to 118	P20 to P27	C	General-purpose I/O ports This function is valid only in single-chip mode.
	A00 to A07		Output pins for lower-order 8 bits of the external address bus This function is valid only in modes where the external bus is enabled.
120, 1 to 7	P30, P31 to P37	C	General-purpose I/O ports This function is valid either in single-chip mode or when the address mid-order control register specification is “port”.
	A08, A09 to A15		Output pins for mid-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address mid-order control register specification is “address”.
9 to 11	P40 to P42	C	General-purpose I/O ports This function is valid either in single-chip mode or when the address high-order control register specification is “port”.
	A16 to A18		Output pins for higher-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address high-order control register specification is “address”.
12 to 16	P43 to P47	C	General-purpose I/O ports This function is valid when either single-chip mode is enabled or the address higher-order control register specification is “port”.
	A19 to A23		Output pins for higher-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address higher-order control register specification is “address”.
	TIN1 to TIN5		16-bit reload timer input pins This function is valid when the timer input specification is “enabled”. The data on the pins is read as timer input (TIN1 to TIN5).

* : FPT-120P-M03, FPT-120C-C02

(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
12 to 16	INT3 to INT7	C	External interrupt request input pins When external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately.
78	P50	C	General-purpose I/O port This function is valid in single-chip mode and when the CLK output specification is disabled.
	CLK		CLK output pin This function is valid in modes where the external bus is enabled and the CLK output specification is enabled.
79	P51	C	General-purpose I/O port This function is valid in single-chip mode or when the ready function is disabled.
	RDY		Ready input pin This function is valid in modes where the external bus is enabled and the ready function is enabled.
80	P52	C	General-purpose I/O port This function is valid in single-chip mode or when the hold function is disabled.
	$\overline{\text{HAK}}$		Hold acknowledge output pin This function is valid in modes where the external bus is enabled and the hold function is enabled.
81	P53	C	General-purpose I/O port This function is valid in single-chip mode or external bus mode and when the hold function is disabled.
	HRQ		Hold request input pin This function is valid in modes where the external bus is enabled and the hold function is enabled. During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other fuctions on this pin, except when using it for output deliberately.
82	P54	C	General-purpose I/O port This function is valid in single-chip mode, when the external bus is in 8-bit mode, or when $\overline{\text{WRH}}$ pin output is disabled.
	$\overline{\text{WRH}}$		Write strobe output pin for the high-order 8 bits of the data bus This function is valid in modes where the external bus is enabled, the external bus is in 16-bit mode, and $\overline{\text{WRH}}$ pin output is enabled.
83	P55	C	General-purpose I/O port This function is valid in single-chip mode or when $\overline{\text{WRL}}$ pin output is disabled.
	$\overline{\text{WRL}}$		Write strobe output pin for the low-order 8 bits of the data bus This function is valid in modes where the external bus is enabled and $\overline{\text{WRL}}$ pin output is enabled.

* : FPT-120P-M03, FPT-120C-C02

(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
84	P56	C	General-purpose I/O port This function is valid in single-chip mode. This function is valid in modes where the external bus is valid.
	$\overline{RD}$		Read strobe output pin for the data bus This function is valid in modes where the external bus is enabled.
85	P57	B	General-purpose I/O port This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	$\overline{WI}$		RAM write disable request input During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other fuctions on this pin, except when using it for output deliberately.
46 to 53	P60 to P67	F	Open-drain I/O ports This function is valid when the analog input enable register specification is “port”.
	AN00 to AN07		10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is “analog input”.
17 to 24	P70 to P77	C	General-purpose I/O ports This function is valid when the output specification for DOT0 to DOT7 is “disabled”.
	DOT0 to DOT7		This function is valid when OCU (output compare unit) output is enabled.
25 to 30	P80 to P85	C	General-purpose I/O ports This function is valid when the output specification for TOT0 to TOT5 is “disabled”.
	TOT0 to TOT5		16-bit reload timer output pins (TOT0 to TOT5)
31, 32	P86, P87	C	General-purpose I/O ports This function is valid when the PPG0, and PPG1 output specification is “disabled”.
	PPG0, PPG1		16-bit PPG timer output pins This function is valid when the PPG control/status register specification is “PPG output pins”.
34 to 41	P90 to P97	F	Open-drain I/O ports This function is valid when the analog input enable register specification is “port”.
	AN08 to AN15		10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is “analog input”.

* : FPT-120P-M03, FPT-120C-C02

(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
55	PA0	C	General-purpose I/O port This function is always valid.
	ASR0		ICU (input capture unit) input pin This function is valid during ICU (input capture unit) input operations.
56	PA1	C	General-purpose I/O port This function is always valid.
	PWC0		PWC input pin During PWC0 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
	POT0		PWC output pin This function is valid during PWC output operations.
57 to 59	PA2 to PA4	C	General-purpose I/O ports This function is always valid.
	PWC1 to PWC3		PWC input pins This function is valid during PWC input operations. During PWC1 to PWC3 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
	POT1 to POT3		PWC output pins This function is valid during PWC output operations.
	ASR1 to ASR3		ICU (input capture unit) input pins This function is valid during ICU (input capture unit) input operations.
60, 61	PA5, PA6	B	General-purpose I/O ports This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	INT0, INT1		DTP/External interrupt request input pins When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
62	PA7	B	General-purpose I/O port This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.

* : FPT-120P-M03, FPT-120C-C02

(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
62	INT2	B	DTP/External interrupt request input pin When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
	$\overline{ATG}$		10-bit A/D converter external trigger input pin When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.
64	PB0	C	General-purpose I/O port This function is valid when the UART0 (ch.0) serial data output specification is “disabled”.
	SOD0		UART0 (ch.0) serial data output This function is valid when the UART0 (ch.0) serial data output specification is “enabled”.
65	PB1	C	General-purpose I/O port This function is always valid.
	SID0		UART0 (ch.0) serial data input pin During UART0 (ch.0) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
66	PB2	C	General-purpose output port This function is valid when the UART0 (ch.0) clock output specification is “disabled”.
	SCK0		UART0 (ch.0) clock output pin The clock output function is valid when the UART0 (ch.0) clock output specification is “enabled”. UART0 (ch.0) external clock input pin. This function is valid when the port is in input mode and the UART0 (ch.0) specification is external clock mode.
67	PB3	C	General-purpose I/O port This function is valid when the UART0 (ch.1) serial data output specification is “disabled”.
	SOD1		UART0 (ch.1) serial data output pin This function is valid when the UART0 (ch.1) serial data output specification is “enabled”.
68	PB4	C	General-purpose I/O port This function is always valid.
	SID1		UART0 (ch.1) serial data input pin During UART0 (ch.1) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.

* : FPT-120P-M03, FPT-120C-C02

(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
69	PB5	C	General-purpose I/O port This function is valid when the UART0 (ch.1) clock output specification is “disabled”.
	SCK1		UART0 (ch.1) clock output pin The clock output function is valid when the UART0 (ch.1) clock output specification is “enabled”. UART0 (ch.1) external clock input pin This function is valid when the port is in input mode and the UART0 (ch.1) specification is external clock mode.
70	PB6	C	General-purpose I/O port This function is valid when the UART0 (ch.2) serial data output specification is “disabled”.
	SOD2		UART0 (ch.2) serial data output pin This function is valid when the UART0 (ch.2) serial data output specification is “enabled”.
71	PB7	C	General-purpose I/O port This function is always valid.
	SID2		UART0 (ch.2) serial data input pin During UART0 (ch.2) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
72	PC0	C	General-purpose I/O port This function is valid when the UART0 (ch.2) clock output specification is “disabled”.
	SCK2		UART0 (ch.2) clock output pin The clock output function is valid when the UART0 (ch.2) clock output specification is “enabled”. UART0 (ch.2) external clock input pin This function is valid when the port is in input mode and the UART0 (ch.2) specification is external clock mode.
73	PC1	C	General-purpose I/O port This function is valid when the UART1 serial data output specification is “disabled”.
	SOD3		UART1 serial data output pin This function is valid when the UART1 serial data output specification is “enabled”.
74	PC2	C	General-purpose I/O port This function is always valid.
	SID3		UART1 serial data input pin During UART1 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.

* : FPT-120P-M03, FPT-120C-C02

(Continued)

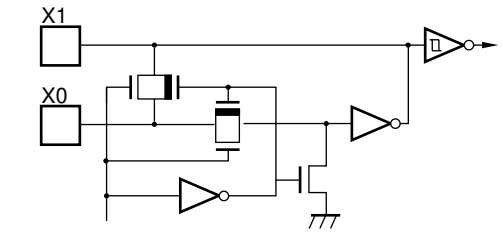
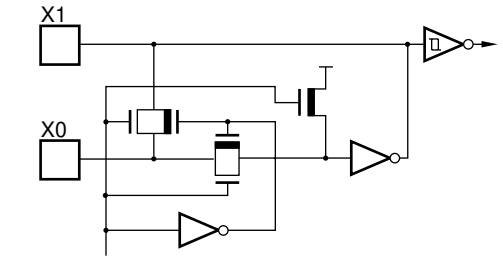
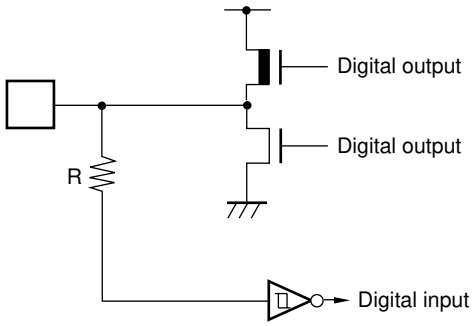
(Continued)

Pin no. QFP*	Pin name	Circuit type	Function
75	PC3	C	General-purpose I/O port This function is valid when the UART1 clock output specification is “disabled”.
	SCK3		UART1 clock output pin The clock output function is valid when the UART1 clock output specification is “enabled”. UART1 external clock input pin This function is valid when the port is in input mode and the UART1 specification is external clock mode.
76	PC4	C	General-purpose I/O port This function is always valid.
	CTS0		UART0 (ch.0) Clear To Send input pin When the UART0 (ch.0) CTS function is enabled, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
77	PC5	C	General-purpose I/O port This function is always valid.
	TRG0		16-bit PPG timer trigger input pin This function is valid when the 16-bit PPG timer trigger input specification is enabled. The data on this pin is read as 16-bit PPG timer trigger input (TRG0). During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately.
8, 54, 94	V_{CC}	Power supply	Power supply for digital circuitry
33, 63, 91, 119	V_{SS}	Power supply	Ground level for digital circuitry
42	AV_{CC}	Power supply	Power supply for analog circuitry When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AV_{CC} to V_{CC}. During normal operation AV_{CC} should be equal to V_{CC}.
43	AVRH	Power supply	Reference voltage input for analog circuitry When turning this pin on or off, always be sure to first apply electric potential equal to or greater than AVRH to AV_{CC}.
44	AVRL	Power supply	Reference voltage input for analog circuitry
45	AV_{SS}	Power supply	Ground level for analog circuitry

* : FPT-120P-M03, FPT-120C-C02

(Continued)

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistor: Approx. 1 MΩ MB90223 MB90224 MB90P224B MB90W224B
		• Oscillation feedback resistor: Approx. 1 MΩ MB90P224A MB90W224A
B		• CMOS-level output • CMOS-level hysteresis input with no standby control

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

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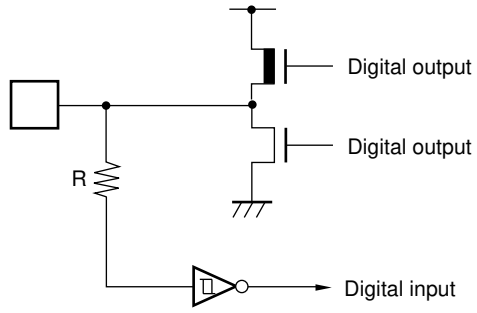
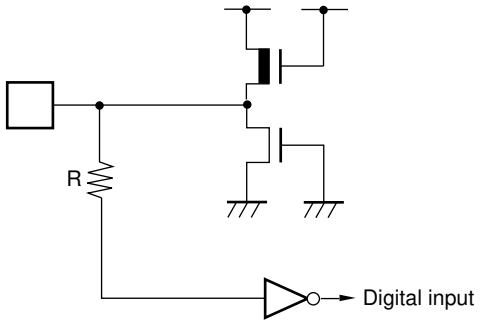
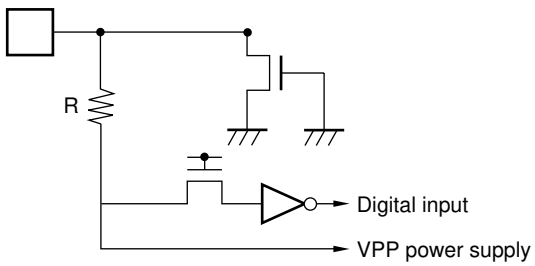
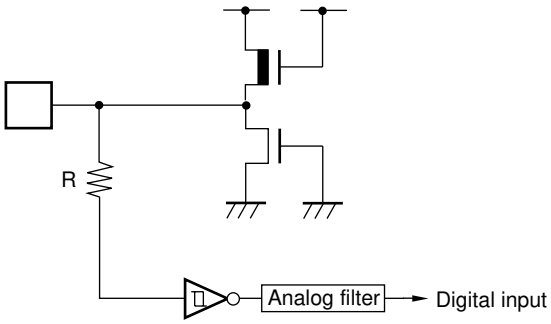
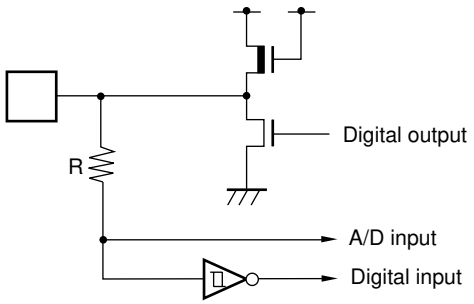
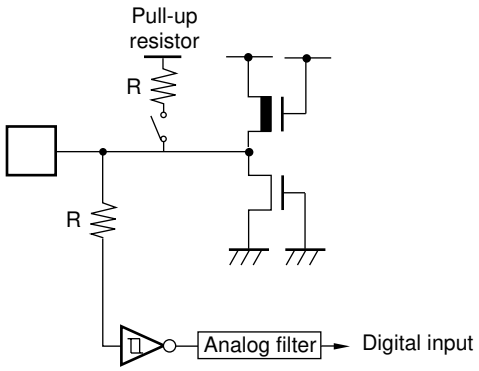
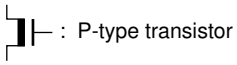
Type	Circuit	Remarks
C		• CMOS-level output • CMOS-level hysteresis input with standby control
D		• CMOS-level input with no standby control Mask ROM products only: MD2: with pull-down resistor MD1: with pull-up resistor MD0: with pull-down resistor
		• CMOS-level input with no standby control MD2 of OTPROM products/EPROM products only
E		• CMOS-level hysteresis input with no standby control • With input analog filter (40 ns Typ.)

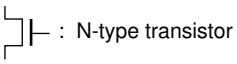
Note: The pull-up and pull-down resistors are always connected, regardless of the state.

(Continued)

(Continued)

Type	Circuit	Remarks
F		• N-channel open-drain output • CMOS-level hysteresis input with A/D control and with standby control
G		• CMOS-level hysteresis input with no standby control and with pull-up resistor • With input analog filter (40 ns Typ.) MB90223, MB90224: $\overline{\text{RST}}$ pin can be set to with or without a pull-up resistor by a mask option. MB90P224A: With pull-up resistor MB90W224A: With pull-up resistor MB90P224B: With no pull-up resistor MB90W224B: With no pull-up resistor





Note: The pull-up and pull-down resistors are always connected, regardless of the state.

■ HANDLING DEVICES

1. Preventing Latchup

CMOS ICs may cause latchup when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins other than medium-and high-voltage pins, or when a voltage exceeding the rating is applied between V_{CC} and V_{SS}.

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let any voltage exceed the maximum rating.
Also, take care to prevent the analog power supply (AV_{CC} and AVRH) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Pins when A/D is not Used

Connect to be AV_{CC} = AVRH = V_{CC} and AV_{SS} = AVRL = V_{SS} even if the A/D converter is not in use.

4. Precautions when Using an External Input

To reset the internal circuit properly by the “L” level input to the $\overline{RST}$ pin, the “L” level input to the $\overline{RST}$ pin must be maintained for at least five machine cycles. Pay attention to it if the chip uses external clock input.

5. V_{CC} and V_{SS} Pins

Apply equal potential to the V_{CC} and V_{SS} pins.

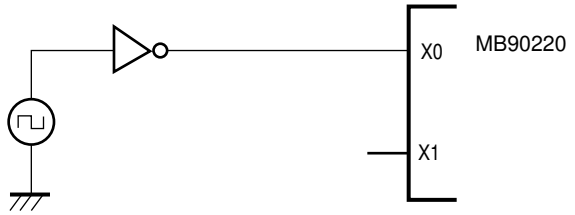
6. Supply Voltage Variation

The operation assurance range for the V_{CC} supply voltage is as given in the ratings. However, sudden changes in the supply voltage can cause misoperation, even if the voltage remains within the rated range. Therefore, it is important to supply a stable voltage to the IC. The recommended power supply control guidelines are that the commercial frequency (50 to 60 Hz) ripple variation (P-P value) on V_{CC} should be less than 10% of the standard V_{CC} value and that the transient rate of change during sudden changes, such as during power supply switching, should be less than 0.1 V/ms.

7. Notes on Using an External Clock

When using an external clock, drive the X0 pin as illustrated below. When an external clock is used, oscillation stabilization time is required even for power-on reset and wake-up from stop mode.

- **Use of External Clock**



Note: When using an external clock, be sure to input external clock more than 6 machine cycles after setting the $\overline{HST}$ pin to “L” to transfer to the hardware standby mode.

8. Power-on Sequence for A/D Converter Power Supplies and Analog Inputs

Be sure to turn on the digital power supply (V_{CC}) before applying voltage to the A/D converter power supplies (AV_{CC}, AVRH, and AVRL) and analog inputs (AN00 to AN15).

When turning power supplies off, turn off the A/D converter power supplies (AV_{CC}, AVRH, and AVRL) and analog inputs (AN00 to AN15) first, then the digital power supply (V_{CC}).

When turning AVRH on or off, be careful not to let it exceed AV_{CC}.

■ PROGRAMMING FOR MB90P224A/P224B/W224A/W224B

In EPROM mode, the MB90P224A/P224B/W224A/W224B functions equivalent to the MBM27C1000. This allows the EPROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter (do not use the electronic signature mode).

1. Program Mode

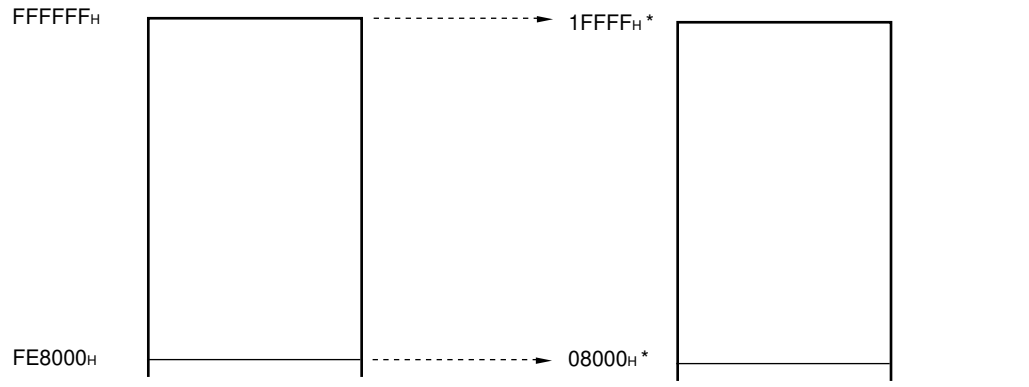
When shipped from Fujitsu, and after each erasure, all bits (96 K × 8 bits) in the MB90P224A/P224B/W224A/W224B are in the "1" state. Data is written to the ROM by selectively programming "0's" into the desired bit locations. Bits cannot be set to "1" electrically.

2. Programming Procedure

(1) Set the EPROM programmer to MBM27C1000.

(2) Load program data into the EPROM programmer at 08000_H to $1FFFF_H$.

Note that ROM addresses $FE8000_H$ to $FFFFFF_H$ in the operation mode in the MB90P224A/P224B/W224A/W224B series assign to 08000_H to $1FFFF_H$ in the EPROM mode (on the EPROM programmer).



* : Be sure to set the programming, the start address and the stop address on the EPROM programmer to 08000_H/$1FFFF_H$.

(3) Mount the MB90P224A/P224B/W224A/W224B on the adapter socket, then fit the adapter socket onto the EPROM programmer. When mounting the device and the adapter socket, pay attention to their mounting orientations.

(4) Start programming the program data to the device.

(5) If programming has not successfully resulted, connect a capacitor of approx. 0.1 μF between V_{CC} and GND, between V_{PP} and GND.

Note: The mask ROM products (MB90223, MB90224) does not support EPROM mode. Data cannot, therefore, be read by the EPROM programmer.

3. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part No.			MB90P224B
Package			QFP-120
Compatible socket adapter **Sun Hayato Co., Ltd.**			ROM-120QF-32DP-16F
Recommended programmer manufacturer and programmer name	**Advantest corp.**	**R4945A (main unit) + R49451A (adapter)**	Recommended

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106
Advantest Corp.: TEL: Except JAPAN (81)-3-3930-4111

4. Erase Procedure

Data written in the MB90W224A/W224B is erased (from “0” to “1”) by exposing the chip to ultraviolet rays with a wavelength of 2,537 Å through the translucent cover.

Recommended irradiation dosage for exposure is 10 Wsec/cm^2. This amount is reached in 15 to 20 minutes with a commercial ultraviolet lamp positioned 2 to 3 cm above the package (when the package surface illuminance is 1200 μW/cm^2).

If the ultraviolet lamp has a filter, remove the filter before exposure. Attaching a mirrored plate to the lamp increases the illuminance by a factor of 1.4 to 1.8, thus shortening the required erasure time. If the translucent part of the package is stained with oil or adhesive, transmission of ultraviolet rays is degraded, resulting in a longer erasure time. In that case, clean the translucent part using alcohol (or other solvent not affecting the package).

The above recommended dosage is a value which takes the guard band into consideration and is a multiple of the time in which all bits can be evaluated to have been erased. Observe the recommended dosage for erasure; the purpose of the guard band is to ensure erasure in all temperature and supply voltage ranges. In addition, check the life span of the lamp and control the illuminance appropriately.

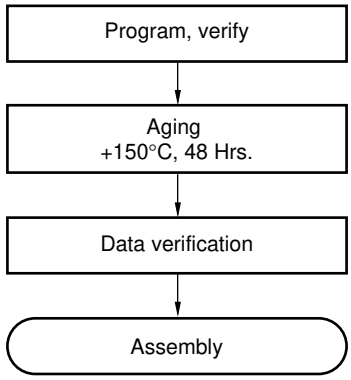
Data in the MB90W224A/W224B is erased by exposure to light with a wavelength of 4,000 Å or less.

Data in the device is also erased even by exposure to fluorescent lamp light or sunlight although the exposure results in a much lower erasure rate than exposure to 2,537 Å ultraviolet rays. Note that exposure to such lights for an extended period will therefore affect system reliability. If the chip is used where it is exposed to any light with a wavelength of 4,000 Å or less, cover the translucent part, for example, with a protective seal to prevent the chip from being exposed to the light.

Exposure to light with a wavelength of 4,000 to 5,000 Å or more will not erase data in the device. If the light applied to the chip has a very high illuminance, however, the device may cause malfunction in the circuit for reasons of general semiconductor characteristics. Although the circuit will recover normal operation when exposure is stopped, the device requires proper countermeasures for use in a place exposed continuously to such light even though the wavelength is 4,000 Å or more.

5. Recommended Screening Conditions

High temperature aging is recommended as the pre-assembly screening procedure.



6. Programming Yeild

MB90P224A/P224B cannot be write-tested for all bits due to their nature. Therefore the write yield cannot always be guaranteed to be 100%.

7. Pin Assignments in EPROM Mode

(1) Pins Compatible with MBM27C1000

MBM27C1000		MB90P224A/P224B/ MB90W224A/W224B	
Pin no.	Pin name	Pin no.	Pin name
1	V_{PP}	87	MD2 (V_{PP})
2	OE	83	P55
3	A15	7	P37
4	A12	4	P34
5	A07	118	P27
6	A06	117	P26
7	A05	116	P25
8	A04	115	P24
9	A03	114	P23
10	A02	113	P22
11	A01	112	P21
12	A00	111	P20
13	D00	95	P00
14	D01	96	P01
15	D02	97	P02
16	GND	33, 63, 91,119	V_{SS}

MBM27C1000		MB90P224A/P224B/ MB90W224A/W224B	
Pin no.	Pin name	Pin no.	Pin name
32	V_{CC}	8, 54, 94	V_{CC}
31	PGM	84	P56
30	N.C.	—	—
29	A14	6	P36
28	A13	5	P35
27	A08	120	P30
26	A09	1	P31
25	A11	3	P33
24	A16	9	P40
23	A10	2	P32
22	CE	82	P54
21	D07	102	P07
20	D06	101	P06
19	D05	100	P05
18	D04	99	P04
17	D03	98	P03

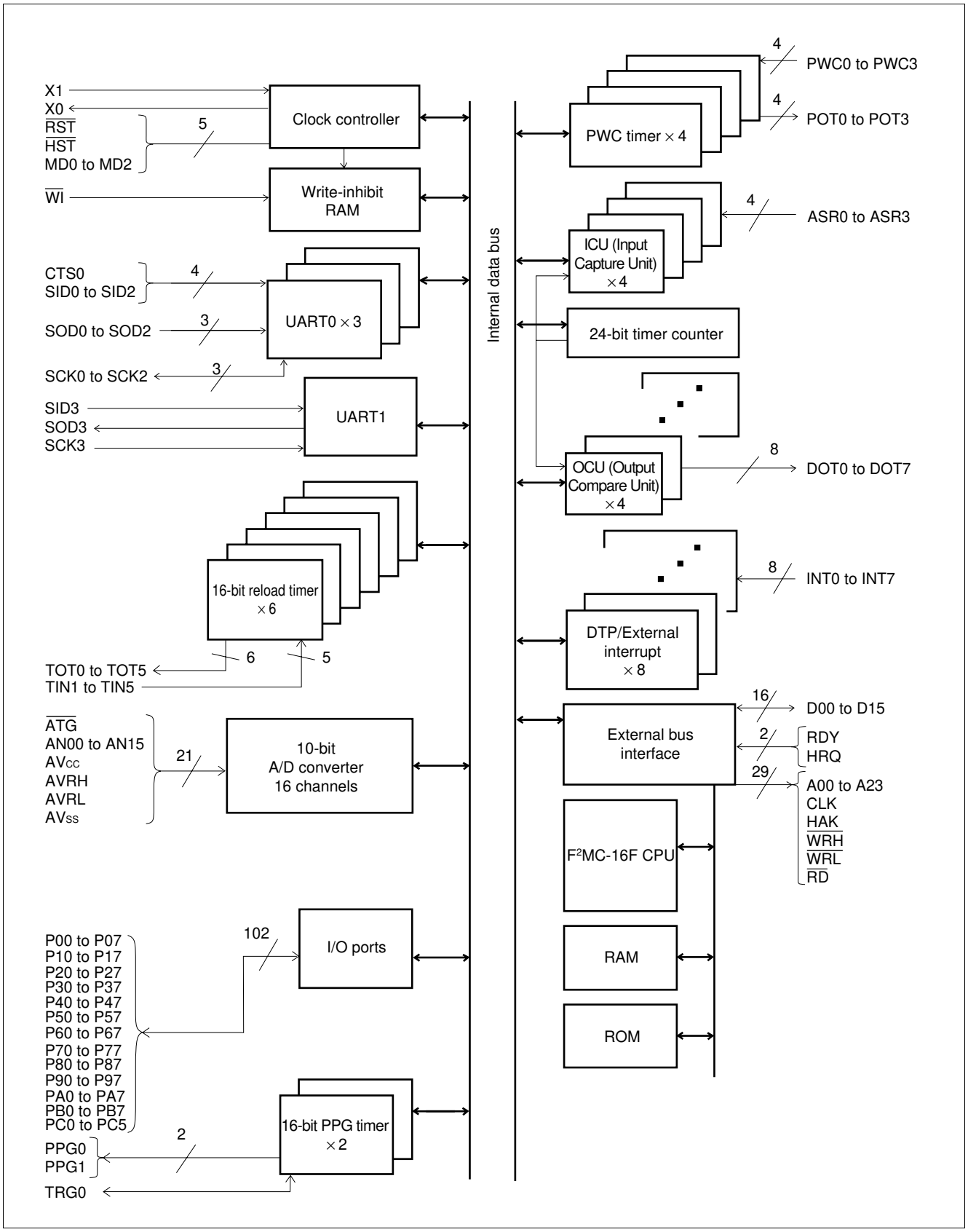
(2) Power Supply and GND Connection Pins

Type	Pin no.	Pin name
Power supply	89 88 86 8, 54, 94	MD0 MD1 $\overline{HST}$ V_{CC}
GND	33, 63, 91, 119 44 45 80 81 90	V_{SS} AVRL AV_{SS} P52 P53 $\overline{RST}$

(3) Pins other than MBM27C1000-compatible Pins

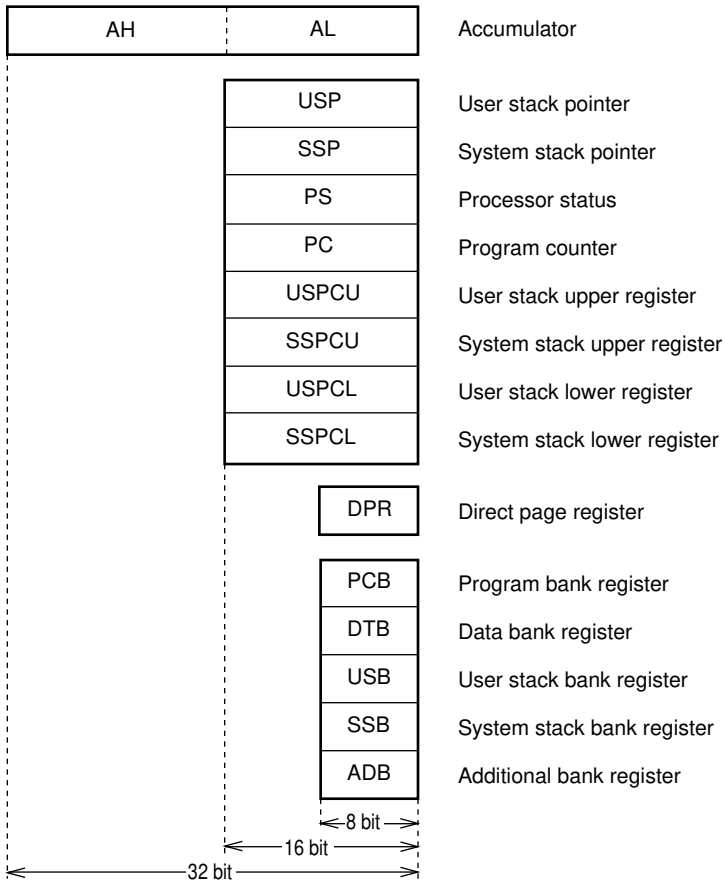
Pin no.	Pin name	Treatment
92	X0	Pull up with 4.7 KΩ resistor
93	X1	OPEN
109 110 10 to 16 42 43 46 47 48 to 53 17 to 24 25 to 32 34 to 41 55 to 61 63 to 70 71 to 76 78 79 85 103 to 108	P16 P17 P41 to P47 AV_{CC} AVRH P60 P61 P62 to P67 P70 to P77 P80 to P82 P90 to P97 PA0 to PA7 PB0 to PB7 PC0 to PC5 P50 P51 P57 P10 to P15	Connect pull-up resistor of about 1 MΩ to each pin

■ BLOCK DIAGRAM

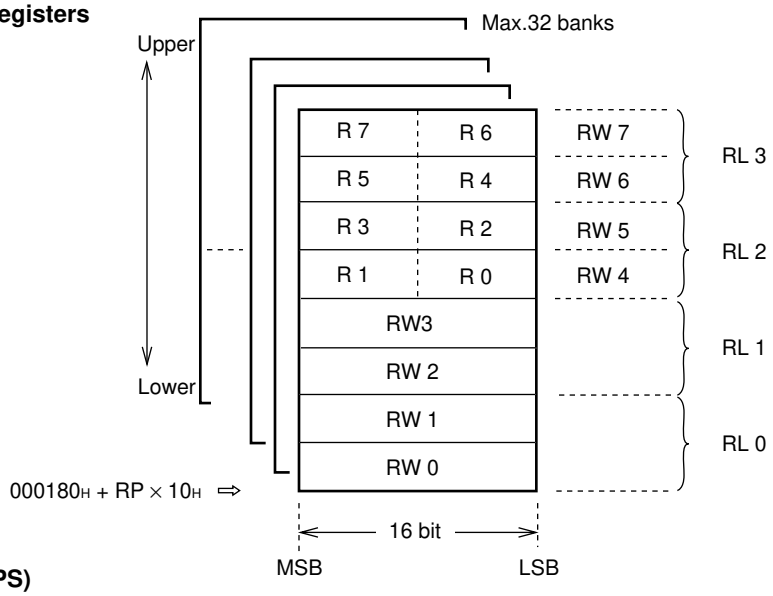


■ PROGRAMMING MODEL

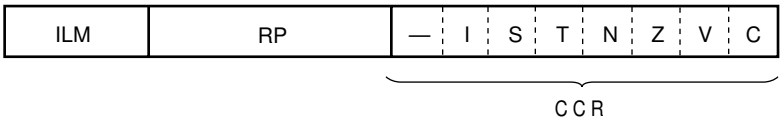
Dedicated Registers



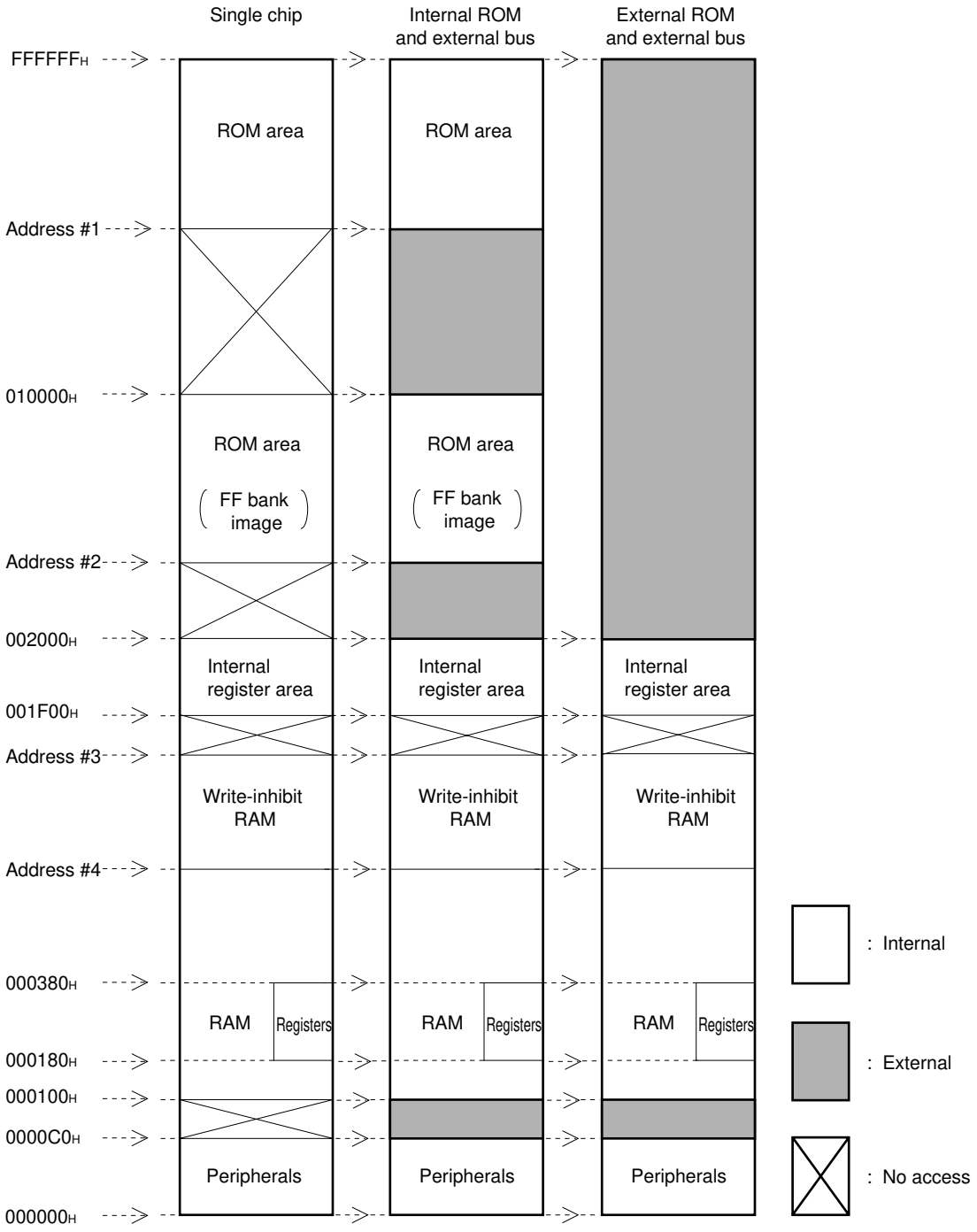
General-purpose Registers



Processor Status (PS)



■ MEMORY MAP



Type	Address #1	Address #2	Address #3	Address #4
MB90223	FF0000H	004000H	000F00H	000D00H
MB90224 MB90P224A/P224B MB90W224A/W224B	FE8000H	004000H	001500H	001300H
MB90V220	(FE0000H)	004000H	001900H	001500H

■ I/O MAP

Address	Register	Register name	Access	Resouce name	Initial value
000000H*3	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
000001H*3	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
000002H*3	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
000003H*3	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
000004H*3	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
000005H*3	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX
000006H	Port 6 data register	PDR6	R/W	Port 6	11111111
000007H	Port 7 data register	PDR7	R	Port 7	XXXXXXXX
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
000009H	Port 9 data register	PDR9	R/W	Port 9	11111111
00000AH	Port A data register	PDRA	R/W	Port A	XXXXXXXX
00000BH	Port B data register	PDRB	R/W	Port B	XXXXXXXX
00000CH	Port C data register	PDRC	R/W	Port C	––XXXXXX
00000DH to 0FH	(Reserved area)*1				
000010H*3	Port 0 data direction register	DDR0	R/W	Port 0	00000000
000011H*3	Port 1 data direction register	DDR1	R/W	Port 1	00000000
000012H*3	Port 2 data direction register	DDR2	R/W	Port 2	00000000
000013H*3	Port 3 data direction register	DDR3	R/W	Port 3	00000000
000014H*3	Port 4 data direction register	DDR4	R/W	Port 4	00000000
000015H*3	Port 5 data direction register	DDR5	R/W	Port 5	00000000
000016H	Port 6 analog input enable register	ADER0	R/W	Port 6	11111111
000017H	Port 7 data direction register	DDR7	R/W	Port 7	11111111
000018H	Port 8 data direction register	DDR8	R/W	Port 8	00000000
000019H	Port 9 analog input enable register	ADER1	R/W	Port 9	11111111
00001AH	Port A data direction register	DDRA	R/W	Port A	00000000
00001BH	Port B data direction register	DDRB	R/W	Port B	00000000
00001CH	Port C data direction register	DDRC	R/W	Port C	––000000
00001DH to 1FH	(Reserved area)*1				
000020H	Mode control register 0	UMC0	R/W	UART 0 (ch.0)	00000100
000021H	Status register 0	USR0	R/W		00010000
000022H	Input data register 0 /output data register 0	UIDR0 /UODR0	R/W		XXXXXXXX

(Continued)