Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

The following document contains information on Cypress products. Although the document is marked with the name "Spansion" and "Fujitsu", the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

Continuity of Specifications
There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

Continuity of Ordering Part Numbers
Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information
Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress
Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13750-4E

16-bit Microcontroller

CMOS

F²MC-16LX MB90920 Series

MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/ MB90F924NC/F924NCS/V920-101/V920-102

■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Built-in PLL clock frequency multiplication circuit.
  Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
  Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
  Detects rising, falling, or both edges.
  16-bit capture register × 8
  The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

2010.9

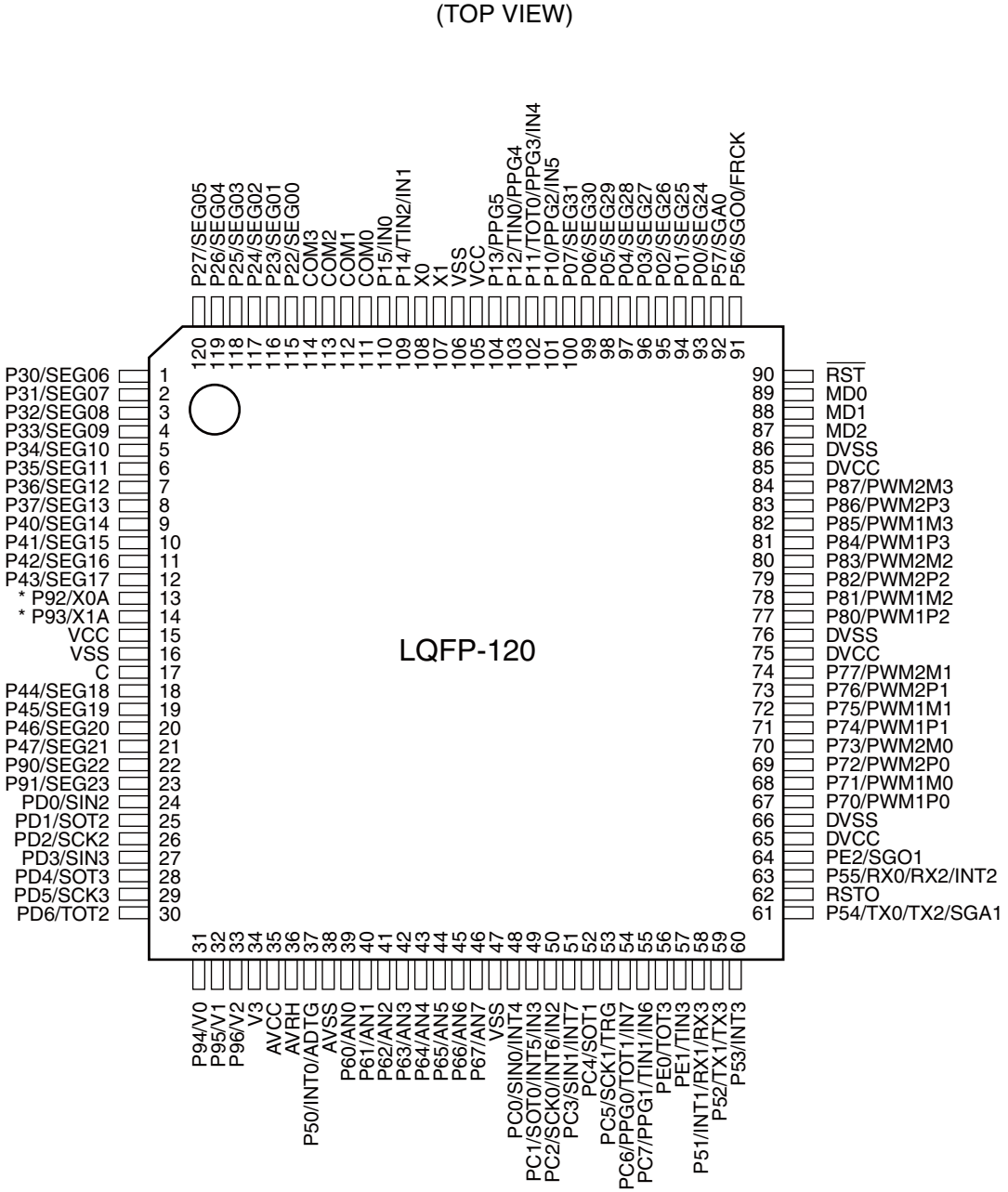
(Continued)

- 16-bit reload timer (4 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Selectable event count function
- Real time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
  Output pins (3 channels), external trigger input pin (1 channel)
  Operation clock frequencies : f_{CP}, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
  Conversion time : 3 µs (at f_{CP} = 32 MHz)
  External trigger activation available (P50/INT0/ADTG)
  Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
  Automatic reset when low voltage is detected
  Program looping detection function
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator (2 channels)
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at f_{CP} = 32 MHz)
  Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
  Automotive/CMOS-Schmitt
- Flash memory security function
  Protects the contents of Flash memory (Flash memory product only)

■ PRODUCT LINEUP

Part number / Parameter	MB90 F922NC	MB90 F922NCS	MB90 F923NC	MB90 F923NCS	MB90 F924NC	MB90 F924NCS	MB90 922NCS	MB90 V920-101	MB90 V920-102
Type	Flash memory product						MASK ROM product	Evaluation product	
CPU	F^2MC-16LX CPU								
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8)								
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No	No	No	Yes
ROM	Flash memory 256 Kbytes		Flash memory 384 Kbytes		Flash memory 512 Kbytes		256 K bytes	External	
RAM	10 Kbytes		16 Kbytes		24 Kbytes		10 K bytes	30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports	93 ports	93 ports	91 ports
LCD controller	32 segment × 4 common								
LIN-UART	UART (LIN/SCI) 4 channels								
CAN interface	4 channels								
16-bit input capture	8 channels								
16-bit reload timer	4 channels								
16-bit free-run timer	1 channel								
Real time watch timer	1 channel								
16-bit PPG timer	6 channels								
External interrupt	8 channels								
8/10-bit A/D converter	8 channels								
Low-voltage/ CPU operating detection reset	Yes							No	
Stepping motor controller	4 channels								
Sound generator	2 channels								
Flash memory security	Yes						—		
Operating voltage	4.0 V to 5.5 V							4.5 V to 5.5 V	
Package	LQFP-120							PGA-299	

■ PIN ASSIGNMENT



(FPT-120P-M21)

* : MB90V920-101, MB90F922NCS,MB90F923NCS,MB90F924NCS,MB90922NCS : P92, P93
MB90V920-102, MB90F922NC,MB90F923NC,MB90F924NC : X0A, X1A

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O circuit type*1	Function
108	X0	A	High-speed oscillation input pin
107	X1		High-speed oscillation output pin
13	X0A	B	Low-speed oscillation input pin
	P92	I	General-purpose I/O port
14	X1A	B	Low-speed oscillation output pin
	P93	I	General-purpose I/O port
90	$\overline{RST}$	C	Reset input pin
93	P00	F	General-purpose I/O port
	SEG24		LCD controller/driver segment output pin
94	P01	F	General-purpose I/O port
	SEG25		LCD controller/driver segment output pin
95	P02	F	General-purpose I/O port
	SEG26		LCD controller/driver segment output pin
96	P03	F	General-purpose I/O port
	SEG27		LCD controller/driver segment output pin
97	P04	F	General-purpose I/O port
	SEG28		LCD controller/driver segment output pin
98	P05	F	General-purpose I/O port
	SEG29		LCD controller/driver segment output pin
99	P06	F	General-purpose I/O port
	SEG30		LCD controller/driver segment output pin
100	P07	F	General-purpose I/O port
	SEG31		LCD controller/driver segment output pin
101	P10	I	General-purpose I/O port
	PPG2		16-bit PPG ch.2 output pin
	IN5		Input capture ch.5 trigger input pin
102	P11	I	General-purpose I/O port
	TOT0		16-bit reload timer ch.0 TOT output pin
	PPG3		16-bit PPG ch.3 output pin
	IN4		Input capture ch.4 trigger input pin
103	P12	I	General-purpose I/O port
	TIN0		16-bit reload timer ch.0 TIN input pin
	PPG4		16-bit PPG ch.4 output pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
7	P36	F	General-purpose I/O port
	SEG12		LCD controller/driver segment output pin
8	P37	F	General-purpose I/O port
	SEG13		LCD controller/driver segment output pin
9	P40	F	General-purpose I/O port
	SEG14		LCD controller/driver segment output pin
10	P41	F	General-purpose I/O port
	SEG15		LCD controller/driver segment output pin
11	P42	F	General-purpose I/O port
	SEG16		LCD controller/driver segment output pin
12	P43	F	General-purpose I/O port
	SEG17		LCD controller/driver segment output pin
18	P44	F	General-purpose I/O port
	SEG18		LCD controller/driver segment output pin
19	P45	F	General-purpose I/O port
	SEG19		LCD controller/driver segment output pin
20	P46	F	General-purpose I/O port
	SEG20		LCD controller/driver segment output pin
21	P47	F	General-purpose I/O port
	SEG21		LCD controller/driver segment output pin
37	P50	I	General-purpose I/O port
	INT0		INT0 external interrupt input pin
	ADTG		A/D converter external trigger input pin
58	P51	I	General-purpose I/O port
	INT1		INT1 external interrupt input pin
	RX1		CAN interface 1 RX input pin
	RX3		CAN interface 3 RX input pin
59	P52	I	General-purpose I/O port
	TX1		CAN interface 1 TX output pin
	TX3		CAN interface 3 TX output pin
60	P53	I	General-purpose I/O port
	INT3		INT3 external interrupt input pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
61	P54	I	General-purpose I/O port
	TX0		CAN interface 0 TX output pin
	TX2		CAN interface 2 TX output pin
	SGA1		Sound generator ch.1 SGA output pin
63	P55	I	General-purpose I/O port
	RX0		CAN interface 0 RX input pin
	RX2		CAN interface 2 RX input pin
	INT2		INT2 external interrupt input pin
91	P56	I	General-purpose I/O port
	SGO0		Sound generator ch.0 SGO output pin
	FRCK		Free-run timer clock input pin
92	P57	I	General-purpose I/O port
	SGA0		Sound generator ch.0 SGA output pin
39	P60	H	General-purpose I/O port
	AN0		A/D converter input pin
40	P61	H	General-purpose I/O port
	AN1		A/D converter input pin
41	P62	H	General-purpose I/O port
	AN2		A/D converter input pin
42	P63	H	General-purpose I/O port
	AN3		A/D converter input pin
43	P64	H	General-purpose I/O port
	AN4		A/D converter input pin
44	P65	H	General-purpose I/O port
	AN5		A/D converter input pin
45	P66	H	General-purpose I/O port
	AN6		A/D converter input pin
46	P67	H	General-purpose I/O port
	AN7		A/D converter input pin
67	P70	L	General-purpose output-only port
	PWM1P0		Stepping motor controller ch.0 output pin
68	P71	L	General-purpose output-only port
	PWM1M0		Stepping motor controller ch.0 output pin
69	P72	L	General-purpose output-only port
	PWM2P0		Stepping motor controller ch.0 output pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
70	P73	L	General-purpose output-only port
	PWM2M0		Stepping motor controller ch.0 output pin
71	P74	L	General-purpose output-only port
	PWM1P1		Stepping motor controller ch.1 output pin
72	P75	L	General-purpose output-only port
	PWM1M1		Stepping motor controller ch.1 output pin
73	P76	L	General-purpose output-only port
	PWM2P1		Stepping motor controller ch.1 output pin
74	P77	L	General-purpose output-only port
	PWM2M1		Stepping motor controller ch.1 output pin
77	P80	L	General-purpose output-only port
	PWM1P2		Stepping motor controller ch.2 output pin
78	P81	L	General-purpose output-only port
	PWM1M2		Stepping motor controller ch.2 output pin
79	P82	L	General-purpose output-only port
	PWM2P2		Stepping motor controller ch.2 output pin
80	P83	L	General-purpose output-only port
	PWM2M2		Stepping motor controller ch.2 output pin
81	P84	L	General-purpose output-only port
	PWM1P3		Stepping motor controller ch.3 output pin
82	P85	L	General-purpose output-only port
	PWM1M3		Stepping motor controller ch.3 output pin
83	P86	L	General-purpose output-only port
	PWM2P3		Stepping motor controller ch.3 output pin
84	P87	L	General-purpose output-only port
	PWM2M3		Stepping motor controller ch.3 output pin
22	P90	F	General-purpose I/O port
	SEG22		LCD controller/driver segment output pin
23	P91	F	General-purpose I/O port
	SEG23		LCD controller/driver segment output pin
31	P94	G	General-purpose I/O port
	V0		LCD controller/driver reference power supply pin
32	P95	G	General-purpose I/O port
	V1		LCD controller/driver reference power supply pin

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
33	P96	G	General-purpose I/O port
	V2		LCD controller/driver reference power supply pin
34	V3	—	LCD controller/driver reference power supply pin
48	PC0	J	General-purpose I/O port
	SIN0		UART ch.0 serial data input pin
	INT4		INT4 external interrupt input pin
49	PC1	I	General-purpose I/O port
	SOT0		UART ch.0 serial data output pin
	INT5		INT5 external interrupt input pin
	IN3		Input capture ch.3 trigger input pin
50	PC2	I	General-purpose I/O port
	SCK0		UART ch.0 serial clock I/O pin
	INT6		INT6 external interrupt input pin
	IN2		Input capture ch.2 trigger input pin
51	PC3	J	General-purpose I/O port
	SIN1		UART ch.1 serial data input pin
	INT7		INT7 external interrupt input pin
52	PC4	I	General-purpose I/O port
	SOT1		UART ch.1 serial data output pin
53	PC5	I	General-purpose I/O port
	SCK1		UART ch.1 serial clock I/O pin
	TRG		16-bit PPG ch.0 to ch.5 external trigger input pin
54	PC6	I	General-purpose I/O port
	PPG0		16-bit PPG ch.0 output pin
	TOT1		16-bit reload timer ch.1 TOT output pin
	IN7		Input capture ch.7 trigger input pin
55	PC7	I	General-purpose I/O port
	PPG1		16-bit PPG ch.1 output pin
	TIN1		16-bit reload timer ch.1 TIN input pin
	IN6		Input capture ch.6 trigger input pin
24	PD0	J	General-purpose I/O port
	SIN2		UART ch.2 serial data input pin
25	PD1	I	General-purpose I/O port
	SOT2		UART ch.2 serial data output pin

(Continued)

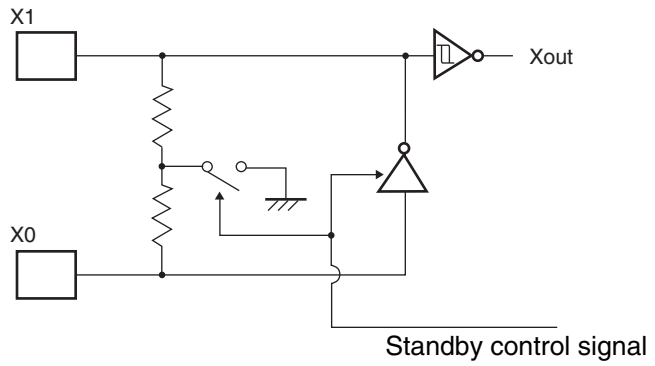
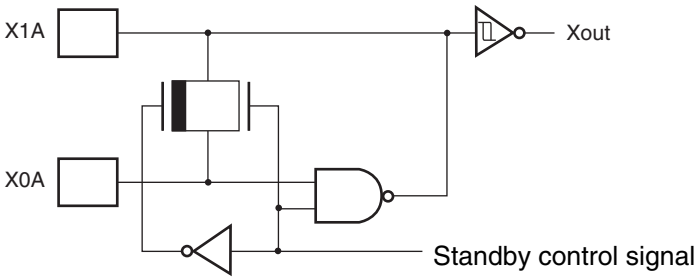
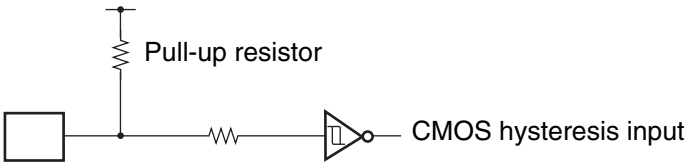
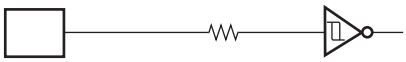
(Continued)

Pin no.	Pin name	I/O circuit type*1	Function
26	PD2	I	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	I	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E*2	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

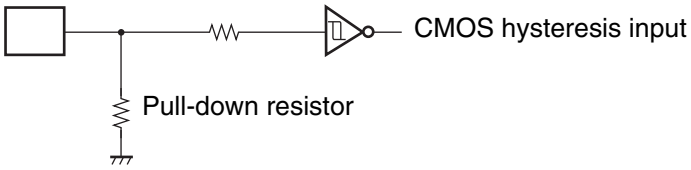
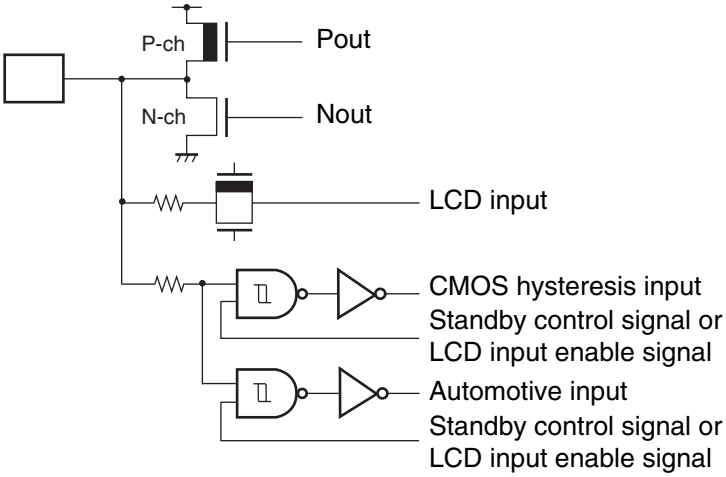
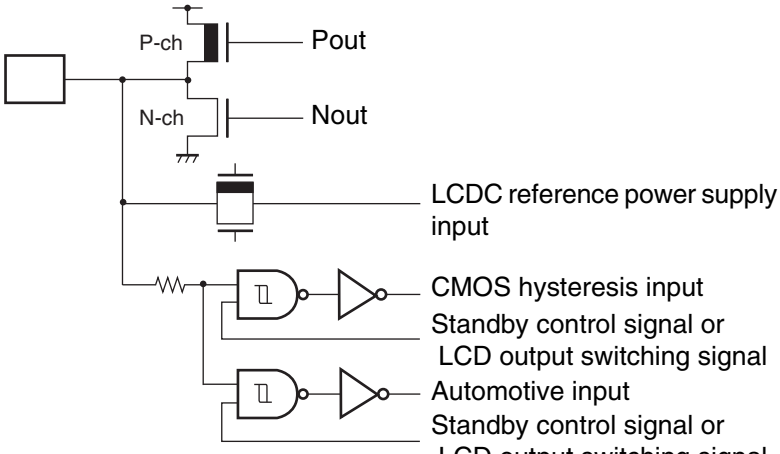
*1 : For I/O circuit type, refer to “ ■ I/O CIRCUIT TYPES”.

*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

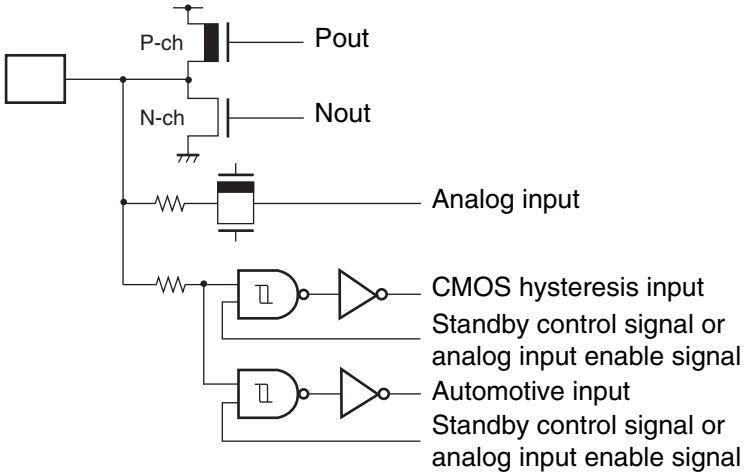
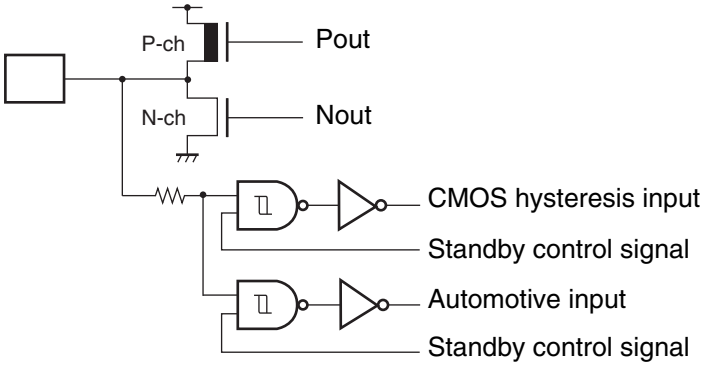
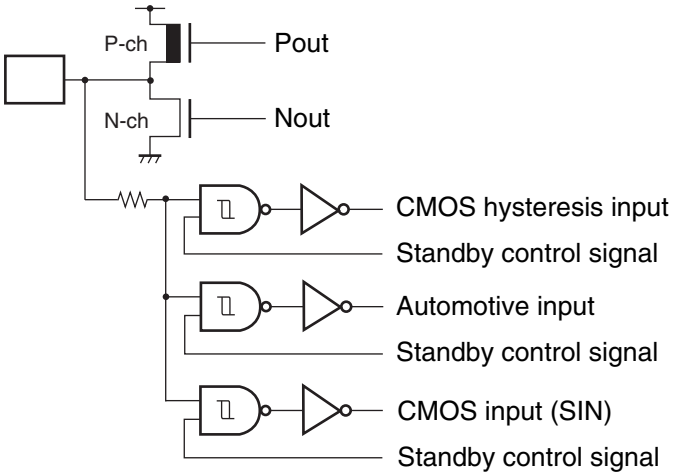
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistance : approx. 1 MΩ (Flash memory product/MASK ROM product/Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistance : approx. 10 MΩ
C		Input-only pin (with pull-up resistance) • Attached pull-up resistor : approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC})
D		Input-only pin • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the Flash memory products uses this circuit type.

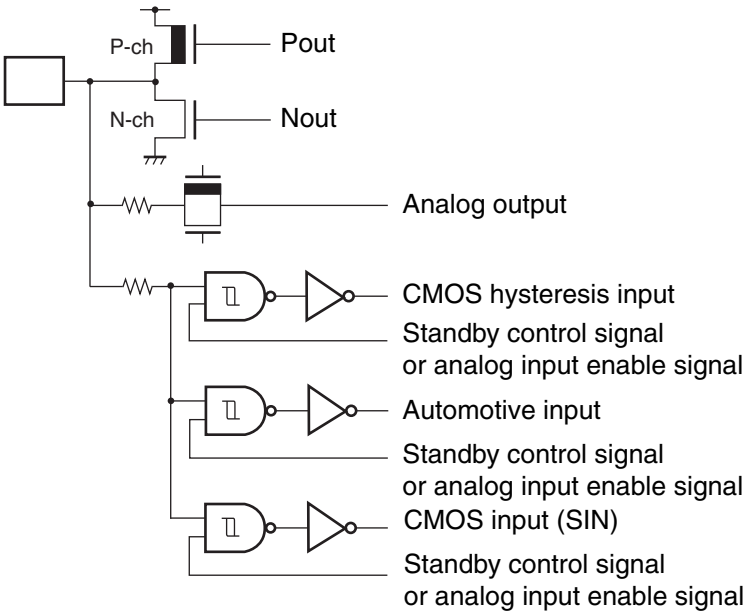
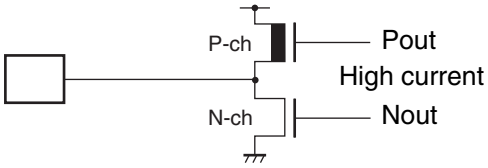
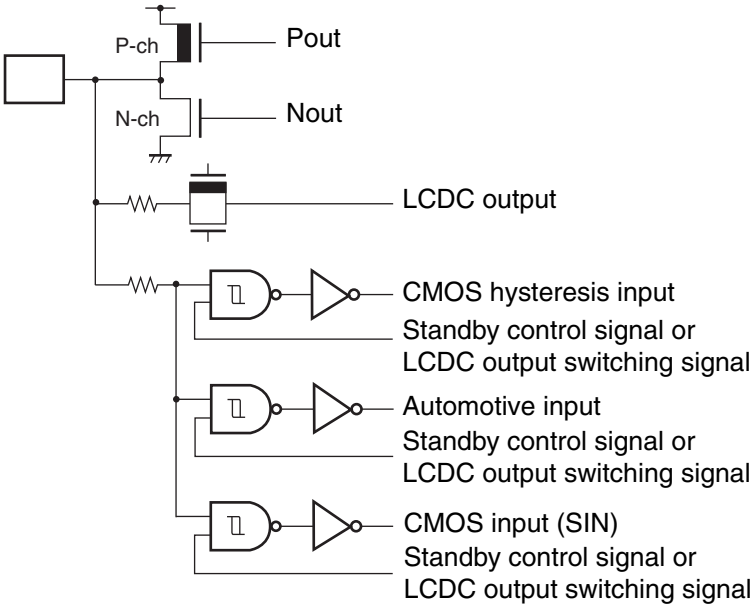
(Continued)

Type	Circuit	Remarks
E		Input-only pin (with pull-down resistance) • Attached pull-down resistance: approx. 50 kΩ • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) Note: The MD2 pin of the evaluation products uses this circuit type.
F		LCD output common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
G		LCDC reference power supply common general-purpose port • CMOS output (I_{OH}/I_{OL} = ±4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

(Continued)

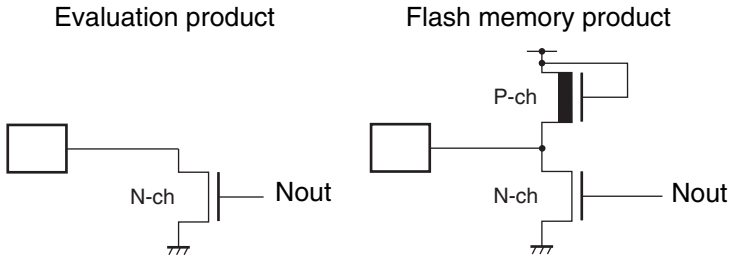
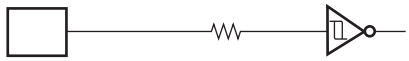
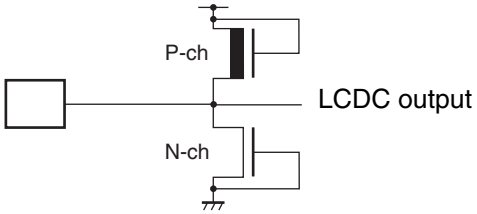
Type	Circuit	Remarks
H		A/D converter input common general-purpose port • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
I		General-purpose port • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
J		General-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

(Continued)

Type	Circuit	Remarks
K		A/D converter input common general-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
L		High current output port (SMC pin) CMOS output (I_{OH}/I_{OL} = ± 30 mA)
M		LCDC output common general-purpose port (serial input)) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • CMOS hysteresis input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})

(Continued)

(Continued)

Type	Circuit	Remarks
N		N-ch open-drain pin I_{OL} = 4 mA
O		Input-only pin Automotive input (V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})
P		LCDC output pin (COM pin)

■ HANDLING DEVICES

- **Strictly observe maximum rated voltages (preventing latch-up)**

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between VCC and VSS pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC}, AVRH), the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC}, AVRH) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

- **Supply voltage stabilization**

Rapid fluctuations in the power supply voltage can cause malfunctions even if the Vcc power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

- **Precautions when turning the power on**

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μs.

- **Handling unused pins**

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 kΩ.

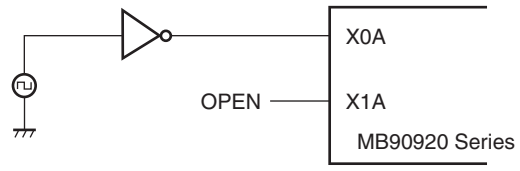
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 kΩ or more.

- **Handling A/D converter power supply pins**

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVRH = V_{SS}$.

- **Notes on using an external clock**

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



Sample external clock connection

- **Notes on operating in PLL clock mode**

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

- **Crystal oscillator circuit**

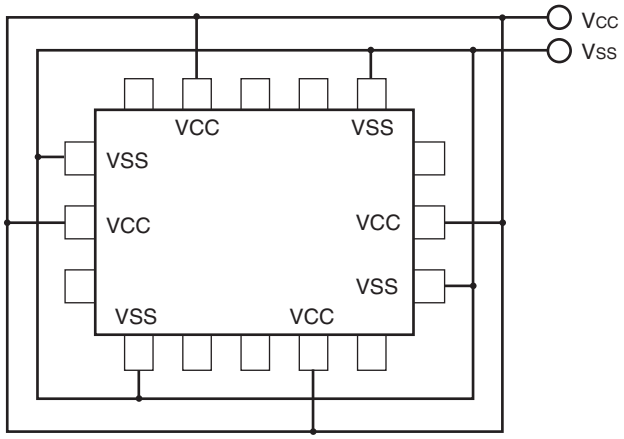
Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- **Power supply pins**

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



Power supply input pins (Vcc/Vss)

In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

- **Sequence for connecting the A/D converter power supply and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that AVRH does not exceed AVcc during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

- **Handling the power supply for high-current output buffer pins** (DV_{CC}, DV_{SS})

  - **Flash memory products and MASK ROM products (MB90F922NC/F922NCS/922NCS/F923NC/ F923NCS/F924NC/F924NCS)**

    In the Flash memory products and MASK ROM products, the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is isolated from the digital power supply (V_{CC}).
    Therefore, DVcc can therefore be set to a higher voltage than Vcc. If the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is supplied before the digital power supply (V_{CC}), however, care needs to be taken because it is possible that the port 7 or port 8 stepping motor outputs may momentarily output an “H” or “L” level. In order to prevent this, connect the digital power supply (V_{CC}) prior to connecting the power supply for the high-current output buffer pins. Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC}, DV_{SS}).

  - **Evaluation product** (**MB90V920-101**/**MB90V920-102**)

    In the evaluation products, the power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) is not isolated from the digital power supply (V_{CC}). Therefore, DV_{CC} must therefore be set to a lower voltage than Vcc. The power supply for the high-current output buffer pins (DV_{CC}, DV_{SS}) must always be applied after the digital power supply (V_{CC}) has been connected, and disconnected before the digital power supply (Vcc) is disconnected (the power supply for the high-current output buffer pins may also be connected and disconnected simultaneously with the digital power supply).
    Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC}, DV_{SS}).

- **Pull-up/pull-down resistors**

MB90920 series does not support internal pull-up/pull-down resistors. Use external components as necessary.

- **Precautions when not using a sub clock signal**

If the X0A and X1A pins are not connected to an oscillator, apply a pull-down resistance to the X0A pin and leave the X1A pin open.

- **Notes on operating when the external clock is stopped**

The MB90920 series is not guaranteed to operate correctly using the internal oscillator circuit when there is no external oscillator or the external clock input is stopped.

- **Flash memory security function**

A security bit is located within the Flash memory region. The security function is activated by writing the protection code 01_H to the security bit.
Do not write the value 01_H to this address if you are not using the security function.
Please refer to following table for the address of the security bit.

	Flash memory size	Address for security bit
MB90F922NC MB90F922NCS	Built-in 2 Mbits Flash Memory	$FC0001_H$
MB90F923NCS	Built-in 3 Mbits Flash Memory	$F80001_H$
MB90F924NCS	Built-in 4 Mbits Flash Memory	$F80001_H$

- **Serial communication**

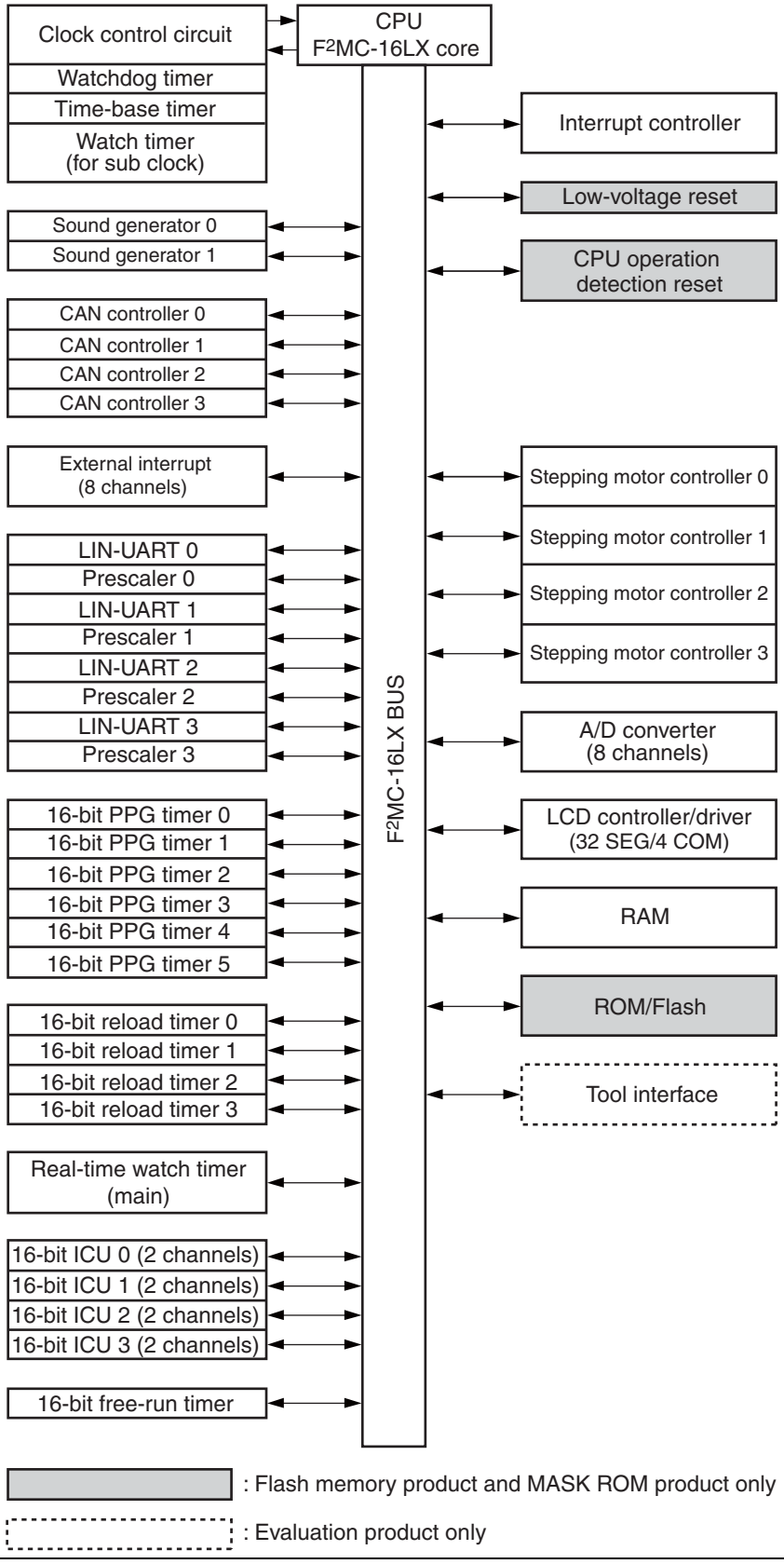
In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

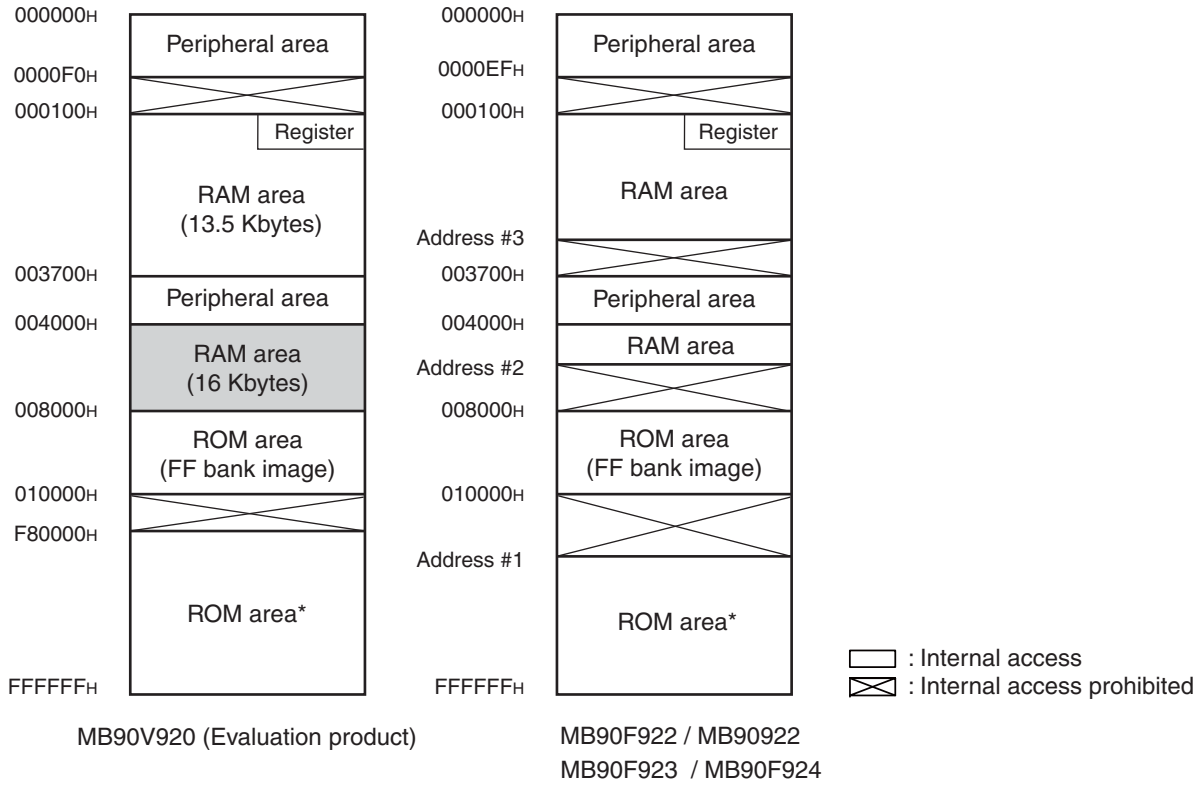
In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

■ BLOCK DIAGRAM



■ MEMORY MAP



Parts No.	ROM (Flash) capacitance	RAM capacitance	Address #1	Address #2	Address #3
MB90F922NC/F922NCS/922NCS	256 Kbytes	10 Kbytes	FC0000H	004000H	002900H
MB90F923NC/F923NCS	384 Kbytes	16 Kbytes	FA0000H	004A00H	003700H
MB90F924NC/F924NCS	512 Kbytes	24 Kbytes	F80000H	006A00H	003700H

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFH appears in the image from 008000H to 00FFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFH.

■ I/O MAP

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH, 00000BH	(Disabled)				
00000CH	Port C data register	PDRC	R/W	Port C	XXXXXXXXB
00000DH	Port D data register	PDRD	R/W	Port D	XXXXXXXXB
00000EH	Port E data register	PDRE	R/W	Port E	XXXXXXXXB
00000FH	(Disabled)				
000010H	Port 0 direction register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 direction register	DDR1	R/W	Port 1	XX000000B
000012H	Port 2 direction register	DDR2	R/W	Port 2	000000XXB
000013H	Port 3 direction register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 direction register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 direction register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 direction register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 direction register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 direction register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 direction register	DDR9	R/W	Port 9	X0000000B
00001AH	Analog input enable	ADER6	R/W	Port 6, A/D	11111111B
00001BH	(Disabled)				
00001CH	Port C direction register	DDRC	R/W	Port C	00000000B
00001DH	Port D direction register	DDRD	R/W	Port D	X0000000B
00001EH	Port E direction register	DDRE	R/W	Port E	XXXXX000B
00001FH	(Disabled)				
000020H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0B
000021H	Higher A/D control status register	ADCS1	R/W		0000000XB
000022H	Lower A/D control status register	ADCR0	R		00000000B
000023H	Higher A/D data register	ADCR1	R		XXXXXX00B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		00000000B
000027H			R/W		00000000B
000028H	Lower timer control status register	TCCSL	R/W		00000000B
000029H	Higher timer control status register	TCCSH	R/W		01-00000B
00002AH	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000B
00002BH	Higher PPG0 control status register	PCNTH0	R/W		00000001B
00002CH	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000B
00002DH	Higher PPG1 control status register	PCNTH1	R/W		00000001B
00002EH	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000B
00002FH	Higher PPG2 control status register	PCNTH2	R/W		00000001B
000030H	External interrupt enable	ENIR	R/W	External interrupt	00000000B
000031H	External interrupt request	EIRR	R/W		00000000B
000032H	Lower external interrupt level	ELVRL	R/W		00000000B
000033H	Higher external interrupt level	ELVRH	R/W		00000000B
000034H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000B
000035H	Serial control register 0	SCR0	R/W, W		00000000B
000036H	Reception/transmission data register 1	RDR0/ TDR0	R/W		00000000B
000037H	Serial status register 0	SSR0	R/W, R		00001000B
000038H	Extended communication control register 0	ECCR0	R/W, R		000000XXB
000039H	Extended status control register 0	ESCR0	R/W		00000100B
00003AH	Baud rate generator register 00	BGR00	R/W		00000000B
00003BH	Baud rate generator register 01	BGR01	R/W, R		00000000B
00003CH to 00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS"				
000050H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000B
000051H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB

(Continued)