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FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13735-6E

16-bit Microcontroller

CMOS

F²MC-16LX MB90335 Series

MB90337/F337/V330A

■ DESCRIPTION

The MB90335 series are 16-bit microcontrollers designed for applications, such as personal computer peripheral devices, that require USB communications. The USB feature supports not only 12-Mbps Function operation but also HOST operation. It is equipped with functions that are suitable for personal computer peripheral devices such as displays and audio devices, and control of mobile devices that support USB communications. While inheriting the AT architecture of the F²MC* family, the instruction set supports the C language and extended addressing modes and contains enhanced signed multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Built-in oscillation circuit and PLL clock frequency multiplication circuit
  - Oscillation clock
  - The main clock is the oscillation clock divided into 2 (for oscillation 6 MHz : 3 MHz)
  - Clock for USB is 48 MHz
  - Machine clock frequency of 6 MHz, 12 MHz or 24 MHz selectable
  - Minimum execution time of instruction : 41.7 ns (6 MHz oscillation clock, 4-time multiplied : machine clock 24 MHz and at operating V_{CC} = 3.3 V)
- **The maximum memory space: 16 Mbytes**
- **24-bit addressing**
- **Bank addressing**

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

2010.5

- **Instruction system**
  - Data types: Bit, Byte, Word, Long word
  - Addressing mode (23 types)
  - Enhanced high-precision computing with 32-bit accumulator
  - Enhanced Multiply/Divide instructions with sign and the RETI instruction
- **Instruction system compatible with high-level language (C language) and multi-task**
  - Employing system stack pointer
  - Instruction set symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 20 interrupts function
- **Data transfer function**
  - Extended intelligent I/O service function (EI²OS) : Maximum of 16 channels
  - μDMAC : Maximum 16 channels
- **Low Power Consumption Mode**
  - Sleep mode (with the CPU operating clock stopped)
  - Time-base timer mode (with the oscillator clock and time-base timer operating)
  - Stop mode (with the oscillator clock stopped)
  - CPU intermittent operation mode (with the CPU operating at fixed intervals of set cycles)
- **Package**
  - LQFP-64P (FPT-64P-M23 : 0.65 mm pin pitch)
- **Process : CMOS technology**
- **Operation guaranteed temperature: − 40 °C to + 85 °C (0 °C to + 70 °C when USB is in use)**

(Continued)

(Continued)

- **Internal peripheral function (resource)**
  - I/O port : Max 45 ports
  - Time-base timer : 1channel
  - Watchdog timer : 1 channel
  - 16-bit reload timer : 1 channel
  - Multi-functional timer
    - 8/16-bit PPG timer (8-bit × 4 channels or 16-bit × 2 channels) the period and duty of the output pulse are freely programmable.
    - 16-bit PWC timer : 1 channel
      Timer function and pulse width measurement function
  - UART: 2 channels
    - Equipped with a full duplex (8-bit long) double buffer
    - Selectable asynchronous transfer or clock-synchronous serial (extended I/O serial) transfer.
  - Extended I/O serial interface : 1 channel
  - DTP/External interrupt circuit (8 channels)
    - Activate the extended intelligent I/O service by external interrupt input
    - Interrupt output by external interrupt input
  - Delayed interrupt output module
    - Outputs an interrupt request for task switching
  - USB: 1 channel
    - USB function (supports USB Full Speed)
    - Supports Full Speed/Up to 6 endpoints can be specified.
    - Dual port RAM (supports FIFO mode).
    - Transfer type: Control, Interrupt, Bulk or Isochronous transfer possible
    - USB HOST function
  - I^2C Interface: 1 channel
    - Supports Intel SM bus standards and Phillips I^2C bus standards
    - Two-wire data transfer protocol specification
    - Master and slave transmission/reception

■ PRODUCT LINEUP

Part number	MB90V330A	MB90F337	MB90337
Type	For evaluation	Built-in Flash Memory	Built-in MASK ROM
ROM capacity	No	64 Kbytes	
RAM capacity	28 Kbytes	4 Kbytes	
Emulator-specific power supply *	Used bit	—	
CPU functions	Number of basic instructions : 351 instructions Minimum instruction execution time : 41.7 ns / at oscillation of 6 MHz (When 4 times are used : Machine clock of 24 MHz) Addressing type : 23 types Program Patch Function : For 2 address pointers Maximum memory space : 16 Mbytes		
Ports	I/O Ports(CMOS) Max 45 ports		
UART	Equipped with full-duplex double buffer Clock synchronous or asynchronous operation selectable. It can also be used for I/O serial. Built-in special baud-rate generator Built-in 2 channels		
16-bit reload timer	16-bit reload timer operation Built-in 1 channel		
Multi-functional timer	8/16-bit PPG timer (8-bit mode × 4 channels, 16-bit mode × 2 channels) 16-bit PWC timer × 1 channel		
DTP/External interrupt	8 channels Interrupt factor : “L”→“H” edge /“H”→“L” edge /“L” level /“H” level selectable		
I^2C	1 channel		
Extended I/O serial interface	1 channel		
USB	1 channel USB function (supports USB Full Speed) USB HOST function		
Withstand voltage of 5 V	8 ports (Excluding UTEST and I/O for I^2C)		
Low Power Consumption Mode	Sleep mode/Timebase timer mode/Stop mode/CPU intermittent mode		
Process	CMOS		
Operating voltage V_{CC}	3.3 V ± 0.3 V (at maximum machine clock 24 MHz)		

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

■ PACKAGES AND PRODUCT MODELS

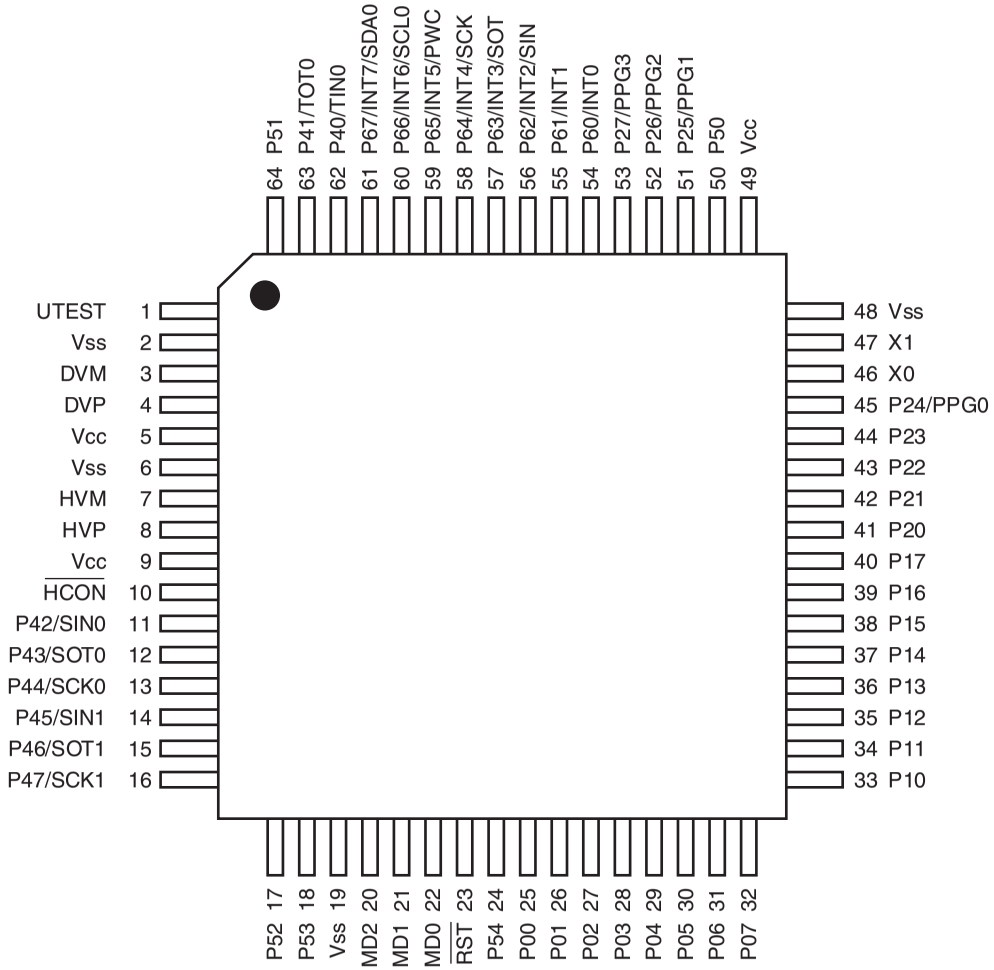
Package	MB90337	MB90F337	MB90V330A
FPT-64P-M23 (LQFP)	○	○	×
PGA-299C-A01 (PGA)	×	×	○

○ : Yes × : No

Note : See “■ PACKAGE DIMENSIONS” for details.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M23)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O Circuit type*	Status at reset/ function	Function
46 , 47	X0, X1	A	Oscillation status	It is a terminal which connects the oscillator. When connecting an external clock, leave the X1 pin side unconnected.
23	$\overline{RST}$	F	Reset input	External reset input pin.
25 to 32	P00 to P07	I	Port input (Hi-Z)	General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD00 to RD07 = 1) by the pull-up resistor setting register (RDR0). (When the power output is set, it is invalid.)
33 to 40	P10 to P17	I		General purpose input/output port. The ports can be set to be added with a pull-up resistor (RD10 to RD17 = 1) by the pull-up resistor setting register (RDR1). (When the power output is set, it is invalid.)
41 to 44	P20 to P23	D		General purpose input/output port.
45	P24	D		General purpose input/output port.
	PPG0			Functions as output pins of PPG timers ch.0.
51 to 53	P25 to P27	D		General purpose input/output port.
	PPG1 to PPG3			Functions as output pins of PPG timers ch.1 to ch.3.
62	P40	H		General purpose input/output port.
	TIN0			Function as event input pin of 16-bit reload timer.
63	P41	H		General purpose input/output port.
	TOT0			Function as output pin of 16-bit reload timer.
11	P42	H		General purpose input/output port.
	SIN0			Functions as a data input pin for UART ch.0.
12	P43	H		General purpose input/output port.
	SOT0			Functions as a data output pin for UART ch.0.
13	P44	H		General purpose input/output port.
	SCK0			Functions as a clock I/O pin for UART ch.0.
14	P45	H		General purpose input/output port.
	SIN1			Functions as a data input pin for UART ch.1.
15	P46	H		General purpose input/output port.
	SOT1			Functions as a data output pin for UART ch.1.
16	P47	H		General purpose input/output port.
	SCK1			Functions as a clock I/O pin for UART ch.1.
50	P50	K		General purpose input/output port.
64	P51	K		General purpose input/output port.
17, 18	P52, P53	K		General purpose input/output port.
24	P54	K		General purpose input/output port.

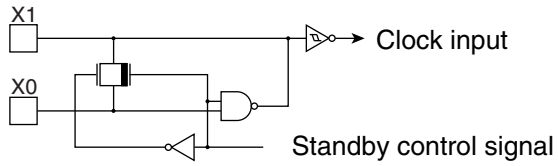
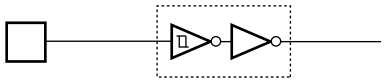
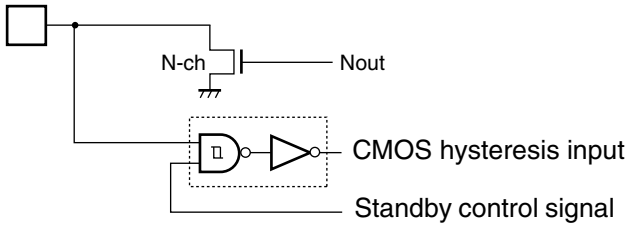
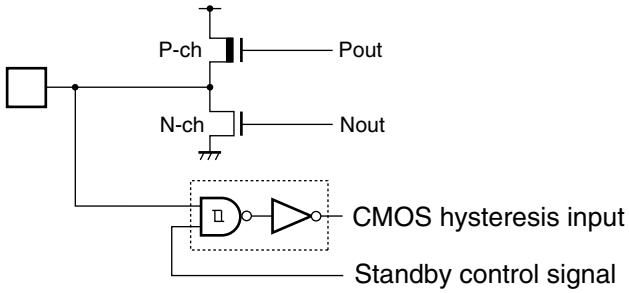
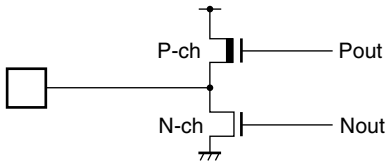
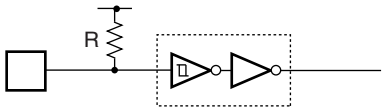
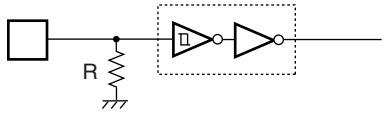
(Continued)

(Continued)

Pin no.	Pin name	I/O Circuit type*	Status at reset/ function	Function
54, 55	P60, P61	C	Port input (Hi-Z)	General purpose input/output port (withstand voltage of 5 V) .
	INT0, INT1			Functions as the input pin for external interrupt ch.0 and ch.1.
56	P62	C		General purpose input/output port (withstand voltage of 5 V) .
	INT2			Functions as the input pin for external interrupt ch.2.
	SIN			Data input pin for extended I/O serial interface.
57	P63	C		General purpose input/output port (withstand voltage of 5 V) .
	INT3			Functions as the input pin for external interrupt ch.3.
	SOT			Data output pin for extended I/O serial interface.
58	P64	C		General purpose input/output port (withstand voltage of 5 V) .
	INT4			Functions as the input pin for external interrupt ch.4.
	SCK			Clock I/O pin for extended I/O serial interface.
59	P65	C		General purpose input/output port (withstand voltage of 5 V) .
	INT5			Functions as the input pin for external interrupt ch.5.
	PWC			Functions as the PWC input pin.
60	P66	C		General purpose input/output port (withstand voltage of 5 V) .
	INT6			Functions as the input pin for external interrupt ch.6.
	SCL0			Functions as the input/output pin for I^2C interface clock. The port output must be placed in Hi-Z state during I^2C interface operation.
61	P67	C		General purpose input/output port (withstand voltage of 5 V) .
	INT7			Functions as the input pin for external interrupt ch.7.
	SDA0			Functions as the I^2C interface data input/output pin. The port output must be placed in Hi-Z state during I^2C interface operation.
1	UTEST	C	UTEST input	USB test pin. Connect this to a pull-down resistor during normal usage.
3	DVM	J	USB input (SUSPEND)	USB function D − pin.
4	DVP	J		USB function D + pin.
7	HVM	J		USB HOST D − pin.
8	HVP	J		USB HOST D + pin.
10	$\overline{\text{HCON}}$	E	High output	External pull-up resistor connection pin.
21, 22	MD1, MD0	B	Mode input	Input pin for selecting operation mode.
20	MD2	G		
5, 9, 49	Vcc	—	Power supply	Power supply pin.
2, 6, 19, 48	Vss			Power supply pin (GND).

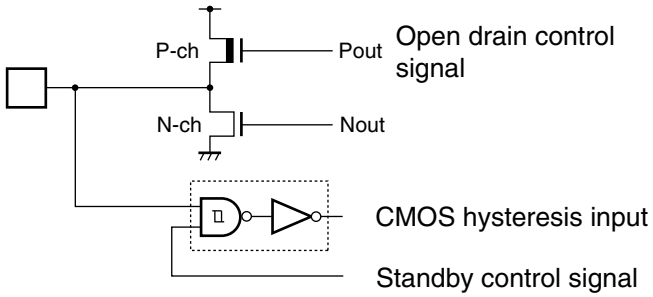
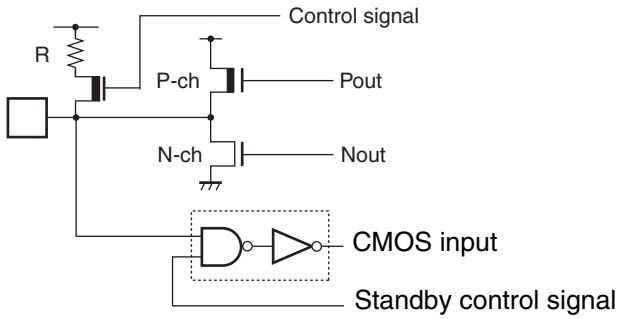
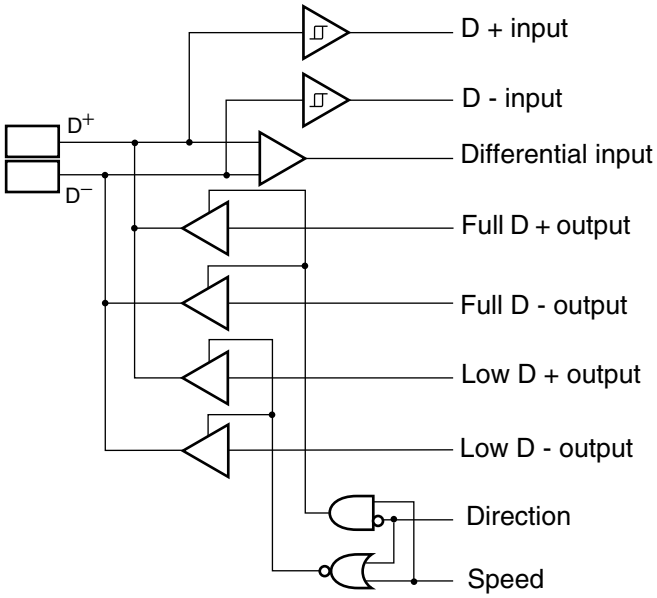
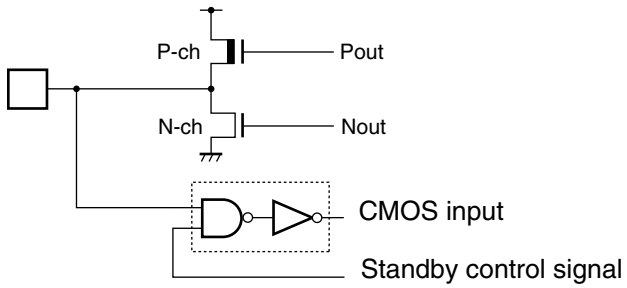
* : For circuit information, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistor of approx. 1 MΩ • With standby control
B		CMOS hysteresis input
C		• CMOS hysteresis input • N-ch open drain output
D		• CMOS output • CMOS hysteresis input (With input interception function at standby) Notes : • Share one output buffer because both output of I/O port and internal resource are used. • Share one input buffer because both input of I/O port and internal resource are used.
E		CMOS output
F		CMOS hysteresis input with pull-up resistor of approx. 50 kΩ
G		• CMOS hysteresis input with pull-down resistor of approx. 50 kΩ • Flash product is not provided with pull-down resistor.

(Continued)

(Continued)

Type	Circuit	Remarks
H		• CMOS output • CMOS hysteresis input (With input interception function at standby) With open drain control signal
I		• CMOS output • CMOS input (With input interception function at standby) • Programmable input pull-up resistor
J		USB I/O pin
K		• CMOS output • CMOS input (With input interception function at standby)

■ HANDLING DEVICES

1. Preventing latch-up and turning on power supply

latch-up may occur on CMOS IC under the following conditions:

- If a voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using CMOS IC, take great care to prevent the occurrence of latch-up.

2. Treatment of unused pins

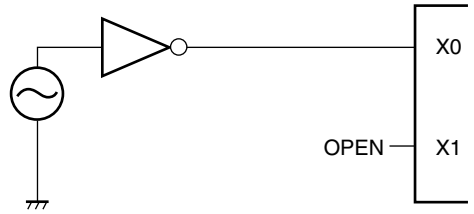
Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

3. About the attention when the external clock is used

Even when using an external clock signal, an oscillation stabilization delay is applied after a power-on reset or when recovering from sub-clock or stop mode. When suing an external clock, 25 MHz should be the upper frequency limit.

The following figure shows a sample use of external clock signals.

- Using external clock



4. Treatment of power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} pins near this device.

5. About crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator) , and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

6. Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

7. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. For stabilization reference, the supply voltage should be stabilized so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 MHz to 60 MHz) fall below 10% of the standard V_{CC} supply voltage and the transient regulation does not exceed 0.1 V/ms at temporary changes such as power supply switching.

8. Writing to flash memory

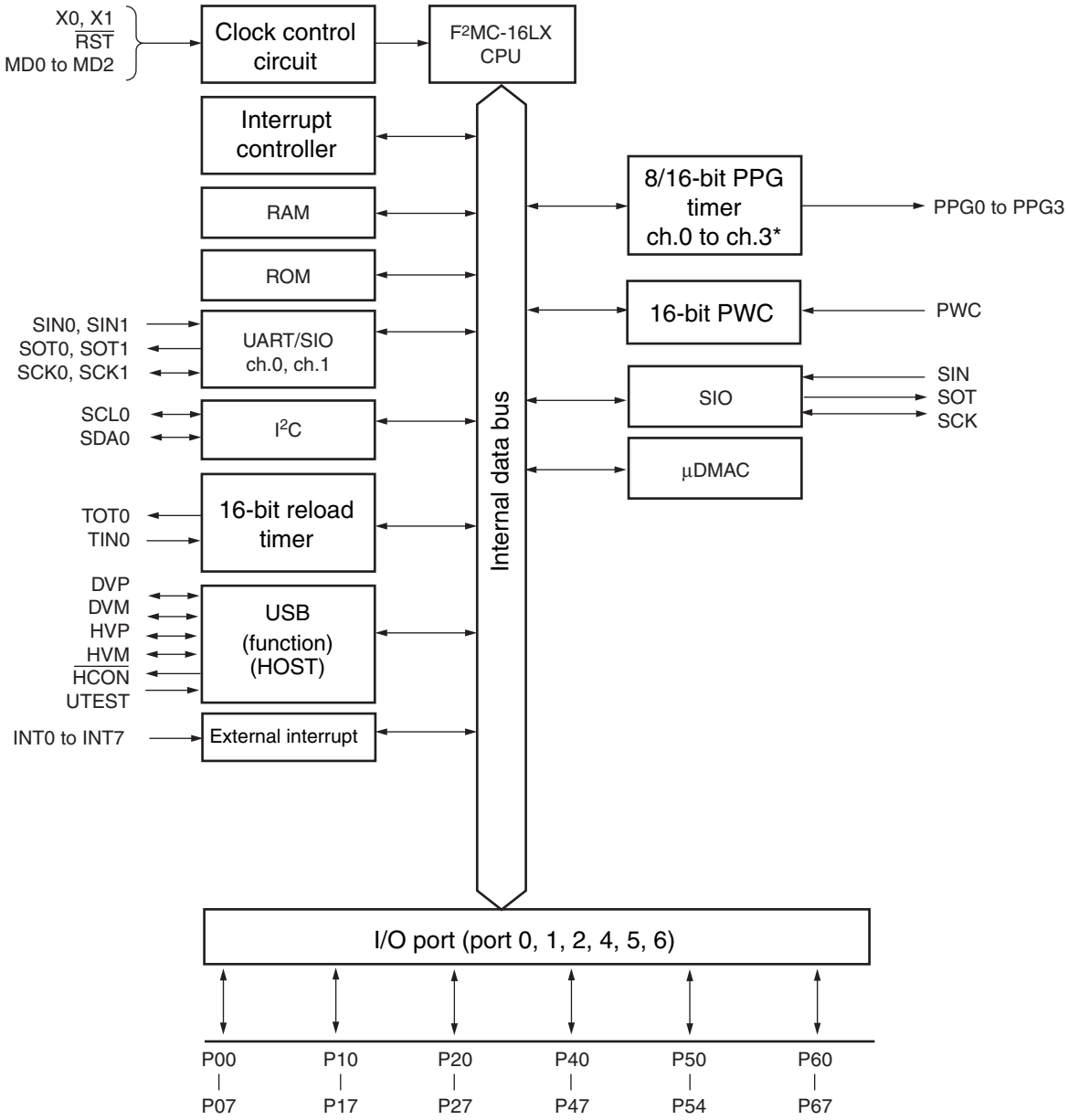
For serial writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.13 V and 3.6 V.

For normal writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

9. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

■ BLOCK DIAGRAM

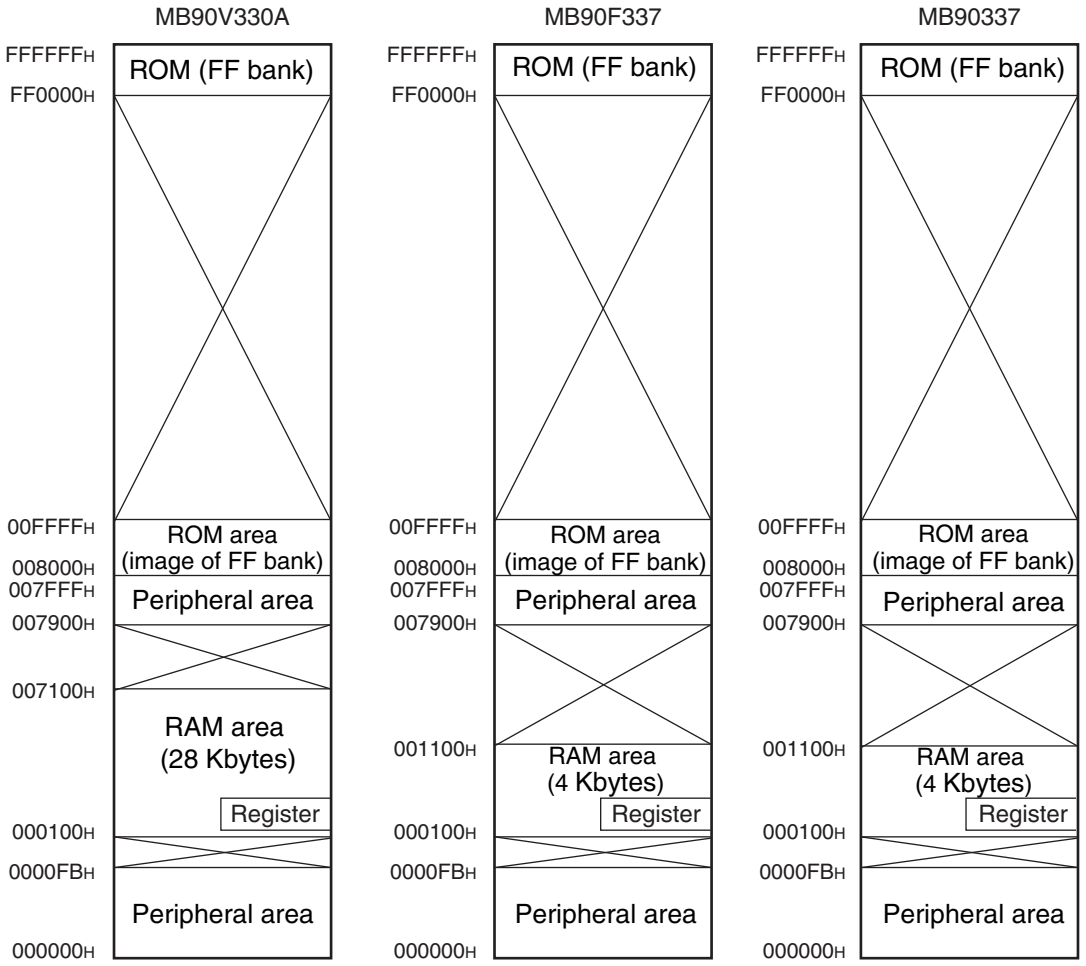


* : Channel for use in 8-bit mode. 2 channels (ch.1, ch.3) are used in 16-bit mode.

Note : I/O ports share pins with peripheral function (resources) .
For details, refer to “■ PIN ASSIGNMENT” and “■ PIN DESCRIPTION”.
Note also that pins used for peripheral function (resources) cannot serve as I/O ports.

■ MEMORY MAP

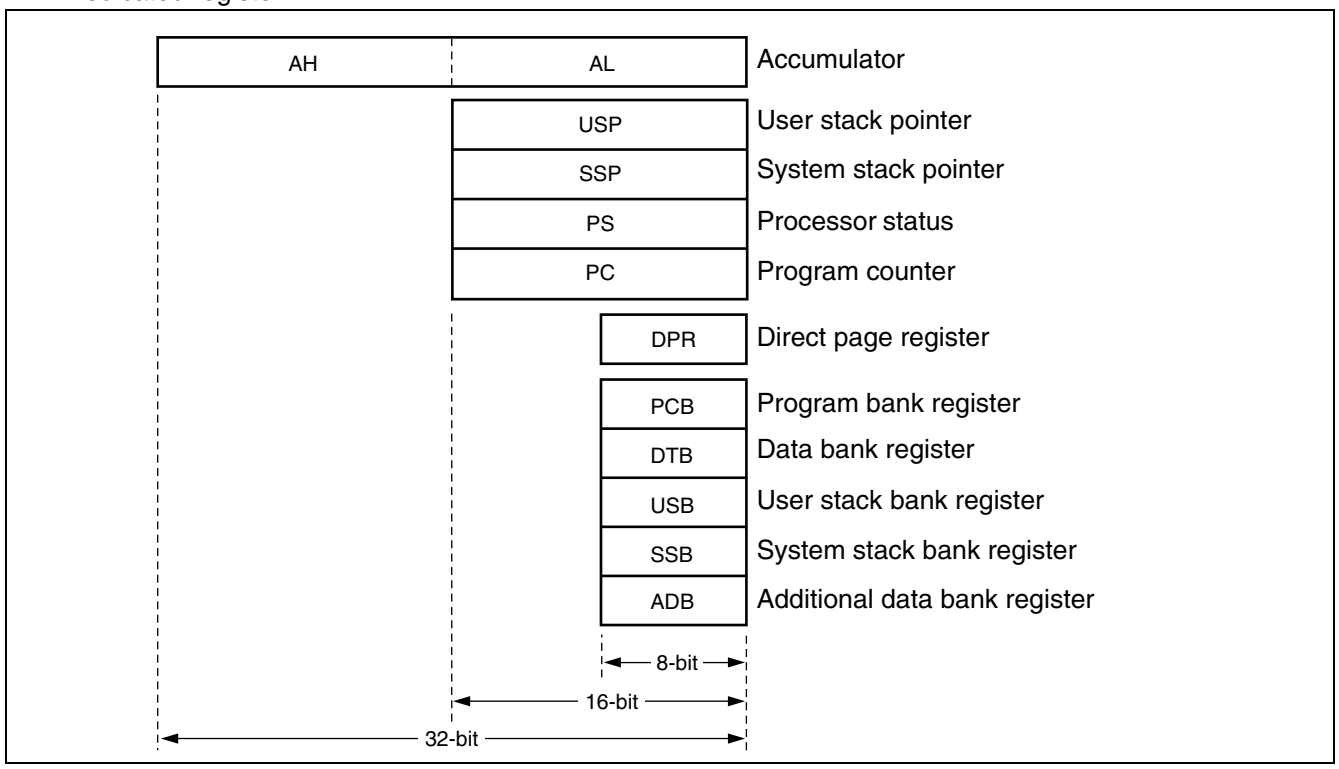
Single chip mode (with ROM mirror function)



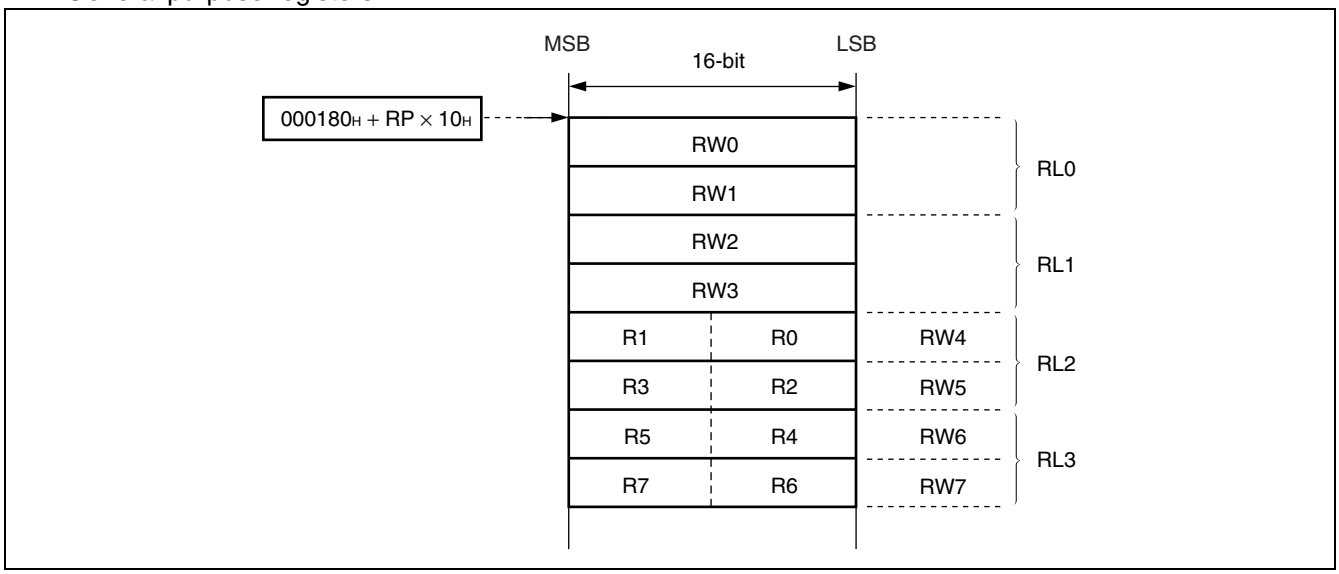
Notes :
- When the ROM mirror function register has been set, the mirror image data at higher addresses ("FF8000H to FFFFFFH") of bank FF is visible from the higher addresses ("008000H to 00FFFFH") of bank 00.
- The ROM mirror function is effective for using the C compiler small model.
- The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Since the ROM area in bank FF exceeds 48 Kbytes, however, the mirror image of all the data in the ROM area cannot be reproduced in bank 00.
- When the C compiler small model is used, the data table mirror image can be shown at "008000H to 00FFFFH" by storing the data table at "FF8000H to FFFFFFH".
  Therefore, data tables in the ROM area can be referred without declaring the far addressing with the pointer.

■ F²MC-16L CPU PROGRAMMING MODEL

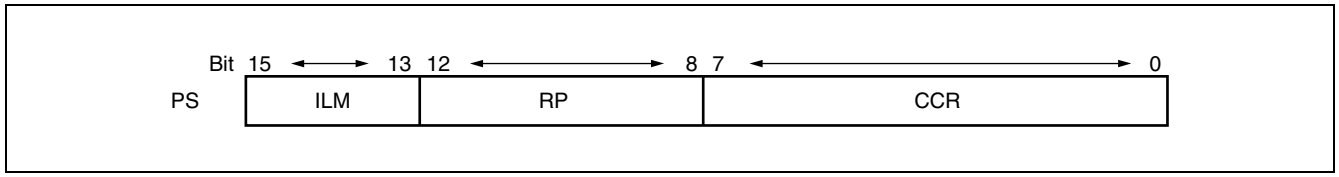
• Dedicated register



• General purpose registers



• Processor status



■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000000H	PDR0	Port 0 Data Register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 Data Register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 Data Register	R/W	Port 2	XXXXXXXXB
000003H	Prohibited				
000004H	PDR4	Port 4 Data Register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 Data Register	R/W	Port 5	- - - XXXXXB
000006H	PDR6	Port 6 Data Register	R/W	Port 6	XXXXXXXXB
000007H to 00000FH	Prohibited				
000010H	DDR0	Port 0 Direction Register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 Direction Register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 Direction Register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	Prohibited				
000014H	DDR4	Port 4 Direction Register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 Direction Register	R/W	Port 5	- - - 0 0 0 0 0B
000016H	DDR6	Port 6 Direction Register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H to 00001AH	Prohibited				
00001BH	ODR4	Port 4 Output Pin Register	R/W	Port 4 (Open-drain control)	0 0 0 0 0 0 0 0B
00001CH	RDR0	Port 0 Pull-up Resistance Register	R/W	Port 0 (PULL-UP)	0 0 0 0 0 0 0 0B
00001DH	RDR1	Port 1 Pull-up Resistance Register	R/W	Port 1 (PULL-UP)	0 0 0 0 0 0 0 0B
00001EH	Prohibited				
00001FH					
000020H	SMR0	Serial Mode Register 0	R/W	UART0	0 0 1 0 0 0 0 0B
000021H	SCR0	Serial Control Register 0	R/W		0 0 0 0 0 1 0 0B
000022H	SIDR0	Serial Input Data Register 0	R		XXXXXXXXB
	SODR0	Serial Output Data Register 0	W		
000023H	SSR0	Serial Status Register 0	R/W		0 0 0 0 1 0 0 0B
000024H	UTRLR0	UART Prescaler Reload Register 0	R/W	Communication Prescaler (UART0)	0 0 0 0 0 0 0 0B
000025H	UTCR0	UART Prescaler Control Register 0	R/W		0 0 0 0 - 0 0 0B
000026H	SMR1	Serial Mode Register 1	R/W	UART1	0 0 1 0 0 0 0 0B
000027H	SCR1	Serial Control Register 1	R/W		0 0 0 0 0 1 0 0B
000028H	SIDR1	Serial Input Data Register 1	R		XXXXXXXXB
	SODR1	Serial Output Data Register 1	W		
000029H	SSR1	Serial Status Register 1	R/W		0 0 0 0 1 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
00002A$_H$	UTRLR1	UART Prescaler Reload Register 1	R/W	Communication Prescaler (UART1)	0 0 0 0 0 0 0 0$_B$
00002B$_H$	UTCR1	UART Prescaler Control Register 1	R/W		0 0 0 0 - 0 0 0$_B$
00002C$_H$ to 00003B$_H$	Prohibited				
00003C$_H$	ENIR	DTP/Interrupt Enable Register	R/W	DTP/External interrupt	0 0 0 0 0 0 0 0$_B$
00003D$_H$	EIRR	DTP/Interrupt source Register	R/W		0 0 0 0 0 0 0 0$_B$
00003E$_H$	ELVR	Request Level Setting Register Lower	R/W		0 0 0 0 0 0 0 0$_B$
00003F$_H$		Request Level Setting Register Upper	R/W		0 0 0 0 0 0 0 0$_B$
000040$_H$ to 000045$_H$	Prohibited				
000046$_H$	PPGC0	PPG0 Operation Mode Control Register	R/W	PPG ch.0	0X0 0 0XX1$_B$
000047$_H$	PPGC1	PPG1 Operation Mode Control Register	R/W	PPG ch.1	0X0 0 0 0 0 1$_B$
000048$_H$	PPGC2	PPG2 Operation Mode Control Register	R/W	PPG ch.2	0X0 0 0XX1$_B$
000049$_H$	PPGC3	PPG3 Operation Mode Control Register	R/W	PPG ch.3	0X0 0 0 0 0 1$_B$
00004A$_H$	Prohibited				
00004B$_H$					
00004C$_H$	PPG01	PPG0 and PPG1 Output Control Register	R/W	PPG ch.0/ch.1	0 0 0 0 0 0XX$_B$
00004D$_H$	Prohibited				
00004E$_H$	PPG23	PPG2 and PPG3 Output Control Register	R/W	PPG ch.2/ch.3	0 0 0 0 0 0 XX$_B$
00004F$_H$ to 000057$_H$	Prohibited				
000058$_H$	SMCS	Serial Mode Control Status Register	R/W	Extended Serial I/O	XXXX0 0 0 0$_B$
000059$_H$					0 0 0 0 0 0 1 0$_B$
00005A$_H$	SDR	Serial Data Register	R/W		XXXXXXXX$_B$
00005B$_H$	SDCR	Communication Prescaler Control Register	R/W	Communication Prescaler	0XXX0 0 0 0$_B$
00005C$_H$	PWCSR	PWC Control Status Register	R/W	16-bit PWC Timer	0 0 0 0 0 0 0 0$_B$
00005D$_H$					0 0 0 0 0 0 0 X$_B$
00005E$_H$	PWCR	PWC Data Buffer Register	R/W		0 0 0 0 0 0 0 0$_B$
00005F$_H$					0 0 0 0 0 0 0 0$_B$
000060$_H$	DIVR	PWC Dividing Ratio Control Register	R/W		- - - - - - 0 0$_B$
000061$_H$	Prohibited				
000062$_H$	TMCSR0	Timer Control Status Register	R/W	16-bit Reload Timer	0 0 0 0 0 0 0 0$_B$
000063$_H$					XXXX 0 0 0 0$_B$
000064$_H$	TMR0	16-bit Timer Register Lower	R		XXXXXXXX$_B$
	TMRLR0	16-bit Reload Register Lower	W		XXXXXXXX$_B$
000065$_H$	TMR0	16-bit Timer Register Upper	R		XXXXXXXX$_B$
	TMRLR0	16-bit Reload Register Upper	W		XXXXXXXX$_B$

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000066H to 00006EH	Prohibited				
00006FH	ROMM	ROM Mirroring Function Selection Register	W	ROM Mirror Function Selection Module	- - - - - - 1 1B
000070H	IBSR0	I²C Bus Status Register	R	I²C Bus Interface	0 0 0 0 0 0 0 0B
000071H	IBCR0	I²C Bus Control Register	R/W		0 0 0 0 0 0 0 0B
000072H	ICCR0	I²C Bus Clock Control Register	R/W		XX 0 XXXXXB
000073H	IADR0	I²C Bus Address Register	R/W		XXXXXXXXB
000074H	IDAR0	I²C Bus Data Register	R/W		XXXXXXXXB
000075H to 00009AH	Prohibited				
00009BH	DCSR	DMA Descriptor Channel Specification Register	R/W	µDMAC	0 0 0 0 0 0 0 0B
00009CH	DSRL	DMA Status Register Lower	R/W		0 0 0 0 0 0 0 0B
00009DH	DSRH	DMA Status Register Upper	R/W		0 0 0 0 0 0 0 0B
00009EH	PACSR	Program Address Detection Control Status Register	R/W	Address Match Detection	0 0 0 0 0 0 0 0B
00009FH	DIRR	Delayed Interrupt Source generate/ release Register	R/W	Delayed Interrupt	- - - - - - - 0B
0000A0H	LPMCR	Low Power Consumption Mode Control Register	R/W	Low Power Consumption control circuit	0 0 0 1 1 0 0 0B
0000A1H	CKSCR	Clock Selection Register	R/W	Clock	1 1 1 1 1 1 0 0B
0000A2H	Prohibited				
0000A3H					
0000A4H	DSSR	DMA Stop Status Register	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000A5H to 0000A7H	Prohibited				
0000A8H	WDTC	Watchdog Timer Control Register	R/W	Watchdog Timer	X - XXX 1 1 1B
0000A9H	TBTC	Time-base Timer Control Register	R/W	Time-base Timer	1 - - 0 0 1 0 0B
0000AAH	Prohibited				
0000ABH					
0000ACH	DERL	DMA Enable Register Lower	R/W	µDMAC	0 0 0 0 0 0 0 0B
0000ADH	DERH	DMA Enable Register Upper	R/W		0 0 0 0 0 0 0 0B
0000AEH	FMCS	Flash Memory Control Status Register	R/W	Flash Memory I/F	0 0 0 X 0 0 0 0B
0000AFH	Prohibited				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000B0H	ICR00	Interrupt Control Register 00	R/W	Interrupt Controller	0 0 0 0 0 1 1 1B
0000B1H	ICR01	Interrupt Control Register 01	R/W		0 0 0 0 0 1 1 1B
0000B2H	ICR02	Interrupt Control Register 02	R/W		0 0 0 0 0 1 1 1B
0000B3H	ICR03	Interrupt Control Register 03	R/W		0 0 0 0 0 1 1 1B
0000B4H	ICR04	Interrupt Control Register 04	R/W		0 0 0 0 0 1 1 1B
0000B5H	ICR05	Interrupt Control Register 05	R/W		0 0 0 0 0 1 1 1B
0000B6H	ICR06	Interrupt Control Register 06	R/W		0 0 0 0 0 1 1 1B
0000B7H	ICR07	Interrupt Control Register 07	R/W		0 0 0 0 0 1 1 1B
0000B8H	ICR08	Interrupt Control Register 08	R/W		0 0 0 0 0 1 1 1B
0000B9H	ICR09	Interrupt Control Register 09	R/W		0 0 0 0 0 1 1 1B
0000BAH	ICR10	Interrupt Control Register 10	R/W		0 0 0 0 0 1 1 1B
0000BBH	ICR11	Interrupt Control Register 11	R/W		0 0 0 0 0 1 1 1B
0000BCH	ICR12	Interrupt Control Register 12	R/W		0 0 0 0 0 1 1 1B
0000BDH	ICR13	Interrupt Control Register 13	R/W		0 0 0 0 0 1 1 1B
0000BEH	ICR14	Interrupt Control Register 14	R/W		0 0 0 0 0 1 1 1B
0000BFH	ICR15	Interrupt Control Register 15	R/W		0 0 0 0 0 1 1 1B
0000C0H	HCNT0	Host Control Register 0	R/W	USB HOST	0 0 0 0 0 0 0 0B
0000C1H	HCNT1	Host Control Register 1	R/W		0 0 0 0 0 0 0 1B
0000C2H	HIRQ	Host Interruption Register	R/W		0 0 0 0 0 0 0 0B
0000C3H	HERR	Host Error Status Register	R/W		0 0 0 0 0 0 1 1B
0000C4H	HSTATE	Host State Status Register	R/W		XX 0 1 0 0 1 0B
0000C5H	HFCOMP	SOF Interrupt FRAME Compare Register	R/W		0 0 0 0 0 0 0 0B
0000C6H	HRTIMER	Retry Timer Setting Register	R/W		0 0 0 0 0 0 0 0B
0000C7H			R/W		0 0 0 0 0 0 0 0B
0000C8H			R/W		XXXXXX 0 0B
0000C9H	HADR	Host Address Register	R/W		X 0 0 0 0 0 0 0B
0000CAH	HEOF	EOF Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CBH			R/W		XX 0 0 0 0 0 0B
0000CCH	HFRAME	FRAME Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CDH			R/W		XXXXX 0 0 0B
0000CEH	HTOKEN	Host Token End Point Register	R/W		0 0 0 0 0 0 0 0B
0000CFH	Prohibited				
0000D0H	UDCC	UDC Control Register	R/W	USB Function	1 0 1 0 0 0 0 0B
0000D1H			R/W		0 0 0 0 0 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000D2H	EP0C	EP0 Control Register	R/W	USB Function	0 1 0 0 0 0 0 0B
0000D3H			R/W		XXXX 0 0 0 0B
0000D4H	EP1C	EP1 Control Register	R/W		0 0 0 0 0 0 0 0B
0000D5H			R/W		0 1 1 0 0 0 0 1B
0000D6H	EP2C	EP2 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D7H			R/W		0 1 1 0 0 0 0 0B
0000D8H	EP3C	EP3 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D9H			R/W		0 1 1 0 0 0 0 0B
0000DAH	EP4C	EP4 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DBH			R/W		0 1 1 0 0 0 0 0B
0000DCH	EP5C	EP5 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DDH			R/W		0 1 1 0 0 0 0 0B
0000DEH	TMSP	Time Stamp Register	R		0 0 0 0 0 0 0 0B
0000DFH			R		XXXXX0 0 0B
0000E0H	UDCS	UDC Status Register	R/W		XX0 0 0 0 0 0B
0000E1H	UDCIE	UDC Interrupt Enable Register	R/W		0 0 0 0 0 0 0 0B
0000E2H	EP0IS	EP0I Status Register	R/W		XXXXXXXXB
0000E3H			R/W		1 0 XXX 1 XXB
0000E4H	EP0OS	EP0O Status Register	R/W, R		0 XXXXXXXB
0000E5H			R/W		1 0 0 XX 0 0 0B
0000E6H	EP1S	EP1 Status Register	R		XXXXXXXXB
0000E7H			R/W		1 0 0 0 0 0 0 XB
0000E8H	EP2S	EP2 Status Register	R		XXXXXXXXB
0000E9H			R/W		1 0 0 0 0 0 0 0B
0000EAH	EP3S	EP3 Status Register	R		XXXXXXXXB
0000EBH			R/W		1 0 0 0 0 0 0 0B
0000ECH	EP4S	EP4 Status Register	R		XXXXXXXXB
0000EDH			R/W		1 0 0 0 0 0 0 0B
0000EEH	EP5S	EP5 Status Register	R		XXXXXXXXB
0000EFH			R/W		1 0 0 0 0 0 0 0B
0000F0H	EP0DT	EP0 Data Register	R/W		XXXXXXXXB
0000F1H			R/W		XXXXXXXXB
0000F2H	EP1DT	EP1 Data Register	R/W		XXXXXXXXB
0000F3H			R/W		XXXXXXXXB
0000F4H	EP2DT	EP2 Data Register	R/W		XXXXXXXXB
0000F5H			R/W		XXXXXXXXB
0000F6H	EP3DT	EP3 Data Register	R/W		XXXXXXXXB
0000F7H			R/W		XXXXXXXXB
0000F8H	EP4DT	EP4 Data Register	R/W		XXXXXXXXB
0000F9H			R/W		XXXXXXXXB

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000FA$_H$	EP5DT	EP5 Data Register	R/W	USB Function	XXXXXXXX$_B$
0000FB$_H$			R/W		XXXXXXXX$_B$
0000FC$_H$ to 0000FF$_H$	Prohibited				
000100$_H$ to 001100$_H$	RAM Area				
001FF0$_H$	PADR0	Program Address Detection Register ch.0 Lower	R/W	Address Match Detection	XXXXXXXX$_B$
001FF1$_H$		Program Address Detection Register ch.0 Middle	R/W		XXXXXXXX$_B$
001FF2$_H$		Program Address Detection Register ch.0 Upper	R/W		XXXXXXXX$_B$
001FF3$_H$	PADR1	Program Address Detection Register ch.1 Lower	R/W		XXXXXXXX$_B$
001FF4$_H$		Program Address Detection Register ch.1 Middle	R/W		XXXXXXXX$_B$
001FF5$_H$		Program Address Detection Register ch.1 Upper	R/W		XXXXXXXX$_B$
007900$_H$	PRLL0	PPG Reload Register Lower ch.0	R/W	PPG ch.0	XXXXXXXX$_B$
007901$_H$	PRLH0	PPG Reload Register Upper ch.0	R/W		XXXXXXXX$_B$
007902$_H$	PRLL1	PPG Reload Register Lower ch.1	R/W	PPG ch.1	XXXXXXXX$_B$
007903$_H$	PRLH1	PPG Reload Register Upper ch.1	R/W		XXXXXXXX$_B$
007904$_H$	PRLL2	PPG Reload Register Lower ch.2	R/W	PPG ch.2	XXXXXXXX$_B$
007905$_H$	PRLH2	PPG Reload Register Upper ch.2	R/W		XXXXXXXX$_B$
007906$_H$	PRLL3	PPG Reload Register Lower ch.3	R/W	PPG ch.3	XXXXXXXX$_B$
007907$_H$	PRLH3	PPG Reload Register Upper ch.3	R/W		XXXXXXXX$_B$
007908$_H$ to 00790B$_H$	Prohibited				
00790C$_H$	FWR0	Flash Memory Program Control Register 0	R/W	Flash	0 0 0 0 0 0 0 0$_B$
00790D$_H$	FWR1	Flash Memory Program Control Register 1	R/W	Flash	0 0 0 0 0 0 0 0$_B$
00790E$_H$	SSR0	Sector Conversion Setting Register	R/W	Flash	0 0 XXXXX0$_B$
00790F$_H$ to 00791F$_H$	Prohibited				

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Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
007920H	DBAPL	DMA Buffer Address Pointer Lower 8-bit	R/W	μDMAC	XXXXXXXXB
007921H	DBAPM	DMA Buffer Address Pointer Middle 8-bit	R/W		XXXXXXXXB
007922H	DBAPH	DMA Buffer Address Pointer Upper 8-bit	R/W		XXXXXXXXB
007923H	DMACS	DMA Control Register	R/W		XXXXXXXXB
007924H	DIOAL	DMA I/O Register Address Pointer Lower 8-bit	R/W		XXXXXXXXB
007925H	DIOAH	DMA I/O Register Address Pointer Upper 8-bit	R/W		XXXXXXXXB
007926H	DDCTL	DMA Data Counter Lower 8-bit	R/W		XXXXXXXXB
007927H	DDCTH	DMA Data Counter Upper 8-bit	R/W		XXXXXXXXB
007928H to 007FFFH	Prohibited				

- Explanation on read/write
  R/W : Readable and Writable
  R : Read only
  W : Write only

- Explanation of initial values
  0 : Initial value is “0”.
  1 : Initial value is “1”.
  X : Initial value is undefined.
  - : Initial value is undefined (None).

Note : No I/O instruction can be used for registers located between 007900H and 007FFFH.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS support	μDMAC	Interrupt vector			Interrupt control register		Priority
			Number*1		Address	ICR	Address	
Reset	×	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	×	#09	09H	FFFFD8H	—	—	
Exceptional treatment	×	×	#10	0AH	FFFFD4H	—	—	
USB Function1	×	0, 1	#11	0BH	FFFFD0H	ICR00	0000B0H	
USB Function2	×	2 to 6*2	#12	0CH	FFFFCCH			
USB Function3	×	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
USB Function4	×	×	#14	0EH	FFFFC4H			
USB HOST1	×	×	#15	0FH	FFFFC0H	ICR02	0000B2H	
USB HOST2	×	×	#16	10H	FFFFBCH			
I²C ch.0	×	×	#17	11H	FFFFB8H	ICR03	0000B3H	
DTP/External interrupt ch.0/ch.1	○	×	#18	12H	FFFFB4H			
No	—	—	#19	13H	FFFFB0H	ICR04	0000B4H	
DTP/External interrupt ch.2/ch.3	○	×	#20	14H	FFFFACH			
No	—	—	#21	15H	FFFFA8H	ICR05	0000B5H	
DTP/External interrupt ch.4/ch.5	○	×	#22	16H	FFFFA4H			
PWC/Reload timer ch.0	△	14	#23	17H	FFFFA0H	ICR06	0000B6H	
DTP/External interrupt ch.6/ch.7	△	×	#24	18H	FFFF9CH			
No	—	—	#25	19H	FFFF98H	ICR07	0000B7H	
No	—	—	#26	1AH	FFFF94H			
No	—	—	#27	1BH	FFFF90H	ICR08	0000B8H	
No	—	—	#28	1CH	FFFF8CH			
No	—	—	#29	1DH	FFFF88H	ICR09	0000B9H	
PPG ch.0/ch.1	×	×	#30	1EH	FFFF84H			
No	—	—	#31	1FH	FFFF80H	ICR10	0000BAH	
PPG ch.2/ch.3	×	×	#32	20H	FFFF7CH			
No	—	—	#33	21H	FFFF78H	ICR11	0000BBH	
No	—	—	#34	22H	FFFF74H			
No	—	—	#35	23H	FFFF70H	ICR12	0000BCH	
No	—	—	#36	24H	FFFF6CH			
UART (Send completed) ch.0/ch.1	○	13	#37	25H	FFFF68H	ICR13	0000BDH	
Extended serial I/O	×	9	#38	26H	FFFF64H			
UART(Reception completed) ch.0/ch.1	◎	12	#39	27H	FFFF60H	ICR14	0000BEH	
Time-base timer	×	×	#40	28H	FFFF5CH			
Flash memory status	×	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delay interrupt output module	×	×	#42	2AH	FFFF54H			Low

(Continued)

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◎ : Available. EI²OS stop function provided (The interrupt request flag is cleared by the interrupt clear signal. With a stop request).
○ : Available (The interrupt request flag is cleared by the interrupt clear signal).
△ : Available when any interrupt source sharing ICR is not used.
× : Unavailable

*1 : If the same level interrupt is output simultaneously, the lower interrupt factor of interrupt vector number has priority.

*2 : Ch.2 and ch.3 can be used in USB HOST operation.

Notes :
- If the same interrupt control register (ICR) has two interrupt factors and the use of the EI²OS is permitted, the EI²OS is activated when either of the factors is detected. As any interrupt other than the activation factor is masked while the EI²OS is running, it is recommended that you should mask either of the interrupt requests when using the EI²OS.
- The interrupt flag is cleared by the EI²OS interrupt clear signal for the resource that has two interrupt factors in the same interrupt control register (ICR).
- If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the μDMAC interrupt clear signal. Therefore, when you use either of two interrupt factors for the DMAC function, another interrupt function is disabled. Set the interrupt request permission bit to " 0 " in the appropriate resource, and take measures by software polling.

■ CONTENT OF USB INTERRUPTION FACTOR

USB interrupt factor	Details
USB function 1	End Point 0-IN, End Point 0-OUT
USB function 2	End Point 1-5 *
USB function 3	SUSP, SOF, BRST, WKOP, COHF
USB function 4	SPIT
USB HOST1	DIRQ, CHHIRQ, URIRQ, RWKIRQ
USB HOST2	SOFIRQ, CMPIRQ

* : End Point 1and 2 can be used in USB HOST operation.

■ USB

1. USB Function

The USB function is an interface supporting the USB (Universal Serial Bus) communications protocol.

Features of USB function

- Supports USB Full Speed
- Supports full speed (12 Mbps).
- The device status is auto-answer.
- Bit stripping, bit stuffing, and automatic generation and check of CRC5 and CRC16.
- Toggle check by data synchronization bit.
- Automatic response to all standard commands except Get/SetDescriptor and SynchFrame commands (these three commands can be processed the same way as the class vendor commands).
- The class vendor commands can be received as data and responded via firmware.
- Supports up to a maximum of six EndPoints (EndPoint0 is fixed to control transfer).
- Two built-in transfer data buffers for each end point (one IN buffer and one OUT buffer for end point 0).
- Supports automatic transfer mode for transfer data via DMA (except buffers for EndPoint0).