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# F<sup>2</sup>MC-16LX 16-bit Microcontroller Datasheet

The MB90340E series with up to 2 FULL-CAN interfaces is especially designed for automotive and other industrial applications. Its main feature are the on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The power to the MCU core (3 V) is supplied by a built-in regulator circuit, giving these microcontrollers superior performance in terms of power consumption and tolerance to EMI.

## Features

### CPU

- Instruction system best suited to controller
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced functionality with signed multiply and divide instructions and the RETI instruction
  - Enhanced high-precision computing with 32-bit accumulator
- Instruction system compatible with high-level language (C language) and multitask
  - Employing system stack pointer
  - Various enhanced pointer indirect instructions
  - Barrel shift instructions
- Increased processing speed
  - 4-byte instruction queue

### Serial interface

- LIN-UART : 4 channels
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
- I<sup>2</sup>C interface : 2 channels (only for devices with a C suffix in the part number)
  - Up to 400 kbps transfer rate

### Interrupt controller

- Powerful 8-level, 34-condition interrupt feature
- Up to 16 external interrupts are supported
- Automatic data transfer function independent of CPU
  - Expanded intelligent I/O service function (EI<sup>2</sup>OS) : up to 16 channels

### I/O ports

- General-purpose input/output port (CMOS output)
  - 80 ports (for devices without an S suffix in the part number - i.e. devices that support the sub clock)
  - 82 ports (for devices with an S suffix in the part number - i.e. devices that do not support the sub clock)

### 8/10-bit A/D converter

- 16 channels (only for devices without a C suffix in the part number)
- 24 channels (only for devices with a C suffix in the part number)

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3  $\mu$ s (at 24 MHz machine clock, including sampling time)

### Address match detection (program patch) function

- Detects address matches against 6 address pointers

### Timer

- Time-base timer, watch timer, watchdog timer : 1 channel
- 8/16-bit PPG timer : 8-bit  $\times$  16 channels, or 16-bit  $\times$  8 channels
- 16-bit reload timer : 4 channels
- 16-bit input/output timer
  - 16-bit free-run timer : 2 channels (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
  - 16-bit input capture: (ICU): 8 channels
  - 16-bit output compare: (OCU): 8 channels

### Full-CAN controller

- Up to 2 channels
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 16 built-in message buffers
- CAN wake-up function

### Low power consumption (standby) mode

- Sleep mode (a mode that halts CPU operating clock)
- Timebase timer mode (a mode where only the oscillation clock, sub clock, timebase timer and watch timer operate)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode

### Clock modulation circuit

### Technology

- CMOS technology

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**1. Product Lineup**

Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Parameter			
Type	Evaluation products	Flash memory products	MASK ROM products
CPU	F <sup>2</sup> MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	External	512 Kbytes : MB90F345E(S), MB90F345CE(S) 256 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 128 Kbytes : MB90F347E(S), MB90F347CE(S) 64 Kbytes : MB90F346E(S), MB90F346CE(S)	256 Kbytes : MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S) 128 Kbytes : MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S) 64 Kbytes : MB90346E(S), MB90346CE(S)
RAM	30 Kbytes	20 Kbytes : MB90F345E(S), MB90F345CE(S) 16 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 6 Kbytes : MB90F347E(S), MB90F347CE(S) 2 Kbytes : MB90F346E(S), MB90F346CE(S)	16 Kbytes : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) 6 Kbytes : MB90347E(S), MB90347CE(S) 2 Kbytes : MB90346E(S), MB90346CE(S)
Emulator-specific power supply*	Yes	—	
Technology	0.35 μm CMOS with regulator for built-in power supply	0.35 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%	3.5 V to 5.5 V : When normal operating (not using A/D converter) 4.0 V to 5.5 V : When using the A/D converter/Flash programming 4.5 V to 5.5 V : When using the external bus	
Temperature range	—	-40°C to +105°C	
Package	PGA-299	QFP-100, LQFP-100	
LIN-UART	5 channels	4 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I <sup>2</sup> C (400 kbps)	2 channels	Devices with a C suffix in the part number : 2 channels Devices without a C suffix in the part number : —	

*(Continued)*

Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Parameter			
A/D Converter	24 input channels	Devices with a C suffix in the part number : 24 channels Devices without a C suffix in the part number : 16 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 $\mu$ s include sample time (per one channel)		
16-bit Reload Timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$ , $f_{sys}/2^3$ , $f_{sys}/2^5$ ( $f_{sys}$ = Machine clock frequency) Supports External Event Count function		
16-bit Free-run Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ , $f_{sys}/2^5$ , $f_{sys}/2^6$ , $f_{sys}/2^7$ ( $f_{sys}$ = Machine clock freq.) Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit free-run timer matches the output compare register A pair of compare registers can be used to generate an output signal.		
16-bit Input Capture (8 channels)	Captures the value of the 16-bit free-run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges).		
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width		
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ or 128 $\mu$ s@ $f_{osc}$ = 4 MHz ( $f_{sys}$ = Machine clock frequency, $f_{osc}$ = Oscillation clock frequency)		
CAN Interface	3 channels	2 channels : MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S) 1 channel : MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	2 channels : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S) 1 channel : MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		

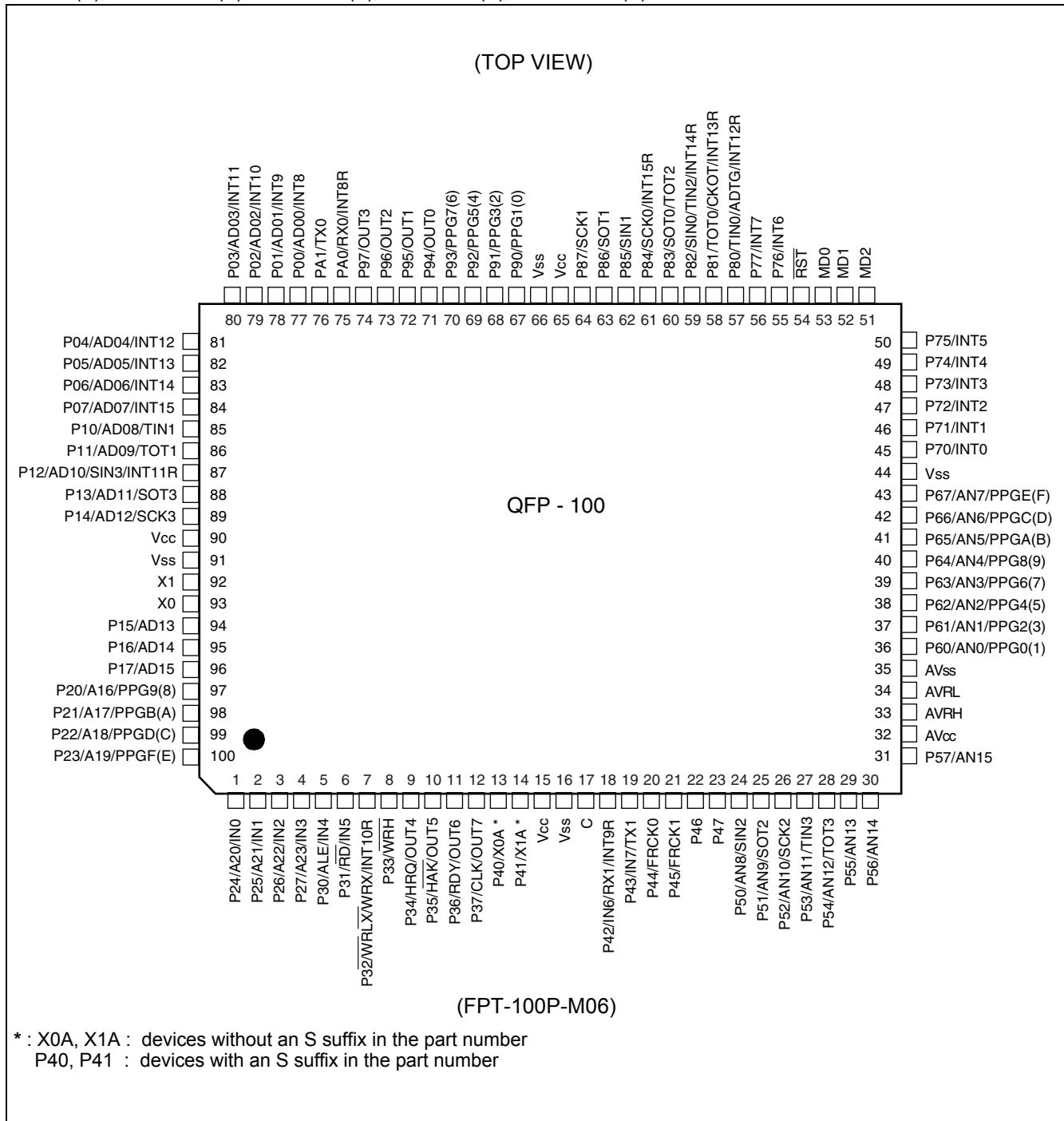
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Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
External Interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI <sup>2</sup> OS) and DMA		
D/A Converter	2 channels	—	
Sub clock (maximum 100 kHz)	Only for MB90V340E-102	Devices with sub clock : devices without an S suffix in the part number Devices without sub clock : devices with an S suffix in the part number	
I/O Ports	Virtually all external pins can be used as general purpose I/O port All ports are push-pull outputs Bit-wise settable as input/output or peripheral signal Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins) TTL input level settable for external bus (32-pin only for external bus)		
Flash Memory	—	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 cycles Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (except for MB90F346E(S) and MB90F346CE (S) )	

\* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01-E) is used.  
Please refer to the Emulator operation manual for details.

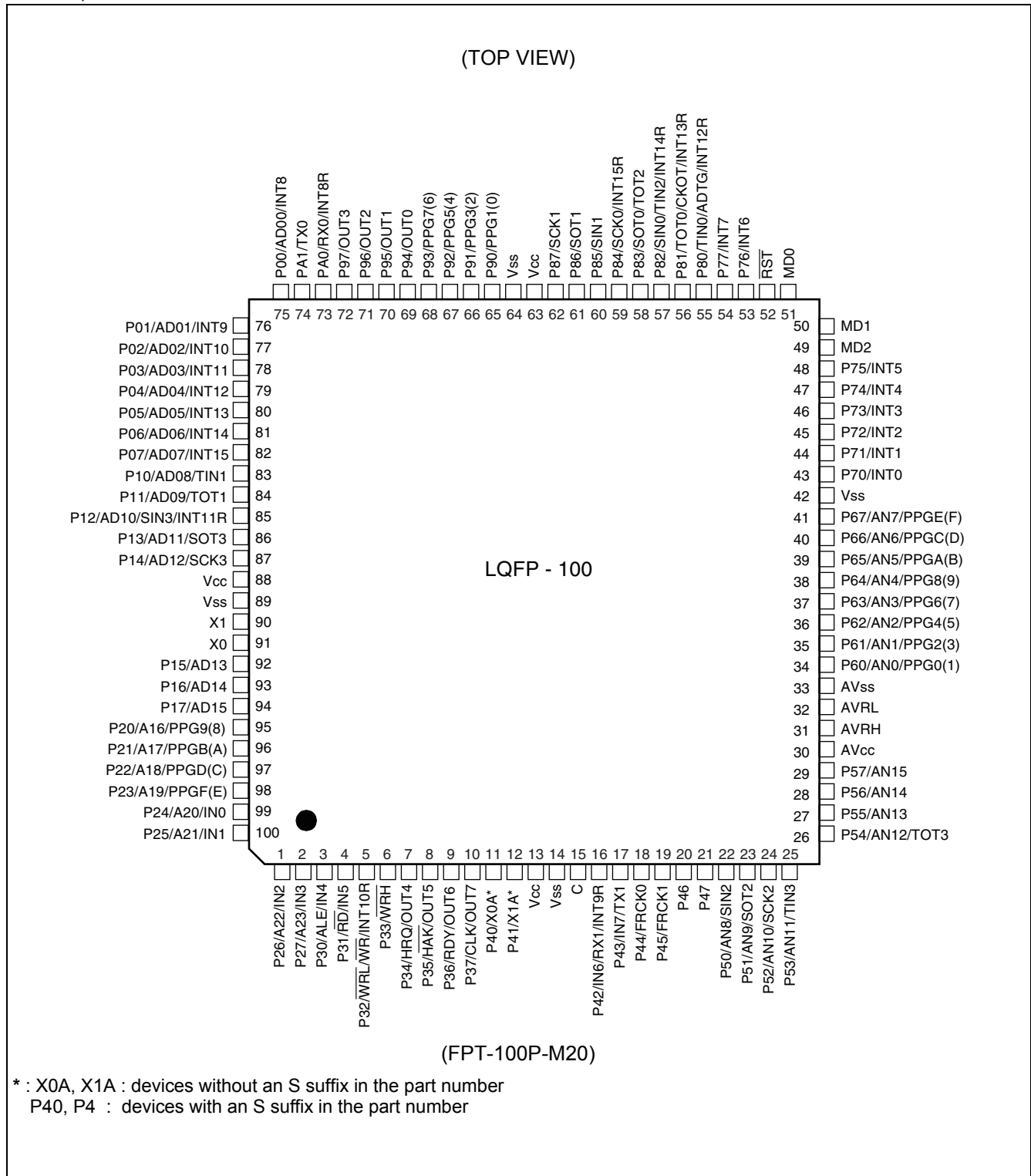
## 2. Pin Assignments

- MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)



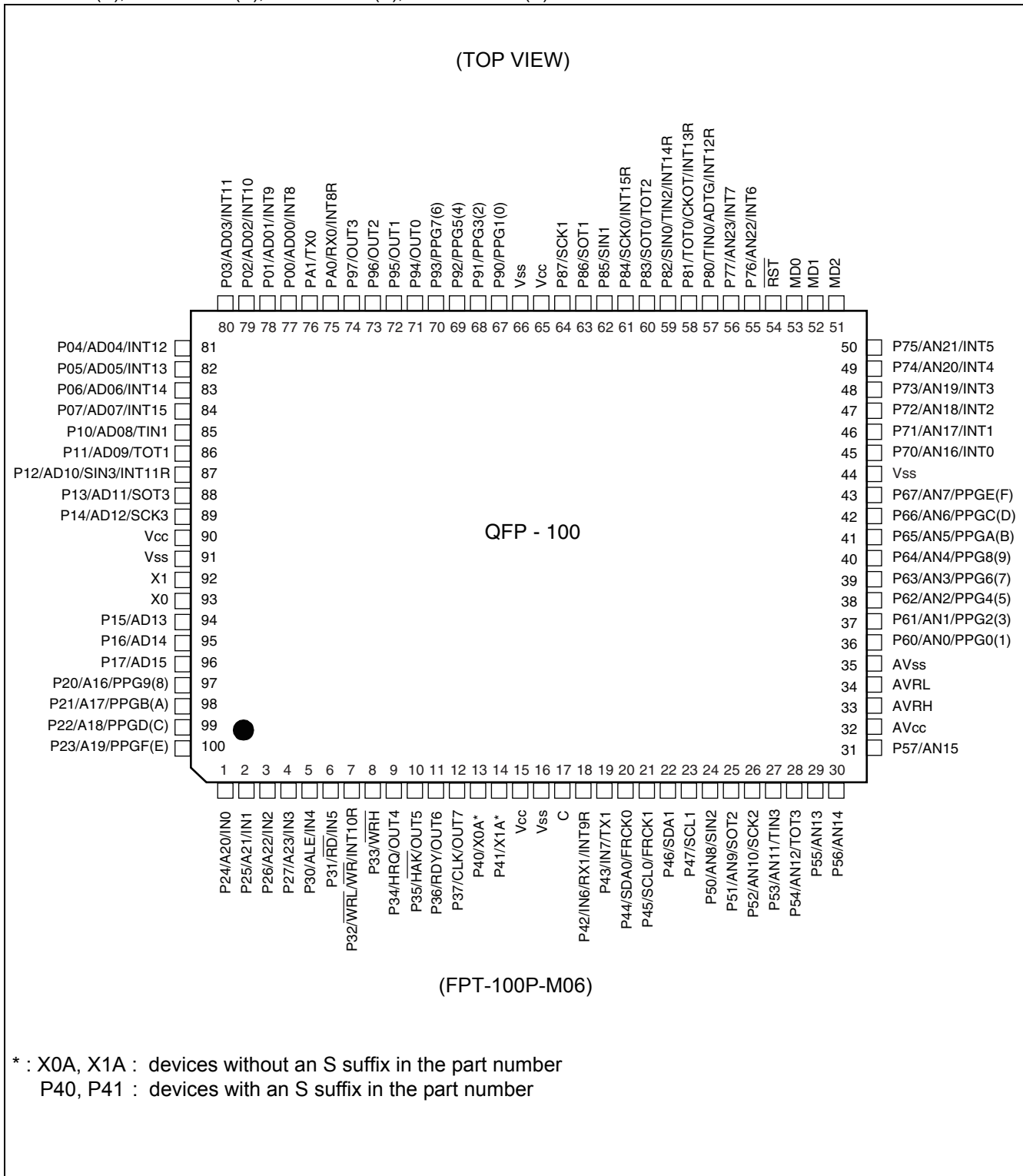
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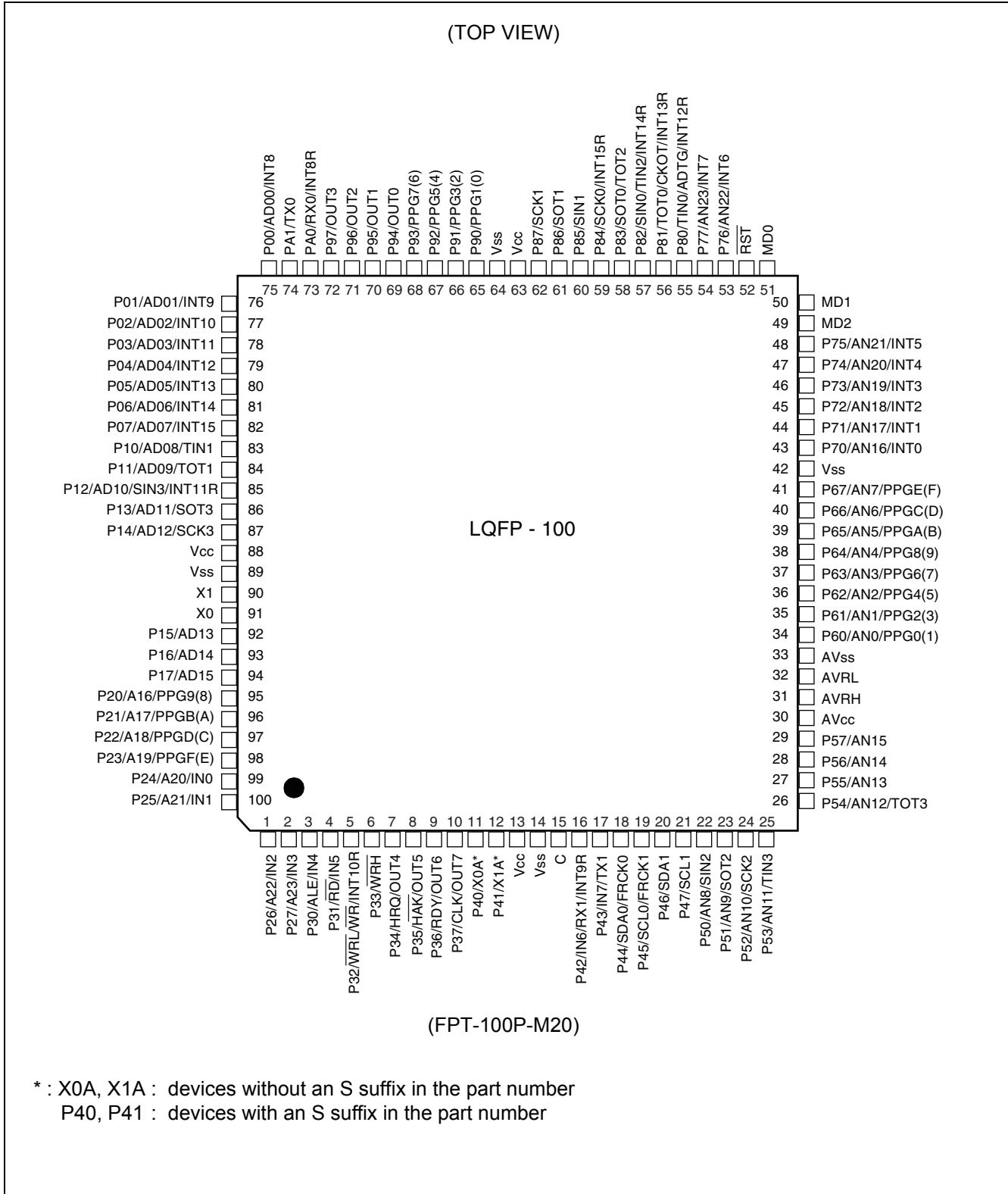


■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)

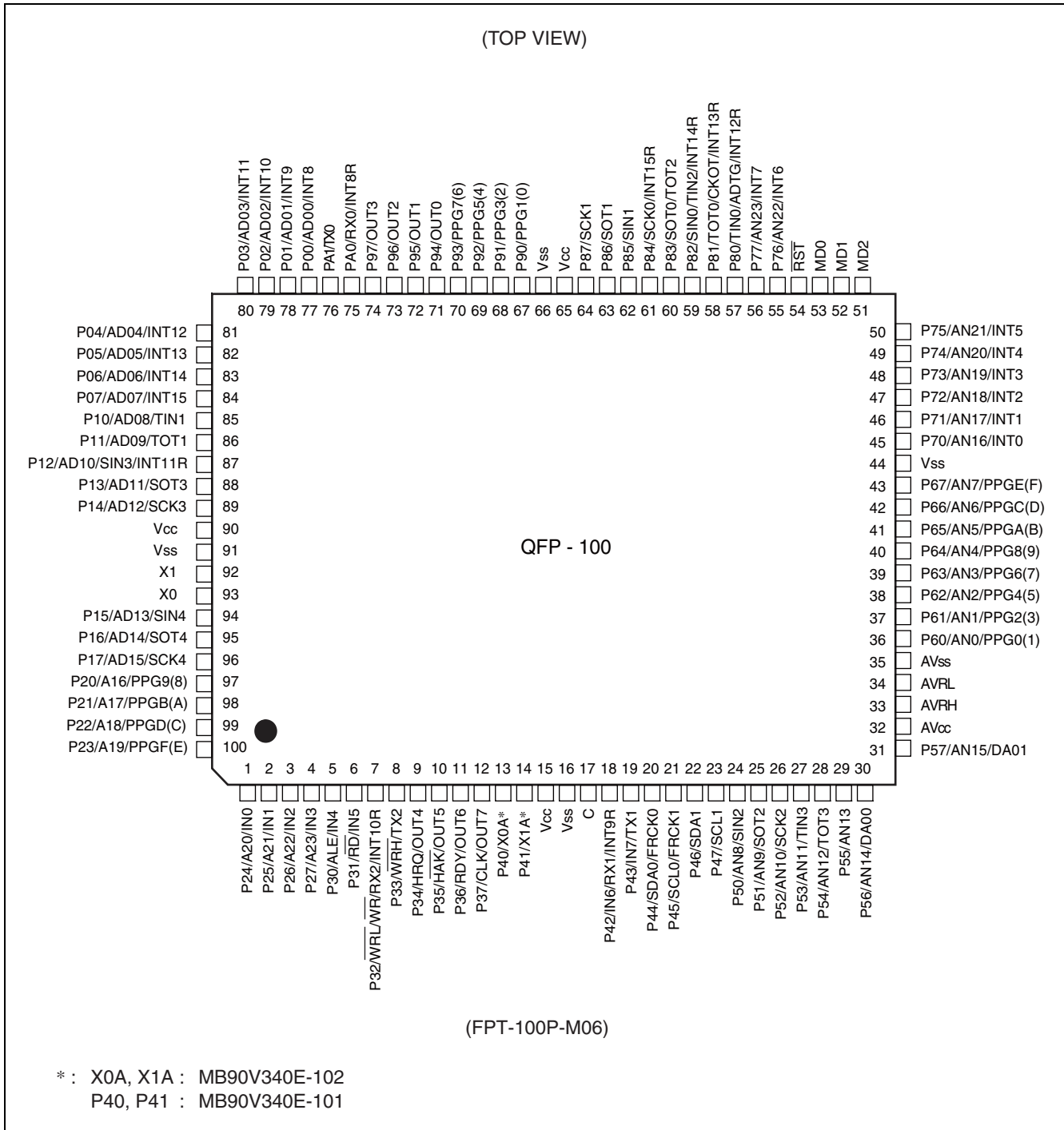


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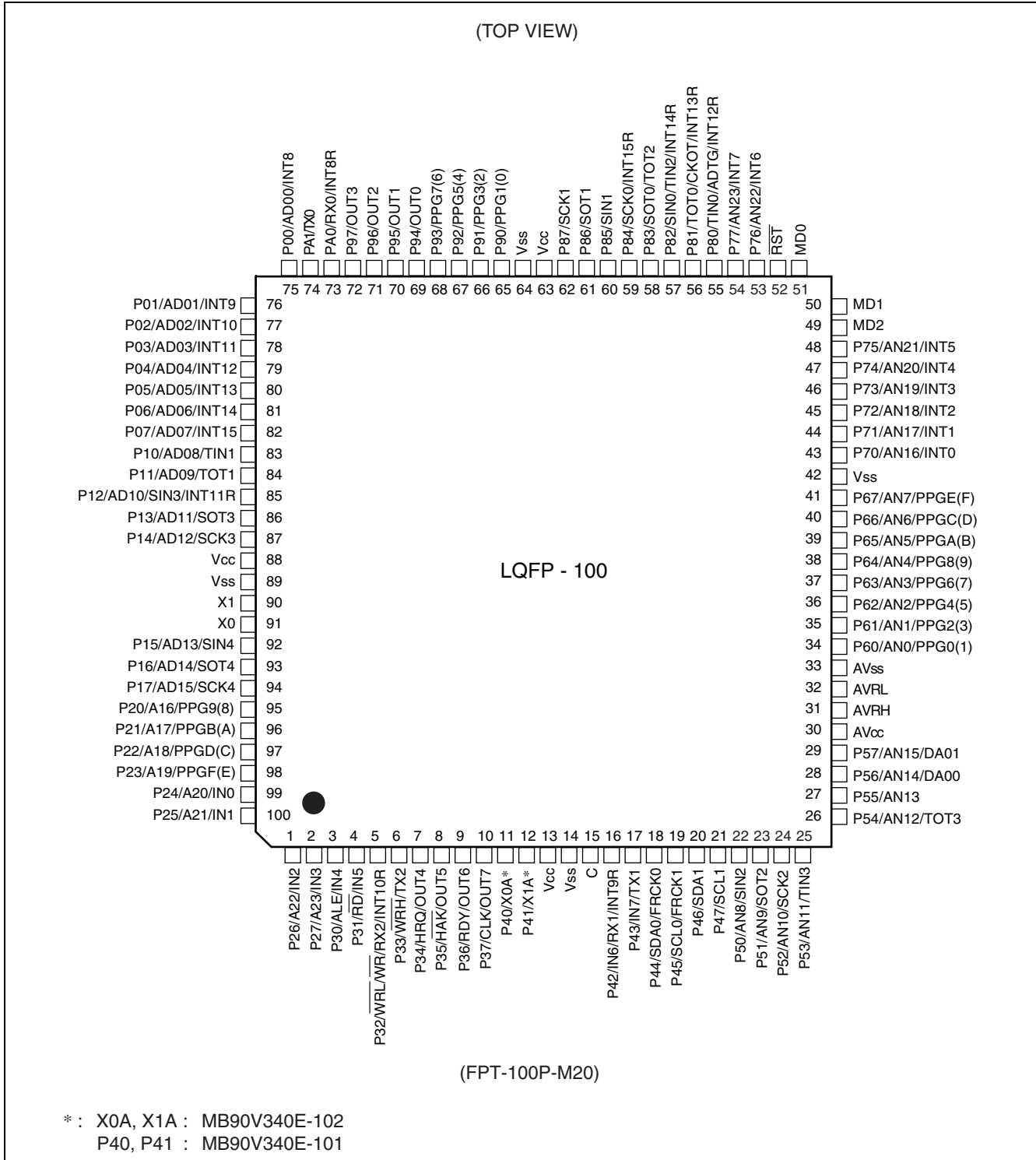
■ MB90V340E-101/MB90V340E-102



This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

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This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

### 3. Pin Description

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures.
5	3	P30	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture.
6	4	P31	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WR/WRL}$ pin output is disabled.
		$\overline{WR} / \overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR/WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin.
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WRH}$ pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
16	14	V <sub>SS</sub>	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 $\mu\text{F}$ .
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV <sub>CC</sub>	K	Analog power input pin for the A/D Converter

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV <sub>CC</sub> .
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV <sub>SS</sub>	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V <sub>SS</sub>	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	RST	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

(Continued)



Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
66	64	V <sub>SS</sub>	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
91	89	V <sub>SS</sub>	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

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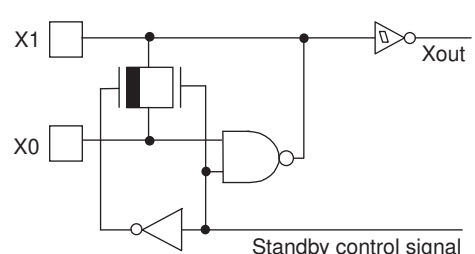
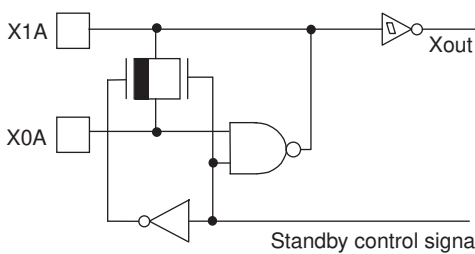
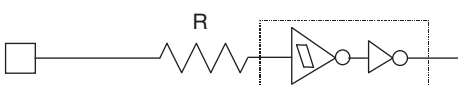
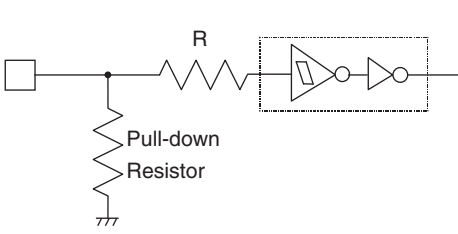
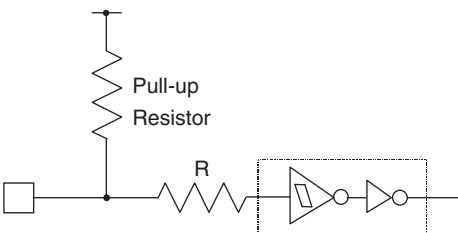
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, PPGB, PP GD, PPGF		Output pins for PPGs

1 : FPT-100P-M06

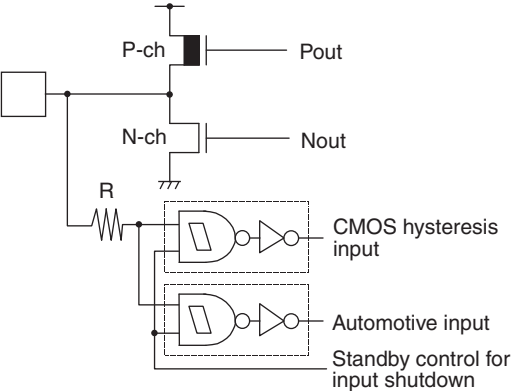
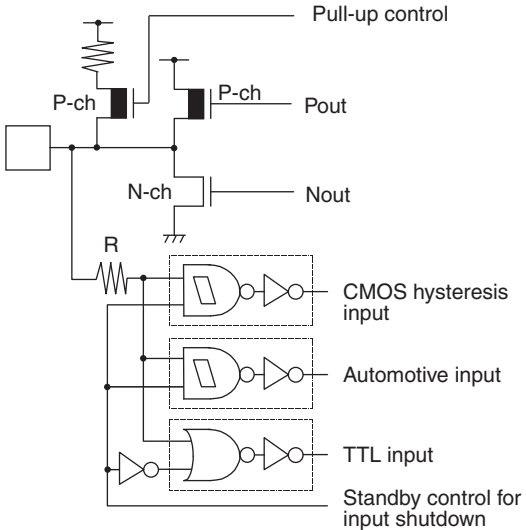
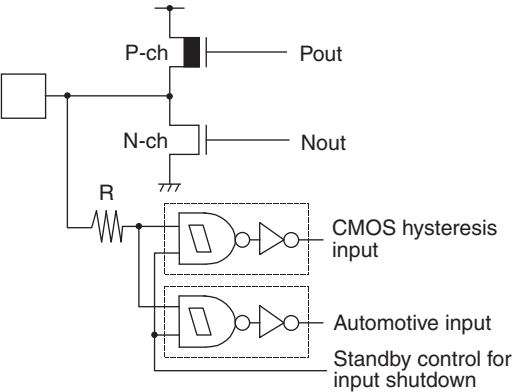
2 : FPT-100P-M20

3 : For I/O circuit type, refer to "I/O Circuit Type".

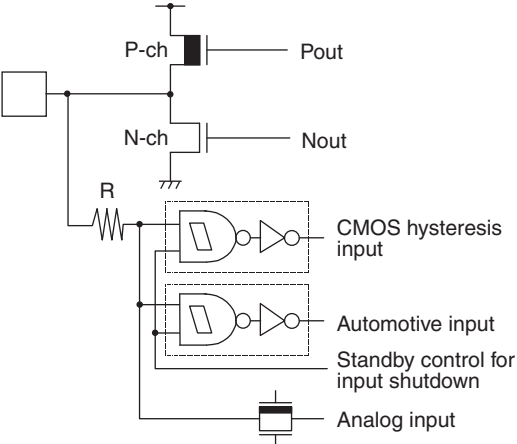
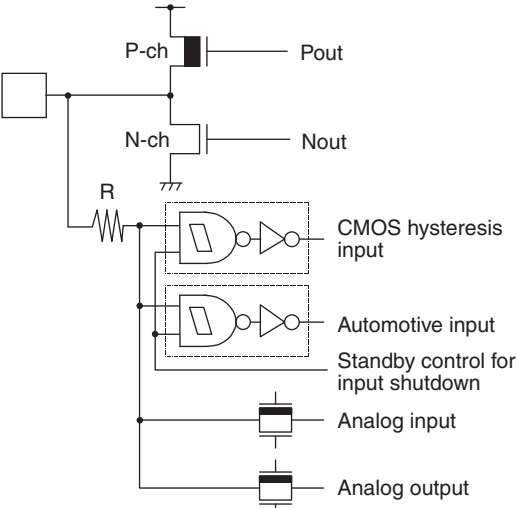
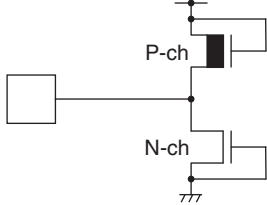
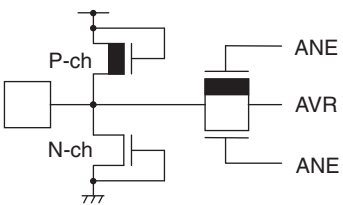
**4. I/O Circuit Type**

Type	Circuit	Remarks
A		<p>Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ</p>
B		<p>Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ</p>
C		<ul style="list-style-type: none"> <li>■ MASK ROM and evaluation products: CMOS hysteresis input pin</li> <li>■ Flash memory products: CMOS input pin</li> </ul>
D		<p>MASK ROM and evaluation products:</p> <ul style="list-style-type: none"> <li>■ CMOS hysteresis input pin</li> <li>■ Pull-down resistor value: approx. 50 kΩ</li> </ul> <p>Flash memory products:</p> <ul style="list-style-type: none"> <li>■ CMOS input pin</li> <li>■ No pull-down</li> </ul>
E		<p>CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ</p>

(Continued)

Type	Circuit	Remarks
F		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>
G		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ TTL input (with function to disconnect input during standby)</li> <li>■ Programmable pull-up resistor: 50 k<math>\Omega</math> approx.</li> </ul>
H		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 3 \text{ mA}</math>, <math>I_{OH} = -3 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>

(Continued)

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
J		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ D/A analog output</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
K		<p>Power supply input protection circuit</p>
L		<ul style="list-style-type: none"> <li>■ A/D converter reference voltage power supply input pin, with the protection circuit</li> <li>■ Flash memory devices do not have a protection circuit against <math>V_{CC}</math> for pin AVRH</li> </ul>

*(Continued)*

Type	Circuit	Remarks
M		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>
N		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ TTL input (with function to disconnect input during standby)</li> </ul> <p>Programmable pull-up resistor: 50 k<math>\Omega</math> approx</p>
O		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>

## 5. Handling Devices

### 1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins.
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AVRH$ ) exceed the digital power-supply voltage.

### 2. Handling unused pins

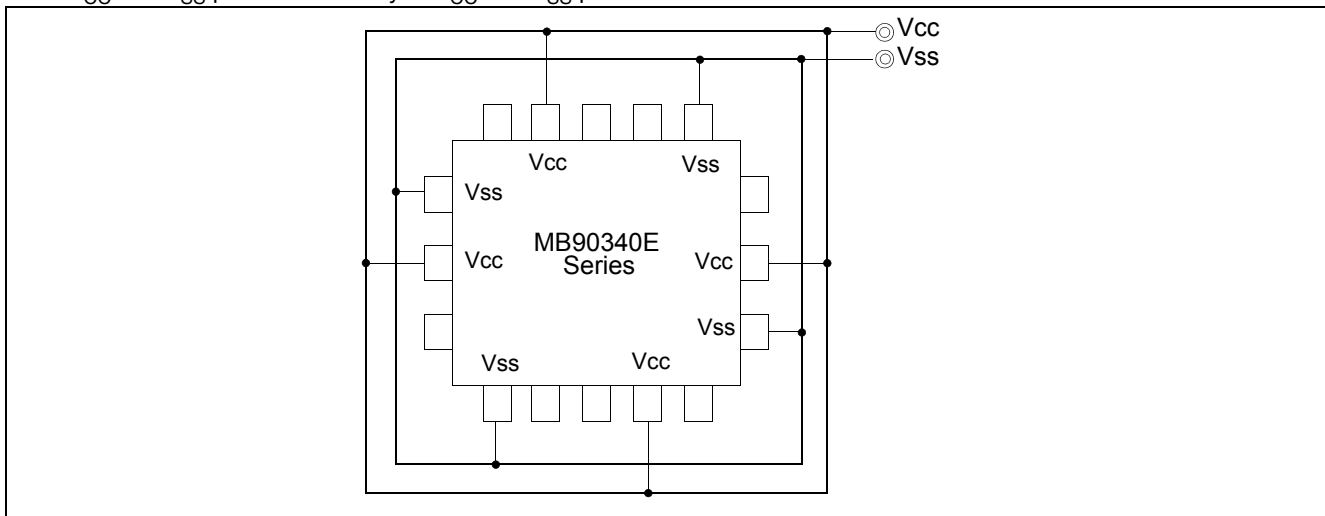
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k $\Omega$  or more.

### 3. Power supply pins ( $V_{CC}/V_{SS}$ )

■ If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally. Connect  $V_{CC}$  and  $V_{SS}$  pins to the device from the current supply source at a possibly low impedance.

■ As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1  $\mu$ F as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



### 4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to  $V_{CC}$  or  $V_{SS}$  pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.



**5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs**

Make sure to turn on the A/D converter power supply ( $AV_{CC}$ ,  $AVRH$ ,  $AVRL$ ) and analog inputs ( $AN0$  to  $AN23$ ) after turning-on the digital power supply ( $V_{CC}$ ).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed  $AVRH$  or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

**6. Connection of Unused A/D Converter Pins when the A/D Converter is Used**

Connect unused pins of A/D converter to  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVRH = AVRL = V_{SS}$ .

**7. Crystal Oscillator Circuit**

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

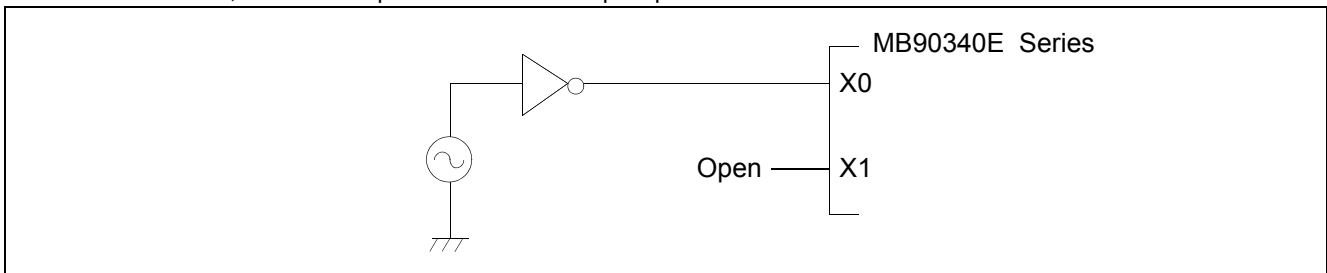
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

**8. Pull-up/down resistors**

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

**9. Using external clock**

To use an external clock, drive the X0 pin and leave the X1 pin open.



**10. Precautions when not using a sub clock signal**

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

**11. Notes on operation in PLL clock mode**

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

**12. Notes on Power-On**

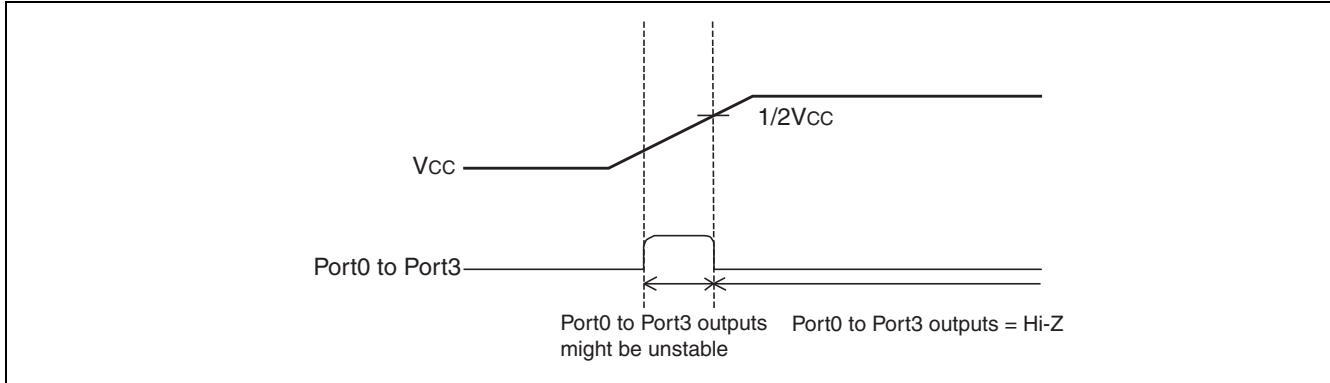
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50  $\mu$ s or more (0.2 V to 2.7 V)

**13. Stabilization of power supply voltage**

A sudden change in the supply voltage may cause the device to malfunction even within the  $V_{CC}$  supply voltage operating range. Therefore, the  $V_{CC}$  supply voltage should be stabilized. For reference, the supply voltage should be controlled so that  $V_{CC}$  ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard  $V_{CC}$  supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

**14. Port 0 to Port 3 Output During Power-on (External-bus Mode)**

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



**15. Notes on Using the CAN Function**

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

**16. Flash Security Function (except for MB90F346E)**

A security bit is located in the area of the flash memory.

If protection code 01<sub>H</sub> is written in the security bit, the flash memory is in the protected state by security.

Therefore please do not write 01<sub>H</sub> in this address if you do not use the security function.

Refer to following table for the address of the security bit.

	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	FE0001 <sub>H</sub>
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	FC0001 <sub>H</sub>
MB90F345E	Embedded 4 Mbits Flash Memory	F80001 <sub>H</sub>

**17. Serial Communication**

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.