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FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13733-6E

16-bit Microcontroller

CMOS

F²MC-16LX MB90800 Series

MB90803/803S/F803/F803S/F804-101/ MB90F804-201/F809/F809S/V800

■ DESCRIPTION

The MB90800 series is a general-purpose 16-bit microcontroller that has been developed for high-speed real-time processing required for industrial and office automation equipment and process control, etc. The LCD controller of 48 segment four common is built into.

Instruction set has taken over the same AT architecture as in the F²MC-8L and F²MC-16L, and is further enhanced to support high level languages, extend addressing mode, enhanced divide/multiply instructions with sign and enrichment of bit processing. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note: F²MC is the abbreviation of Fujitsu Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Operating clock (PLL clock) : divided-by-2 of oscillation (at oscillation of 6.25 MHz) or 1 to 4 times the oscillation (at oscillation of 6.25 MHz to 25 MHz).
  - Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock, operation at Vcc = 3.3 V)
- **The maximum memory space:16 Mbytes**
  - 24-bit internal addressing
  - Bank addressing

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2009.9

(Continued)

- **Optimized instruction set for controller applications**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - High code efficiency
  - Enhanced high-precision computing with 32-bit accumulator
  - Enhanced Multiply/Divide instructions with sign and the RETI instruction
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Instruction set has symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  - The priority level can be set to programmable.
  - Interrupt function with 32 factors
- **Data transfer function**
  - Expanded intelligent I/O service function (EI^{2}OS): Maximum of 16 channels
- **Low Power Consumption Mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Time-base timer mode (a mode that operates oscillation clock and time-base timer)
  - Watch mode (mode in which only the subclock and watch timers operate)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking mode (operating CPU at each set cycle)
- **Package**
  - QFP-100 (FPT-100P-M06 : 0.65 mm lead pitch)
- **Process : CMOS technology**

■ PRODUCT LINEUP

Item \ Part number	MB90V800-101/201	MB90F804-101/201	MB90803/MB90803S	MB90F803/MB90F803S	MB90F809/MB90F809S
Type	Evaluation product	Flash memory products	Mask ROM products	Flash memory products	
System clock	On-chip PLL clock multiplication method(× 1, × 2, × 3, × 4, 1/2 when PLL stops) Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock)				
Sub clock	With sub clock: 201 option Without sub clock: 101 option		With sub clock: Part number of products without "S" suffix Without sub clock: Part number of products with "S" suffix		
ROM capacity	No	256 Kbytes	128 Kbytes	128 Kbytes dual operation	192 Kbytes
RAM capacity	28 Kbytes	16 Kbytes	4 Kbytes	4 Kbytes	10 Kbytes
CPU functions	Number of basic instructions : 351 Minimum instruction execution time : 40.0 ns/6.25 MHz oscillator (When four times is used : machine clock 25 MHz, Power supply voltage : 3.3 V ± 0.3 V) Addressing type : 23 types Program Patch Function : 2 address pointers The maximum memory space : 16 Mbytes				
Ports	I/O port (CMOS) 68 ports (shared with resources), (70 ports when the subclock is not used)				
LCD controller/driver	Segment driver that can drive the LCD panel (liquid crystal display) directly, and common driver 48 SEG × 4 COM				
16-bit input/output timer — 16-bit free-run timer	1 channel Overflow interrupt				
16-bit input/output timer — Output compare (OCU)	2 channels Pin input factor: matching of the compare register				
16-bit input/output timer — Input capture (ICU)	2 channels Rewriting a register value upon a pin input (rising edge, falling edge, or both edges)				
16-bit Reload Timer	16-bit reload timer operation (toggle output, single shot output selectable) The event count function is optional. The event count function is optional. Three channels are built in.				
16-bit PPG timer	Output pin × 2 ports Operating clock frequency : fcp, fcp/22, fcp/24, fcp/26 Two channels are built in.				
Time-base timer	1 channel				
Watchdog timer	1 channel				
Timer clock output circuit	Clock with a frequency of external input clock divided by 16/32/64/128 can be output externally.				
I²C bus	I²C Interface. 1 channel is built-in.				

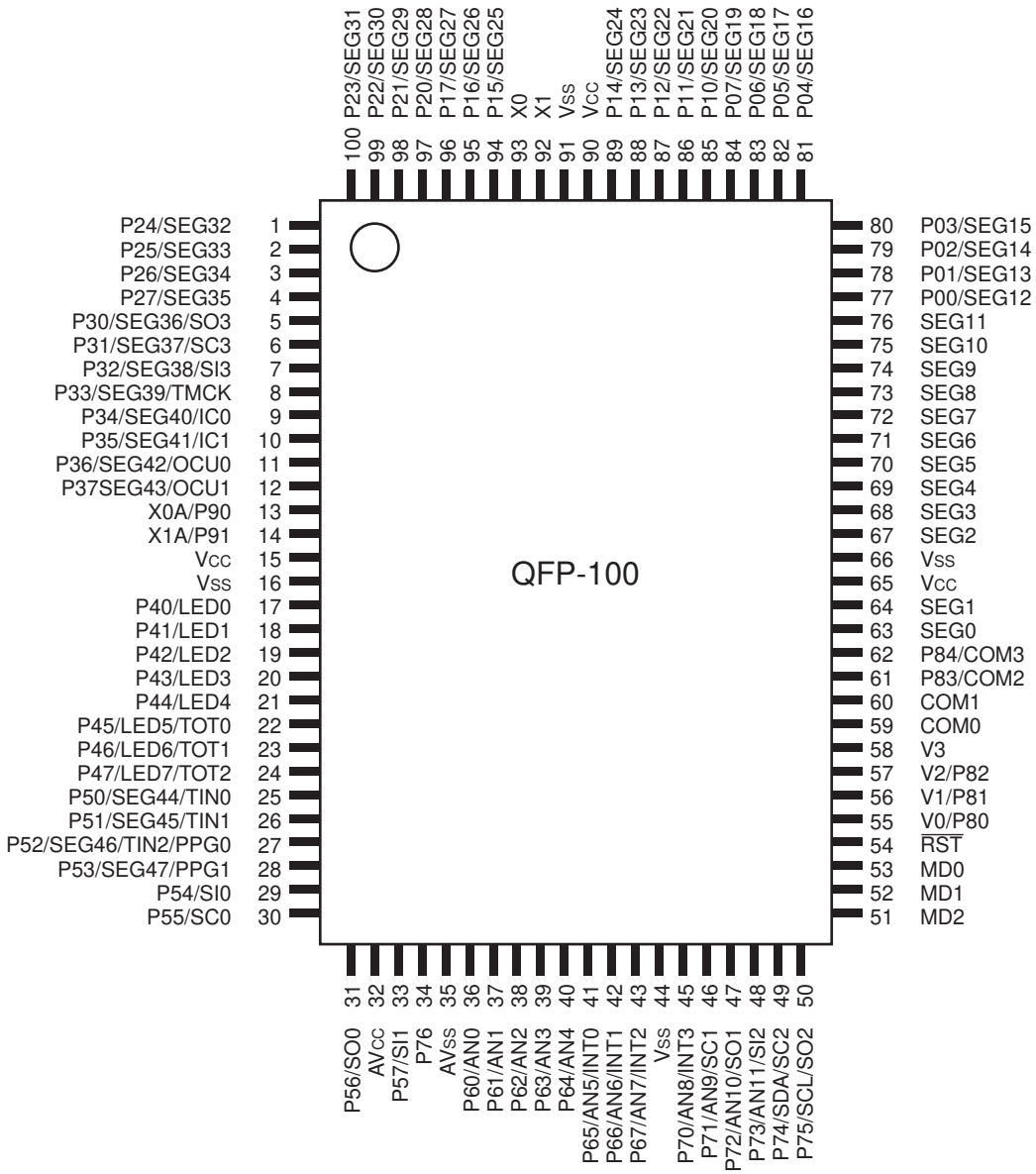
(Continued)

(Continued)

Part number / Item	MB90V800-101/201	MB90F804-101/201	MB90803/ MB90803S	MB90F803/ MB90F803S	MB90F809/ MB90F809S
8/10-bit A/D converter	12 channels (input multiplex) The 8-bit resolution or 10-bit resolution can be set. Conversion time : 5.9 µs (When machine clock 16.8 MHz works).				
UART	Full-duplex double buffer Asynchronous/synchronous transmit (with start/stop bits) are supported. Two channels are built in.				
Extended I/O serial interface	Two channels are built in.				
Interrupt delay interrupt	One channel				
DTP/External interrupt	4 channels Interrupt causes : “L”→“H” edge/“H”→“L” edge/“L” level/“H” level selectable				
Low Power Consumption Mode	Sleep mode/Time-base timer mode/Watch mode/Stop mode/CPU intermittent mode				
Process	CMOS				
Operating voltage	2.7 V to 3.6 V				

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-100P-M06)

■ PIN DESCRIPTION

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
92, 93	X1, X0	A	Oscillation status	It is a terminal which connects the oscillator. When connecting an external clock, leave the x1 pin unconnected.
13, 14	X0A, X1A	B	Oscillation status	It is 32 kHz oscillation pin. (Dual-line model)
	P90, P91	G	Port input (High-Z)	General purpose input/output port. (Single-line model)
51	MD2	M	Mode Pins	Input pin for selecting operation mode. Connect directly to Vss.
52, 53	MD1, MD0	L	Mode Pins	Input pin for selecting operation mode. Connect directly to Vcc.
54	$\overline{\text{RST}}$	K	Reset input	External reset input pin.
63, 64, 67 to 76	SEG0 to SEG11	D	LCD SEG output	A segment output terminal of the LCD controller/ driver.
77 to 84	SEG12 to SEG19	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P00 to P07			General purpose input/output port.
85 to 89, 94 to 96	SEG20 to SEG27	E		A segment output terminal of the LCD controller/ driver.
	P10 to P17			General purpose input/output port.
97 to 100, 1 to 4	SEG28 to SEG35	E		A segment output terminal of the LCD controller/ driver.
	P20 to P27			General purpose input/output port.
5	SEG36	E		A segment output terminal of the LCD controller/ driver.
	P30			General purpose input/output port.
	SO3			Serial data output pin of serial I/O ch.3. Valid when serial data output of serial I/O ch.3 is enabled.
6	SEG37	E		A segment output terminal of the LCD controller/ driver.
	P31			General purpose input/output port.
	SC3			Serial clock I/O pin of serial I/O ch.3. Valid when serial clock output of serial I/O ch.3 is enabled.

(Continued)

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
7	SEG38	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P32			General purpose input/output port.
	SI3			Serial data input pin of serial I/O ch.3. This pin may be used during serial I/O ch.3 in input mode, so it cannot use as other pin function.
8	SEG39	E		A segment output terminal of the LCD controller/ driver.
	P33			General purpose input/output port.
	TMCK			Timer clock output pin. It is effective when permitting the power output.
9, 10	SEG40, SEG41	E		A segment output terminal of the LCD controller/ driver.
	P34, P35			General purpose input/output port.
	IC0, IC1			External trigger input pin of input capture ch.0/ch.1.
11, 12	SEG42, SEG43	E		A segment output terminal of the LCD controller/ driver.
	P36, P37			General purpose input/output port.
	OCU0, OCU1			Output terminal for the output compares ch.0/ch.1.
17 to 21	LED0 to LED4	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P40 to P44			General purpose input/output port.
22 to 24	LED5 to LED7	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P45 to P47			General purpose input/output port.
	TOT0 to TOT2			External event output pin of reload timer ch.0 to ch.2. It is effective when permitting the external event output.
25, 26	SEG44, SEG45	E		A segment output terminal of the LCD controller/ driver.
	P50, P51			General purpose input/output port.
	TIN0, TIN1			External clock input pin of reload timer ch.0, ch.1. It is effective when permitting the external clock input.

(Continued)

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
27	SEG46	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P52			General purpose input/output port.
	TIN2			External clock input pin of reload timer ch.2. It is effective when permitting the external clock input.
	PPG0			PPG timer (ch.0) output pin.
28	SEG47	E		A segment output terminal of the LCD controller/ driver.
	P53			General purpose input/output port.
	PPG1			PPG (ch.1) timer output pin.
29	SIO	G		Serial data input pin of UART ch.0. This pin may be used during UART ch.0 in receiving mode, so it cannot use as other pin function.
	P54			General purpose input/output port.
30	SC0	G		Serial clock input/output pin of UART ch.0. It is effective when permitting the serial clock output of UART ch.0.
	P55			General purpose input/output port.
31	SO0	G		Serial data output pin of UART ch.0. It is effective when permitting the serial clock output of UART ch.0.
	P56			General purpose input/output port.
33	SI1	G		Serial data input pin of UART ch.1. This pin may be used during UART ch.1 in receiving mode, so it cannot use as other pin function.
	P57			General purpose input/output port.
34	P76	G		General purpose input/output port.
36 to 40	AN0 to AN4	I		Analog input pin ch.0 to ch.4 of A/D converter. Enabled when analog input setting is “enabled”(set by ADER).
	P60 to P64			General purpose input/output port.

(Continued)

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
41 to 43	AN5 to AN7	I	Analog input (High-Z)	Analog input pin ch.5 to ch.7 of A/D converter. Enabled when analog input setting is “enabled”.
	P65 to P67			General purpose input/output port.
	INT0 to INT2			Functions as an external interrupt ch.0 to ch.2 input pin.
45	AN8	I		Analog input pin ch.8 of A/D converter. Enabled when analog input setting is “enabled”.
	P70			General purpose input/output port.
	INT3			Functions as an external interrupt ch.3 input pin.
46	AN9	I	Port input (High-Z)	Analog input pin ch.9 of A/D converter. Enabled when analog input setting is “enabled”.
	P71			General purpose input/output port.
	SC1			Serial clock input/output pin of UART ch.1. It is effective when permitting the serial clock output of UART ch.1.
47	AN10	I		Analog input pin ch.10 of A/D converter. Enabled when analog input setting is “enabled”.
	P72			General purpose input/output port.
	SO1			Serial data output pin of serial I/O ch.1. Valid when serial data output of serial I/O ch.1 is enabled.
48	AN11	I		Analog input pin ch.11 of A/D converter. Enabled when analog input setting is “enabled”.
	P73			General purpose input/output port.
	SI2			Serial data input pin of serial I/O ch.2. This pin may be used during serial I/O ch.2 in input mode, so it cannot use as other pin function.

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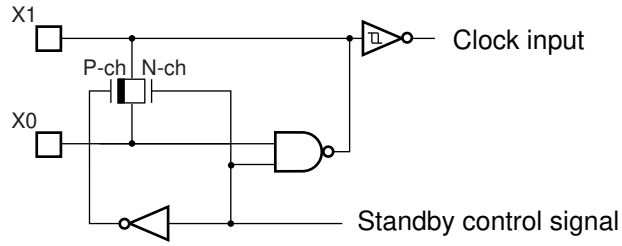
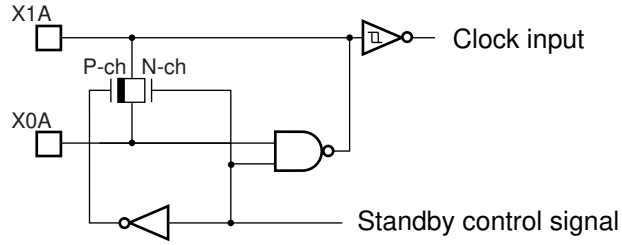
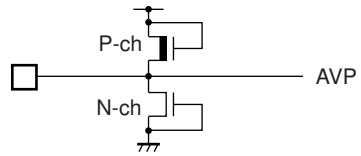
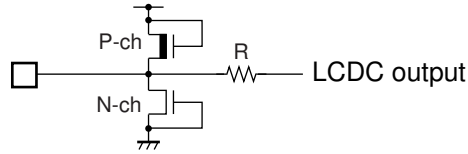
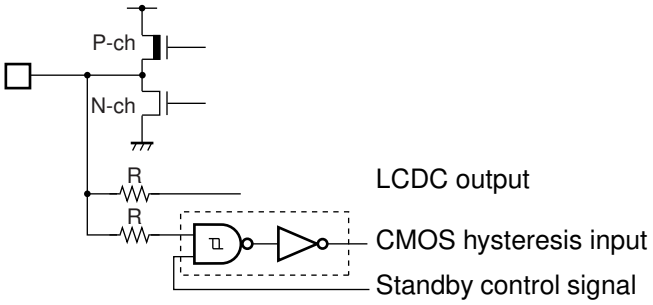
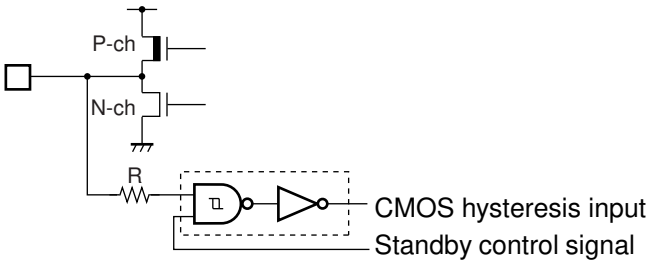
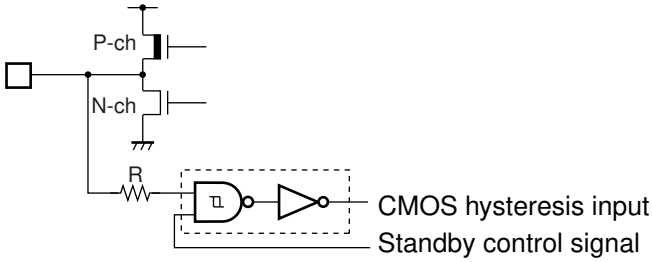
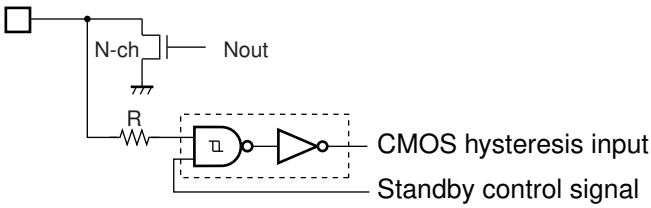
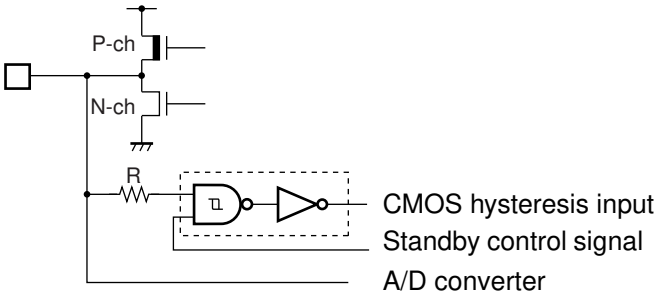
Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
49	SDA	H	Port input (High-Z)	Data input/output pin of I²C Interface. This pin is enabled when the I²C interface is operated. While the I²C interface is running, the port must be set for input use.
	P74			General purpose input/output port. (N-ch open-drain, withstand voltage of 5 V.)
	SC2			Serial clock input pin of serial I/O ch.2. Valid when serial clock output of serial I/O ch.2 is enabled.
50	SCL	H		Clock input/output pin of I²C Interface. This pin is enabled when the I²C interface is operated. While the I²C interface is running, the port must be set for input use.
	P75			General purpose input/output port. (N-ch open-drain, withstand voltage of 5 V.)
	SO2			Serial data output pin of serial I/O ch.2. Valid when serial data output of serial I/O ch.2 is enabled.
55 to 57	V0 to V2	J	LCD drive power supply input	LCD controller/driver. Reference power terminals of LCD controller/driver.
	P80 to P82			General purpose input/output port.
59, 60	COM0, COM1	D	LCD COM output	A common output terminal of the LCD controller/ driver.
61, 62	P83, P84	E	Port input (High-Z)	General purpose input/output port.
	COM2, COM3			A common output terminal of the LCD controller/ driver.
32	AV_{CC}	C	Power supply	A/D converter exclusive power supply input pin.
35	AV_{SS}	C		A/D converter-exclusive GND power supply pin.
58	V3	J		LCD controller/driver Reference power terminals of LCD controller/driver.
15, 65, 90	V_{CC}	—		These are power supply input pins.
16, 44, 66, 91	V_{SS}	—		GND power supply pin.

* : Refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation feedback resistance : 1 MΩ approx.
B		Low-rate oscillation feedback resistor, approx.10 MΩ
C		Analog power supply input protection circuit
D		LCDC output
E		• CMOS output • LCDC output • CMOS hysteresis input (With input interception function at standby)

(Continued)

Type	Circuit	Remarks
F		• CMOS output (Heavy-current I_{OL} =15 mA for LED drive) • CMOS hysteresis input (With input interception function at standby)
G		• CMOS output • CMOS hysteresis input (With input interception function at standby) Notes : • The I/O port and internal resources share one output buffer for their outputs. • The I/O port and internal resources share one input buffer for their input.
H		• CMOS hysteresis input (With input interception function at standby) • N-ch open drain output
I		• CMOS output • CMOS hysteresis input (With input interception function at standby) • Analog input (If the bit of analog input enable register = 1, the analog input of A/D converter is enabled.) Notes : • The I/O port and internal resources share one output buffer for their outputs. • The I/O port and internal resources share one input buffer for their inputs.

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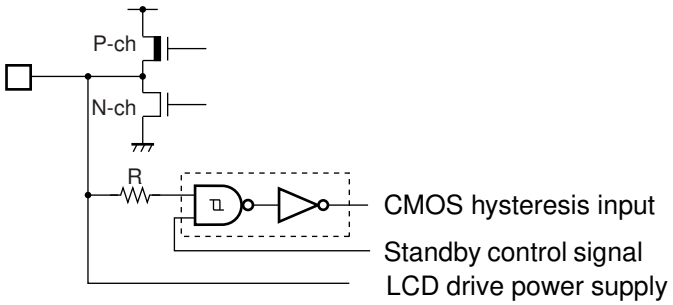
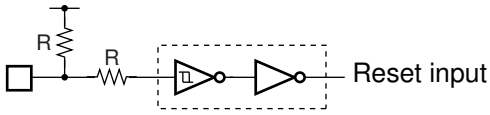
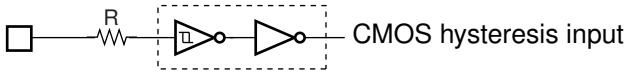
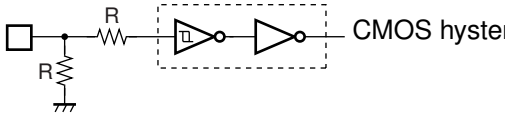
Type	Circuit	Remarks
J		• CMOS output • CMOS hysteresis input (With input interception function at standby) • LCD drive power supply input
K		CMOS hysteresis input with pull-up resistor.
L		CMOS hysteresis input
M		CMOS hysteresis input with pull-down resistor

■ HANDLING DEVICES

1. Preventing Latch-up, Turning on Power Supply

Latch-up may occur on CMOS IC under the following conditions:

- If a voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins,
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- If the AV_{CC} power supply is turned on before the V_{CC} voltage.

Ensure that you apply a voltage to the analog power supply at the same time as V_{CC} or after you turn on the digital power supply (when you perform power-off, turn off the analog power supply first or at the same time as V_{CC} and the digital power supply).

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using CMOS IC, take great care to prevent the occurrence of latch-up.

2. Treatment of unused pins

If unused input pins are left open, they may cause abnormal operation or latch-up which may lead to permanent damage to the semiconductor. Any such pins should be pulled up or pulled down through resistance of at least 2 kΩ.

Any unused input/output pins should be left open in output status, or if found set to input status, they should be treated in the same way as input pins.

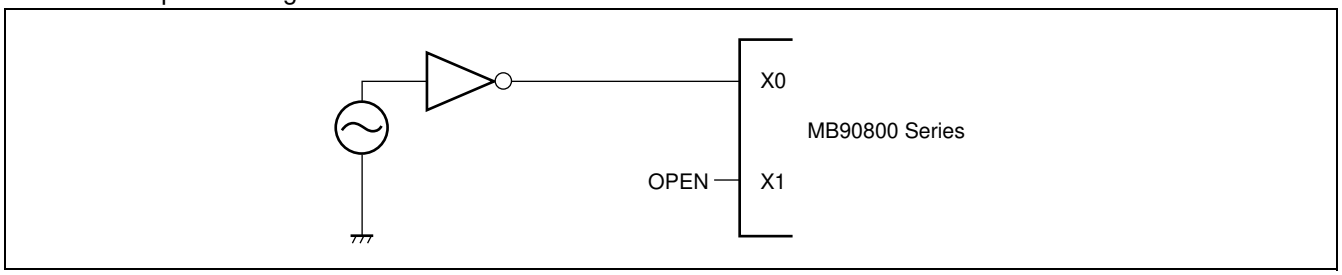
Any unused output pins should be left open.

3. Treatment of A/D converter power supply pins

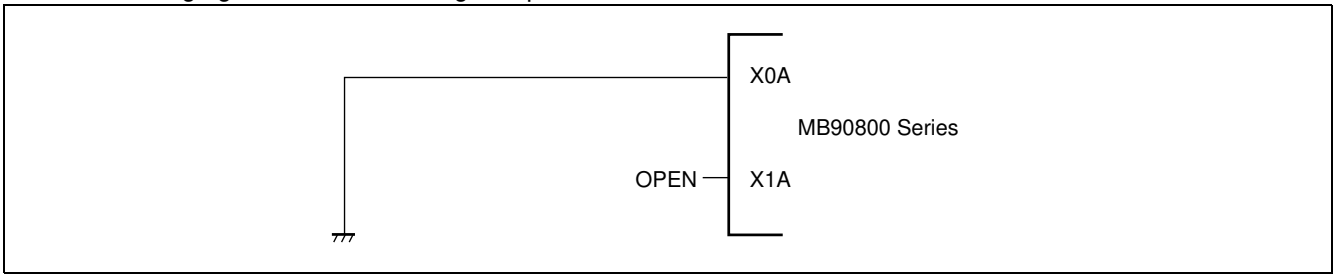
Even if the A/D converter is not used, pins should be connected so that $AV_{CC} = V_{CC}$, and $AV_{SS} = V_{SS}$.

4. About the attention when the external clock is used

In using an external clock, drive pin X0 only and leave pin X1 open.
The example of using an external clock is shown below.



Please set X0A = GND and X1A = open without subclock mode.
The following figure shows the using sample.



5. Treatment of power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect all power supply pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} near this device.

6. About Crystal oscillators circuit

Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1 pins and X0A/X1A pins, the crystal oscillator (or the ceramic oscillator) and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0/X1 pins and X0A/X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

7. Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

8. Stabilization of Supply Power Supply

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range.Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

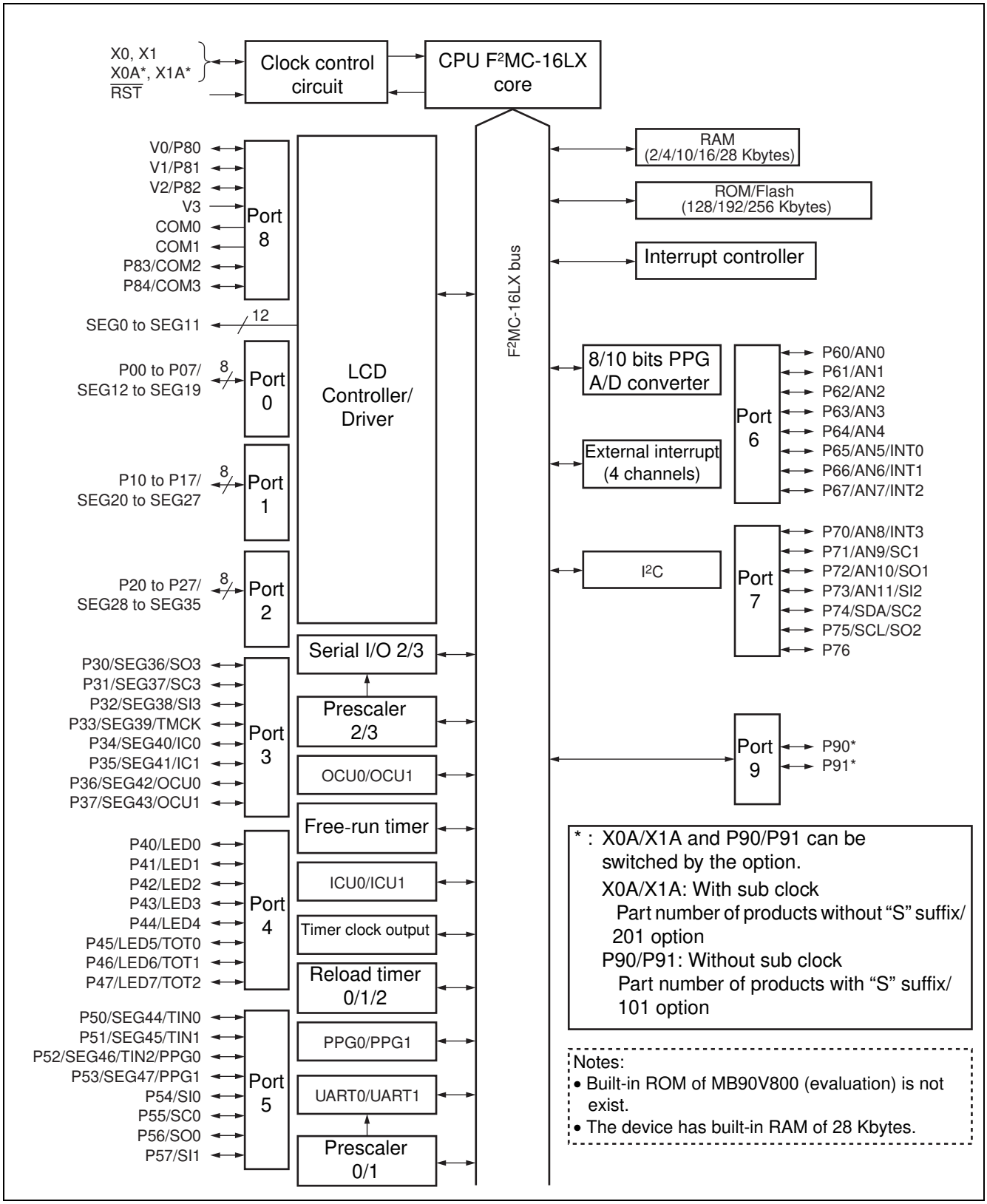
9. Note on Using the two-subsystem product as one-subsystem product

If you are using only one subsystem of the MB90800 series that come in one two-subsystem product, use it with X0A = V_{SS} and X1A = OPEN.

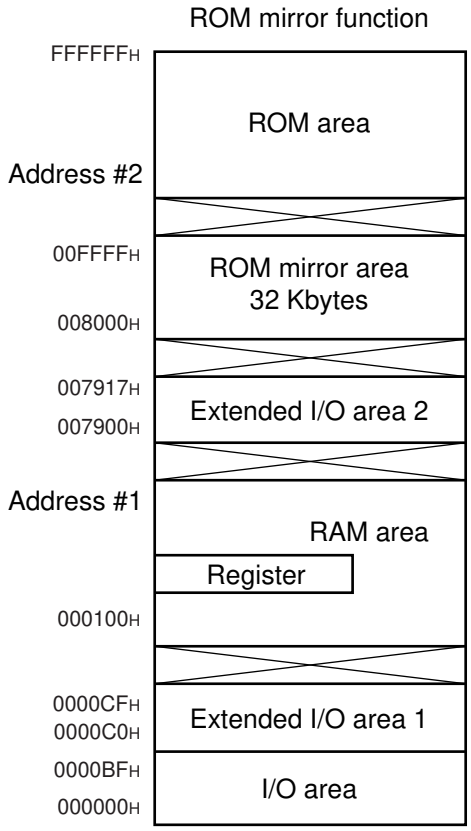
10. Write to FLASH

Ensure that you must write to FLASH at the operating voltage V_{CC} = 3.0 V to 3.6 V.

■ BLOCK DIAGRAM



■ MEMORY MAP



Part number	Address #1	Address #2
MB90803/S, MB90F803/S	0010FFH	FE0000H
MB90F809/S	0028FFH	FD0000H
MB90F804-101/201	0040FFH	FC0000H
MB90V800-101/201	0070FFH	F80000H*

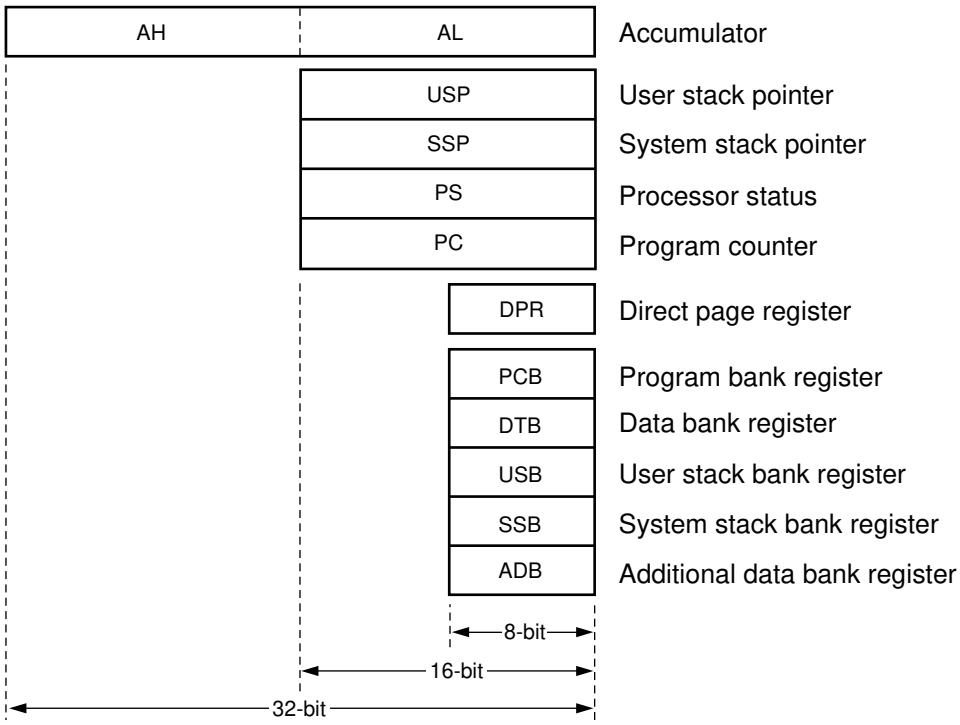
* : ROM is not built into MB90V800.
F80000H is ROM decipherment region on the tool side.

Memory Map of MB90800 Series

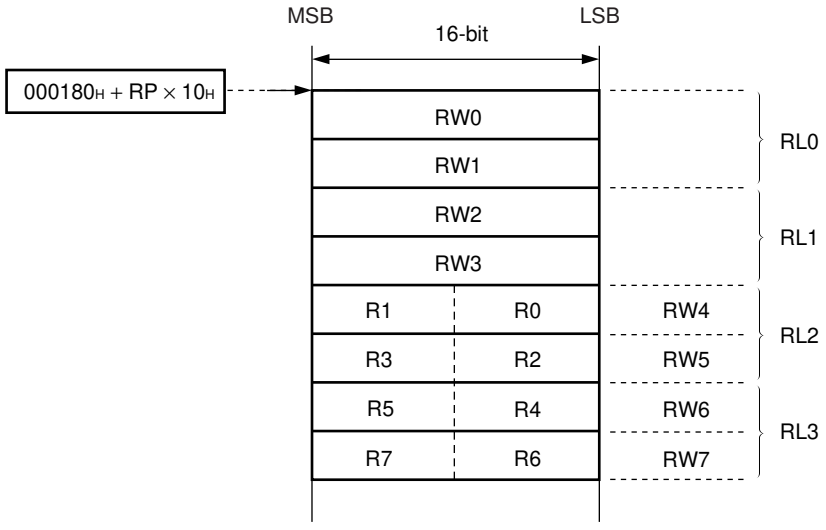
Notes : • When the ROM mirror function register has been set, the mirror image data at higher addresses (“FF4000H to FFFFFFH”) of bank FF is visible from the higher addresses (“008000H to 00FFFFH”) of bank 00.
• The ROM mirror function is for using the C compiler small model.
• The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Note that because the ROM area of bank FF exceeds.
32 Kbytes, all data in the ROM area cannot be shown in mirror image in bank 00.
• When the C compiler small model is used, the data table can be shown as mirror image at “008000H to 00FFFFH ”by storing the data table at “FF8000H to FFFFFFH”. Therefore, data tables in the ROM area can be referenced without declaring the far addressing with the pointer.

■ F²MC-16L CPU Programming model

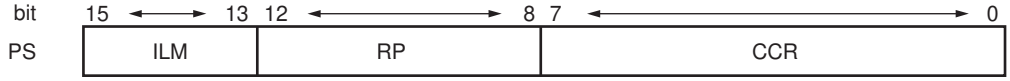
• Dedicated Registers



• General purpose registers



• Processor status



■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000000H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	Port 7	- XXXXXXXB
000008H	PDR8	Port 8 data register	R/W	Port 8	- - - XXXXXB
000009H	PDR9	Port 9 data register	R/W	Port 9	- - - - - - XXB
00000AH to 00000FH	Prohibited				
000010H	DDR0	Port 0 direction register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 direction register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 direction register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	DDR3	Port 3 direction register	R/W	Port 3	0 0 0 0 0 0 0 0B
000014H	DDR4	Port 4 direction register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 direction register	R/W	Port 5	0 0 0 0 0 0 0 0B
000016H	DDR6	Port 6 direction register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H	DDR7	Port 7 direction register	R/W	Port 7	- 0 0 0 0 0 0 0B
000018H	DDR8	Port 8 direction register	R/W	Port 8	- - - 0 0 0 0 0B
000019H	DDR9	Port 9 direction register	R/W	Port 9	- - - - - - 0 0B
00001AH to 00001DH	Prohibited				
00001EH	ADER0	Analog input enable 0 register	R/W	Port 6, A/D	1 1 1 1 1 1 1 1B
00001FH	ADER1	Analog input enable 1 register	R/W	Port 7, A/D	- - - - 1 1 1 1B
000020H	SMR0	Serial mode register	R/W	UART0	0 0 0 0 0 - 0 0B
000021H	SCR0	Serial control register	R/W		0 0 0 0 0 1 0 0B
000022H	SIDR0/ SODR0	Serial input/output register	R/W		XXXXXXXXB
000023H	SSR0	Serial data register	R/W		0 0 0 0 1 0 0 0B
000024H	Prohibited				
000025H	CDCR0	Communication prescaler control register	R/W	Prescaler 0	0 0 - - 0 0 0 0B
000026H	Prohibited				
000027H					

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000028H	SMR1	Serial mode register	R/W	UART1	0 0 0 0 0 - 0 0B
000029H	SCR1	Serial control register	R/W, W		0 0 0 0 0 1 0 0B
00002AH	SIDR1/ SODR1	Serial input/output register	R/W		XXXXXXXXB
00002BH	SSR1	Serial data register	R/W, R		0 0 0 0 1 0 0 0B
00002CH	Prohibited				
00002DH	CDCR1	Communication prescaler control register	R/W	Prescaler 1	0 0 - - 0 0 0 0B
00002EH	Prohibited				
00002FH					
000030H	ENIR	Interrupt/DTP enable	R/W	External interrupt	- - - - 0 0 0 0B
000031H	EIRR	Interrupt/DTP source	R/W		- - - - XXXXB
000032H	ELVR	Request level set register	R/W		0 0 0 0 0 0 0 0B
000033H	Prohibited				
000034H	ADCS0	Control status register (lower)	R/W	A/D converter	0 0 - - - - - - B
000035H	ADCS1	Control status register (upper)	W, R/W		0 0 0 0 0 0 0 0B
000036H	ADCR0	Data register (lower)	R		XXXXXXXXB
000037H	ADCR1	Data register (upper)	R, W		0 0 1 0 1 - XXB
000038H	Prohibited				
000039H	ADMR	A/D conversion channel set register	R/W	A/D converter	0 0 0 0 0 0 0 0B
00003AH	CPCLR	Compare clear register	R/W	16-bit free-run timer	XXXXXXXXB
00003BH					XXXXXXXXB
00003CH	TCDT	Timer counter data register	R/W		0 0 0 0 0 0 0 0B
00003DH					0 0 0 0 0 0 0 0B
00003EH	TCCSL	Timer counter control/status register (lower)	R/W		0 0 0 0 0 0 0 0B
00003FH	TCCSH	Timer counter control/status register (upper)	R/W		0 - - 0 0 0 0 0B
000040H to 000043H	Prohibited				
000044H	IPCP0	Input capture data register 0	R	Input Capture 0/1	XXXXXXXXB
000045H					XXXXXXXXB
000046H	IPCP1	Input capture data register 1			XXXXXXXXB
000047H					XXXXXXXXB
000048H	ICS01	Control status register	R/W		0 0 0 0 0 0 0 0B
000049H	Prohibited				
00004AH	OCCP0	Compare register 0	R/W	Output compare 0	0 0 0 0 0 0 0 0B
00004BH					0 0 0 0 0 0 0 0B
00004CH	OCCP1	Compare register 1	R/W	Output compare 1	0 0 0 0 0 0 0 0B
00004DH					0 0 0 0 0 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
00004E$_H$	OCSL	Control status register (lower)	R/W	Output Compare 0/1	0 0 0 0 - - 0 0$_B$
00004F$_H$	OCSH	Control status register (upper)	R/W		- - - 0 0 0 0 0$_B$
000050$_H$	TMCSR0L	Timer control status register (lower)	R/W	16-bit reload timer 0	0 0 0 0 0 0 0 0$_B$
000051$_H$	TMCSR0H	Timer control status register (upper)	R/W		- - - - 0 0 0 0$_B$
000052$_H$	TMR0/ TMRLR0	16-bit timer register/Reload register	R/W		XXXXXXXX$_B$
000053$_H$					XXXXXXXX$_B$
000054$_H$	TMCSR1L	Timer control status register (lower)	R/W	16-bit reload timer 1	0 0 0 0 0 0 0 0$_B$
000055$_H$	TMCSR1H	Timer control status register (upper)	R/W		- - - - 0 0 0 0$_B$
000056$_H$	TMR1/ TMRLR1	16-bit timer register/Reload register	R/W		XXXXXXXX$_B$
000057$_H$					XXXXXXXX$_B$
000058$_H$	TMCSR2L	Timer control status register (lower)	R/W	16-bit reload timer 2	0 0 0 0 0 0 0 0$_B$
000059$_H$	TMCSR2H	Timer control status register (upper)	R/W		- - - - 0 0 0 0$_B$
00005A$_H$	TMR2/ TMRLR2	16-bit timer register/Reload register	R/W		XXXXXXXX$_B$
00005B$_H$					XXXXXXXX$_B$
00005C$_H$	LCRL	LCDC control register (lower)	R/W	LCD controller/ driver	0 0 0 1 0 0 0 0$_B$
00005D$_H$	LCRH	LCDC control register (upper)	R/W		0 0 0 0 0 0 0 0$_B$
00005E$_H$	LCRR	LCDC range register	R/W		0 0 0 0 0 0 0 0$_B$
00005F$_H$	Prohibited				
000060$_H$	SMCS0	Serial mode control status register	R, R/W	SIO (Extended Serial I/O)	0 0 0 0 0 0 1 0$_B$
000061$_H$			R/W		- - - - 0 0 0 0$_B$
000062$_H$	SDR0	Serial Data Register	R/W		XXXXXXXX$_B$
000063$_H$	SDCR0	Communication prescaler control register	R/W	Communication prescaler (SIO)	0 - - - 0 0 0 0$_B$
000064$_H$	SMCS1	Serial mode control status register	R, R/W	SIO (Extended Serial I/O)	0 0 0 0 0 0 1 0$_B$
000065$_H$			R/W		- - - - 0 0 0 0$_B$
000066$_H$	SDR1	Serial Data Register	R/W		XXXXXXXX$_B$
000067$_H$	SDCR1	Communication prescaler control register	R/W	Communication prescaler (SIO)	0 - - - 0 0 0 0$_B$
000068$_H$	Prohibited				
000069$_H$					
00006A$_H$	IBSR	I^{2}C status register	R	I^{2}C	0 0 0 0 0 0 0 0$_B$
00006B$_H$	IBCR	I^{2}C control register	R/W		0 0 0 0 0 0 0 0$_B$
00006C$_H$	ICCR	I^{2}C clock control register	R/W		XX0XXXXX$_B$
00006D$_H$	IADR	I^{2}C address register	R/W		XXXXXXXX$_B$
00006E$_H$	IDAR	I^{2}C data register	R/W		XXXXXXXX$_B$
00006F$_H$	ROMM	ROM mirror function select register	R/W, W	ROM mirror	XXXXXXX1$_B$

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000070H	PDCRL0	PDCRL0/PDCRH0 PPG down counter register	R	16-bit PPG0	1 1 1 1 1 1 1 1B
000071H	PDCRH0				1 1 1 1 1 1 1 1B
000072H	PCSRL0	PCSRL0/PCSRH0 PPG cycle set register	W		XXXXXXXXB
000073H	PCSRH0				XXXXXXXXB
000074H	PDUTL0	PDUTL0/PDUTH0 PPG duty setting register	W		XXXXXXXXB
000075H	PDUTH0				XXXXXXXXB
000076H	PCNTL0	PCNTL0/PCNTH0 PPG control status register	R/W		- - 0 0 0 0 0 0B
000077H	PCNTH0				0 0 0 0 0 0 0 -B
000078H	PDCRL1	PDCRL1/PDCRH1 PPG down counter register	R	16-bit PPG1	1 1 1 1 1 1 1 1B
000079H	PDCRH1				1 1 1 1 1 1 1 1B
00007AH	PCSRL1	PCSRL1/PCSRH1 PPG cycle set register	W		XXXXXXXXB
00007BH	PCSRH1				XXXXXXXXB
00007CH	PDUTL1	PDUTL1/PDUTH1 PPG duty setting register	W		XXXXXXXXB
00007DH	PDUTH1				XXXXXXXXB
00007EH	PCNTL1	PCNTL1/PCNTH1 PPG control status register	R/W		- - 0 0 0 0 0 0B
00007FH	PCNTH1				0 0 0 0 0 0 0 -B
000080H to 000095H	(Reserved)				
000096H	Prohibited				
000097H	(Reserved)				
000098H to 00009DH	Prohibited				
00009EH	PACSR	ROM correction control register	R/W	ROM Correction	0 0 0 0 0 0 0 0B
00009FH	DIRR	Delayed interrupt source generated/ release register	R/W	Delayed interrupt	- - - - - - - 0B
0000A0H	LPMCR	Low power consumption mode control register	R/W, W	Low power consumption control circuit	0 0 0 1 1 0 0 0B
0000A1H	CKSCR	Clock selector register	R/W, R		1 1 1 1 1 1 0 0B
0000A2H to 0000A7H	Prohibited				
0000A8H	WDTC	Watchdog timer control register	R, W	Watchdog timer	XXXXX 1 1 1B
0000A9H	TBTC	Time-base timer control register	R/W, W	Time-base timer	1 - - 0 0 1 0 0B
0000AAH	WTC	Watch timer control register	R/W, R	Watch timer (Sub clock)	1 X0 1 1 0 0 0B
0000ABH to 0000ADH	Prohibited				

(Continued)

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000AE$_H$	FMCS	Flash control register	R/W	Flash I/F	0 0 0 X 0 0 0 0$_B$
0000AF$_H$	TMCS	Timer clock output control register	R/W	Timer clock divide	XXXXX 0 0 0$_B$
0000B0$_H$	ICR00	Interrupt control register 00	R/W, W, R	Interrupt controller	0 0 0 0 0 1 1 1$_B$
0000B1$_H$	ICR01	Interrupt control register 01	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B2$_H$	ICR02	Interrupt control register 02	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B3$_H$	ICR03	Interrupt control register 03	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B4$_H$	ICR04	Interrupt control register 04	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B5$_H$	ICR05	Interrupt control register 05	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B6$_H$	ICR06	Interrupt control register 06	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B7$_H$	ICR07	Interrupt control register 07	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B8$_H$	ICR08	Interrupt control register 08	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000B9$_H$	ICR09	Interrupt control register 09	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000BA$_H$	ICR10	Interrupt control register 10	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000BB$_H$	ICR11	Interrupt control register 11	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000BC$_H$	ICR12	Interrupt control register 12	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000BD$_H$	ICR13	Interrupt control register 13	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000BE$_H$	ICR14	Interrupt control register 14	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000BF$_H$	ICR15	Interrupt control register 15	R/W, W, R		0 0 0 0 0 1 1 1$_B$
0000CA$_H$	FWR0	Flash Program Control Register 0	R/W	Flash I/F (MB90F803/S only object)	0 0 0 0 0 0 0 0$_B$
0000CB$_H$	FWR1	Flash Program Control Register 1	R/W		0 0 0 0 0 0 0 0$_B$
0000CC$_H$	SSR0	Sector Conversion Setting Register	R/W		0 0 XXXXX 0$_B$
001FF0$_H$	PADR0	Program address detection register 0	R/W	Address matching detection function	XXXXXXXX$_B$
001FF1$_H$					XXXXXXXX$_B$
001FF2$_H$					XXXXXXXX$_B$
001FF3$_H$	PADR1	Program address detection register 1	R/W		XXXXXXXX$_B$
001FF4$_H$					XXXXXXXX$_B$
001FF5$_H$					XXXXXXXX$_B$
007900$_H$ to 007917$_H$	VRAM	LCD display RAM	R/W	LCD controller/ driver	XXXXXXXX$_B$

- Read/Write
  R/W : Readable and Writable
  R : Read only
  W : Write only

- Initial values
  0 : Initial Value is “0”.
  1 : Initial Value is “1”.
  X : Initial Value is Indeterminate.
  - : Unused bit

■ INTERRUPT SOURCES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS readiness	Interrupt vector			Interrupt control register		Priority
		Number*		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	#09	09H	FFFFD8H	—	—	
Exceptional treatment	×	#10	0AH	FFFFD4H	—	—	
DTP/External interrupt ch.0	○	#11	0BH	FFFFD0H	ICR00	0000B0H	
DTP/External interrupt ch.1	○	#13	0DH	FFFFC8H	ICR01	0000B1H	
Serial I/O ch.2	×	#15	0FH	FFFFC0H	ICR02	0000B2H	
DTP/External interrupt ch.2/ch.3	○	#16	10H	FFFFBCH			
Serial I/O ch.3	×	#17	11H	FFFFB8H	ICR03	0000B3H	
16-bit free-run timer	○	#18	12H	FFFFB4H			
Watch timer	×	#19	13H	FFFFB0H	ICR04	0000B4H	
16-bit Reload Timer ch.2	○	#21	15H	FFFFA8H	ICR05	0000B5H	
16-bit Reload Timer ch.0	△	#23	17H	FFFFA0H	ICR06	0000B6H	
16-bit Reload Timer ch.1	△	#24	18H	FFFF9CH			
Input capture ch.0	△	#25	19H	FFFF98H	ICR07	0000B7H	
Input capture ch.1	△	#26	1AH	FFFF94H			
PPG timer ch.0 counter-borrow	○	#27	1BH	FFFF90H	ICR08	0000B8H	
Output compare match	○	#29	1DH	FFFF88H	ICR09	0000B9H	
PPG timer ch.1 counter-borrow	○	#31	1FH	FFFF80H	ICR10	0000BAH	
Time-base timer	×	#33	21H	FFFF78H	ICR11	0000BBH	
UART0 reception end	◎	#35	23H	FFFF70H	ICR12	0000BCH	
UART0 transmission end	△	#36	24H	FFFF6CH			
A/D converter conversion termination	○	#37	25H	FFFF68H	ICR13	0000BDH	
I²C Interface	×	#38	26H	FFFF64H			
UART1 : Reception	◎	#39	27H	FFFF60H	ICR14	0000BEH	
UART1 : Transmission	△	#40	28H	FFFF5CH			
Flash memory status	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delayed interrupt output module	×	#42	2AH	FFFF54H			Low

○ : Available
× : Unavailable
◎ : Available EI²OS function is provided.
△ : Available when a cause of interrupt sharing a same ICR is not used.

* : When interrupts of the same level are output at the same time, the interrupt with the smallest interrupt vector number has the priority.
- For a resource that has two interrupt causes in the same interrupt control register (ICR), use of EI²OS is enabled, EI²OS is started upon detection of one of the interrupt causes. As interrupts other than the start cause are masked during EI²OS start, masking one of the interrupt causes is recommended when using EI²OS.
- For a resource that has two interrupt causes in the same interrupt control register (ICR), the interrupt flag is cleared by an EI²OS interrupt clear signal.