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MB91460C Series

FR60 32-bit Microcontroller

MB91460C series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART and CAN controllers.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal peripheral resources

- General-purpose ports : Maximum 104 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously.
  - 2 transfer sources (internal peripheral/software)
  - Activation source can be selected using software
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200H to 240H, 1000H to 1024H)
- A/D converter (successive approximation type)
  - 10-bit resolution: 30 channels
  - Conversion time: minimum 1 µs
- External interrupt inputs : 15 channels
  - 8 channels shared with CAN RX or I^2C pins
- Bit search module (for REALOS)
  - Function to search the first bit position of “1”, “0”, “changed” from the MSB (most significant bit) within one word
- LIN-USART (full duplex double buffer): 5 channels
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
- I^2C bus interface (supports 400 kbps): 3 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 3 channels
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Stepper motor controller : 6 channels
  - 4 high current output to each channel
  - 2 synchronized PWMs per channel (8/10-bit)
- Sound generator : 1 channel
  - Tone frequency : PWM frequency divide-by-two (reload value + 1)
- Alarm comparator : 1 channel
  - Monitor external voltage
  - Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : 12 channels
- 16-bit PFM timer : 1 channel
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 4 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 3 channels (3*8-bit or 2*16-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit
- Clock supervisor
  - Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor

- Sub-clock calibration
  - Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer
  - Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
  - Sub-oscillator stabilization timer
  - Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

Note: MB91F463CA is under development.

Package and technology

- Package: QFP-144
- CMOS 180 nm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 105°C

Contents

1. Product Lineup

Feature	MB91V460	MB91F463CA	MB91F465CA	MB91F467CA MB91F467CB
Max. core frequency (CLKB)	80 MHz	100 MHz	100 MHz	100 MHz
Max. resource frequency (CLKP)	40 MHz	50 MHz	50 MHz	50 MHz
Max. external bus frequency (CLKT)	40 MHz	-	-	-
Max. CAN frequency (CLKCAN)	20 MHz	50 MHz	50 MHz	50 MHz
Max. FlexRay frequency (SCLK)	-	-	-	-
Technology	0.35µm	0.18µm	0.18µm	0.18µm
Watchdog timer	yes	yes	yes	yes
Watchdog timer (RC osc. based)	yes (disengageable)	yes	yes	yes
Bit Search	yes	yes	yes	yes
Reset input (INITX)	yes	yes	yes	yes
Hardware standby input (HSTX)	yes	no	no	no
Clock Modulator	yes	yes	yes	yes
Clock Monitor	yes	yes	yes	yes
Low Power Mode	yes	yes	yes	yes
DMA	5 ch	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch)*1	MPU (4 ch)*1	MPU (8 ch)*1	MPU (8 ch)*1
Flash memory	Emulation SRAM 32bit read data	288 KByte	544 KByte	1088 KByte
Satellite Flash memory	-	-	-	-
Flash Protection	-	yes	yes	yes
D-RAM	64 KByte	16 KByte	16 KByte	32 KByte
ID-RAM	64 KByte	8 KByte	16 KByte	32 KByte
Flash-Cache (Instruction cache)	16 KByte	4 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch	8 ch	8 ch
ICU	8 ch	8 ch	8 ch	8 ch
OCU	8 ch	4 ch	4 ch	4 ch
Reload Timer	8 ch	8 ch	8 ch	8 ch
PPG 16-bit	16 ch	12 ch	12 ch	12 ch
PFM 16-bit	1 ch	1 ch	1 ch	1 ch
Sound Generator	1 ch	1 ch	1 ch	1 ch
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	3 ch (8-bit) / 2ch (16-bit)	3 ch (8-bit) / 2ch (16-bit)	3 ch (8-bit) / 2ch (16-bit)
C_CAN	6 ch (128msg)	3 ch (32msg)	3 ch (32msg)	3 ch (32msg)
LIN-USART	4 ch + 4 ch FIFO + 8 ch	1 ch + 4 ch FIFO	1 ch + 4 ch FIFO	1 ch + 4 ch FIFO

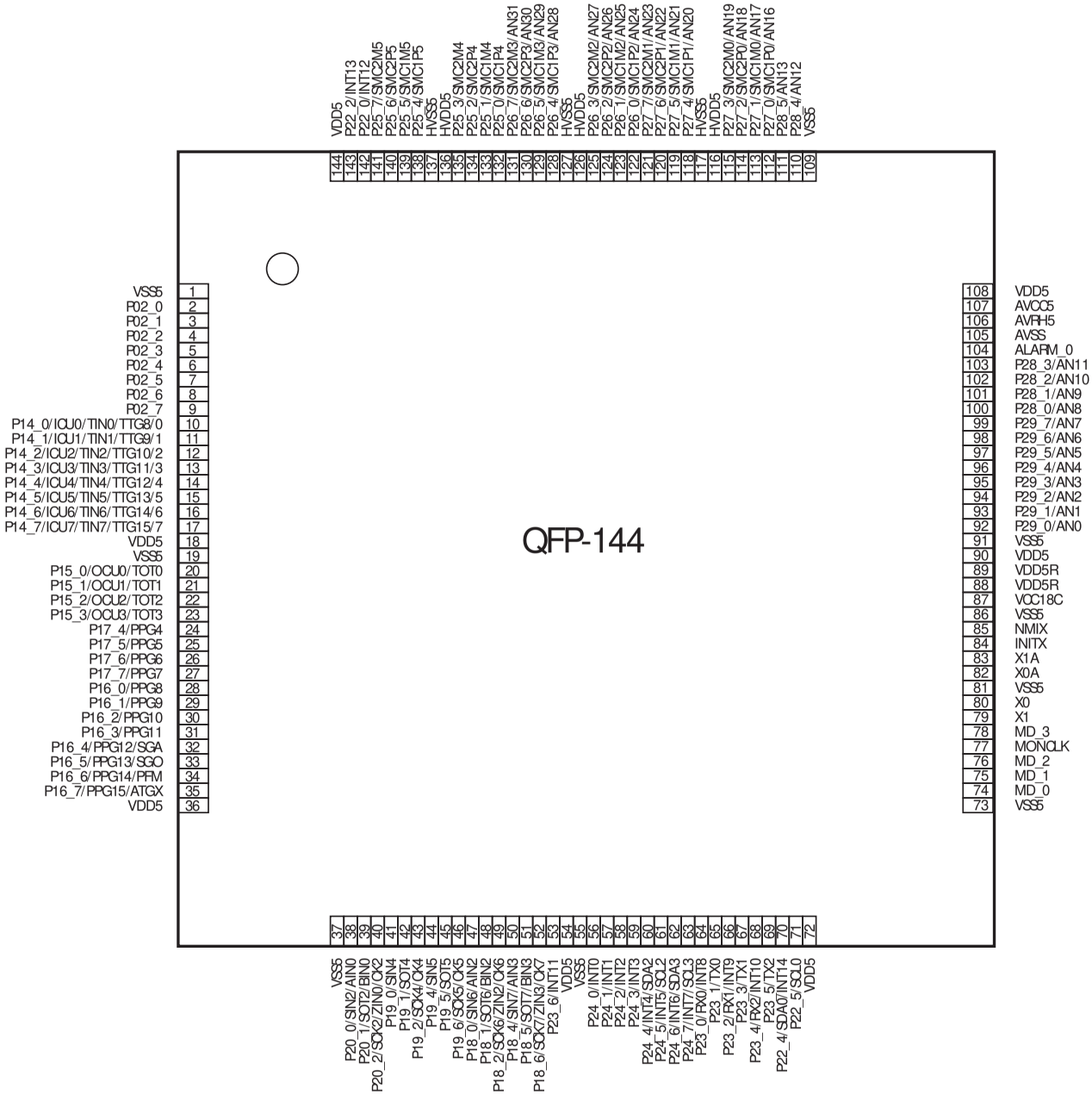
Feature	MB91V460	MB91F463CA	MB91F465CA	MB91F467CA MB91F467CB
I^2C (400K)	4 ch	3 ch	3 ch	3 ch
FR external bus	yes (32bit addr, 32bit data)	-	-	-
External Interrupts	16 ch	15 ch	15 ch	15 ch
NMI Interrupts	1 ch	1 ch	1 ch	1 ch
SMC	6 ch	6 ch	6 ch	6 ch
LCD controller (40x4)	1 ch	-	-	-
ADC (10-bit)	32 ch	30 ch	30 ch	30 ch
Alarm Comparator	2 ch	1 ch	1 ch	1 ch
Supply Supervisor (low voltage detection)	yes	yes	yes	yes
Clock Supervisor	yes	yes	yes	yes
Main clock oscillator	4 MHz	4 MHz	4 MHz	4 MHz
Sub clock oscillator	32kHz	32kHz	32kHz	32kHz
RC oscillator	100kHz	100kHz / 2MHz	100kHz / 2MHz	100kHz / 2MHz
PLL	x 20	x 25	x 25	x 25
DSU4	yes	no	no	no
EDSU	yes (32 BP)*1	yes (8 BP)*1	yes (16 BP)*1	yes (16 BP)*1
Supply voltage	3V/5V	3V/5V	3V/5V	3V/5V
Regulator	yes	yes	yes	yes
Power consumption	n.a.	< 1 W	< 1 W	< 1 W
Temperature Range (Ta)	0.70 C	-40.105 C	-40.105 C	-40.105 C
Package	BGA660	QFP-144	QFP-144	QFP-144
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 5 sec. typical	< 5 sec. typical	< 6 sec typical

*1: MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

2. Pin Assignment

2.1 MB91F463CA, MB91F465CA, MB91F467Cx

(TOP VIEW)



3. Pin Description

3.1 MB91F463CA, MB91F465CA, MB91F467Cx

Pin no.	Pin name	I/O	I/O circuit type*	Function
2 to 9	P02_0 to P02_7	I/O	A	General-purpose input/output ports
10 to 17	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN0 to TIN7			External trigger input pins of reload timer
	TTG8/0 to TTG15/7			External trigger input pins of PPG timer
20 to 23	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
24 to 27	P17_4 to P17_7	I/O	A	General-purpose input/output ports
	PPG4 to PPG7			Output pins of PPG timer
28 to 31	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			Output pins of PPG timer
32	P16_4	I/O	A	General-purpose input/output ports
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
33	P16_5	I/O	A	General-purpose input/output ports
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
34	P16_6	I/O	A	General-purpose input/output ports
	PPG14			Output pins of PPG timer
	PFM			Pulse frequency modulator output pin
35	P16_7	I/O	A	General-purpose input/output ports
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2

Pin no.	Pin name	I/O	I/O circuit type*	Function
41	P19_0	I/O	A	General-purpose input/output ports
	SIN4			Data input pin of USART4
42	P19_1	I/O	A	General-purpose input/output ports
	SOT4			Data output pin of USART4
43	P19_2	I/O	A	General-purpose input/output ports
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
44	P19_4	I/O	A	General-purpose input/output ports
	SIN5			Data input pin of USART5
45	P19_5	I/O	A	General-purpose input/output ports
	SOT5			Data output pin of USART5
46	P19_6	I/O	A	General-purpose input/output ports
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
47	P18_0	I/O	A	General-purpose input/output ports
	SIN6			Data input pin of USART6
	AIN2			Up/down counter input pin
48	P18_1	I/O	A	General-purpose input/output ports
	SOT6			Data output pin of USART6
	BIN2			Up/down counter input pin
49	P18_2	I/O	A	General-purpose input/output ports
	SCK6			Clock input/output pin of USART6
	ZIN2			Up/down counter input pin
	CK6			External clock input pin of free-run timer 6
50	P18_4	I/O	A	General-purpose input/output ports
	SIN7			Data input pin of USART7
	AIN3			Up/down counter input pin
51	P18_5	I/O	A	General-purpose input/output ports
	SOT7			Data output pin of USART7
	BIN3			Up/down counter input pin
52	P18_6	I/O	A	General-purpose input/output ports
	SCK7			Clock input/output pin of USART7
	ZIN3			Up/down counter input pin
	CK7			External clock input pin of free-run timer 7
53	P23_6	I/O	A	General-purpose input/output ports
	INT11			External Interrupt input (CAN wakeup)

Pin no.	Pin name	I/O	I/O circuit type*	Function
56 to 59	P24_0 to P24_3	I/O	A	General-purpose input/output ports
	INT0 to INT3			External Interrupt input
60	P24_4	I/O	A	General-purpose input/output ports
	INT4			External Interrupt input
	SDA2			I^2C bus DATA input/output pin (open drain)
61	P24_5	I/O	A	General-purpose input/output ports
	INT5			External Interrupt input
	SCL2			I^2C bus clock input/output pin (open drain)
62	P24_6	I/O	A	General-purpose input/output ports
	INT6			External Interrupt input
	SDA3			I^2C bus DATA input/output pin (open drain)
63	P24_7	I/O	A	General-purpose input/output ports
	INT7			External Interrupt input
	SCL3			I^2C bus clock input/output pin (open drain)
64	P23_0	I/O	A	General-purpose input/output ports
	RX0			RX input/output pin of CAN0
	INT8			External Interrupt input (CAN wakeup)
65	P23_1	I/O	A	General-purpose input/output ports
	TX0			TX output pin of CAN0
66	P23_2	I/O	A	General-purpose input/output ports
	RX1			RX input/output pin of CAN1
	INT9			External Interrupt input (CAN wakeup)
67	P23_3	I/O	A	General-purpose input/output ports
	TX1			TX output pin of CAN1
68	P23_4	I/O	A	General-purpose input/output ports
	RX2			RX input/output pin of CAN2
	INT10			External Interrupt input (CAN wakeup)
69	P23_5	I/O	A	General-purpose input/output ports
	TX2			TX output pin of CAN2
70	P22_4	I/O	A	General-purpose input/output ports
	SDA0			I^2C bus DATA input/output pin (open drain)
	INT14			External Interrupt input (I^2C wakeup)
71	P22_5	I/O	A	General-purpose input/output ports
	SCL0			I^2C bus clock input/output pin (open drain)
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	G	Clock monitor pin
78	MD_3	I	G	To be connected to VSS

Pin no.	Pin name	I/O	I/O circuit type*	Function
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) output
82	X0A	—	J2	Sub clock (oscillation) output
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-Maskable Interrupt input
92 to 99	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
100 to 103	P28_0 to P28_3	I/O	B	General-purpose input/output ports
	AN8 to AN11			Analog input pins of A/D converter
104	ALARM_0	I	I	Alarm comparator input pin
110, 111	P28_4, P28_5	I/O	B	General-purpose input/output ports
	AN12 to AN13			Analog input pins of A/D converter
112	P27_0	I/O	F	General-purpose input/output ports
	SMC1P0			Controller output pin of Stepper motor
	AN16			Analog input pins of A/D converter
113	P27_1	I/O	F	General-purpose input/output ports
	SMC1M0			Controller output pin of Stepper motor
	AN17			Analog input pins of A/D converter
114	P27_2	I/O	F	General-purpose input/output ports
	SMC2P0			Controller output pin of Stepper motor
	AN18			Analog input pins of A/D converter
115	P27_3	I/O	F	General-purpose input/output ports
	SMC2M0			Controller output pin of Stepper motor
	AN19			Analog input pins of A/D converter
118	P27_4	I/O	F	General-purpose input/output ports
	SMC1P1			Controller output pin of Stepper motor
	AN20			Analog input pins of A/D converter
119	P27_5	I/O	F	General-purpose input/output ports
	SMC1M1			Controller output pin of Stepper motor
	AN21			Analog input pins of A/D converter
120	P27_6	I/O	F	General-purpose input/output ports
	SMC2P1			Controller output pin of Stepper motor
	AN22			Analog input pins of A/D converter
121	P27_7	I/O	F	General-purpose input/output ports
	SMC2M1			Controller output pin of Stepper motor
	AN23			Analog input pins of A/D converter

Pin no.	Pin name	I/O	I/O circuit type*	Function
122	P26_0	I/O	F	General-purpose input/output ports
	SMC1P2			Controller output pin of Stepper motor
	AN24			Analog input pins of A/D converter
123	P26_1	I/O	F	General-purpose input/output ports
	SMC1M2			Controller output pin of Stepper motor
	AN25			Analog input pins of A/D converter
124	P26_2	I/O	F	General-purpose input/output ports
	SMC2P2			Controller output pin of Stepper motor
	AN26			Analog input pins of A/D converter
125	P26_3	I/O	F	General-purpose input/output ports
	SMC2M2			Controller output pin of Stepper motor
	AN27			Analog input pins of A/D converter
128	P26_4	I/O	F	General-purpose input/output ports
	SMC1P3			Controller output pin of Stepper motor
	AN28			Analog input pins of A/D converter
129	P26_5	I/O	F	General-purpose input/output ports
	SMC1M3			Controller output pin of Stepper motor
	AN29			Analog input pins of A/D converter
130	P26_6	I/O	F	General-purpose input/output ports
	SMC2P3			Controller output pin of Stepper motor
	AN30			Analog input pins of A/D converter
131	P26_7	I/O	F	General-purpose input/output ports
	SMC2M3			Controller output pin of Stepper motor
	AN31			Analog input pins of A/D converter
132	P25_0	I/O	E	General-purpose input/output ports
	SMC1P4			Controller output pin of Stepper motor
133	P25_1	I/O	E	General-purpose input/output ports
	SMC1M4			Controller output pin of Stepper motor
134	P25_2	I/O	E	General-purpose input/output ports
	SMC2P4			Controller output pin of Stepper motor
135	P25_3	I/O	E	General-purpose input/output ports
	SMC2M4			Controller output pin of Stepper motor
138	P25_4	I/O	E	General-purpose input/output ports
	SMC1P5			Controller output pin of Stepper motor
139	P25_5	I/O	E	General-purpose input/output ports
	SMC1M5			Controller output pin of Stepper motor

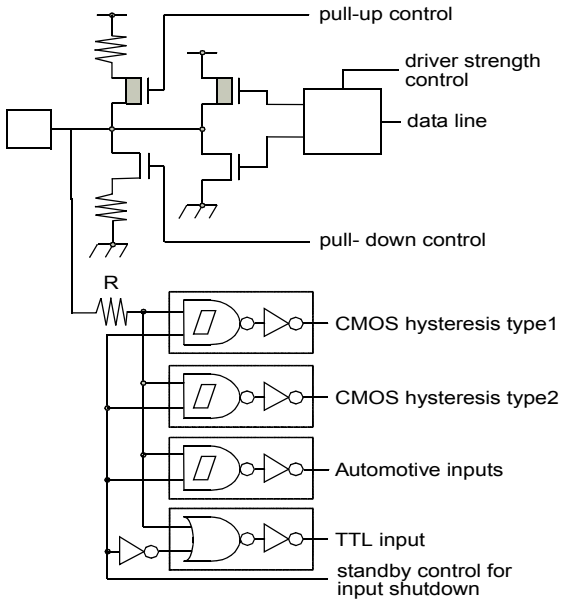
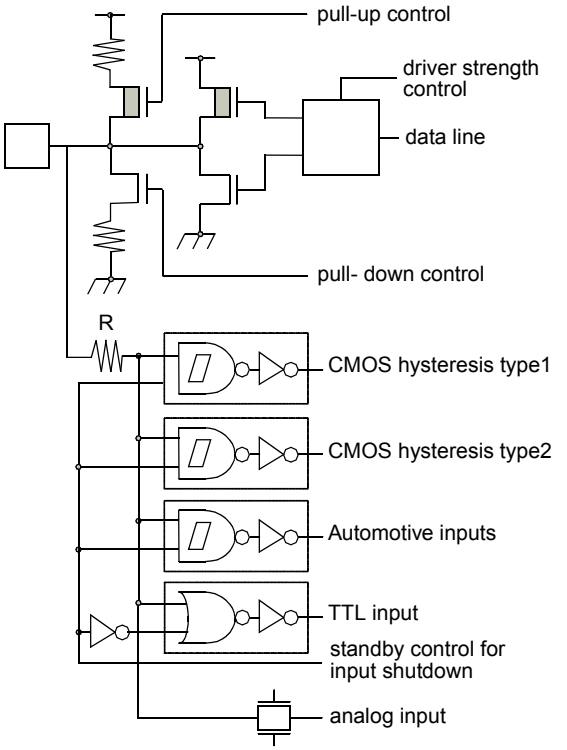
Pin no.	Pin name	I/O	I/O circuit type*	Function
140	P25_6	I/O	E	General-purpose input/output ports
	SMC2P5			Controller output pin of Stepper motor
141	P25_7	I/O	E	General-purpose input/output ports
	SMC2M5			Controller output pin of Stepper motor
142	P22_0	I/O	A	General-purpose input/output ports
	INT12			External Interrupt input (I^2C wakeup)
143	P22_2	I/O	A	General-purpose input/output ports
	INT13			External Interrupt input (I^2C wakeup)

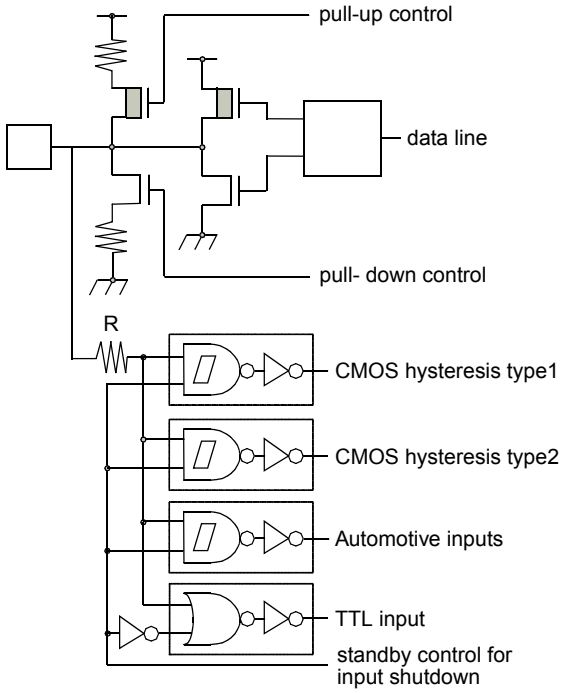
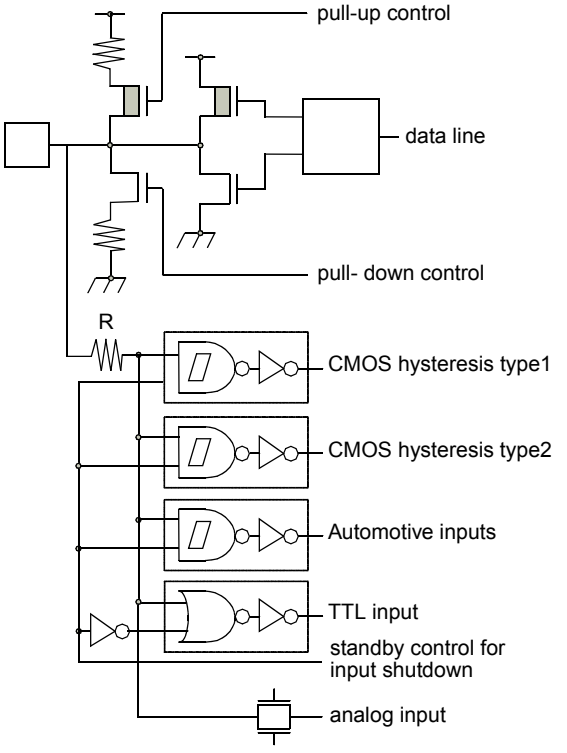
* : For information about the I/O circuit type, refer to “4. I/O Circuit Types”.

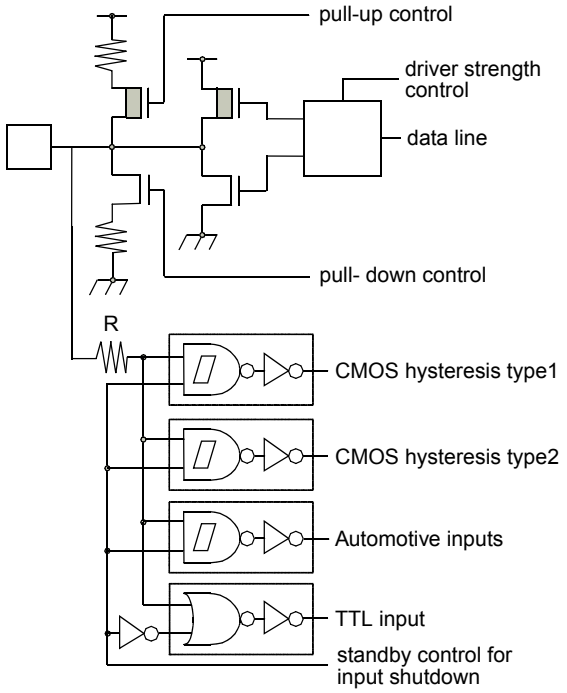
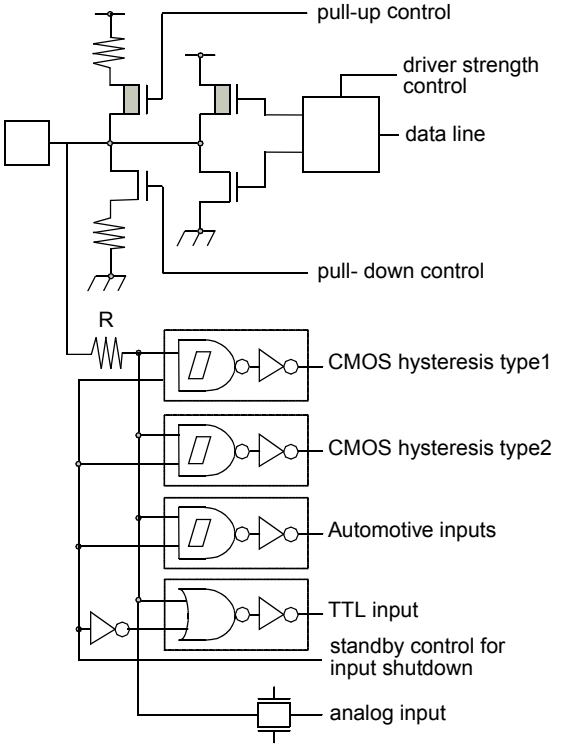
[Power supply/Ground pins]

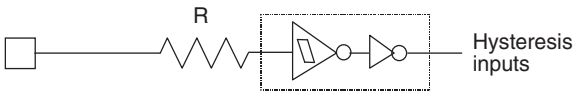
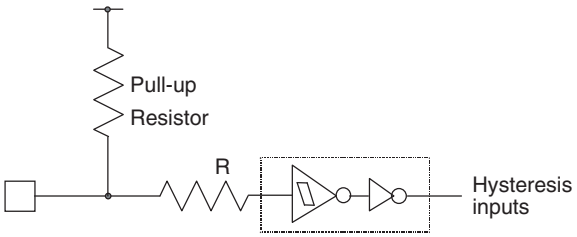
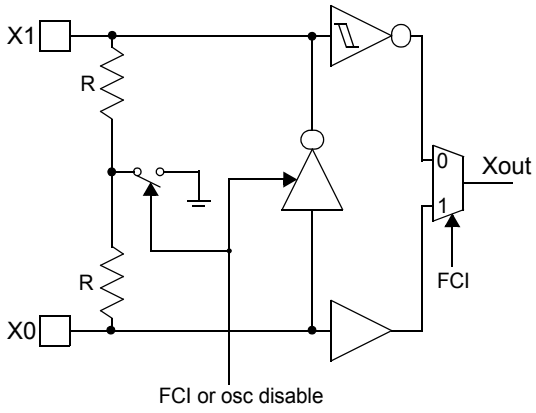
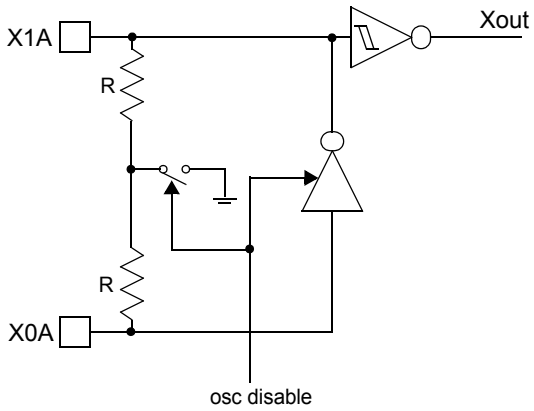
Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109	VSS5	Supply	Ground pins
117, 127, 137	HVSS5		Ground pins for Stepper motor controller
18, 36, 54, 72, 90, 108, 144	VDD5		Power supply pins
116, 126, 136	HVDD5		Power supply pins for Stepper motor controller
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator

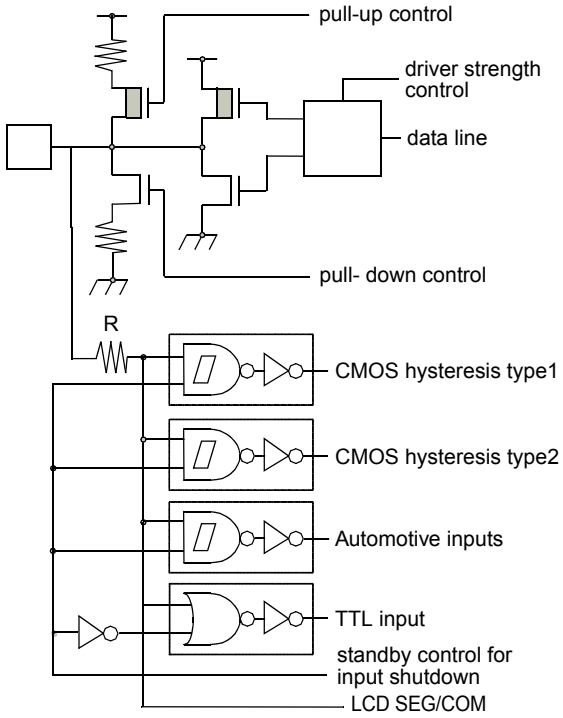
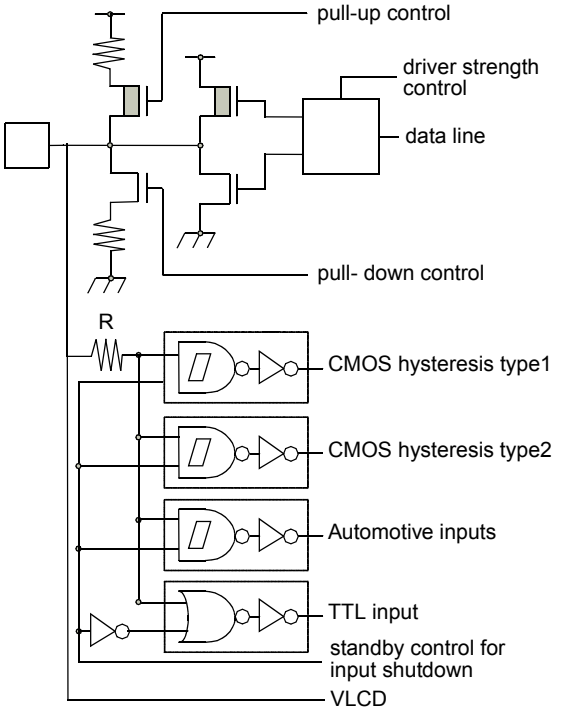
4. I/O Circuit Types

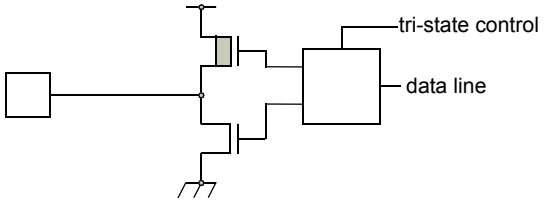
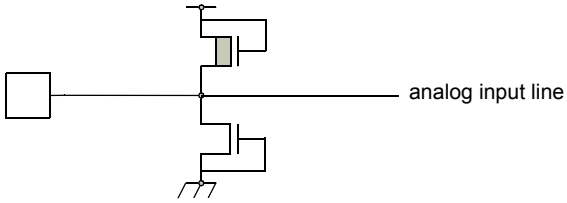
Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: • Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$ *1) or less than ($V_{SS}5$ or $HV_{SS}5$ *1) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note *1: $HV_{DD}5$, $HV_{SS}5$ are available only on devices having Stepper Motor Controller.

5.2 Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

5.3 Power supply pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 µF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

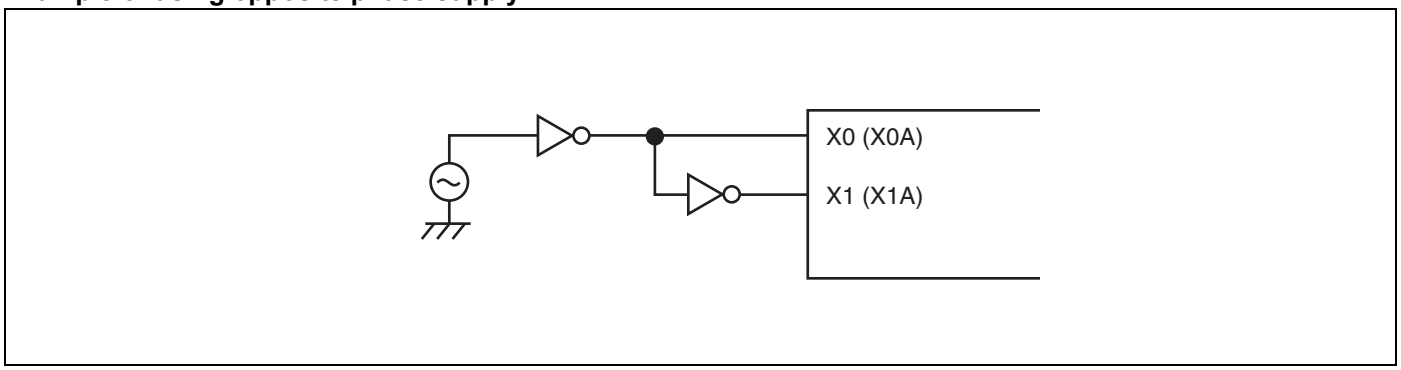
5.4 Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5.5 Notes on using external clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Example of using opposite phase supply



(Continued)

(Continued)

5.6 Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7 Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

6. Notes on Debugger

6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

6.2 Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

6.3 Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

6.4 Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

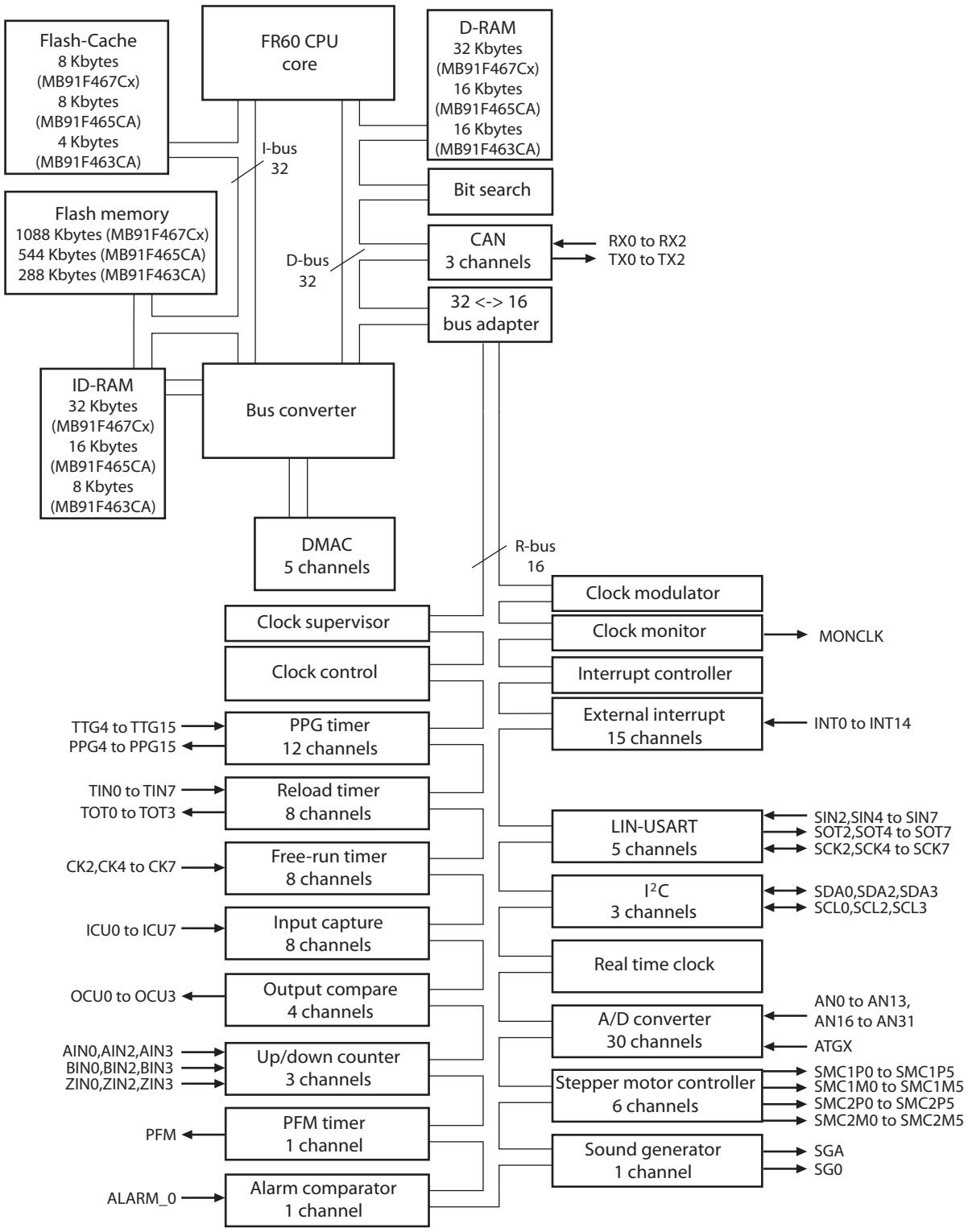
a. a user interrupt or NMI is accepted;
b. single-step execution is performed;
c. execution breaks due to a data event or from the emulator menu.
   1. D0 and D1 flags are updated in advance.
   2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
   3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.

1. The PS register is updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

7. Block Diagram

7.1 MB91F463CA, MB91F465CA, MB91F467Cx



8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

8.2 Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

8.3 Programming model

8.3.1 Basic programming model