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FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12628-2E

8-bit Microcontrollers

CMOS

New 8FX MB95310L/370L Series

MB95F314E/F314L/F316E/F316L/F318E/F318L
MB95F374E/F374L/F376E/F376L/F378E/F378L

■ DESCRIPTION

MB95310L/370L is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

■ FEATURES

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instructions
  - Bit manipulation instructions, etc.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

- Clock
  - Selectable main clock source
    Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    Main CR clock (1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz)
    Main PLL clock (up to 16.25 MHz, maximum machine clock frequency: 16.25 MHz)
  - Selectable subclock source
    Sub-OSC clock (32.768 kHz)
    External clock (32.768 kHz)
    Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)
- Timer
  - 8/16-bit composite timer
  - 8/16-bit PPG
  - 16-bit reload timer
  - Event counter
  - Time-base timer
  - Watch prescaler
- UART-SIO
  - Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer
  - Full duplex double buffer

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For the information for microcontroller supports, see the following website.

http://edevice.fujitsu.com/micom/en-support/

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FUJITSU

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- I²C
  Built-in wake-up function
- External interrupt
  - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter
  8-bit or 10-bit resolution can be selected
- LCD controller (LCDC)
  - 40 SEG × 4 COM (MB95F314E/F314L/F316E/F316L/F318E/F318L)
  - 32 SEG × 4 COM (MB95F374E/F374L/F376E/F376L/F378E/F378L)
  - Internal divider resistor
  - With blinking function
- Low power consumption (standby) modes
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode
- I/O port
  - MB95F314E/F314L/F316E/F316L/F318E/F318L (maximum no. of I/O ports: 71)
    General-purpose I/O ports (N-ch open drain) : 3
    General-purpose I/O ports (CMOS I/O) : 68
  - MB95F374E/F374L/F376E/F376L/F378E/F378L (maximum no. of I/O ports: 55)
    General-purpose I/O ports (N-ch open drain) : 3
    General-purpose I/O ports (CMOS I/O) : 52
- On-chip debug
  - 1-wire serial control
  - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
  - Built-in hardware watchdog timer
  - Built-in software watchdog timer
- Low-voltage detection reset circuit
  - Built-in low-voltage detector
  - Three configurable low-voltage detection levels for generating reset
  - Five configurable low-voltage detection levels for generating interrupts
- Clock supervisor counter
  Built-in clock supervisor counter function
- Programmable port input voltage level
  CMOS input level / hysteresis input level
- Dual operation Flash memory
  The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  Protects the content of the Flash memory

■ PRODUCT LINE-UP

• MB95310L Series

Parameter \ Part number	MB95F314E	MB95F316E	MB95F318E	MB95F314L	MB95F316L	MB95F318L
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	Yes			No		
Reset input	Dedicated					
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 71 • CMOS I/O : 68 • N-ch open drain: 3					
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	2 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	4 channels					
	8-bit or 10-bit resolution can be selected.					

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Part number / Parameter	MB95F314E	MB95F316E	MB95F318E	MB95F314L	MB95F316L	MB95F318L
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
LCD controller (LCDC)	• COM output: 4 (Max) • SEG output: 40 (Max) • LCD drive power supply (bias) pin: 4 (Max) • 40 SEG × 4 COM: 160 pixels can be displayed					
	• Duty LCD mode • Operate in LCD standby mode • Blinking function • Internal divider resistor for LCD drive					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel” • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source of 1 second and setting counter value to 60)					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-80P-M37					

- MB95370L Series

Part number / Parameter	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	Yes			No		
Reset input	Dedicated					
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max): 55 • CMOS I/O: 52 • N-ch open drain: 3					
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	2 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	4 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					

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Part number / Parameter	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
LCD controller (LCDC)	• COM output: 4 (Max) • SEG output: 32 (Max) • LCD drive power supply (bias) pin: 3 (Max) • 32 SEG × 4 COM: 128 pixels can be displayed					
	• Duty LCD mode • Operate in LCD standby mode • Blinking function • Internal divider resistor for LCD drive					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel“ • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source of 1 second and setting counter value to 60)					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-64P-M38 FPT-64P-M39					

■ OSCILLATION STABILIZATION WAIT TIME

The main CR clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{10} - 2) / F_{CRH}$	Approx. 128 µs (when the main CR clock is 8 MHz)

The main PLL clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{14} - 2) / F_{CH}$	Approx. 14.1 ms (when the main PLL clock is 4 MHz)

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95F314E	MB95F316E	MB95F318E	MB95F314L	MB95F316L	MB95F318L
FPT-80P-M37	O					
FPT-64P-M38	X					
FPT-64P-M39	X					

Part number / Package	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
FPT-80P-M37	X					
FPT-64P-M38	O					
FPT-64P-M39	O					

O: Available
X: Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

• Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “■ ELECTRICAL CHARACTERISTICS”.

• Package

For details of information on each package, see “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSION”.

• Operating voltage

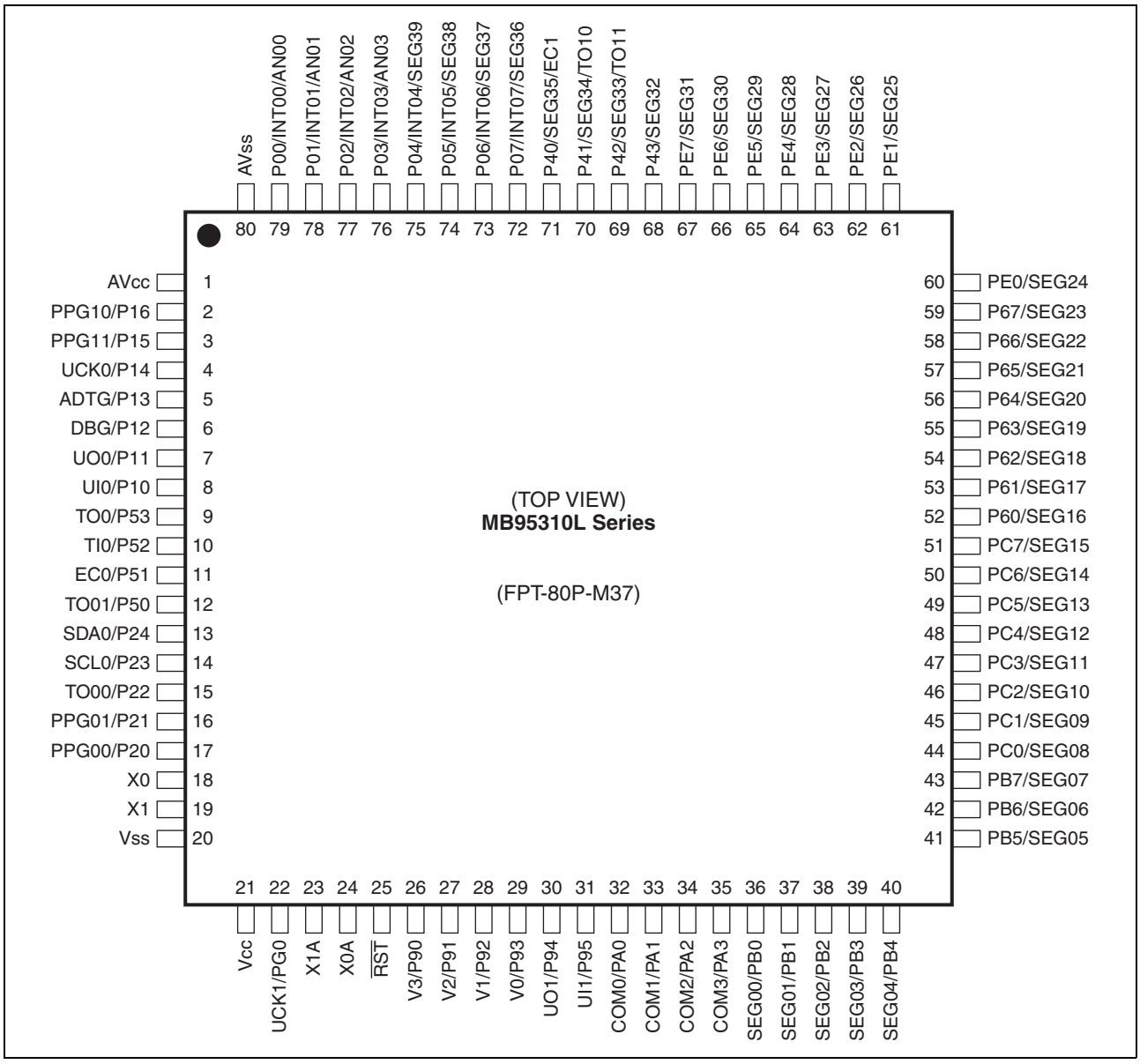
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “■ ELECTRICAL CHARACTERISTICS”.

• On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 31 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in the hardware manual of the MB95310L/370L Series.

■ PIN ASSIGNMENT



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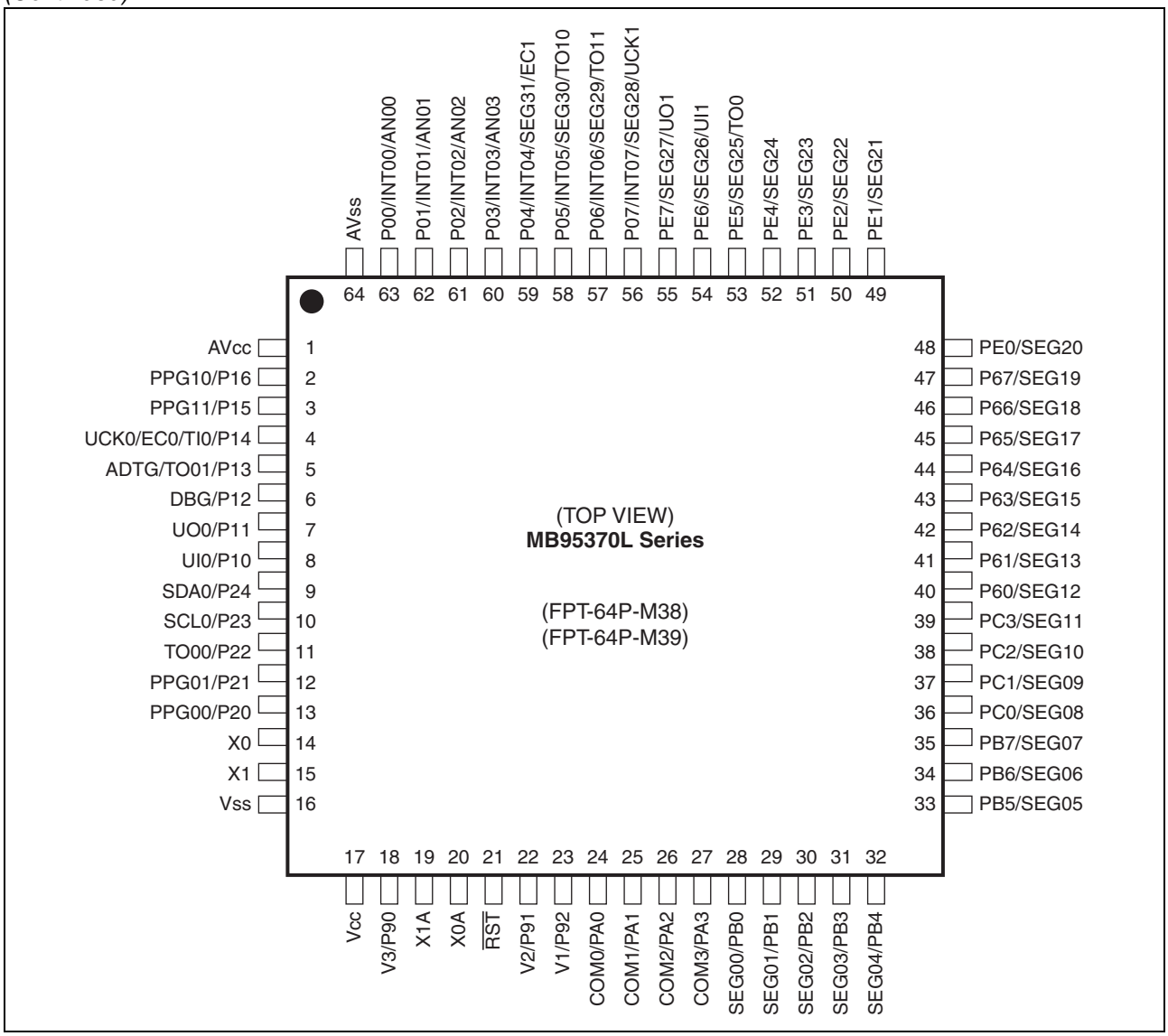
AVss
P00/INT00/AN00
P01/INT01/AN01
P02/INT02/AN02
P03/INT03/AN03
P04/INT04/SEG31/EC1
P05/INT05/SEG30/TO10
P06/INT06/SEG29/TO11
P07/INT07/SEG28/UCK1
PE7/SEG27/UO1
PE6/SEG26/UI1
PE5/SEG25/TO0
PE4/SEG24
PE3/SEG23
PE2/SEG22
PE1/SEG21
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
PPG10/P16 2
PPG11/P15 3
UCK0/EC0/TI0/P14 4
ADTG/TO01/P13 5
DBG/P12 6
UO0/P11 7
UI0/P10 8
SDA0/P24 9
SCL0/P23 10
TO00/P22 11
PPG01/P21 12
PPG00/P20 13
X0 14
X1 15
Vss 16
48 PE0/SEG20
47 P67/SEG19
46 P66/SEG18
45 P65/SEG17
44 P64/SEG16
43 P63/SEG15
42 P62/SEG14
41 P61/SEG13
40 P60/SEG12
39 PC3/SEG11
38 PC2/SEG10
37 PC1/SEG09
36 PC0/SEG08
35 PB7/SEG07
34 PB6/SEG06
33 PB5/SEG05
(TOP VIEW)
MB95370L Series
(FPT-64P-M38)
(FPT-64P-M39)
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
Vcc
V3/P90
X1A
X0A
RST
V2/P91
V1/P92
COM0/PA0
COM1/PA1
COM2/PA2
COM3/PA3
SEG00/PB0
SEG01/PB1
SEG02/PB2
SEG03/PB3
SEG04/PB4

■ PIN DESCRIPTION (MB95310L Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P16	H	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
3	P15	H	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
4	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
5	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
6	P12	C	General-purpose I/O port
	DBG		DBG input pin
7	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
8	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
9	P53	H	General-purpose I/O port
	TO0		16-bit reload timer ch. 0 output pin
10	P52	H	General-purpose I/O port
	TI0		16-bit reload timer ch. 0 input pin The pin can also be used as the event counter input pin when the event counter function is used.
11	P51	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
12	P50	H	General-purpose I/O port
	TO01		8/16-bit composite timer ch. 0 output pin
13	P24	I	General-purpose I/O port
	SDA0		I^2C data I/O pin
14	P23	I	General-purpose I/O port
	SCL0		I^2C clock I/O pin
15	P22	H	General-purpose I/O port
	TO00		8/16-bit composite timer ch. 0 output pin
16	P21	H	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
17	P20	H	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
18	X0	A	Main clock oscillation pin
19	X1	A	Main clock oscillation pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
20	V_{SS}	—	Power supply pin (GND)
21	V_{CC}	—	Power supply pin
22	PG0	H	General-purpose I/O port
	UCK1		UART/SIO ch. 1 clock I/O pin
23	X1A	A	Subclock oscillation pin (32 kHz)
24	X0A	A	Subclock oscillation pin (32 kHz)
25	$\overline{RST}$	B	Reset pin
26	P90	R	General-purpose I/O port
	V3		LCDC drive power supply pin
27	P91	R	General-purpose I/O port
	V2		LCDC drive power supply pin
28	P92	R	General-purpose I/O port
	V1		LCDC drive power supply pin
29	P93	R	General-purpose I/O port
	V0		LCDC drive power supply pin
30	P94	H	General-purpose I/O port
	UO1		UART/SIO ch. 0 data output pin
31	P95	G	General-purpose I/O port
	UI1		UART/SIO ch. 0 data input pin
32	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
33	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
34	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
35	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
36	PB0	M	General-purpose I/O port
	SEG00		LCDC SEG output pin
37	PB1	M	General-purpose I/O port
	SEG01		LCDC SEG output pin
38	PB2	M	General-purpose I/O port
	SEG02		LCDC SEG output pin
39	PB3	M	General-purpose I/O port
	SEG03		LCDC SEG output pin
40	PB4	M	General-purpose I/O port
	SEG04		LCDC SEG output pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
41	PB5	M	General-purpose I/O port
	SEG05		LCDC SEG output pin
42	PB6	M	General-purpose I/O port
	SEG06		LCDC SEG output pin
43	PB7	M	General-purpose I/O port
	SEG07		LCDC SEG output pin
44	PC0	M	General-purpose I/O port
	SEG08		LCDC SEG output pin
45	PC1	M	General-purpose I/O port
	SEG09		LCDC SEG output pin
46	PC2	M	General-purpose I/O port
	SEG10		LCDC SEG output pin
47	PC3	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
48	PC4	M	General-purpose I/O port
	SEG12		LCDC SEG output pin
49	PC5	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
50	PC6	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
51	PC7	M	General-purpose I/O port
	SEG15		LCDC SEG output pin
52	P60	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
53	P61	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
54	P62	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
55	P63	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
56	P64	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
57	P65	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
58	P66	M	General-purpose I/O port
	SEG22		LCDC SEG output pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
59	P67	M	General-purpose I/O port
	SEG23		LCDC SEG output pin
60	PE0	M	General-purpose I/O port
	SEG24		LCDC SEG output pin
61	PE1	M	General-purpose I/O port
	SEG25		LCDC SEG output pin
62	PE2	M	General-purpose I/O port
	SEG26		LCDC SEG output pin
63	PE3	M	General-purpose I/O port
	SEG27		LCDC SEG output pin
64	PE4	M	General-purpose I/O port
	SEG28		LCDC SEG output pin
65	PE5	M	General-purpose I/O port
	SEG29		LCDC SEG output pin
66	PE6	N	General-purpose I/O port
	SEG30		LCDC SEG output pin
67	PE7	M	General-purpose I/O port
	SEG31		LCDC SEG output pin
68	P43	M	General-purpose I/O port
	SEG32		LCDC SEG output pin
69	P42	M	General-purpose I/O port
	SEG33		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
70	P41	M	General-purpose I/O port
	SEG34		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin
71	P40	M	General-purpose I/O port
	SEG35		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
72	P07	Q	General-purpose I/O port
	INT07		External interrupt input pin
	SEG36		LCDC SEG output pin
73	P06	Q	General-purpose I/O port
	INT06		External interrupt input pin
	SEG37		LCDC SEG output pin

(Continued)

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Pin no.	Pin name	I/O circuit type*	Function
74	P05	Q	General-purpose I/O port
	INT05		External interrupt input pin
	SEG38		LCDC SEG output pin
75	P04	Q	General-purpose I/O port
	INT04		External interrupt input pin
	SEG39		LCDC SEG output pin
76	P03	J	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
77	P02	J	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
78	P01	J	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
79	P00	J	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
80	AV_{SS}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

■ PIN DESCRIPTION (MB95370L Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P16	H	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
3	P15	H	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
4	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
	EC0		8/16-bit composite timer ch. 0 clock input pin The pin can also be used as the event counter input pin when the event counter function is used.
	TI0		16-bit reload timer ch. 0 input pin
5	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
	TO01		8/16-bit composite timer ch. 0 output pin
6	P12	C	General-purpose I/O port
	DBG		DBG input pin
7	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
8	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
9	P24	I	General-purpose I/O port
	SDA0		I^2C data I/O pin
10	P23	I	General-purpose I/O port
	SCL0		I^2C clock I/O pin
11	P22	H	General-purpose I/O port
	TO00		8/16-bit composite timer ch. 0 output pin
12	P21	H	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
13	P20	H	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
14	X0	A	Main clock oscillation pin
15	X1	A	Main clock oscillation pin
16	V_{SS}	—	Power supply pin (GND)
17	V_{CC}	—	Power supply pin
18	P90	R	General-purpose I/O port
	V3		LCDC drive power supply pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
19	X1A	A	Subclock oscillation pin (32 kHz)
20	X0A		Subclock oscillation pin (32 kHz)
21	$\overline{RST}$	B	Reset pin
22	P91	R	General-purpose I/O port
	V2		LCDC drive power supply pin
23	P92	R	General-purpose I/O port
	V1		LCDC drive power supply pin
24	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
25	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
26	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
27	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
28	PB0	M	General-purpose I/O port
	SEG00		LCDC SEG output pin
29	PB1	M	General-purpose I/O port
	SEG01		LCDC SEG output pin
30	PB2	M	General-purpose I/O port
	SEG02		LCDC SEG output pin
31	PB3	M	General-purpose I/O port
	SEG03		LCDC SEG output pin
32	PB4	M	General-purpose I/O port
	SEG04		LCDC SEG output pin
33	PB5	M	General-purpose I/O port
	SEG05		LCDC SEG output pin
34	PB6	M	General-purpose I/O port
	SEG06		LCDC SEG output pin
35	PB7	M	General-purpose I/O port
	SEG07		LCDC SEG output pin
36	PC0	M	General-purpose I/O port
	SEG08		LCDC SEG output pin
37	PC1	M	General-purpose I/O port
	SEG09		LCDC SEG output pin
38	PC2	M	General-purpose I/O port
	SEG10		LCDC SEG output pin

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Pin no.	Pin name	I/O circuit type*	Function
39	PC3	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
40	P60	M	General-purpose I/O port
	SEG12		LCDC SEG output pin
41	P61	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
42	P62	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
43	P63	M	General-purpose I/O port
	SEG15		LCDC SEG output pin
44	P64	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
45	P65	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
46	P66	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
47	P67	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
48	PE0	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
49	PE1	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
50	PE2	M	General-purpose I/O port
	SEG22		LCDC SEG output pin
51	PE3	M	General-purpose I/O port
	SEG23		LCDC SEG output pin
52	PE4	M	General-purpose I/O port
	SEG24		LCDC SEG output pin
53	PE5	M	General-purpose I/O port
	SEG25		LCDC SEG output pin
	TO0		16-bit reload timer ch. 0 output pin
54	PE6	N	General-purpose I/O port
	SEG26		LCDC SEG output pin
	UI1		UART/SIO ch. 1 data input pin
55	PE7	M	General-purpose I/O port
	SEG27		LCDC SEG output pin
	UO1		UART/SIO ch. 1 data output pin

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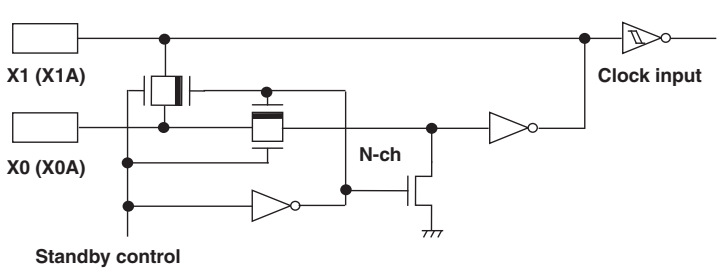
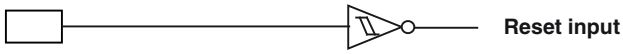
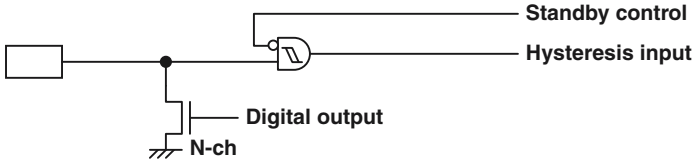
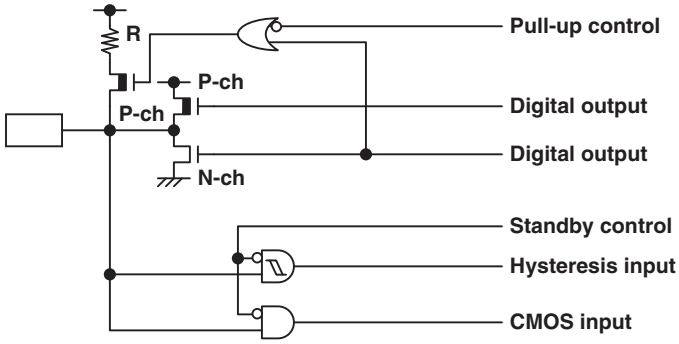
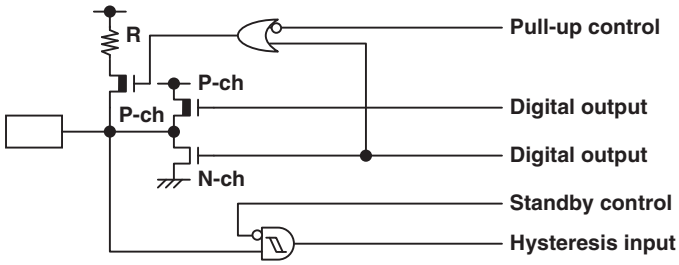
Pin no.	Pin name	I/O circuit type*	Function
56	P07	Q	General-purpose I/O port
	INT07		External interrupt input pin
	SEG28		LCDC SEG output pin
	UCK1		UART/SIO ch. 1 clock I/O pin
57	P06	Q	General-purpose I/O port
	INT06		External interrupt input pin
	SEG29		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
58	P05	Q	General-purpose I/O port
	INT05		External interrupt input pin
	SEG30		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin
59	P04	Q	General-purpose I/O port
	INT04		External interrupt input pin
	SEG31		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
60	P03	J	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
61	P02	J	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
62	P01	J	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
63	P00	J	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
64	AV_{SS}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • Low-speed side Feedback resistance: approx. 24 MΩ Dumping resistance: approx. 144 kΩ
B		Reset input
C		• N-ch open drain output • Hysteresis input
G		• CMOS output • Hysteresis input • CMOS input • Pull-up control available
H		• CMOS output • Hysteresis input • Pull-up control available

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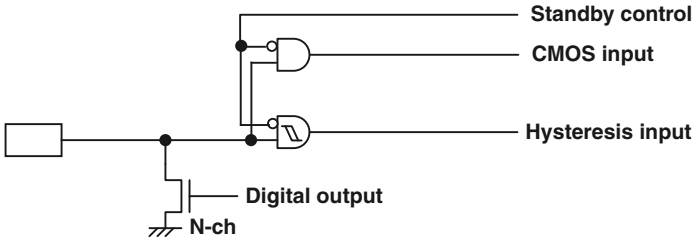
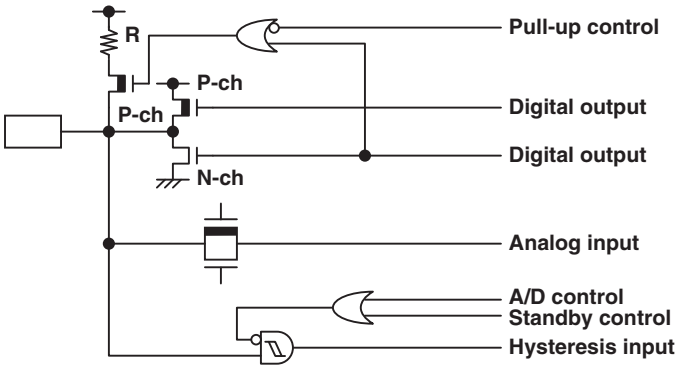
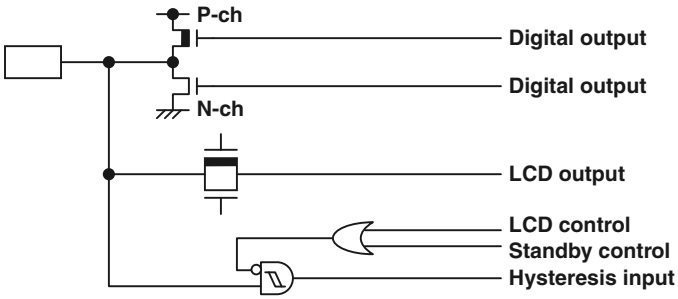
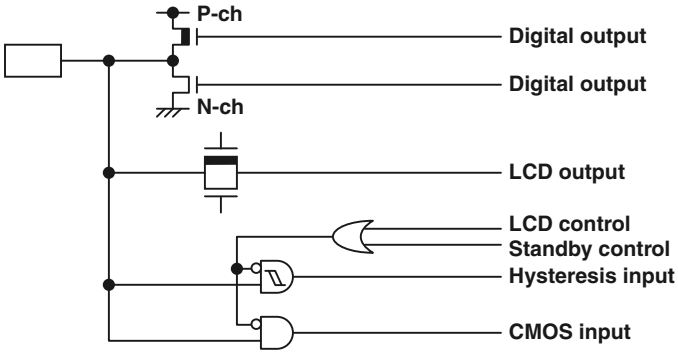
Type	Circuit	Remarks
I		• N-ch open drain output • CMOS input • Hysteresis input
J		• CMOS output • Hysteresis input • Analog input • Pull-up control available
M		• CMOS output • LCD output • Hysteresis input
N		• CMOS output • LCD output • Hysteresis input • CMOS input

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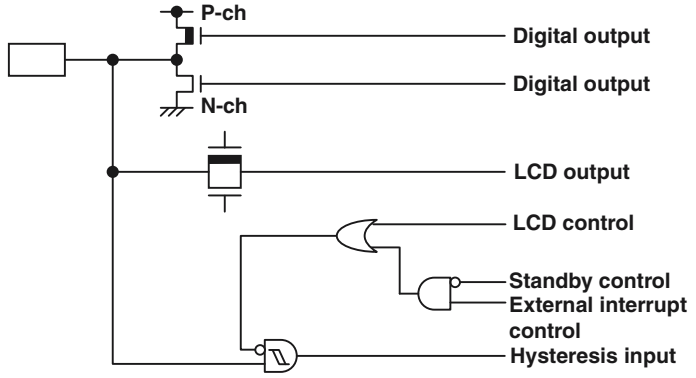
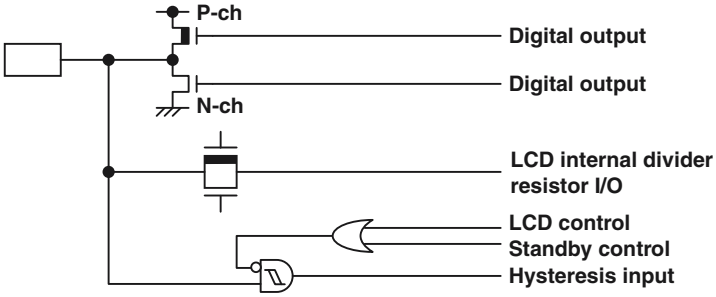
Type	Circuit	Remarks
Q		• CMOS output • LCD output • Hysteresis input
R		• CMOS output • LCD power supply • Hysteresis input

■ NOTES ON DEVICE HANDLING

• Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “1. Absolute Maximum Ratings” of “■ ELECTRICAL CHARACTERISTICS” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

• Stabilizing supply voltage

Supply voltage must be stabilized.
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

• Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

■ PIN CONNECTION

• Treatment of unused input pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

• Notes on handling the external clock pins while using the CR clock

Connect the X0 pin and the X0A pin to the V_{SS} pin and leave the X1 pin and the X1A pin unconnected.

• Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

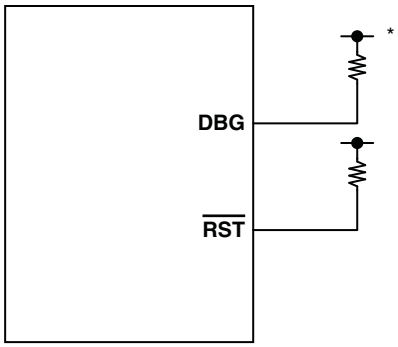
• DBG pin

Connect the DBG pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.
The DBG pin should not stay at “L” level after power-on until the reset output is released.

• $\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

- DBG/$\overline{\text{RST}}$ pins connection diagram



*: Since the DBG input pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.