Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Contact us

The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix "MB". However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix "CY".

How to Check the Ordering Part Number
1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information
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New 8FX 8-bit Microcontrollers

The MB95810K Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral resources.

Features

- F^{2}MC-8FX CPU core
  - ❏ Instruction set optimized for controllers
    - Multiplication and division instructions
    - 16-bit arithmetic operations
    - Bit test branch instructions
    - Bit manipulation instructions, etc.

- Clock
  - ❏ Selectable main clock source
    - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    - Main CR clock (4 MHz ±2%)
    - Main CR PLL clock
      - The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.
      - The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.
      - The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.
      - The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.
      - ❏ Selectable subclock source
    - Suboscillation clock (32.768 kHz)
    - External clock (32.768 kHz)
    - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

- Timer
  - ❏ 8/16-bit composite timer × 2 channels
  - ❏ 8/16-bit PPG × 2 channels
  - ❏ 16-bit PPG timer × 2 channels
  - ❏ 16-bit reload timer × 1 channel
  - ❏ Time-base timer × 1 channel
  - ❏ Watch prescaler × 1 channel

- UART/SIO × 1 channel
  - ❏ Full duplex double buffer
  - ❏ Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer

- I^{2}C bus interface × 1 channel
  - ❏ Built-in wake-up function

- LIN-UART
  - ❏ Full duplex double buffer
  - ❏ Capable of clock asynchronous serial data transfer and clock synchronous serial data transfer

- External interrupt × 12 channels
  - ❏ Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)

  - ❏ Can be used to wake up the device from different low power consumption (standby) modes

- 8/10-bit A/D converter × 12 channels
  - ❏ 8-bit or 10-bit resolution can be selected.

- Low power consumption (standby) modes
  - ❏ There are four standby modes as follows:
    - Stop mode
    - Sleep mode
    - Watch mode
    - Time-base timer mode
  - ❏ In standby mode, two further options can be selected: normal standby mode and deep standby mode.

- I/O port (no. of I/O ports: 58)
  - ❏ General-purpose I/O ports (CMOS I/O): 54
  - ❏ General-purpose I/O ports (N-ch open drain): 4

- On-chip debug
  - ❏ 1-wire serial control
  - ❏ Serial writing supported (asynchronous mode)

- Hardware/software watchdog timer
  - ❏ Built-in hardware watchdog timer
  - ❏ Built-in software watchdog timer

- Power-on reset
  - ❏ A power-on reset is generated when the power is switched on.

- Low-voltage detection (LVD) reset circuit
  - ❏ The LVD function is enabled by default. For details, see "18.2 Recommended Operating Conditions" in "Electrical Characteristics".
  - ❏ The LVD function can be controlled through software.
  - ❏ The LVD reset circuit control register (LVDCC) enables or disables the LVD reset.
  - ❏ The LVD reset circuit has an internal low-voltage detector. The combination of detection voltage and release voltage can be selected from four options.

- Comparator × 2 channels
  - ❏ Built-in dedicated BGR
  - ❏ The comparator reference voltage can be selected between the BGR voltage and the comparator pin.

- Clock supervisor counter
  - ❏ Built-in clock supervisor counter

- Dual operation Flash memory
  - ❏ The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

- Flash memory security function
  - ❏ Protects the content of the Flash memory.

Contents

1. Product Line-up

Part number / Parameter	MB95F814K	MB95F816K	MB95F818K
Type	Flash memory product		
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.		
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	512 bytes	1 Kbyte	2 Kbyte
Power-on reset	Yes		
Low-voltage detection reset	Controlled through software		
Reset input	Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)		
General-purpose I/O	• I/O port : 58 • CMOS I/O : 54 • N-ch open drain : 4		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)		
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the software watchdog timer.		
Wild register	It can be used to replace 3 bytes of data.		
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled. • The LIN function can be used as a LIN master or a LIN slave.		
8/10-bit A/D converter	12 channels		
	8-bit or 10-bit resolution can be selected.		
8/16-bit composite timer	2 channels		
	• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.		
External interrupt	12 channels		
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.		

Part number Parameter	MB95F814K	MB95F816K	MB95F818K
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).		
UART/SIO	1 channel		
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.		
I²C bus interface	1 channel		
	• Master/slave transmission and receiving • It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.		
8/16-bit PPG	2 channels		
	• Each channel can be used as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • The counter operating clock can be selected from eight clock sources.		
16-bit PPG timer	2 channels		
	• PWM mode and one-shot mode are available to use. • The counter operating clock can be selected from eight clock sources. • It supports external trigger start.		
16-bit reload timer	1 channel		
	• Two clock modes and two counter operating modes are available to use. • It can output square wave. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode		
Watch counter	• Count clock: it can be selected from eight clock sources from the watch prescaler. • The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source of one second is selected and 60 is selected as the counter value.)		
Watch prescaler	Eight different time intervals can be selected.		
Comparator	2 channels		
	The reference voltage of each channel can be selected between the BGR voltage and the comparator pin.		
Flash memory	• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Flash security feature for protecting the content of the Flash memory		

Number of program/erase cycles	1000	10000	100000
Data retention time	20 years	10 years	5 years

Part number Parameter	MB95F814K	MB95F816K	MB95F818K
Standby mode	There are four standby modes as follows: • Stop mode • Sleep mode • Watch mode • Time-base timer mode In standby mode, two further options can be selected: normal standby mode and deep standby mode		
Package	FPT-64P-M38 FPT-64P-M39		

2. Packages And Corresponding Products

Part number Package	MB95F814K	MB95F816K	MB95F818K
FPT-64P-M38	O	O	O
FPT-64P-M39	O	O	O

O: Available

3. Differences Among Products And Notes On Product Selection

• Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash program/erase.
  For details of current consumption, see "Electrical Characteristics".

• Package
  For details of information on each package, see "Packages And Corresponding Products" and "Package Dimension".

• Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see "Electrical Characteristics".

• On-chip debug function
  The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to "CHAPTER 25 EXAMPLE OF SERIAL PROGRAMMING CONNECTION" in "New 8FX MB95810K Series Hardware Manual".

4. Pin Assignment

Top-side pins (left to right, pins 64 to 49): AVss, P30/AN00/CMP0_N, P31/AN01/CMP0_P, P32/AN02/CMP0_O, P33/AN03/CMP1_N, P34/AN04/CMP1_P, P35/AN05/CMP1_O, P36/AN06, P37/AN07, P40/AN08, P41/AN09, P42/AN10, P43/AN11, P67/SIN, P66/SOT, P65/SCK

Left-side pins (top to bottom, pins 1 to 16):
1 AVcc
2 AVR
3 PE3/INT13
4 PE2/INT12
5 PE1/INT11
6 PE0/INT10
7 P83/TRG0*/ADTG*
8 P82
9 P81
10 P80
11 P71/TI0
12 P70/TO0
13 P72
14 PF0/X0
15 PF1/X1
16 Vss

Center: (TOP VIEW) LQFP64 (FPT-64P-M38) (FPT-64P-M39)

Right-side pins (top to bottom, pins 48 to 33):
48 P64/EC1
47 P63/TO11
46 P62/TO10
45 P61/PPG11
44 P60/PPG10
43 P53/TRG1
42 P52/PPG1
41 P51/SDA0
40 P50/SCL0
39 P24/EC0
38 P23/TO01
37 P22/TO00
36 P21/PPG01
35 P20/PPG00
34 P14/PPG0
33 P13/UCK0/TRG0*/ADTG*

Bottom-side pins (left to right, pins 17 to 32): Vcc, C, PG2/X1A, PG1/X0A, PF2/RST, P00/INT00, P01/INT01, P02/INT02, P03/INT03, P04/INT04, P05/INT05, P06/INT06, P07/INT07, P10/UI0, P11/UO0, P12/DBG

*: TRG0 and ADTG can be mapped to either P13 or P83 by using the SYSC register.

5. Pin Functions

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
1	AV$_{CC}$	—	Analog power supply pin for 8/10-bit A/D converter	—	—	—	—
2	AVR	—	Reference input pin for 8/10-bit A/D converter	—	—	—	—
3	PE3	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT13		External interrupt input pin				
4	PE2	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT12		External interrupt input pin				
5	PE1	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT11		External interrupt input pin				
6	PE0	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT10		External interrupt input pin				
7	P83	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TRG0*4		16-bit PPG timer ch. 0 trigger input pin				
	ADTG*4		8/10-bit A/D converter trigger input pin				
8	P82	F	General-purpose I/O port	Hysteresis	CMOS	—	O
9	P81	F	General-purpose I/O port	Hysteresis	CMOS	—	O
10	P80	F	General-purpose I/O port	Hysteresis	CMOS	—	O
11	P71	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TI0		16-bit reload timer ch. 0 input pin				
12	P70	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO0		16-bit reload timer ch. 0 output pin				
13	P72	F	General-purpose I/O port	Hysteresis	CMOS	—	O
14	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
15	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
16	V$_{SS}$	—	Power supply pin (GND)	—	—	—	—
17	V$_{CC}$	—	Power supply pin	—	—	—	—
18	C	—	Decoupling capacitor connection pin	—	—	—	—
19	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
20	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
21	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	RST		Reset pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
22	P00	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT00		External interrupt input pin				
23	P01	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT01		External interrupt input pin				
24	P02	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT02		External interrupt input pin				
25	P03	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT03		External interrupt input pin				
26	P04	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT04		External interrupt input pin				
27	P05	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT05		External interrupt input pin				
28	P06	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT06		External interrupt input pin				
29	P07	D	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT07		External interrupt input pin				
30	P10	I	General-purpose I/O port	CMOS	CMOS	—	O
	UI0		UART/SIO ch. 0 data input pin				
31	P11	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	UO0		UART/SIO ch. 0 data output pin				
32	P12	G	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
33	P13	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	UCK0		UART/SIO ch. 0 clock I/O pin				
	TRG0*4		16-bit PPG timer ch. 0 trigger input pin				
	ADTG*4		8/10-bit A/D converter trigger input pin				
34	P14	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG0		16-bit PPG timer ch. 0 output pin				
35	P20	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG00		8/16-bit PPG ch. 0 output pin				
36	P21	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG01		8/16-bit PPG ch. 0 output pin				
37	P22	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO00		8/16-bit composite timer ch. 0 output pin				
38	P23	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO01		8/16-bit composite timer ch. 0 output pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
39	P24	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	EC0		8/16-bit composite timer ch. 0 clock input pin				
40	P50	H	General-purpose I/O port	CMOS	CMOS	O	—
	SCL		I²C bus interface ch. 0 clock I/O pin				
41	P51	H	General-purpose I/O port	CMOS	CMOS	O	—
	SDA		I²C bus interface ch. 0 data I/O pin				
42	P52	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG1		16-bit PPG timer ch. 1 output pin				
43	P53	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TRG1		16-bit PPG timer ch. 1 trigger input pin				
44	P60	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG10		8/16-bit PPG ch. 1 output pin				
45	P61	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	PPG11		8/16-bit PPG ch. 1 output pin				
46	P62	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO10		8/16-bit composite timer ch. 1 output pin				
47	P63	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO11		8/16-bit composite timer ch. 1 output pin				
48	P64	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	EC1		8/16-bit composite timer ch. 1 clock input pin				
49	P65	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	SCK		LIN-UART clock I/O pin				
50	P66	F	General-purpose I/O port	Hysteresis	CMOS	—	O
	SOT		LIN-UART data output pin				
51	P67	I	General-purpose I/O port	CMOS	CMOS	—	O
	SIN		LIN-UART data input pin				
52	P43	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN11		8/10-bit A/D converter analog input pin				
53	P42	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN10		8/10-bit A/D converter analog input pin				
54	P41	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN09		8/10-bit A/D converter analog input pin				
55	P40	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN08		8/10-bit A/D converter analog input pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
56	P37	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN07		8/10-bit A/D converter analog input pin				
57	P36	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN06		8/10-bit A/D converter analog input pin				
58	P35	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN05		8/10-bit A/D converter analog input pin				
	CMP1_O		Comparator ch. 1 digital output pin				
59	P34	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN04		8/10-bit A/D converter analog input pin				
	CMP1_P		Comparator ch. 1 non-inverting analog input (positive input) pin				
60	P33	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN03		8/10-bit A/D converter analog input pin				
	CMP1_N		Comparator ch. 1 inverting analog input (negative input) pin				
61	P32	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN02		8/10-bit A/D converter analog input pin				
	CMP0_O		Comparator ch. 0 digital output pin				
62	P31	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN01		8/10-bit A/D converter analog input pin				
	CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				
63	P30	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AN00		8/10-bit A/D converter analog input pin				
	CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				
64	AV_{SS}	—	8/10-bit A/D converter power supply pin (GND)	—	—	—	—

(O: Available)
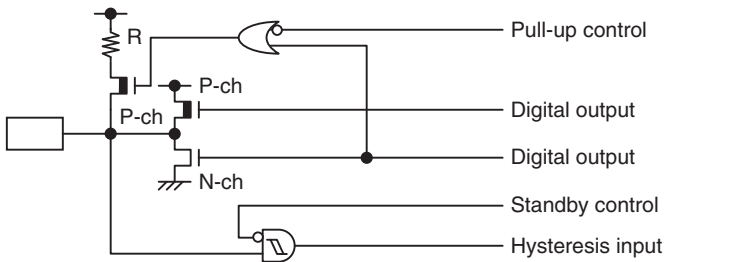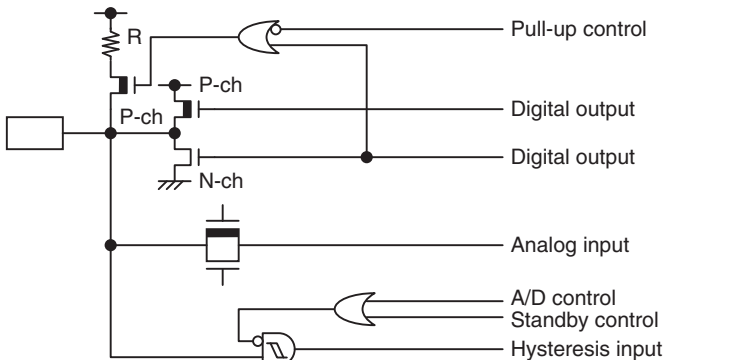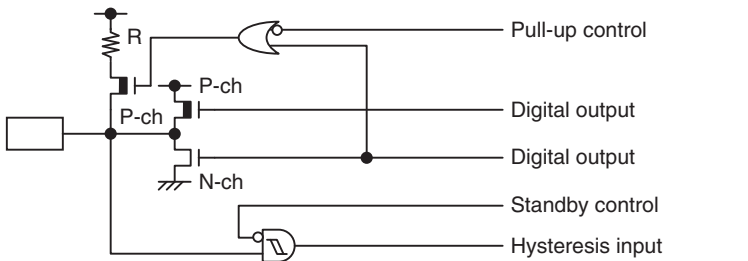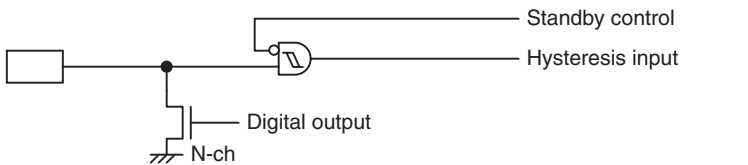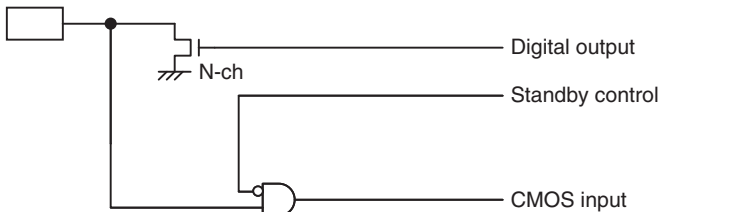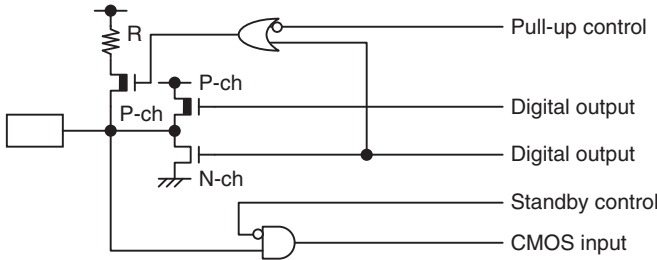*1: For the I/O circuit types, see "I/O Circuit Type".
*2: N-ch open drain
*3: Pull-up
*4: TRG0 and ADTG can be mapped to either P13 or P83 by using the SYSC register.

6. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 5 MΩ • CMOS output • Hysteresis input • Pull-up control

Type	Circuit	Remarks
D	R, P-ch, P-ch, N-ch — Pull-up control / Digital output / Digital output / Standby control / Hysteresis input	• CMOS output • Hysteresis input • Pull-up control • High current output
E	R, P-ch, P-ch, N-ch — Pull-up control / Digital output / Digital output / Analog input / A/D control / Standby control / Hysteresis input	• CMOS output • Hysteresis input • Pull-up control • Analog input
F	R, P-ch, P-ch, N-ch — Pull-up control / Digital output / Digital output / Standby control / Hysteresis input	• CMOS output • Hysteresis input • Pull-up control
G	Standby control / Hysteresis input / Digital output / N-ch	• N-ch open drain output • Hysteresis input
H	N-ch — Digital output / Standby control / CMOS input	• N-ch open drain output • CMOS input

Type	Circuit	Remarks
I		• CMOS output • CMOS input • Pull-up control

7. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

7.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

• Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

• Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

• Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

● **Latch-up**

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

● **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

● **Fail-Safe Design**

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

● **Precautions Related to Usage of Devices**

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

● **Lead Insertion Type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- **Lead-Free Packaging**

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

  Condition: 125°C/24 h

- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%.
  Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Notes On Device Handling

- Preventing latch-ups
  When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
  In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "18.1 Absolute Maximum Ratings" of "Electrical Characteristics" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
  When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage
  Supply voltage must be stabilized.
  A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
  As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock
  When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub-clock mode or stop mode.

9. Pin Connection

- Treatment of unused pins

    If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins

    To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

    It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin

    Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.

    After power-on, ensure that the DBG pin does not stay at "L" level until the reset output is released.

    The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

- $\overline{RST}$ pin

    Connect the $\overline{RST}$ pin to an external pull-up resistor of 2 kΩ or above.

    To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{RST}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.

    The PF2/$\overline{RST}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{RST}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

- Analog power supply

    Always set the same potential to the AV_{CC} pin and the V_{CC} pin. When V_{CC} is larger than AV_{CC}, the current may flow through the AN00 to AN11 pins.

- Treatment of power supply pins on the 8/10-bit A/D converter

    Ensure that AV_{CC} is equal to V_{CC} and AV_{SS} equal to V_{SS} even when the 8/10-bit A/D converter is not in use.

    Noise riding on the AV_{CC} pin may cause accuracy degradation. Therefore, connect a ceramic capacitor of 0.1 µF (approx.) as a bypass capacitor between the AV_{CC} pin and the AV_{SS} pin in the vicinity of this device.

- C pin

    Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.
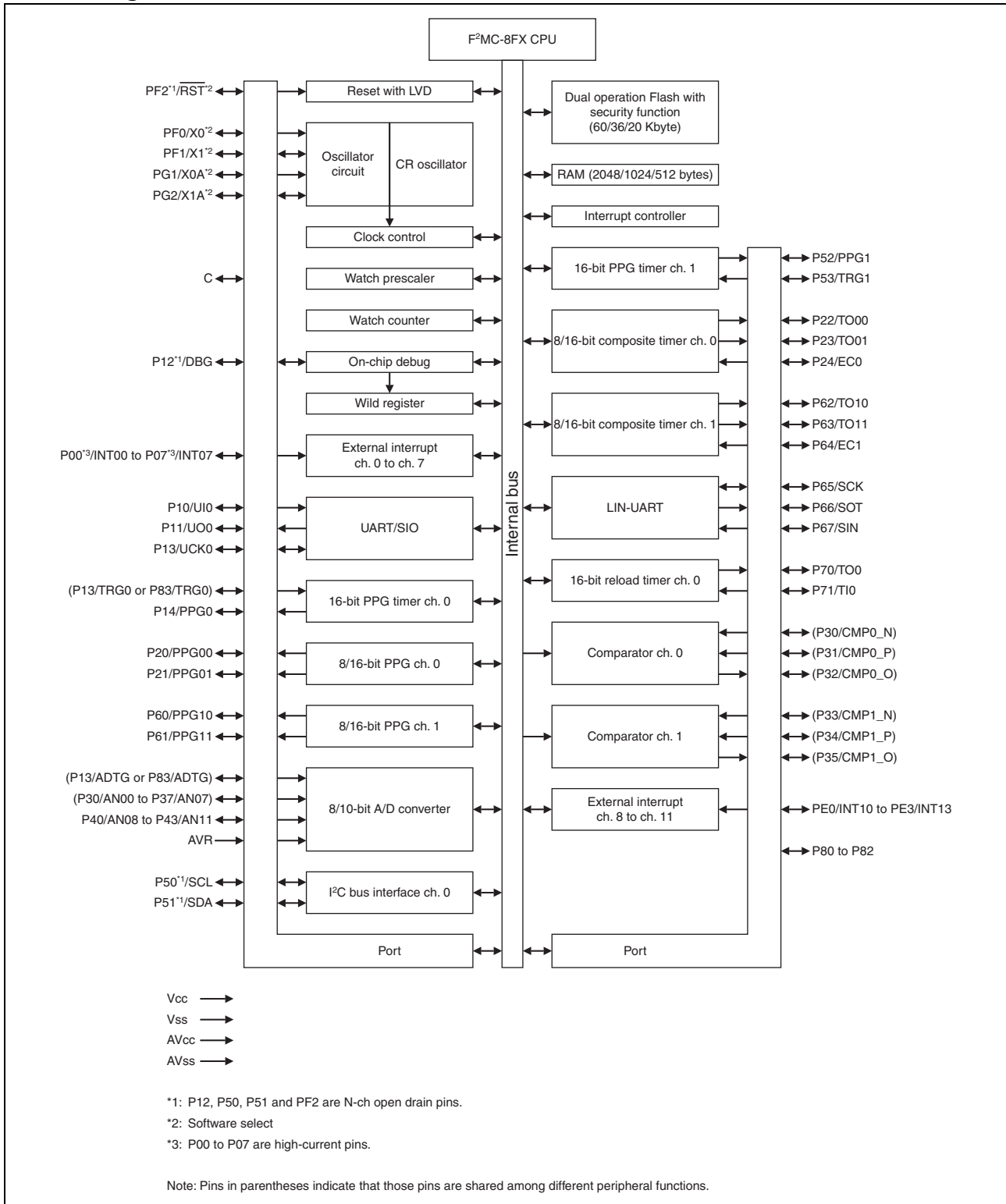
- DBG/$\overline{RST}$/C pins connection diagram
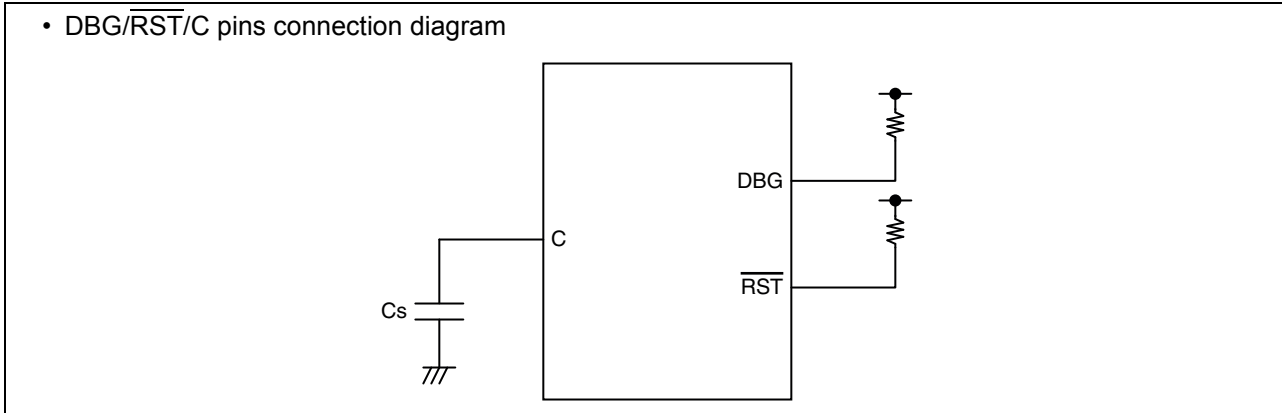
- Note on serial communication

  In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

10. Block Diagram

*1: P12, P50, P51 and PF2 are N-ch open drain pins.

*2: Software select

*3: P00 to P07 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

11. CPU Core

• Memory space

The memory space of the MB95810K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95810K Series are shown below.

• Memory maps
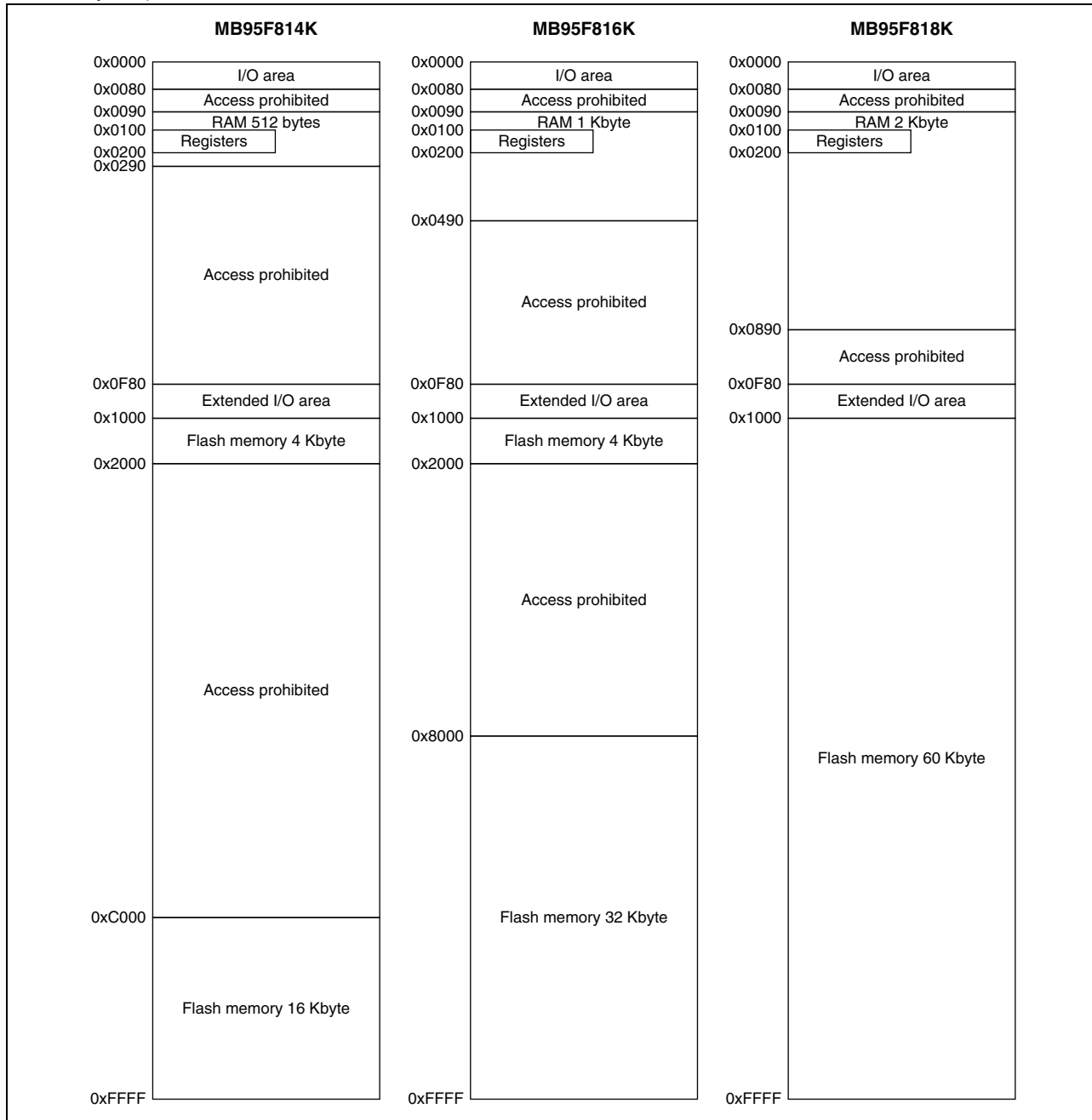
12. Memory Space

The memory space of the MB95810K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas for specific applications such as general-purpose registers and a vector table.

12.1 I/O area (addresses: 0x0000 to 0x007F)
- This area contains the control registers and data registers for built-in peripheral functions.
- As the I/O area forms part of the memory space, it can be accessed in the same way as the memory. It can also be accessed at high-speed by using direct addressing instructions.

12.2 Extended I/O area (addresses: 0x0F80 to 0x0FFF)
- This area contains the control registers and data registers for built-in peripheral functions.
- As the extended I/O area forms part of the memory space, it can be accessed in the same way as the memory.

12.3 Data area
- Static RAM is incorporated in the data area as the internal data area.
- The internal RAM size varies according to product.
- The RAM area from 0x0090 to 0x00FF can be accessed at high-speed by using direct addressing instructions.
- In MB95F818K, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F816K, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F814K, the area from 0x0090 to 0x028F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- The area from 0x0100 to 0x01FF can be used as a general-purpose register area.

12.4 Program area
- The Flash memory is incorporated in the program area as the internal program area.
- The Flash memory size varies according to product.
- The area from 0xFFC0 to 0xFFFF is used as the vector table.
- The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register.

12.5 Memory space map
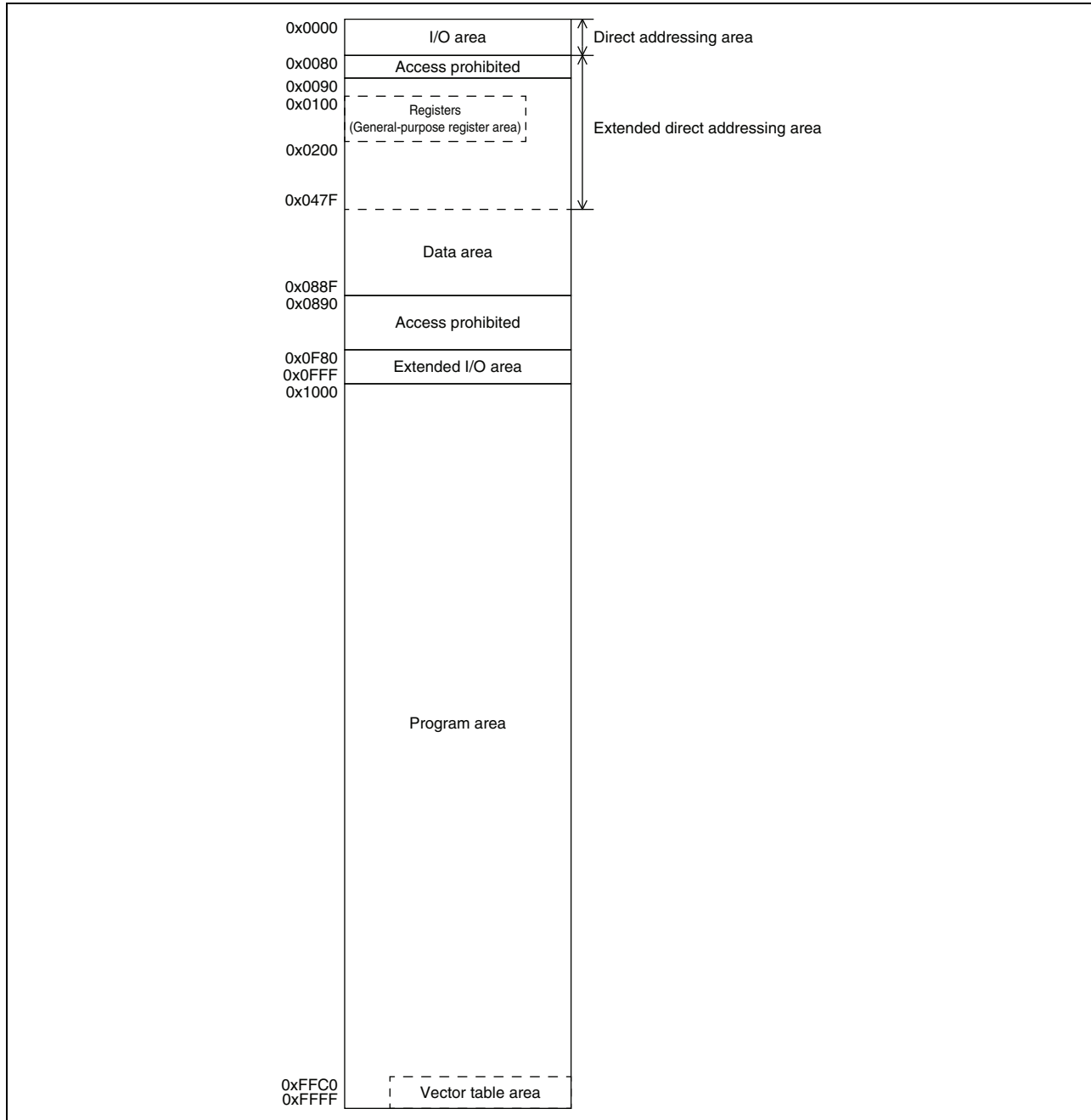
13. Areas For Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

- General-purpose register area (Addresses: 0x0100 to 0x01FF)
  - This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
  - As this area forms part of the RAM area, it can also be used as conventional RAM.
  - When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.

- Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to "CHAPTER 27 NON-VOLATILE REGISTER (NVR) INTERFACE" in "New 8FX MB95810K Series Hardware Manual".

- Vector table area (Addresses: 0xFFC0 to 0xFFFF)
  - This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
  - The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

  "Interrupt Source Table" lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.
  For details, refer to "CHAPTER 4 RESET", "CHAPTER 5 INTERRUPTS" and "A.2 Special Instruction ■ Special Instruction ● CALLV #vct" in "APPENDIX" in "New 8FX MB95810K Series Hardware Manual".

- Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001		0x0100 to 0x017F
0b010		0x0180 to 0x01FF
0b011		0x0200 to 0x027F
0b100	0x0080 to 0x00FF	0x0280 to 0x02FF[*1]
0b101		0x0300 to 0x037F
0b110		0x0380 to 0x03FF
0b111		0x0400 to 0x047F[*2]

*1: Due to the memory size limit, the available access area is up to "0x028F" in MB95F814K.
*2: Due to the memory size limit, the available access area is up to "0x047F" in MB95F816K/F818K.

14. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	PDR2	Port 2 data register	R/W	0b00000000
0x000F	DDR2	Port 2 direction register	R/W	0b00000000
0x0010	PDR3	Port 3 data register	R/W	0b00000000
0x0011	DDR3	Port 3 direction register	R/W	0b00000000
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014	PDR5	Port 5 data register	R/W	0b00000000
0x0015	DDR5	Port 5 direction register	R/W	0b00000000
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018	PDR7	Port 7 data register	R/W	0b00000000
0x0019	DDR7	Port 7 direction register	R/W	0b00000000
0x001A	PDR8	Port 8 data register	R/W	0b00000000
0x001B	DDR8	Port 8 direction register	R/W	0b00000000
0x001C	STBC2	Standby control register 2	R/W	0b00000000
0x001D to 0x0024	—	(Disabled)	—	—
0x0025	PUL8	Port 8 pull-up register	R/W	0b00000000
0x0026	PDRE	Port E data register	R/W	0b00000000
0x0027	DDRE	Port E direction register	R/W	0b00000000
0x0028	PDRF	Port F data register	R/W	0b00000000