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MB96345/346, MB96F345
MB96F346/F347/F348

F²MC-16FX, MB96340 Series, 16-bit Proprietary Microcontroller Datasheet

MB96340 series is based on Cypress advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

MB96F345 : These devices are under development and specification is preliminary. These products under development may change its specification without notice.

Features

Feature	Description
Technology	■ 0.18μm CMOS
CPU	■ F^{2}MC-16FX CPU ■ Up to 56 MHz internal, 17.8 ns instruction cycle time ■ Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) ■ 8-byte instruction execution queue ■ Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	■ On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) ■ 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). ■ Up to 56 MHz external clock for devices with fast clock input feature ■ 32-100 kHz subsystem quartz clock ■ 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog ■ Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. ■ Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) ■ Clock modulator
On-chip voltage regulator	■ Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	■ Reset is generated when supply voltage is below minimum.
Code Security	■ Protects ROM content from unintended read-out
Memory Patch Function	■ Replaces ROM content ■ Can also be used to implement embedded debug support
DMA	■ Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	■ Fast Interrupt processing ■ 8 programmable priority levels ■ Non-Maskable Interrupt (NMI)
Timers	■ Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) ■ Watchdog Timer
CAN	■ Supports CAN protocol version 2.0 part A and B ■ ISO16845 certified ■ Bit rates up to 1 Mbit/s ■ 32 message objects ■ Each message object has its own identifier mask ■ Programmable FIFO mode (concatenation of message objects) ■ Maskable interrupt ■ Disabled Automatic Retransmission mode for Time Triggered CAN applications ■ Programmable loop-back mode for self-test operation
USART	■ Full duplex USARTs (SCI/LIN) ■ Wide range of baud rate settings using a dedicated reload timer ■ Special synchronous options for adapting to different synchronous serial protocols ■ LIN functionality working either as master or slave LIN device

Feature	Description
I^2C	■ Up to 400 kbps ■ Master and Slave functionality, 8-bit and 10-bit addressing
A/D converter	■ SAR-type ■ 10-bit resolution ■ Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
A/D Converter Reference Voltage switch	■ 2 independent positive A/D converter reference voltages available
Reload Timers	■ 16-bit wide ■ Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency ■ Event count function
Free Running Timers	■ Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency
Input Capture Units	■ 16-bit wide ■ Signals an interrupt upon external event ■ Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	■ 16-bit wide ■ Signals an interrupt when a match with 16-bit I/O Timer occurs ■ A pair of compare registers can be used to generate an output signal.
Programmable Pulse Generator	■ 16-bit down counter, cycle and duty setting registers ■ Interrupt at trigger, counter borrow and/or duty match ■ PWM operation and one-shot operation ■ Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input ■ Can be triggered by software or reload timer
Real Time Clock	■ Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator ■ Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) ■ Read/write accessible second/minute/hour registers ■ Can signal interrupts every half second/second/minute/hour/day ■ Internal clock divider and prescaler provide exact 1s clock
External Interrupts	■ Edge sensitive or level sensitive ■ Interrupt mask and pending bit per channel ■ Each available CAN channel RX has an external interrupt for wake-up ■ Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	■ Disabled after reset ■ Once enabled, can not be disabled other than by reset. ■ Level high or level low sensitive ■ Pin shared with external interrupt 0.
External bus interface	■ 8-bit or 16-bit bidirectional data ■ Up to 24-bit addresses ■ 6 chip select signals ■ Multiplexed address/data lines ■ Wait state request ■ External bus master possible ■ Timing programmable

Feature	Description
Alarm comparator	■ Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds ■ Threshold voltages defined externally or generated internally ■ Status is readable, interrupts can be masked separately
I/O Ports	■ Virtually all external pins can be used as general purpose I/O ■ All push-pull outputs (except when used as I2C SDA/SCL line) ■ Bit-wise programmable as input/output or peripheral signal ■ Bit-wise programmable input enable ■ Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices) ■ Bit-wise programmable pull-up resistor ■ Bit-wise programmable output driving strength for EMI optimization
Packages	■ 100-pin plastic QFP and LQFP
Flash Memory	■ Supports automatic programming, Embedded Algorithm ■ Write/Erase/Erase-Suspend/Resume commands ■ A flag indicating completion of the algorithm ■ Number of erase cycles: 10,000 times ■ Data retention time: 20 years ■ Erase can be performed on each sector individually ■ Sector protection ■ Flash Security feature to protect the content of the Flash ■ Low voltage detection during Flash erase

Contents

1. Product Lineup

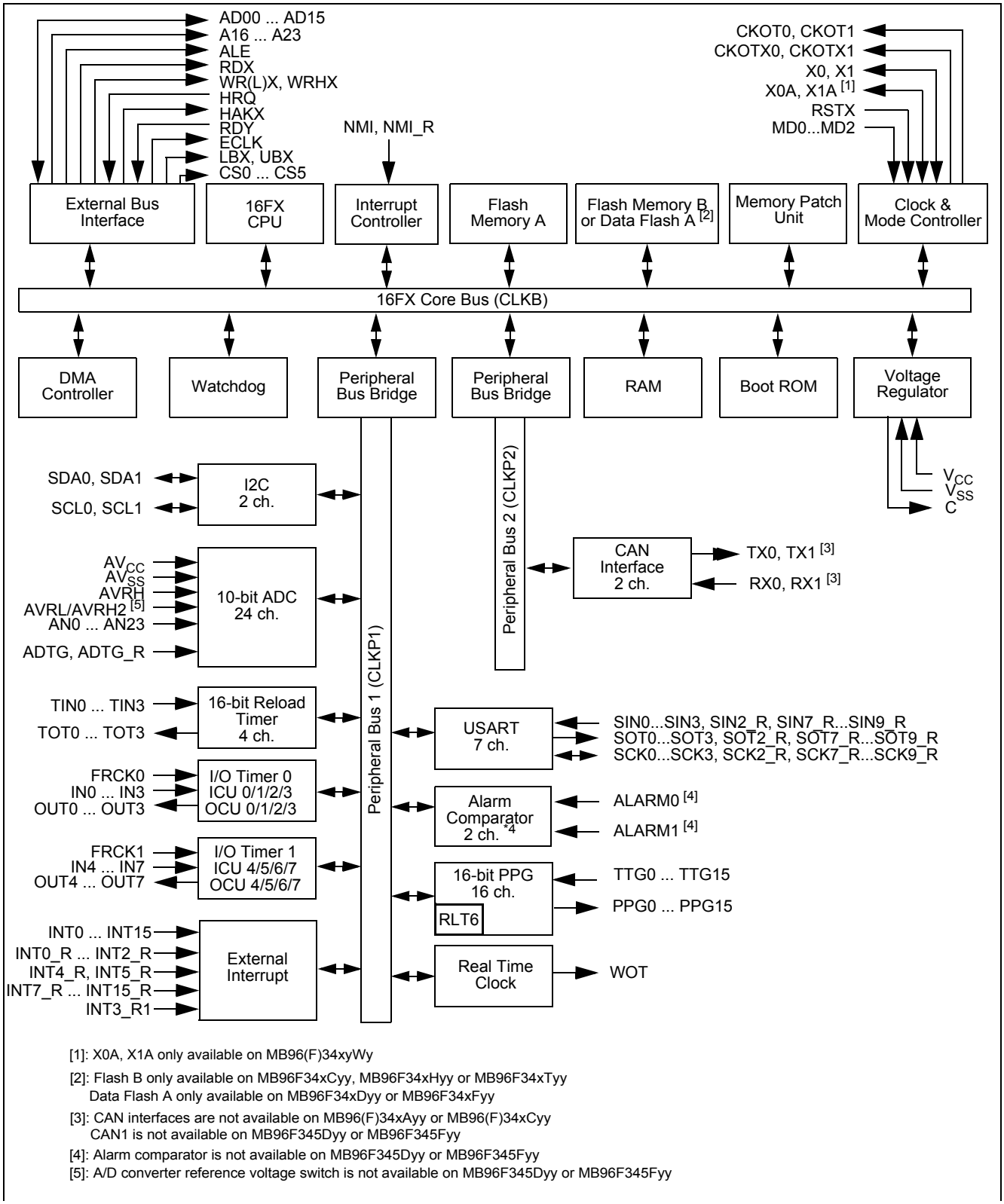
Features		MB96V300B	MB96(F)34x
Product type		Evaluation sample	Flash product: MB96F34x Mask ROM product: MB9634x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
FS			64KB Data Flash / Low voltage reset persistently on / Single clock
DS			64KB Data Flash / Low voltage reset can be disabled / Single clock
FW			64KB Data Flash / Low voltage reset persistently on / Dual clock
DW			64KB Data Flash / Low voltage reset can be disabled / Dual clock
AS			No CAN / Low voltage reset can be disabled / Single clock devices
CS			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock
AW			No CAN / Low voltage reset can be disabled / Dual clock
CW			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
160KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96345Y [1], MB96345R [1]
224KB [Flash A: 160KB, Data Flash A: 64KB]	8KB		MB96F345F [1], MB96F345D [1]
288KB	16KB		MB96F346Y, MB96346Y [1], MB96F346R, MB96346R [1], MB96F346A
416KB	16KB		MB96F347Y, MB96F347R, MB96F347A
544KB	24KB		MB96F348Y, MB96F348R, MB96F348A
576KB [Flash A: 544KB, Flash B: 32KB]	24KB		MB96F348T, MB96F348H, MB96F348C
Package		BGA416	FPT-100P-M20 FPT-100P-M22
DMA		16 channels	6 channels
USART		10 channels	7 channels

Features	MB96V300B	MB96(F)34x
I^2C	2 channels	2 channels
A/D Converter	40 channels	24 channels
A/D Converter Reference Voltage switch	yes	yes (except MB96F345Dyy or MB96F345Fyy)
16-bit Reload Timer	6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface	5 channels	MB96(F)34xAyy or MB96(F)34xCyy: no MB96F345Dyy or MB96F345Fyy: 1 channel others: 2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	MB96F345Dyy or MB96F345Fyy: no others: 2 channels
External bus interface	Yes	Yes (multiplexed address/data)
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

[1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



[1]: X0A, X1A only available on MB96(F)34xyWy

[2]: Flash B only available on MB96F34xCyy, MB96F34xHyy or MB96F34xTyy
Data Flash A only available on MB96F34xDyy or MB96F34xFyy

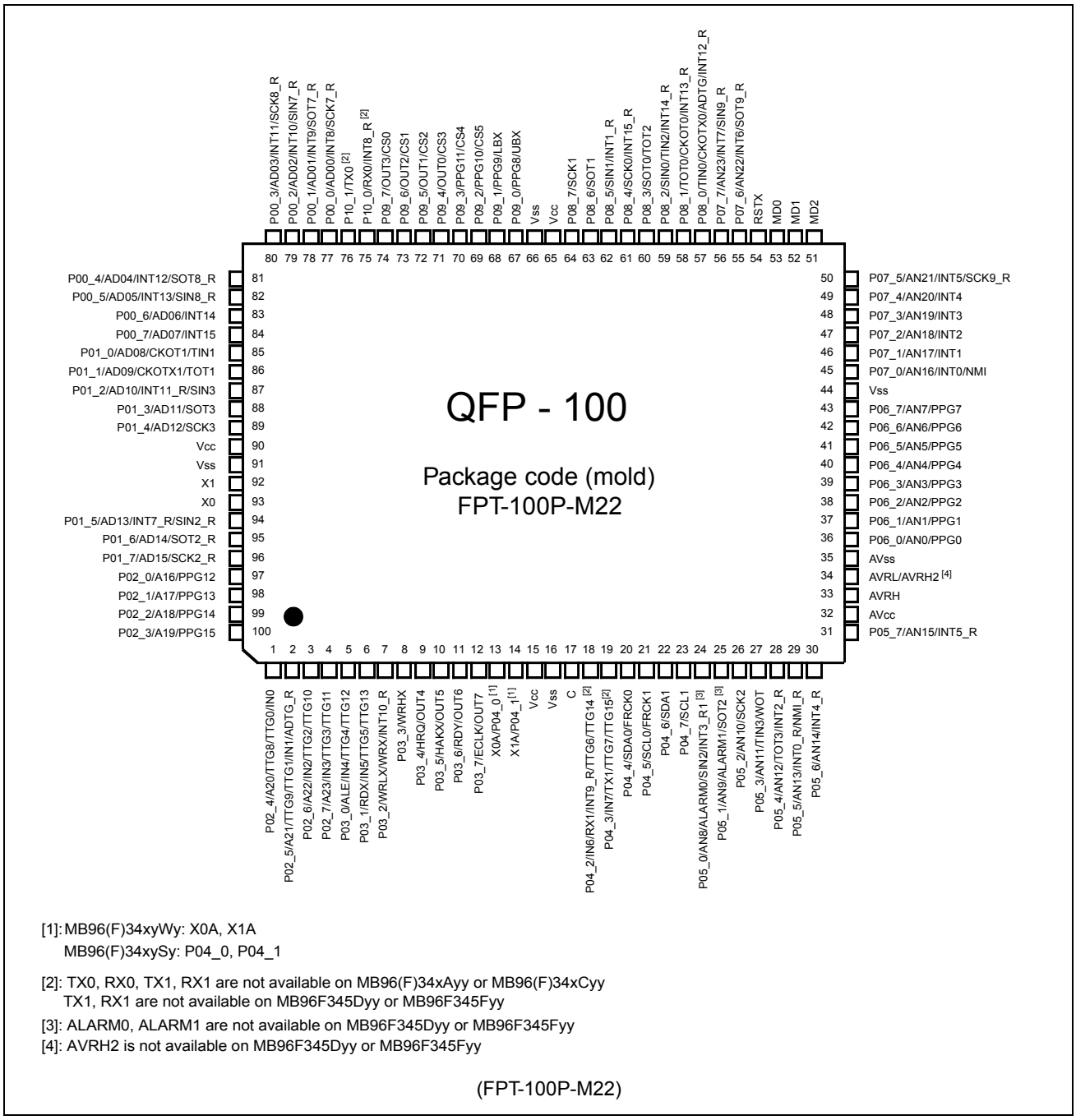
[3]: CAN interfaces are not available on MB96(F)34xAyy or MB96(F)34xCyy
CAN1 is not available on MB96F345Dyy or MB96F345Fyy

[4]: Alarm comparator is not available on MB96F345Dyy or MB96F345Fyy

[5]: A/D converter reference voltage switch is not available on MB96F345Dyy or MB96F345Fyy

3. Pin Assignments

Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

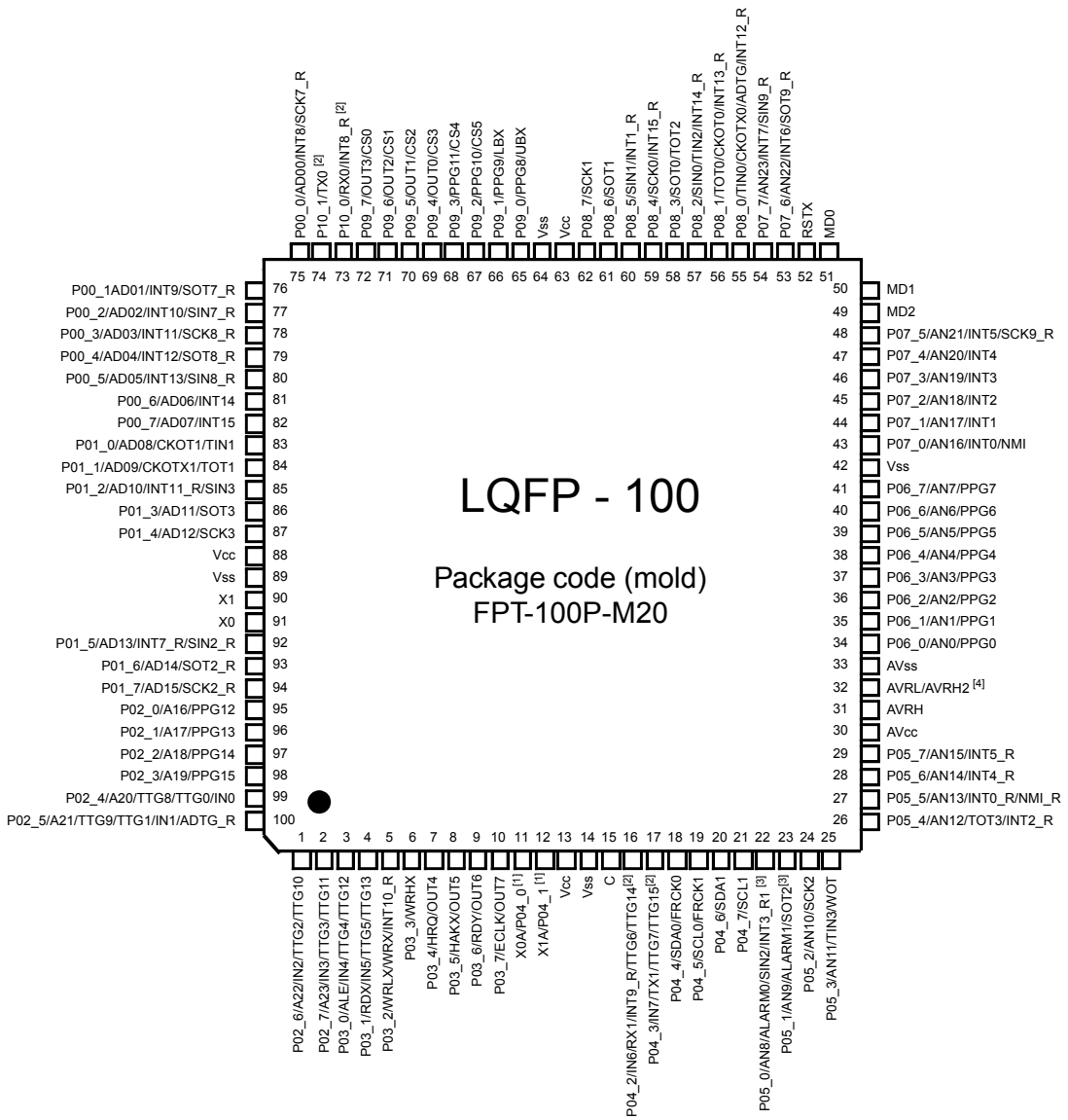
[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

Figure 3. Pin assignment of MB96(F)34x (FPT-100P-M20)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M20)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

4. Pin Function Description

Table 1: Pin Function description

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output

Table 1: Pin Function description

Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I^2C interface n clock I/O input/output
SDAn	I2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

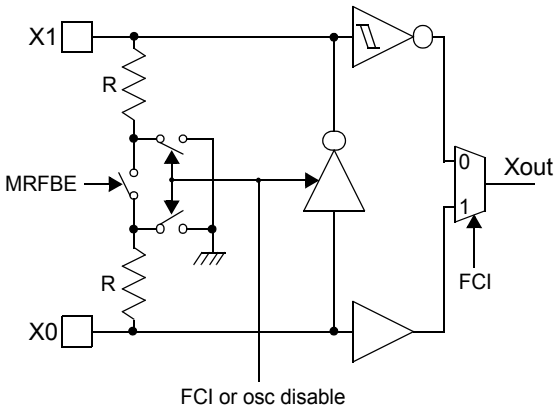
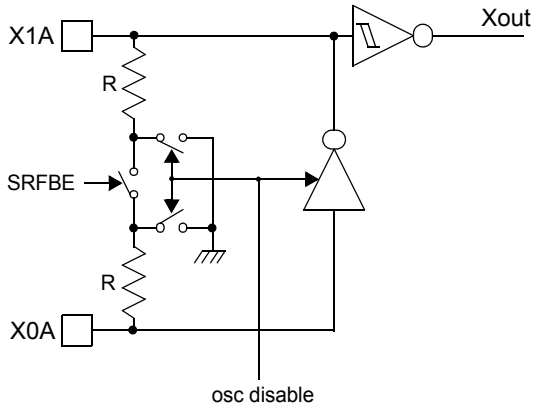
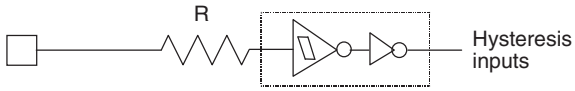
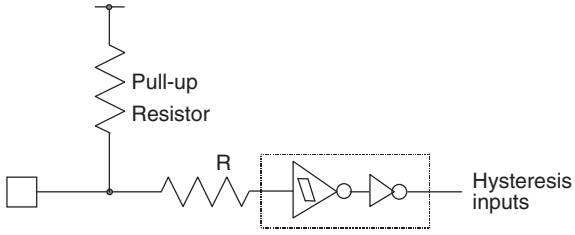
5. Pin Circuit Type

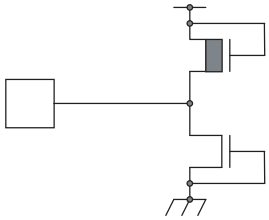
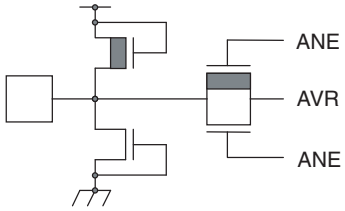
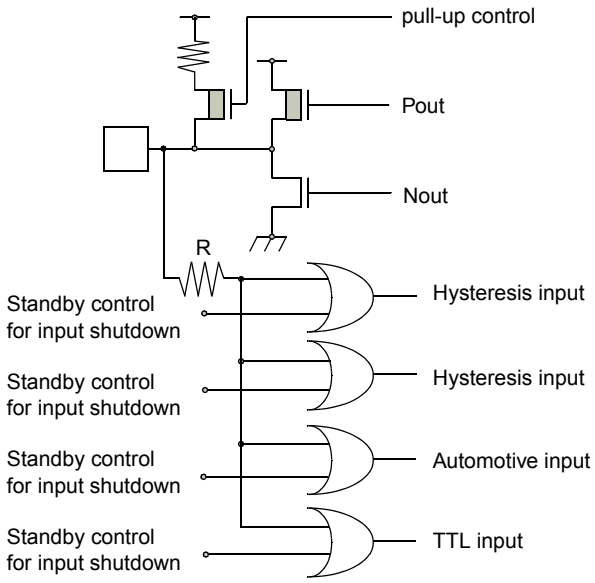
Table 2: Pin circuit types

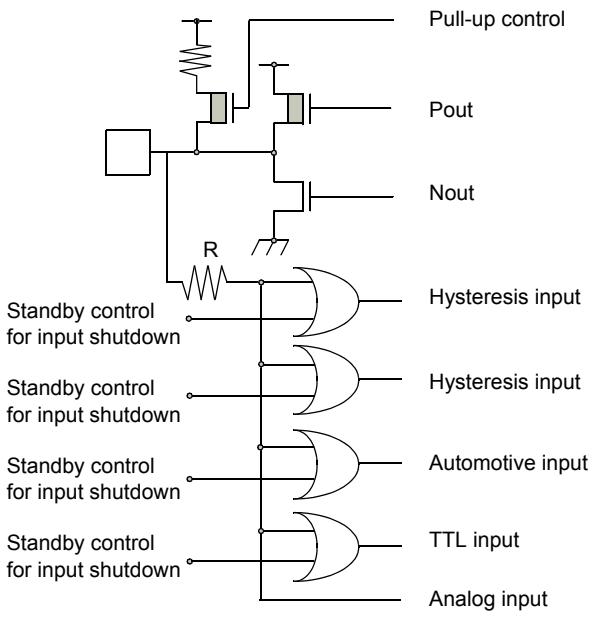
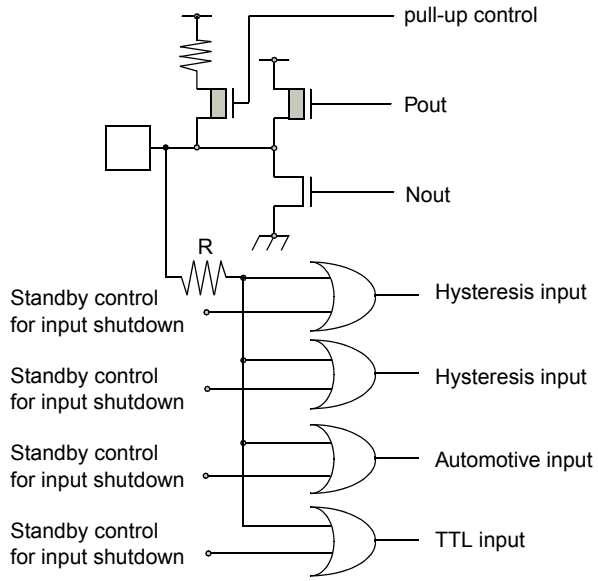
FPT-100P-M20		FPT-100P-M22	
Pin no.	Circuit type [1]	Pin no.	Circuit type [1]
1-10	H	1-12	H
11,12	B [2]	13, 14	B [2]
11,12	H [3]	13, 14	H [3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to “ I/O Circuit Type” for details on the I/O circuit types
[2]: Devices with suffix ”W”
[3]: Devices without suffix ”W”

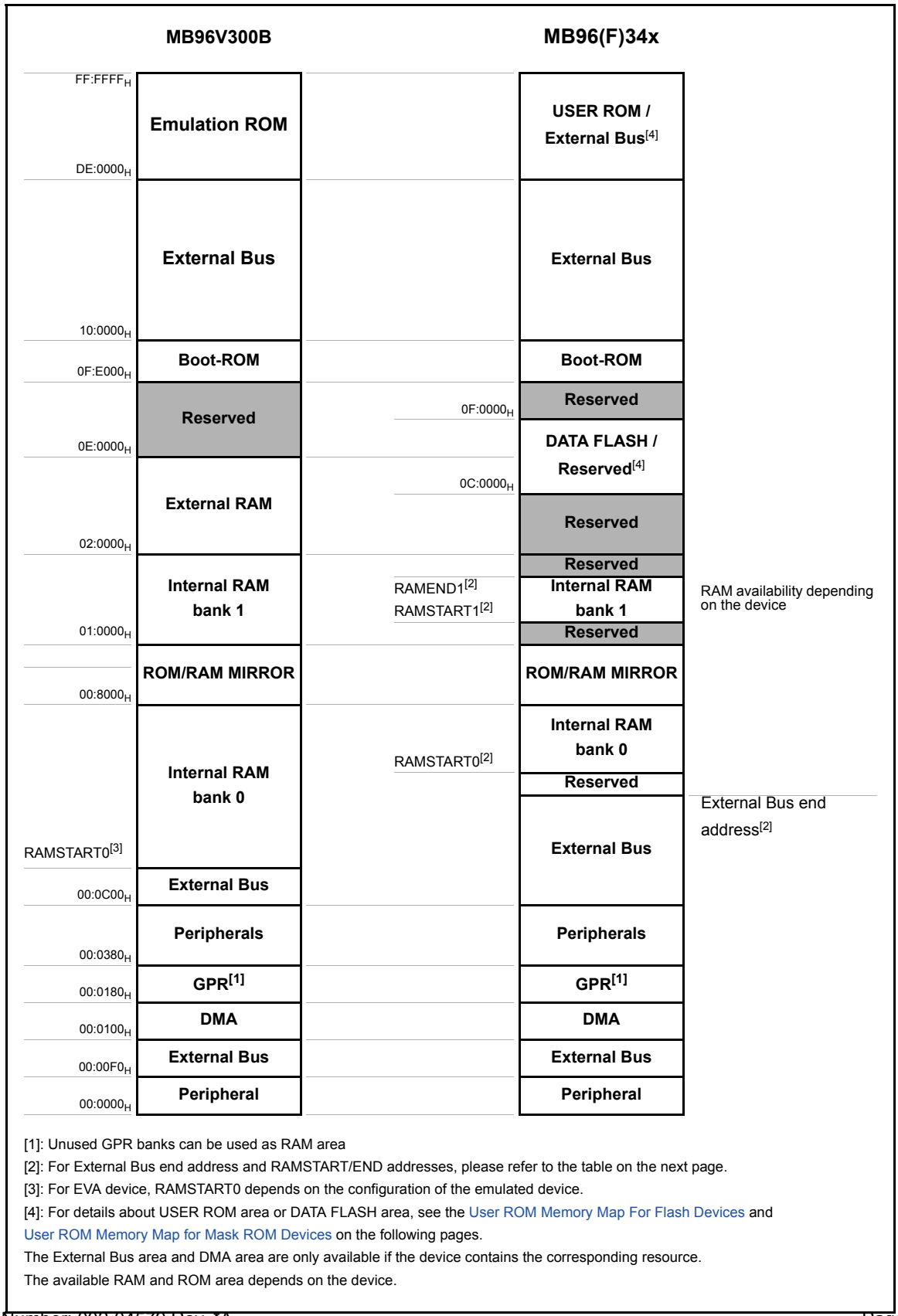
6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: ■ Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		■ Mask ROM and EVA device:CMOS Hysteresis input pin ■ Flash device:CMOS input pin
E		■ CMOS Hysteresis input pin ■ Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		■ Power supply input protection circuit
G		■ A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit ■ Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 ■ Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Type	Circuit	Remarks
I		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		■ CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

7. Memory Map



[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the User ROM Memory Map For Flash Devices and User ROM Memory Map for Mask ROM Devices on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ RAM Start/End and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96(F)345	8KByte	-	$00:21FF_H$	$00:6240_H$	-	-
MB96(F)346,MB96F347	16KByte	-	$00:21FF_H$	$00:4240_H$	-	-
MB96F348	24KByte	-	$00:21FF_H$	$00:2240_H$	-	-

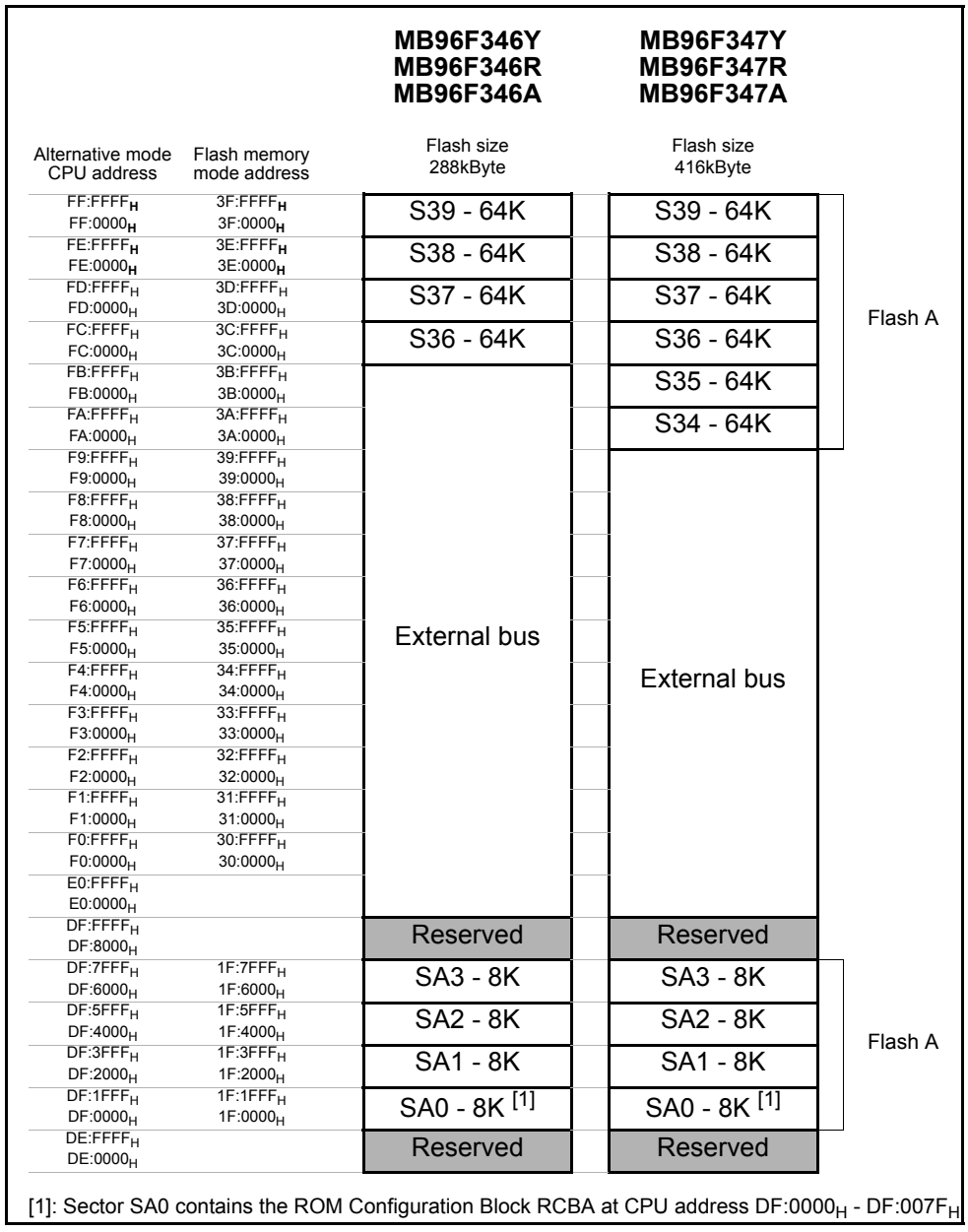
8. User ROM Memory Map For Flash Devices

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	S39 - 64K	Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	S38 - 64K	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$	External bus	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$		
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$		
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$		
$F9:FFFF_H$ $F9:0000_H$	$39:FFFF_H$ $39:0000_H$		
$F8:FFFF_H$ $F8:0000_H$	$38:FFFF_H$ $38:0000_H$		
$F7:FFFF_H$ $F7:0000_H$	$37:FFFF_H$ $37:0000_H$		
$F6:FFFF_H$ $F6:0000_H$	$36:FFFF_H$ $36:0000_H$		
$F5:FFFF_H$ $F5:0000_H$	$35:FFFF_H$ $35:0000_H$		
$F4:FFFF_H$ $F4:0000_H$	$34:FFFF_H$ $34:0000_H$		
$F3:FFFF_H$ $F3:0000_H$	$33:FFFF_H$ $33:0000_H$		
$F2:FFFF_H$ $F2:0000_H$	$32:FFFF_H$ $32:0000_H$		
$F1:FFFF_H$ $F1:0000_H$	$31:FFFF_H$ $31:0000_H$		
$F0:FFFF_H$ $F0:0000_H$	$30:FFFF_H$ $30:0000_H$		
$E0:FFFF_H$ $E0:0000_H$			
$DF:FFFF_H$ $DF:8000_H$		Reserved	
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8K	Flash A
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8K	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8K	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SA0 - 8K [1]	
$DE:FFFF_H$ $DE:0000_H$		Reserved	
$0E:FFFF_H$ $0E:FF00_H$	$(0E:FFFF_H)$ $(0E:FF00_H)$	SDA0-256 [2]	Data Flash A
$0E:FEFF_H$ $0E:0000_H$		Reserved	
$0D:FFFF_H$ $0D:C000_H$	$(0F:FFFF_H)$ $(0F:C000_H)$	SDA4-16K	Data Flash A
$0D:BFFF_H$ $0D:8000_H$	$(0F:BFFF_H)$ $(0F:8000_H)$	SDA3-16K	
$0D:7FFF_H$ $0D:4000_H$	$(0F:7FFF_H)$ $(0F:4000_H)$	SDA2-16K	
$0D:3FFF_H$ $0D:0000_H$	$(0F:3FFF_H)$ $(0F:0000_H)$	SDA1-16K	
$0C:FFFF_H$ $0C:0000_H$		Reserved	

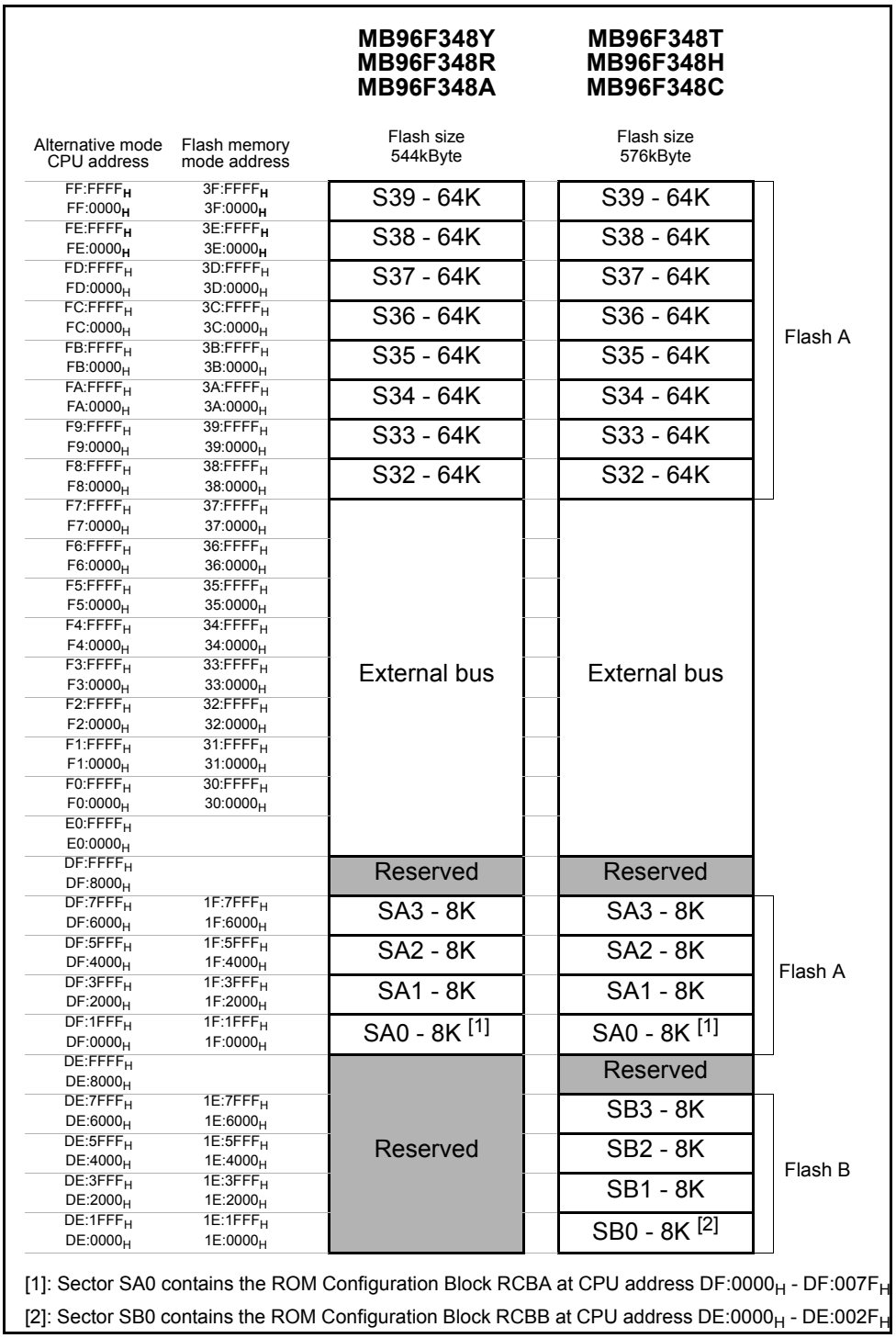
[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address $DF:0000_H$ - $DF:007F_H$

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address $DE:FF00_H$ - $DE:FF2F_H$



Alternative mode CPU address	Flash memory mode address	MB96F346Y MB96F346R MB96F346A Flash size 288kByte	MB96F347Y MB96F347R MB96F347A Flash size 416kByte	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	S37 - 64K	S37 - 64K	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$	S36 - 64K	S36 - 64K	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$	External bus	S35 - 64K	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$		S34 - 64K	
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$		External bus	
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$			
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$			
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$			
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$			
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$			
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$			
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$			
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$			
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$			
E0:FFFF$_H$ E0:0000$_H$				
DF:FFFF$_H$ DF:8000$_H$		Reserved	Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K [1]	SA0 - 8K [1]	
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	

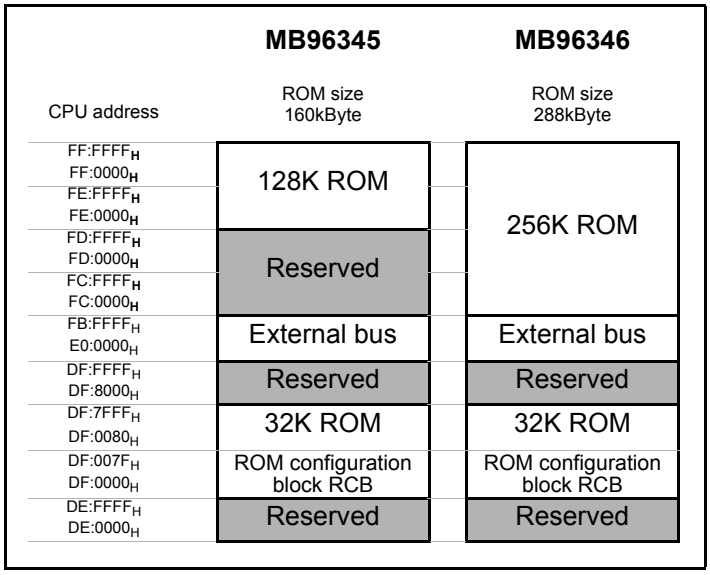
[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$



[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

[2]: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000$_H$ - DE:002F$_H$

9. User ROM Memory Map for Mask ROM Devices



10. Serial Programming Communication Interface

Table 3: USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)

MB96F34x			
Pin number	Pin number	USART Number	Normal function
LQFP-100	QFP-100		
57	59	USART0	SIN0
58	60		SOT0
59	61		SCK0
60	62	USART1	SIN1
61	63		SOT1
62	64		SCK1
22	24	USART2	SIN2
23	25		SOT2
24	26		SCK2
85	87	USART3	SIN3
86	88		SOT3
87	89		SCK3

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 76/78.If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

11. I/O Map

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000_H	I/O Port P00 - Port Data Register	PDR00		R/W
000001_H	I/O Port P01 - Port Data Register	PDR01		R/W
000002_H	I/O Port P02 - Port Data Register	PDR02		R/W
000003_H	I/O Port P03 - Port Data Register	PDR03		R/W
000004_H	I/O Port P04 - Port Data Register	PDR04		R/W
000005_H	I/O Port P05 - Port Data Register	PDR05		R/W
000006_H	I/O Port P06 - Port Data Register	PDR06		R/W
000007_H	I/O Port P07 - Port Data Register	PDR07		R/W
000008_H	I/O Port P08 - Port Data Register	PDR08		R/W
000009_H	I/O Port P09 - Port Data Register	PDR09		R/W
$00000A_H$	I/O Port P10 - Port Data Register	PDR10		R/W
$00000B_H$-000017_H	Reserved			-
000018_H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019_H	ADC0 - Control Status register High	ADCSH		R/W
$00001A_H$	ADC0 - Data Register Low	ADCRL	ADCR	R
$00001B_H$	ADC0 - Data Register High	ADCRH		R
$00001C_H$	ADC0 - Setting Register		ADSR	R/W
$00001D_H$	ADC0 - Setting Register			R/W
$00001E_H$	ADC0 - Extended Configuration Register	ADECR		R/W
$00001F_H$	Reserved			-
000020_H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021_H	FRT0 - Data register of free-running timer			R/W
000022_H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023_H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024_H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025_H	FRT1 - Data register of free-running timer			R/W
000026_H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027_H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028_H	OCU0 - Output Compare Control Status	OCS0		R/W
000029_H	OCU1 - Output Compare Control Status	OCS1		R/W
$00002A_H$	OCU0 - Compare Register		OCCP0	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00002B_H$	OCU0 - Compare Register			R/W
$00002C_H$	OCU1 - Compare Register		OCCP1	R/W
$00002D_H$	OCU1 - Compare Register			R/W
$00002E_H$	OCU2 - Output Compare Control Status	OCS2		R/W
$00002F_H$	OCU3 - Output Compare Control Status	OCS3		R/W
000030_H	OCU2 - Compare Register		OCCP2	R/W
000031_H	OCU2 - Compare Register			R/W
000032_H	OCU3 - Compare Register		OCCP3	R/W
000033_H	OCU3 - Compare Register			R/W
000034_H	OCU4 - Output Compare Control Status	OCS4		R/W
000035_H	OCU5 - Output Compare Control Status	OCS5		R/W
000036_H	OCU4 - Compare Register		OCCP4	R/W
000037_H	OCU4 - Compare Register			R/W
000038_H	OCU5 - Compare Register		OCCP5	R/W
000039_H	OCU5 - Compare Register			R/W
$00003A_H$	OCU6 - Output Compare Control Status	OCS6		R/W
$00003B_H$	OCU7 - Output Compare Control Status	OCS7		R/W
$00003C_H$	OCU6 - Compare Register		OCCP6	R/W
$00003D_H$	OCU6 - Compare Register			R/W
$00003E_H$	OCU7 - Compare Register		OCCP7	R/W
$00003F_H$	OCU7 - Compare Register			R/W
000040_H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041_H	ICU0/ICU1 - Edge register	ICE01		R/W
000042_H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043_H	ICU0 - Capture Register High	IPCPH0		R
000044_H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045_H	ICU1 - Capture Register High	IPCPH1		R
000046_H	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047_H	ICU2/ICU3 - Edge register	ICE23		R/W
000048_H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049_H	ICU2 - Capture Register High	IPCPH2		R
$00004A_H$	ICU3 - Capture Register Low	IPCPL3	IPCP3	R