Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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MB96380 Series

F²MC-16FX 16-bit Proprietary Microcontroller

MB96380 series is based on Cypress advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

Note: MB96384/385/F385/F388/F389 devices are under development and specification is preliminary. These products under development may change its specification without notice.

Features

Technology

- 0.18µm CMOS

CPU

- F²MC-16FX CPU
- Up to 56 MHz internal, 17.8 ns instruction cycle time
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 8-byte instruction execution queue
- Signed multiply (16-bit · 16-bit) and divide (32-bit/16-bit) instructions available

System clock

- On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)
- 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).
- Up to 56 MHz external clock for devices with fast clock input feature
- 32-100 kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
- Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.
- Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)
- Clock modulator

On-chip voltage regulator

- Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures

Low voltage reset

- Reset is generated when supply voltage is below minimum.

Code Security

- Protects ROM content from unintended read-out

Memory Patch Function

- Replaces ROM content
- Can also be used to implement embedded debug support

DMA

- Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Watchdog Timer

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

I^2C

- Up to 400 kbps
- Master and Slave functionality, 8-bit and 10-bit addressing

A/D converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

A/D Converter Reference Voltage switch

- 2 independent positive A/D converter reference voltages available

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input
- Can be triggered by software or reload timer

Stepper Motor Controller

- Stepper Motor Controller with integrated high current output drivers
- Four high current outputs for each channel
- Two synchronized 8/10-bit PWMs per channel
- Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock
- Separate power supply for high current output drivers

LCD Controller

- LCD controller with up to 4 COM × 65 SEG
- Internal or external voltage generation
- Duty cycle: Selectable from options: 1/2, 1/3 and 1/4
- Fixed 1/3 bias
- Programmable frame period
- Clock source selectable from three options (peripheral clock, subclock or RC oscillator clock)
- On-chip drivers for internal divider resistors or external divider resistors
- On-chip data memory for display
- LCD display can be operated in Timer Mode
- Blank display: selectable
- All SEG, COM and V pins can be switched between general and specialized purposes
- External divided resistors can be also used to shut off the current when LCD is deactivated

Sound Generator

- 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
- PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset
- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

External bus interface

- 8-bit or 16-bit bidirectional data
- Up to 24-bit addresses
- 6 chip select signals
- Multiplexed address/data lines
- Non-multiplexed address/data lines
- Wait state request
- External bus master possible
- Timing programmable

Alarm comparator

- Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds
- Threshold voltages defined externally or generated internally
- Status is readable, interrupts can be masked separately

I/O Ports

- Virtually all external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL
- Bit-wise programmable pull-up resistor
- Bit-wise programmable output driving strength for EMI optimization

Package

- 120-pin plastic LQFP

Flash Memory

- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Number of erase cycles: 10,000 times
- Data retention time: 20 years
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

Contents

1. Product Lineup

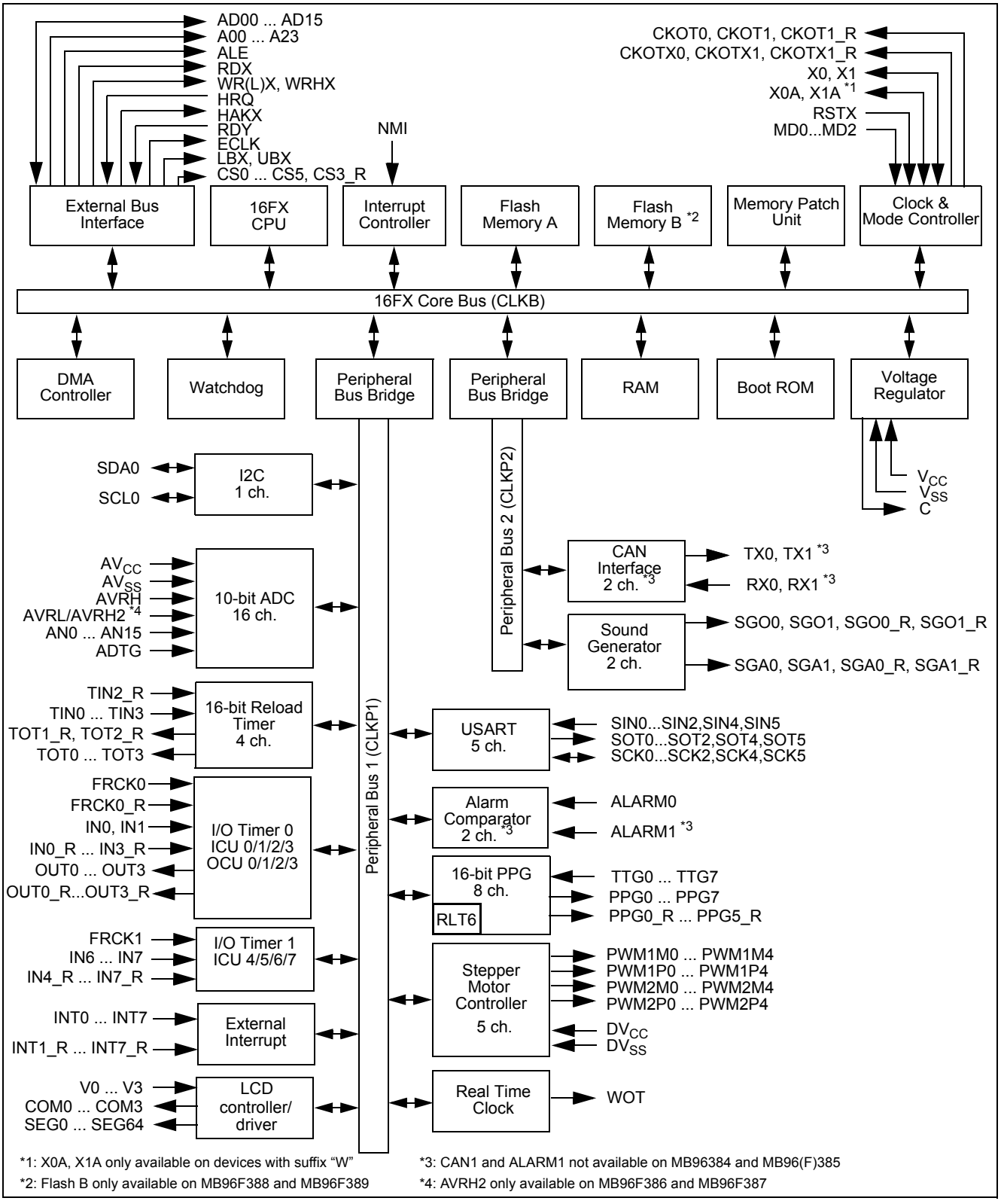
Features		MB96V300B	MB96(F)38x
Product type		Evaluation sample	Flash product: MB96F38x Mask ROM product: MB9638x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
128KB	6KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96384Y[*1], MB96384R[*1]
160KB	8KB		MB96385Y[*1], MB96385R[*1], MB96F385Y[*1], MB96F385R[*1]
288KB	16KB		MB96F386Y, MB96F386R
416KB	16KB		MB96F387Y, MB96F387R
576KB [Flash A: 544KB, Flash B: 32KB]	28KB		MB96F388T[*1], MB96F388H[*1]
832KB [Flash A: 544KB, Flash B: 288KB]	32KB		MB96F389Y[*1], MB96F389R[*1],
Package		BGA416	FPT-120P-M21
DMA		16 channels	7 channels
USART		10 channels	5 channels
I2C		2 channels	1 channel
A/D Converter		40 channels	16 channels
A/D Converter Reference Voltage switch		yes	Only for MB96F386Y, MB96F386R, MB96F387Y, MB96F387R
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	2 channels
16-bit Output Compare		12 channels	4 channels

Features	MB96V300B	MB96(F)38x
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	8 channels
CAN Interface	5 channels	Other than below: 2 channels MB96384Y*1, MB96384R*1, MB96(F)385Y*1, MB96(F)385R*1,: 1 channel
Stepping Motor Controller	6 channels	5 channels
External Interrupts	16 channels	8 channels
Non-Maskable Interrupt	1 channel	
Sound generator	2 channels	2 channels
LCD Controller	4 COM x 72 SEG	4 COM x 65 SEG
Real Time Clock	1	
I/O Ports	136	94 for part number with suffix "W", 96 for part number with suffix "S"
Alarm comparator	2 channels	Other than below: 2 channels MB96384Y*1, MB96384R*1, MB96(F)385Y*1, MB96(F)385R*1,: 1 channel
External bus interface	Yes	
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

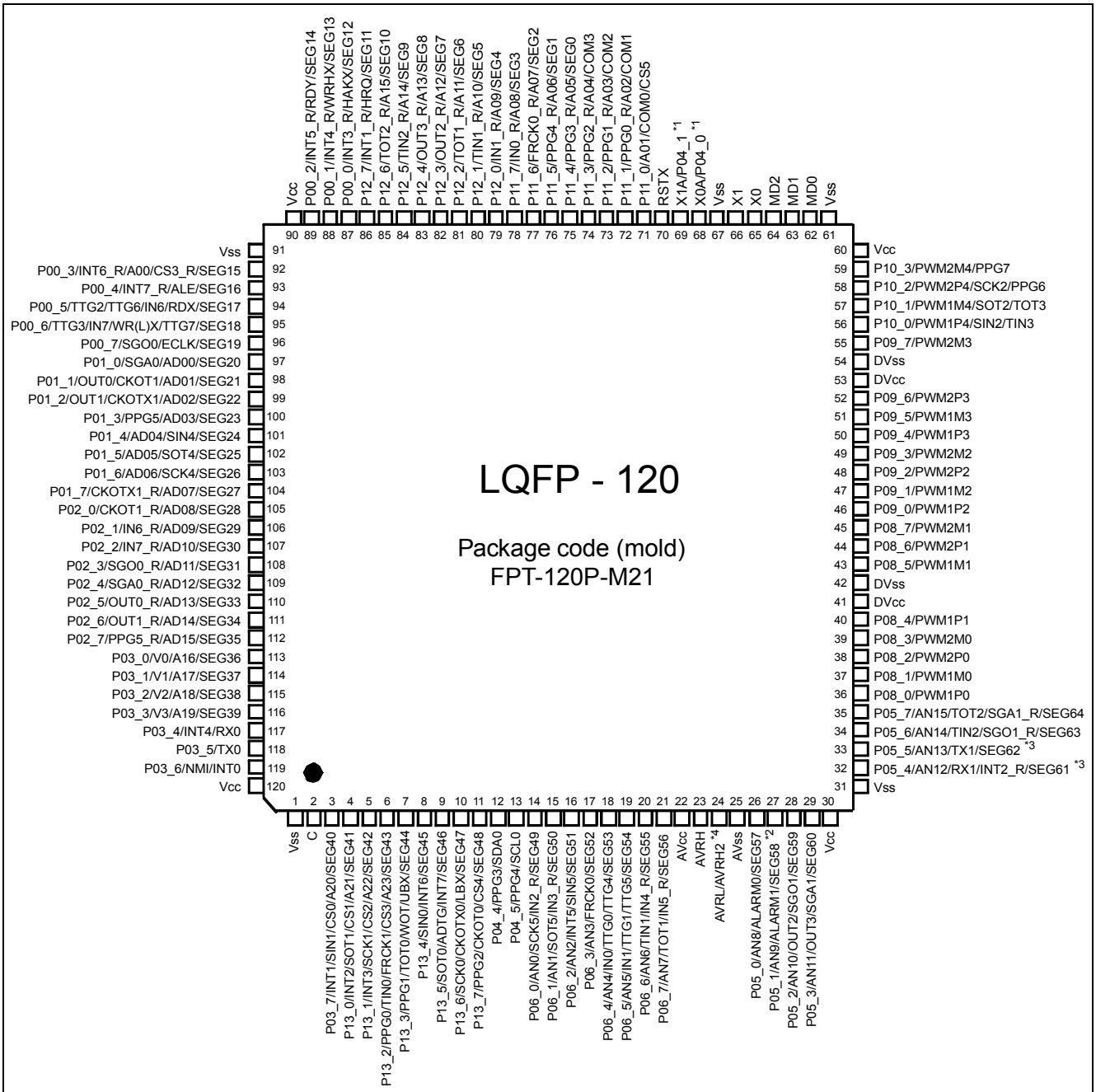
2. Block Diagram

Block diagram of MB96(F)38x



3. Pin Assignment

Pin assignment of MB96(F)38x



*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1

*2: Alarm1 not available on MB96384 and MB96(F)385

*3: TX1 resp. RX1 not available on MB96384 and MB96(F)385

*4: AVRH2 only available on MB96F386 and MB96F387

(FPT-120P-M21)

4. Pin Function Description

Pin Function description (1 of 3)

Pin name	Feature	Description
ADn	External bus	External bus interface (non multiplexed mode) data input/output. External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus non-multiplexed address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
COMn	LCD	LCD COM pins
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
CSn_R	External bus	Relocated External bus chip select n output
DV_{CC}	Supply	SMC pins power supply
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input

Pin Function description (2 of 3)

Pin name	Feature	Description
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
PWMn	SMC	SMC PWM high current
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SEGn	LCD	LCD segment n
SGA	Sound Generator	SG amplitude output
SGO	Sound Generator	SG sound/tone output
SGA_R	Sound Generator	Relocated SG amplitude output
SGO_R	Sound Generator	Relocated SG sound/tone output
SINn	USART	USART n serial data input
SOTn	USART	USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output

Pin Function description (3 of 3)

Pin name	Feature	Description
Vn	LCD	LCD voltage references
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix “W”)
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix “W”)

5. Pin Circuit Type

Pin circuit types (1 of 2)

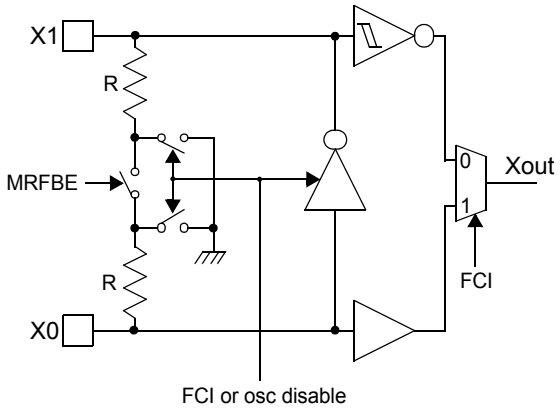
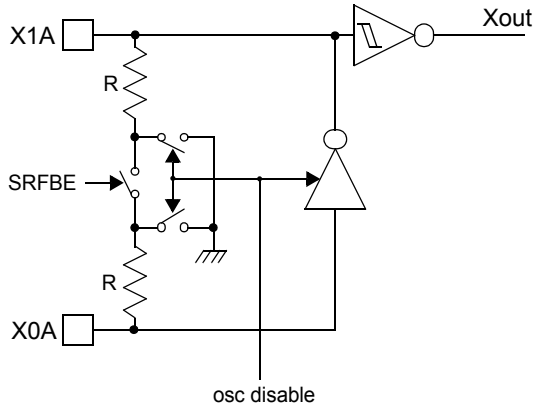
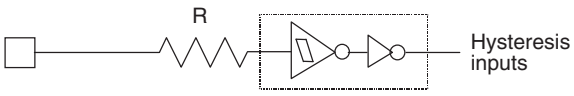
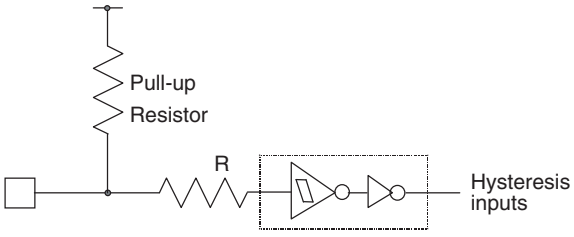
FPT-120P-M21	
Pin no.	Circuit type [*1]
1	Supply
2	F
3 to 11	J
12,13	N
14 to 21	K
22	Supply
23 to 24	G
25	Supply
26 to 29	K
30,31	Supply
32 to 35	K
36 to 40	M
41,42	Supply
43 to 52	M
53,54	Supply
55 to 59	M
60, 61	Supply
62 to 64	C
65, 66	A
67	Supply
68,69	B [*2]
68,69	H [*3]
70	E
71 to 89	J
90 to 91	Supply
92 to 112	J
113 to 116	L

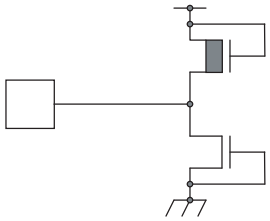
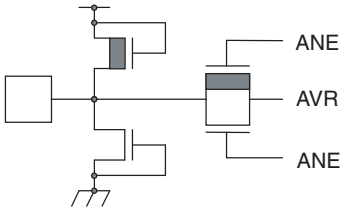
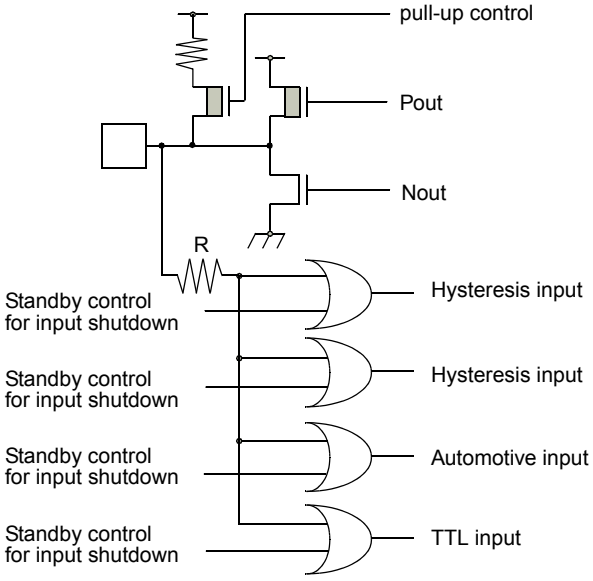
Pin circuit types (2 of 2)

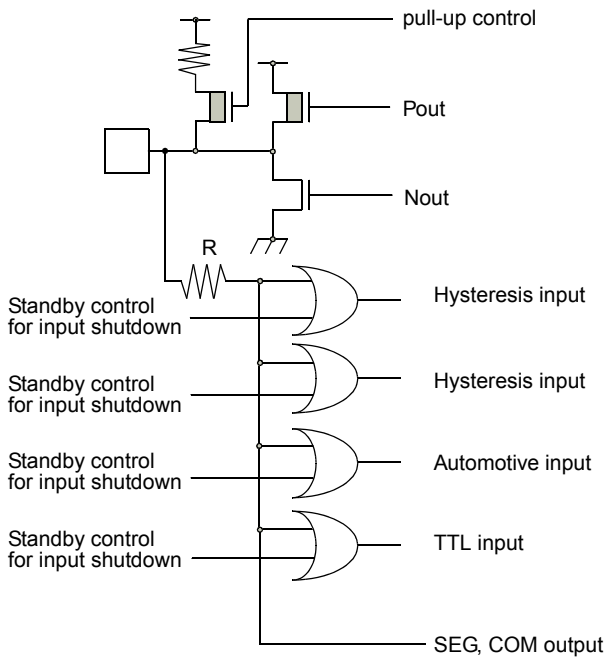
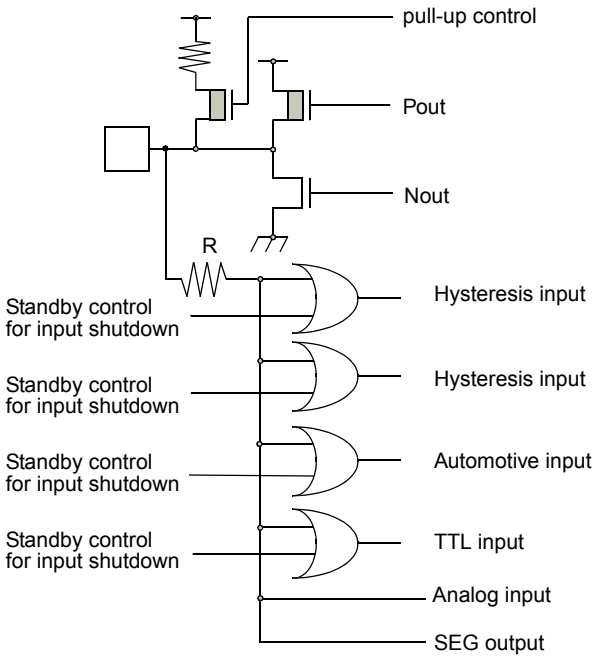
FPT-120P-M21	
Pin no.	Circuit type *1
117 to 119	H
120	Supply

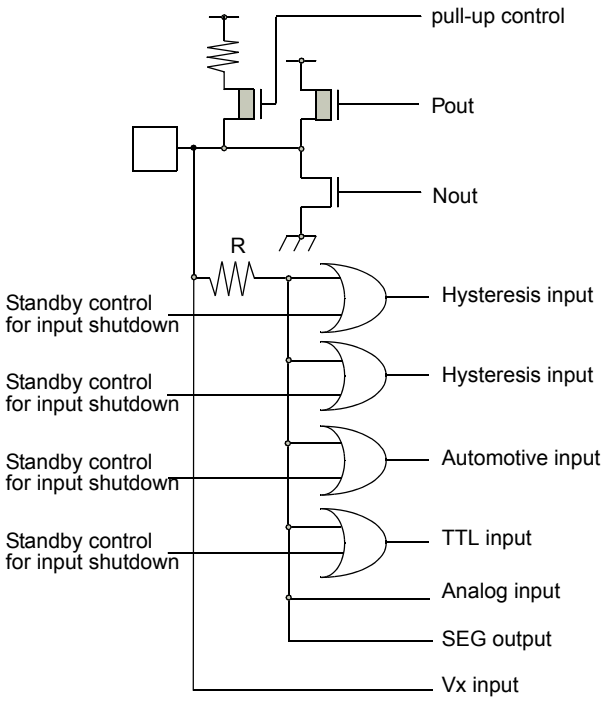
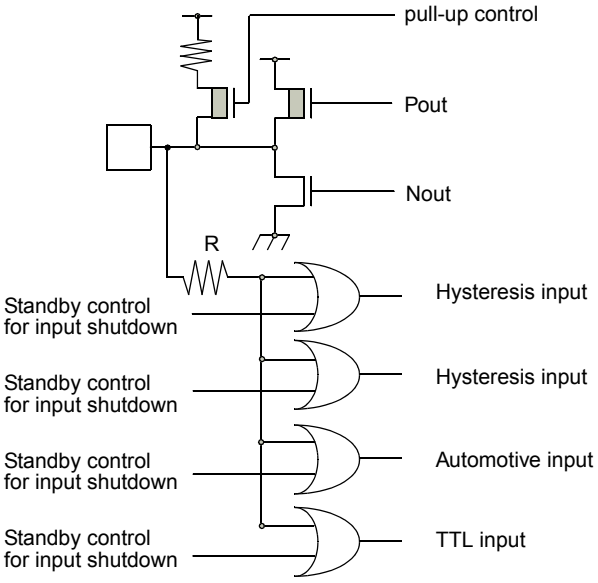
*1: Please refer to 6.“I/O Circuit Type” for details on the I/O circuit types
*2: Devices with suffix “W”
*3: Devices without suffix “W”

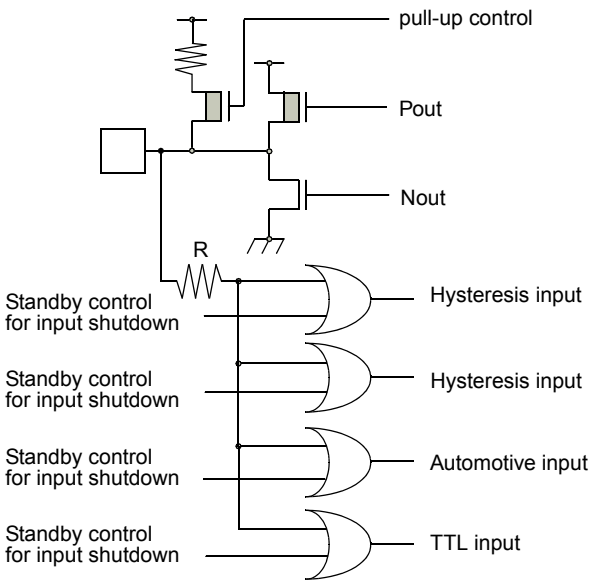
6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

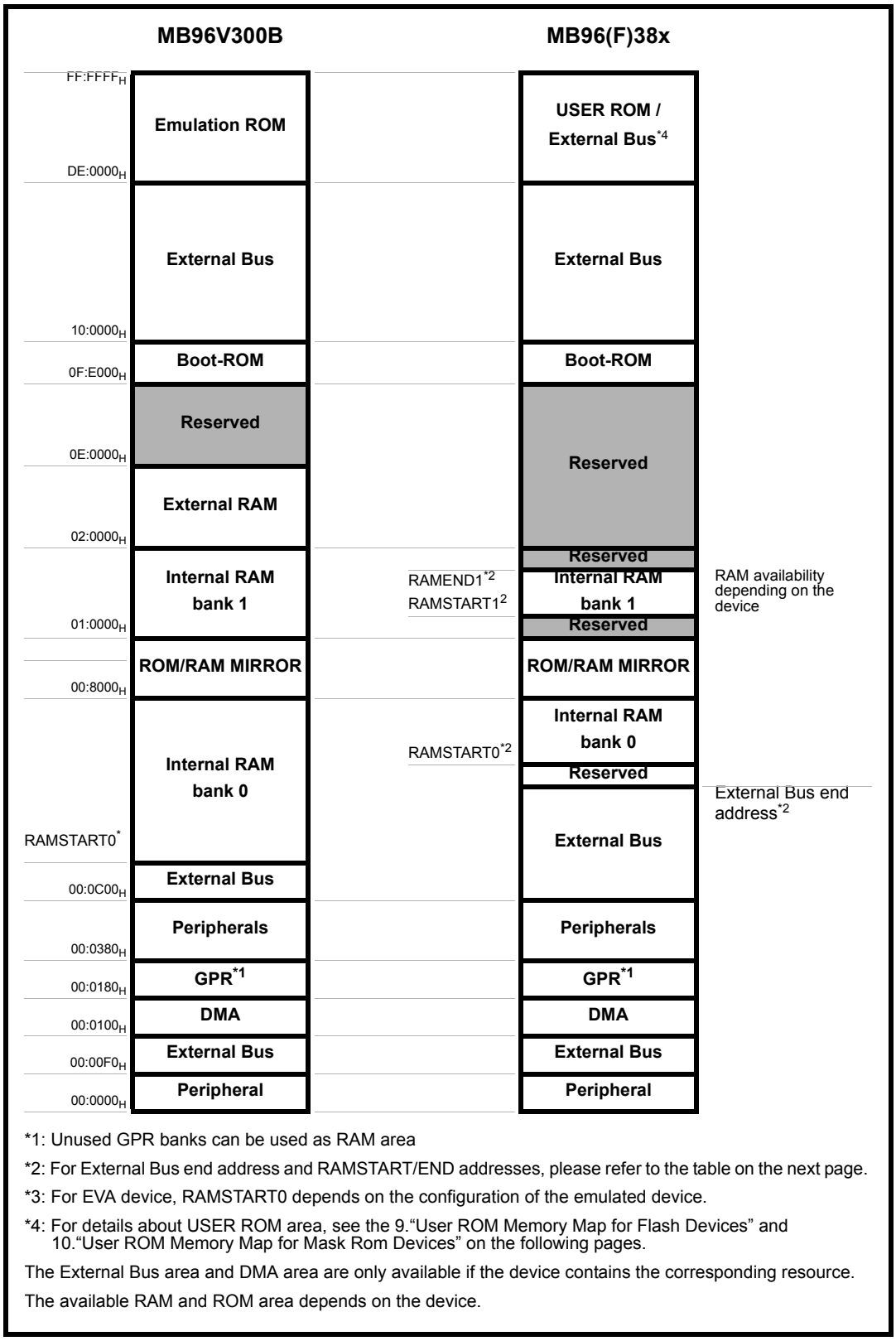
Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 • Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
J		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • SEG or COM output
K		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50kΩ approx. • Analog input • SEG output

Type	Circuit	Remarks
L		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • Analog input • Vx input • SEG output
M		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, I_{OL} = 30mA, I_{OH} = -30mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

7. Memory Map



*1: Unused GPR banks can be used as RAM area

*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the 9.“User ROM Memory Map for Flash Devices” and 10.“User ROM Memory Map for Mask Rom Devices” on the following pages.

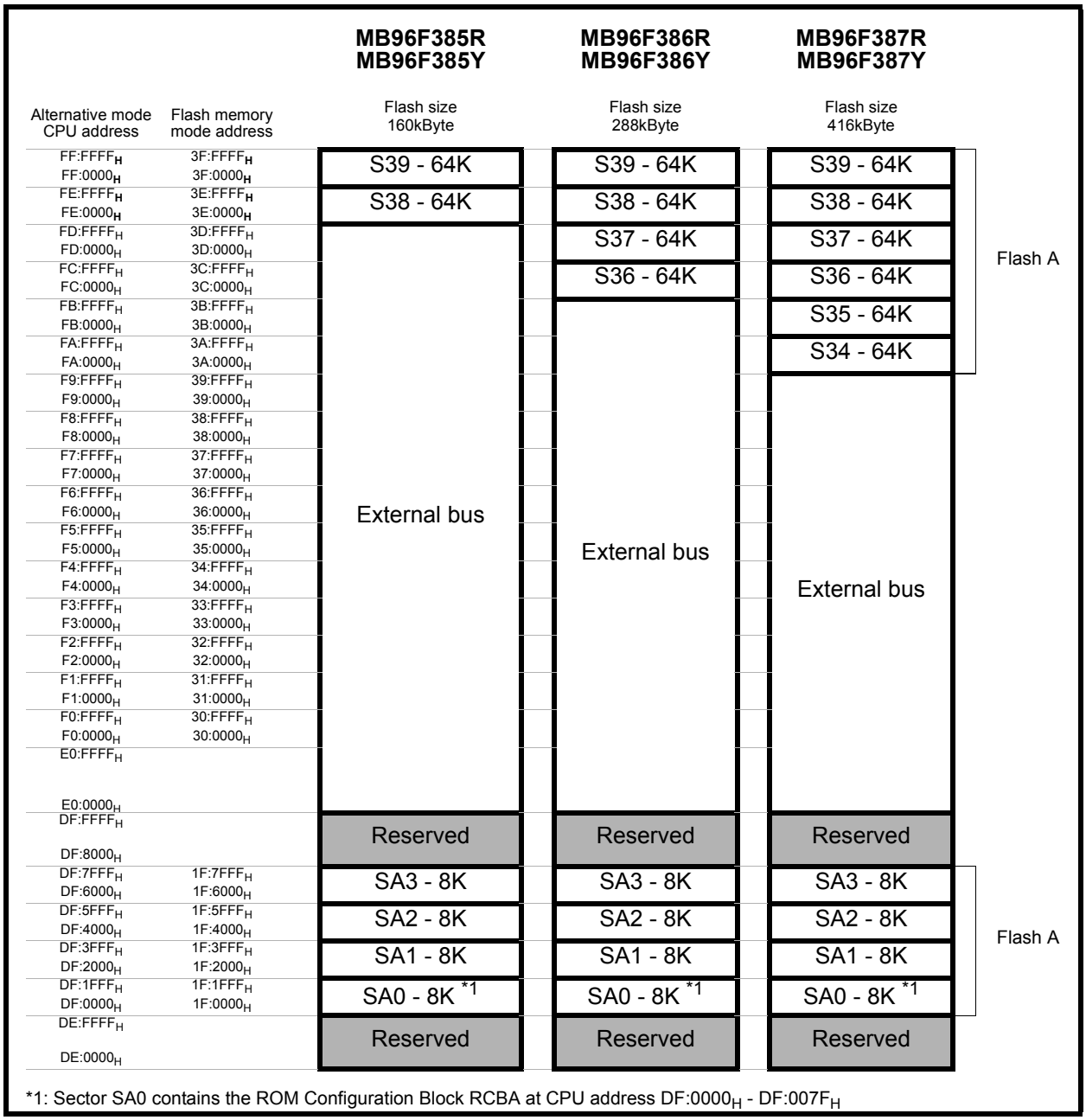
The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

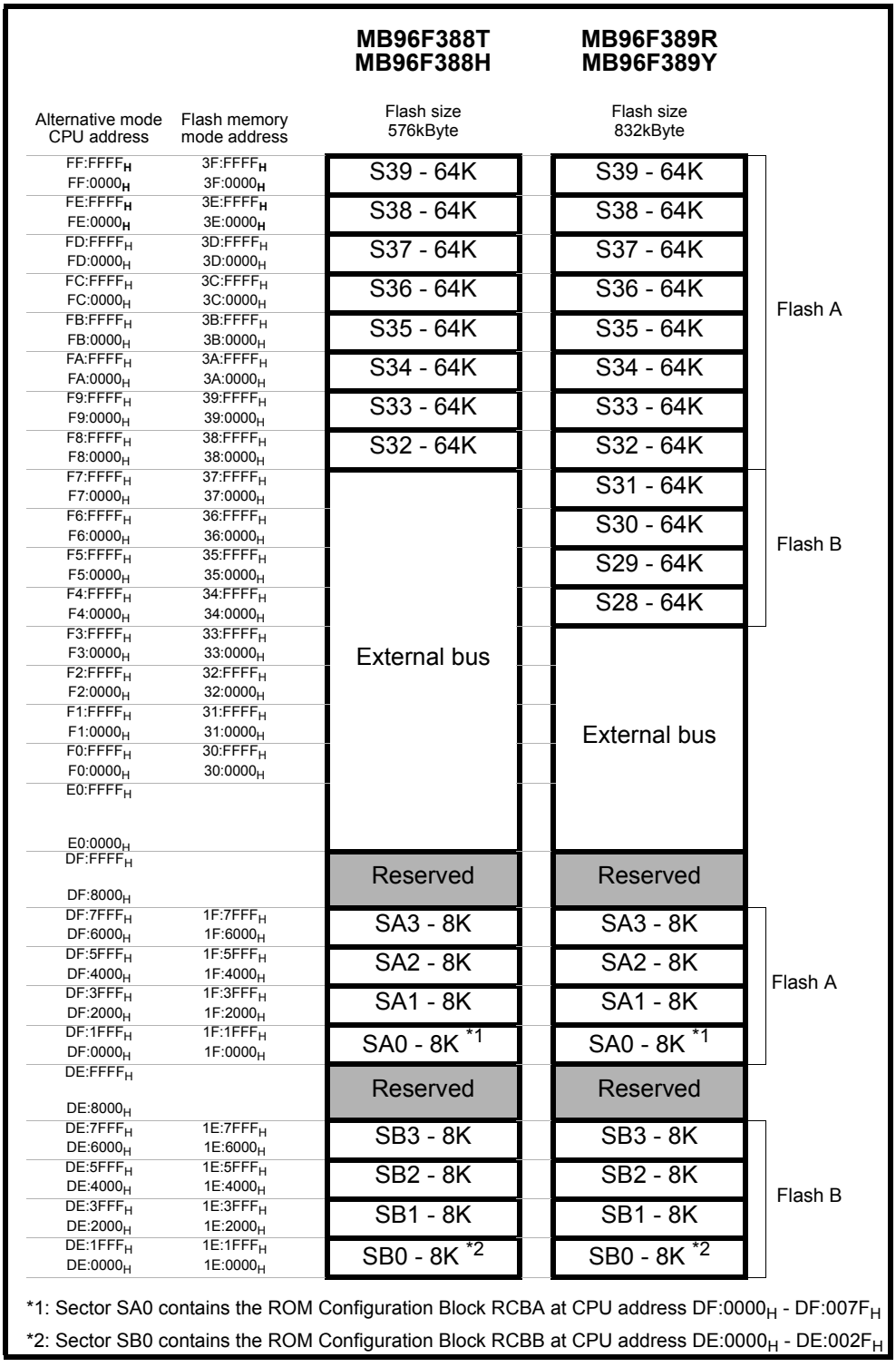
8. RAMSTART/END and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96384	6KByte	-	$00:61FF_H$	$00:6A40_H$	-	-
MB96385/F385	8KByte	-	$00:61FF_H$	$00:6240_H$	-	-
MB96F386, MB96F387	16KByte	-	$00:41FF_H$	$00:4240_H$	-	-
MB96F388	28KByte	-	$00:11FF_H$	$00:1240_H$	-	-
MB96F389	28KByte	4KByte	$00:11FF_H$	$00:1240_H$	$01:8000_H$	$01:8FFF_H$

9. User ROM Memory Map for Flash Devices



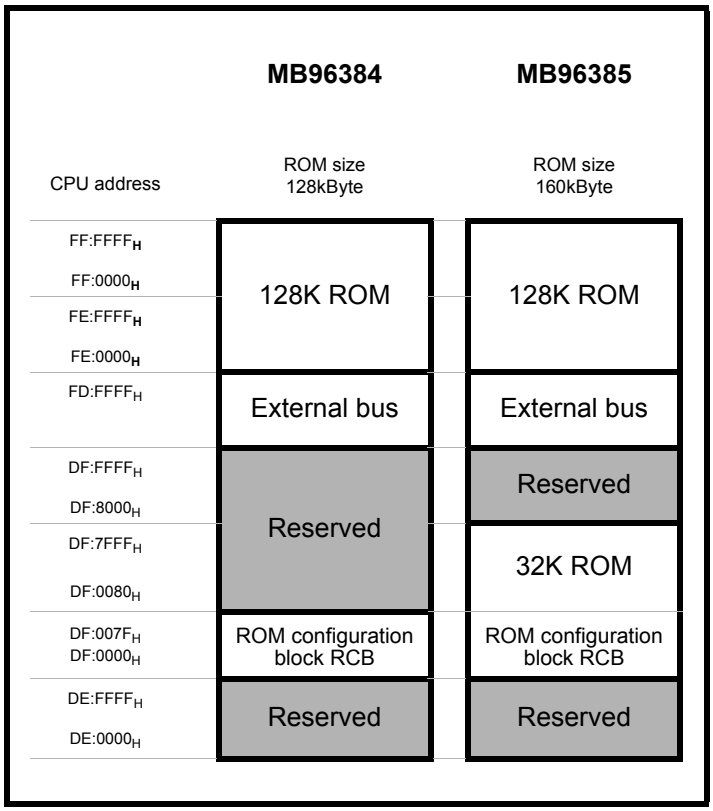
*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

*2: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000$_H$ - DE:002F$_H$

10. User ROM Memory Map for Mask Rom Devices



11. Serial Programming Communication Interface

USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)

MB96F38x		
Pin number	USART Number	Normal function
LQFP-120		
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
56	USART2	SIN2
57		SOT2
58		SCK2

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 88.
If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

12. I/O Map

I/O map MB96(F)38x (Sheet 1 of 30)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000_H	I/O Port P00 - Port Data Register	PDR00	-	R/W
000001_H	I/O Port P01 - Port Data Register	PDR01	-	R/W
000002_H	I/O Port P02 - Port Data Register	PDR02	-	R/W
000003_H	I/O Port P03 - Port Data Register	PDR03	-	R/W
000004_H	I/O Port P04 - Port Data Register	PDR04	-	R/W
000005_H	I/O Port P05 - Port Data Register	PDR05	-	R/W
000006_H	I/O Port P06 - Port Data Register	PDR06	-	R/W
000007_H	Reserved	-	-	-
000008_H	I/O Port P08 - Port Data Register	PDR08	-	R/W
000009_H	I/O Port P09 - Port Data Register	PDR09	-	R/W
$00000A_H$	I/O Port P10 - Port Data Register	PDR10	-	R/W
$00000B_H$	I/O Port P11 - Port Data Register	PDR11	-	R/W
$00000C_H$	I/O Port P12 - Port Data Register	PDR12	-	R/W
$00000D_H$	I/O Port P13 - Port Data Register	PDR13	-	R/W
$00000E_H$-000017_H	Reserved	-	-	-
000018_H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019_H	ADC0 - Control Status register High	ADCSH	-	R/W
$00001A_H$	ADC0 - Data Register Low	ADCRL	ADCR	R
$00001B_H$	ADC0 - Data Register High	ADCRH	-	R
$00001C_H$	ADC0 - Setting Register	-	ADSR	R/W
$00001D_H$	ADC0 - Setting Register	-	-	R/W
$00001E_H$	ADC0 - Extended Configuration Register	ADECR	-	R/W
$00001F_H$	Reserved	-	-	-
000020_H	FRT0 - Data register of free-running timer	-	TCDT0	R/W
000021_H	FRT0 - Data register of free-running timer	-	-	R/W
000022_H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023_H	FRT0 - Control status register of free-running timer High	TCCSH0	-	R/W
000024_H	FRT1 - Data register of free-running timer	-	TCDT1	R/W
000025_H	FRT1 - Data register of free-running timer	-	-	R/W