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The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
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About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

MB96650 series is based on Cypress's advanced F²MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F²MC-16LX family thus allowing for easy migration of F²MC-16LX Software to the new F²MC-16FX products. F²MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time. For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz to 8MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

Technology

0.18μm CMOS

CPU

- F²MC-16FX CPU
- Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
- 8-byte instruction queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

System clock

- On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
- 4MHz to 8MHz crystal oscillator (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 8MHz external clock for devices with fast clock input feature
- 32.768kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
- Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
- The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
- Low Power Consumption - 13 operating modes (different Run, Sleep, Timer, Stop modes)

On-chip voltage regulator

Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption

Low voltage detection function

Reset is generated when supply voltage falls below programmable reference voltage

Code Security

Protects Flash Memory content from unintended read-out

DMA

Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1Mbps
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)

- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

I²C

- Up to 400kbps
- Master and Slave functionality, 7-bit and 10-bit addressing

A/D converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function
- Scan Disable Function

Source Clock Timers

Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free-Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with 1 , $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2×8 -bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1 , $1/4$, $1/16$, $1/64$ of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture
- Start delay

Quadrature Position/Revolution Counter (QPRC)

- Up/down count mode, Phase difference count mode, Count mode with direction
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge or Level sensitive
- Interrupt mask bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I²C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

Built-in On Chip Debugger (OCD)

- One-wire debug tool interface
- Break function:
 - Hardware break: 6 points (shared with code event)
 - -Software break: 4096 points
- Event function
 - Code event: 6 points (shared with hardware break)
 - -Data event: 6 points
 - Event sequencer: 2 levels + reset
- Execution time measurement function
- Trace function: 42 branches
- Security function

Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the automatic algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase or write

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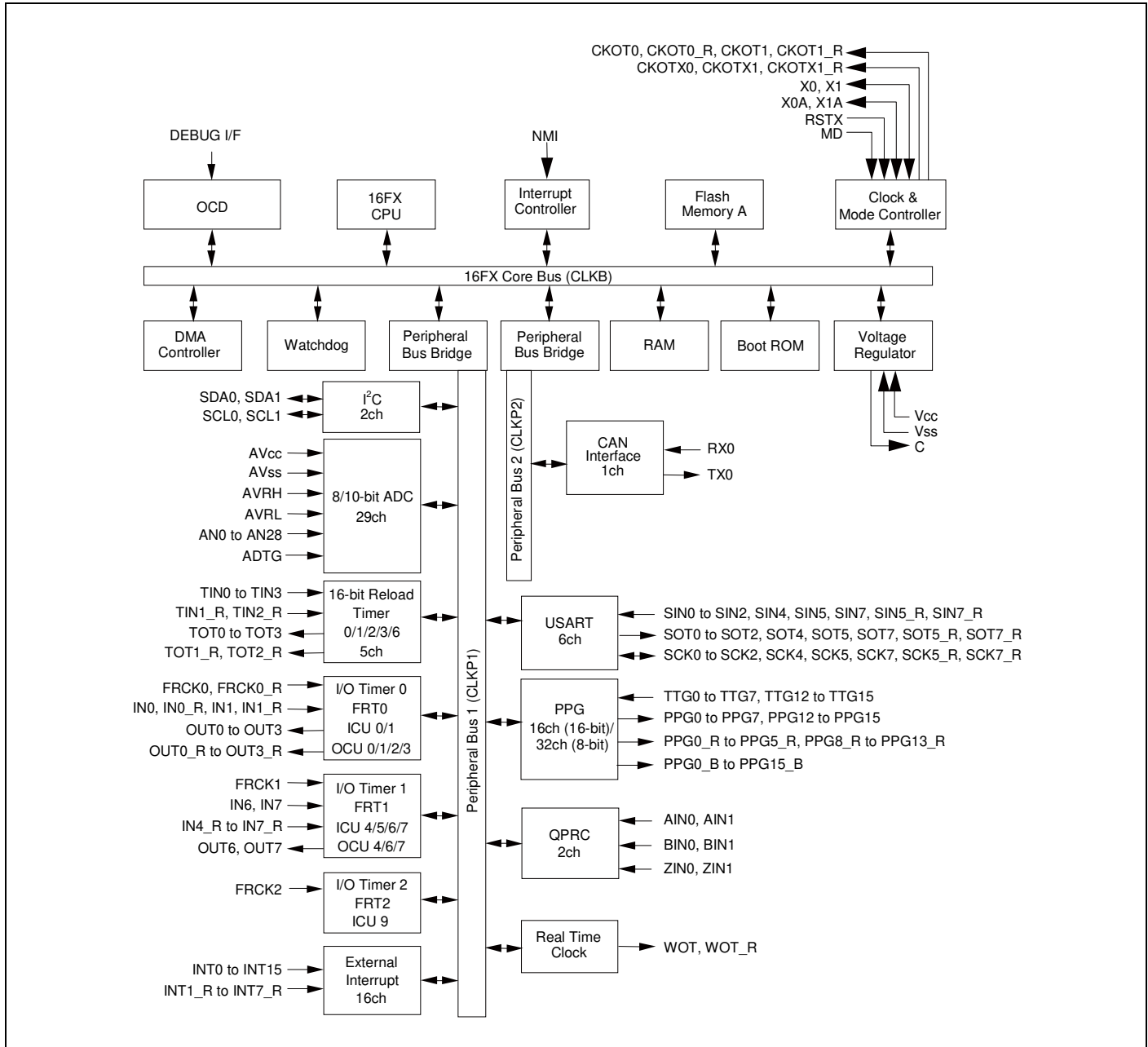
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1. Product Lineup

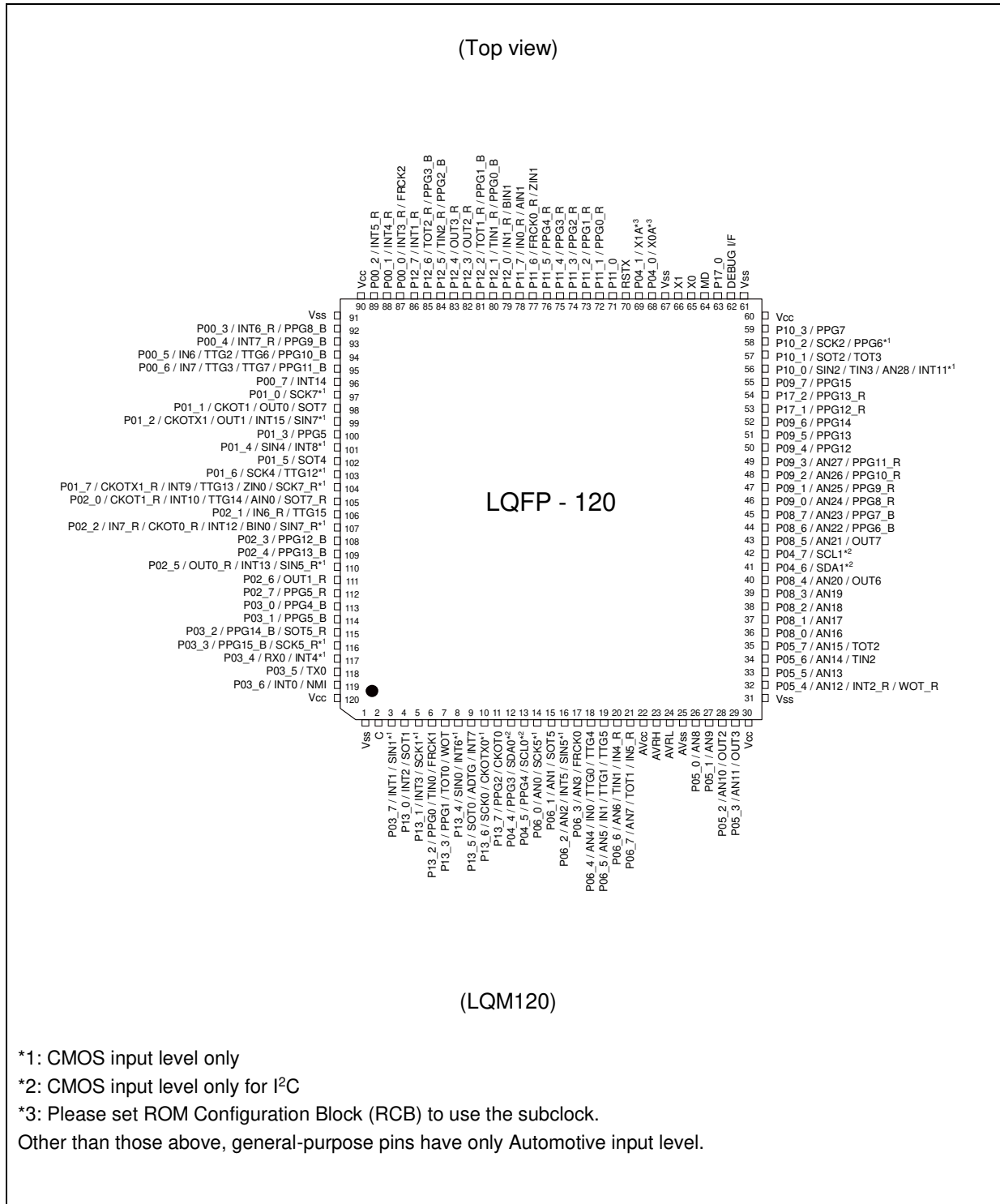
Features		MB96650	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
64.5KB + 32KB	10KB	MB96F653R, MB96F653A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB	16KB	MB96F655R, MB96F655A	
256.5KB + 32KB	24KB	MB96F656R	
384.5KB + 32KB	28KB	MB96F657R	
Package		LQFP-120: LQM120	
DMA		4ch	
USART		6ch	LIN-USART 0 to 2/4/5/7
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO	No	
I ² C		2ch	I ² C 0/1
8/10-bit A/D Converter		29ch	AN 0 to 28
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	No	
16-bit Reload Timer (RLT)		5ch	RLT 0 to 3/6
16-bit Free-Running Timer (FRT)		3ch	FRT 0 to 2
16-bit Input Capture Unit (ICU)		7ch (1 channel for LIN-USART)	ICU 0/1/4 to 7/9 ICU 9 for LIN-USART
16-bit Output Compare Unit (OCU)		7ch	OCU 0 to 4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)		16ch (16-bit) / 32ch (8-bit)	PPG 0 to 15
	with Timing point capture	Yes	
	with Start delay	Yes	
	with Ramp	No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 0 32 Message Buffers
External Interrupts (INT)		16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		99 (Dual clock mode) 101 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.

2. Block Diagram



3. Pin Assignment



4. Pin Description

Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVRL	ADC	A/D converter low reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
CKOTXn_R	Clock Output function	Relocated Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
FRCKn	Free-Running Timer	Free-Running Timer n input pin
FRCKn_R	Free-Running Timer	Relocated Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SCLn	I ² C	I ² C interface n clock I/O input/output pin
SDAn	I ² C	I ² C interface n serial data I/O input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TINn_R	Reload Timer	Relocated Reload Timer n event input pin

Pin name	Feature	Description
TOTn	Reload Timer	Reload Timer n output pin
TOTn_R	Reload Timer	Relocated Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin
WOT	RTC	Real Time clock output pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin

5. Pin Circuit Type

Pin no.	I/O circuit type*	Pin name
1	Supply	Vss
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	M	P13_1 / INT3 / SCK1
6	H	P13_2 / PPG0 / TIN0 / FRCK1
7	H	P13_3 / PPG1 / TOT0 / WOT
8	M	P13_4 / SIN0 / INT6
9	H	P13_5 / SOT0 / ADTG / INT7
10	M	P13_6 / SCK0 / CKOTX0
11	H	P13_7 / PPG2 / CKOT0
12	N	P04_4 / PPG3 / SDA0
13	N	P04_5 / PPG4 / SCL0
14	I	P06_0 / AN0 / SCK5
15	K	P06_1 / AN1 / SOT5
16	I	P06_2 / AN2 / INT5 / SIN5
17	K	P06_3 / AN3 / FRCK0
18	K	P06_4 / AN4 / IN0 / TTG0 / TTG4
19	K	P06_5 / AN5 / IN1 / TTG1 / TTG5
20	K	P06_6 / AN6 / TIN1 / IN4_R
21	K	P06_7 / AN7 / TOT1 / IN5_R
22	Supply	AVcc
23	G	AVRH
24	G	AVRL
25	Supply	AVss
26	K	P05_0 / AN8
27	K	P05_1 / AN9
28	K	P05_2 / AN10 / OUT2
29	K	P05_3 / AN11 / OUT3
30	Supply	Vcc
31	Supply	Vss
32	K	P05_4 / AN12 / INT2_R / WOT_R
33	K	P05_5 / AN13
34	K	P05_6 / AN14 / TIN2
35	K	P05_7 / AN15 / TOT2
36	K	P08_0 / AN16

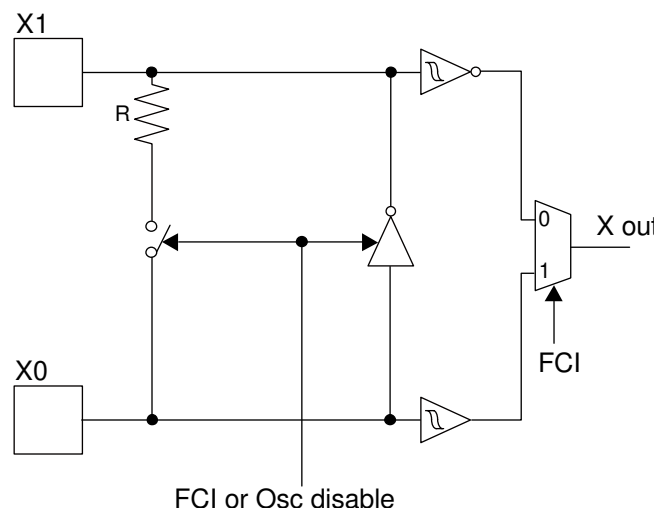
Pin no.	I/O circuit type*	Pin name
37	K	P08_1 / AN17
38	K	P08_2 / AN18
39	K	P08_3 / AN19
40	K	P08_4 / AN20 / OUT6
41	N	P04_6 / SDA1
42	N	P04_7 / SCL1
43	K	P08_5 / AN21 / OUT7
44	K	P08_6 / AN22 / PPG6_B
45	K	P08_7 / AN23 / PPG7_B
46	K	P09_0 / AN24 / PPG8_R
47	K	P09_1 / AN25 / PPG9_R
48	K	P09_2 / AN26 / PPG10_R
49	K	P09_3 / AN27 / PPG11_R
50	H	P09_4 / PPG12
51	H	P09_5 / PPG13
52	H	P09_6 / PPG14
53	H	P17_1 / PPG12_R
54	H	P17_2 / PPG13_R
55	H	P09_7 / PPG15
56	I	P10_0 / SIN2 / TIN3 / AN28 / INT11
57	H	P10_1 / SOT2 / TOT3
58	M	P10_2 / SCK2 / PPG6
59	H	P10_3 / PPG7
60	Supply	Vcc
61	Supply	Vss
62	O	DEBUG I/F
63	H	P17_0
64	C	MD
65	A	X0
66	A	X1
67	Supply	Vss
68	B	P04_0 / X0A
69	B	P04_1 / X1A
70	C	RSTX
71	H	P11_0
72	H	P11_1 / PPG0_R
73	H	P11_2 / PPG1_R
74	H	P11_3 / PPG2_R
75	H	P11_4 / PPG3_R

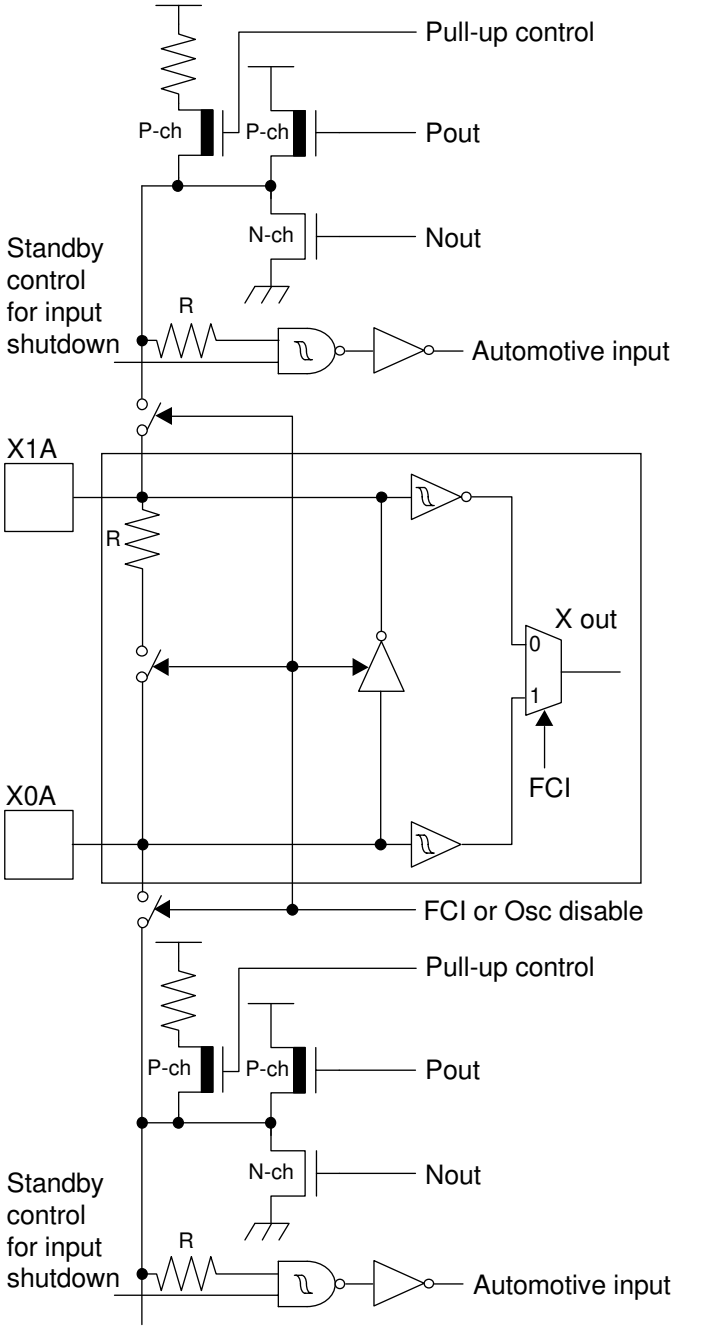
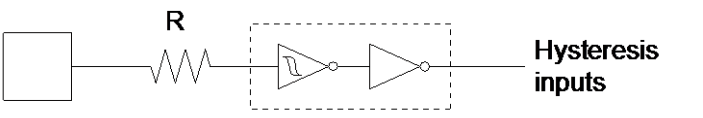
Pin no.	I/O circuit type*	Pin name
76	H	P11_5 / PPG4_R
77	H	P11_6 / FRCK0_R / ZIN1
78	H	P11_7 / IN0_R / AIN1
79	H	P12_0 / IN1_R / BIN1
80	H	P12_1 / TIN1_R / PPG0_B
81	H	P12_2 / TOT1_R / PPG1_B
82	H	P12_3 / OUT2_R
83	H	P12_4 / OUT3_R
84	H	P12_5 / TIN2_R / PPG2_B
85	H	P12_6 / TOT2_R / PPG3_B
86	H	P12_7 / INT1_R
87	H	P00_0 / INT3_R / FRCK2
88	H	P00_1 / INT4_R
89	H	P00_2 / INT5_R
90	Supply	Vcc
91	Supply	Vss
92	H	P00_3 / INT6_R / PPG8_B
93	H	P00_4 / INT7_R / PPG9_B
94	H	P00_5 / IN6 / TTG2 / TTG6 / PPG10_B
95	H	P00_6 / IN7 / TTG3 / TTG7 / PPG11_B
96	H	P00_7 / INT14
97	M	P01_0 / SCK7
98	H	P01_1 / CKOT1 / OUT0 / SOT7
99	M	P01_2 / CKOTX1 / OUT1 / INT15 / SIN7
100	H	P01_3 / PPG5
101	M	P01_4 / SIN4 / INT8
102	H	P01_5 / SOT4
103	M	P01_6 / SCK4 / TTG12
104	M	P01_7 / CKOTX1_R / INT9 / TTG13 / ZIN0 / SCK7_R
105	H	P02_0 / CKOT1_R / INT10 / TTG14 / AIN0 / SOT7_R
106	H	P02_1 / IN6_R / TTG15
107	M	P02_2 / IN7_R / CKOT0_R / INT12 / BIN0 / SIN7_R
108	H	P02_3 / PPG12_B
109	H	P02_4 / PPG13_B
110	M	P02_5 / OUT0_R / INT13 / SIN5_R
111	H	P02_6 / OUT1_R
112	H	P02_7 / PPG5_R
113	H	P03_0 / PPG4_B
114	H	P03_1 / PPG5_B

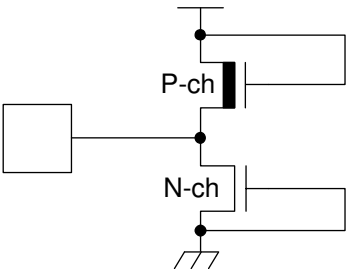
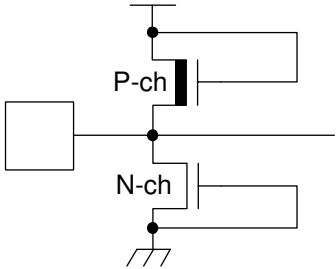
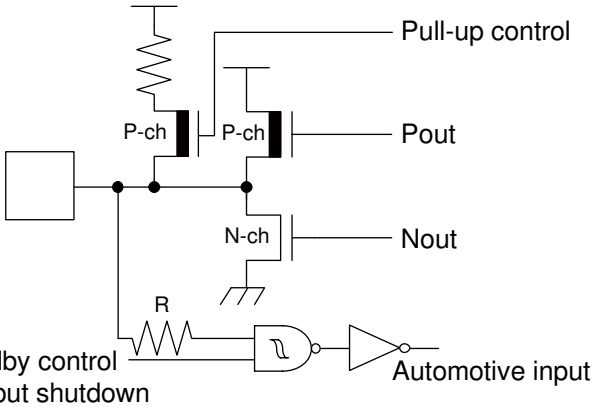
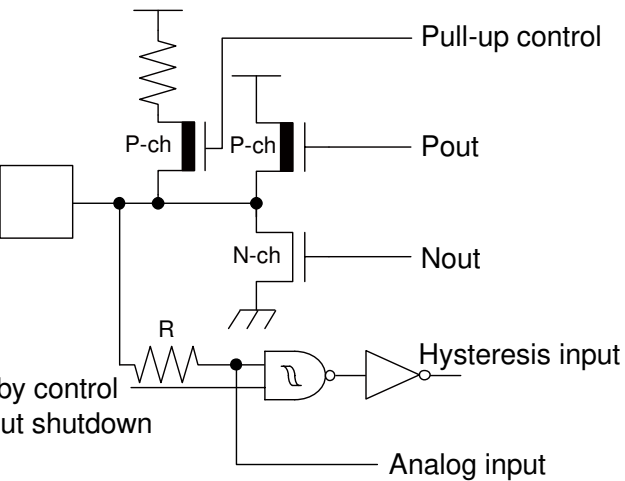
Pin no.	I/O circuit type*	Pin name
115	H	P03_2 / PPG14_B / SOT5_R
116	M	P03_3 / PPG15_B / SCK5_R
117	M	P03_4 / RX0 / INT4
118	H	P03_5 / TX0
119	H	P03_6 / INT0 / NMI
120	Supply	Vcc

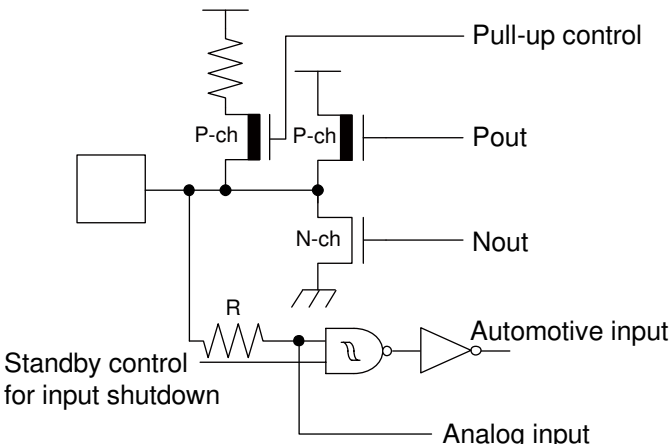
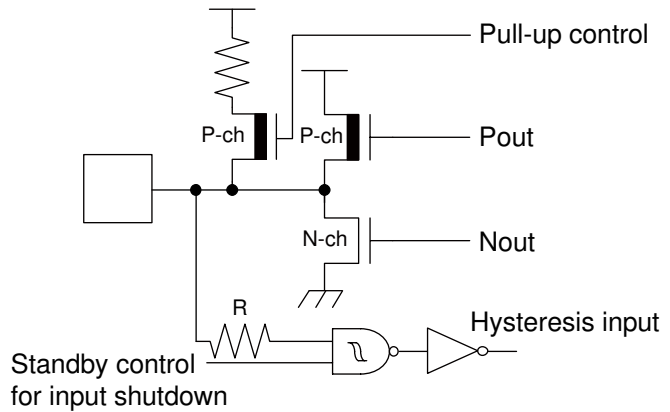
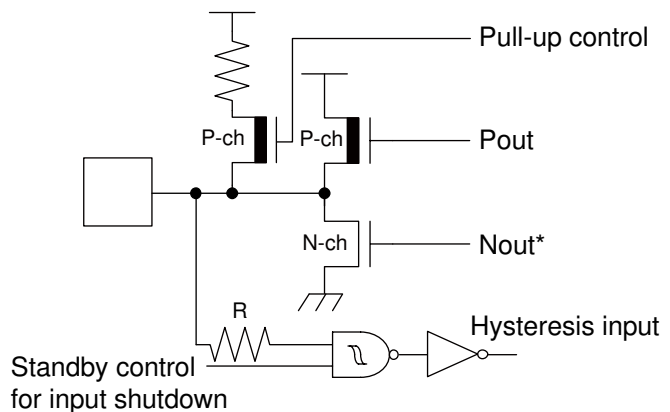
*: See “I/O circuit type” for details on the I/O circuit types.

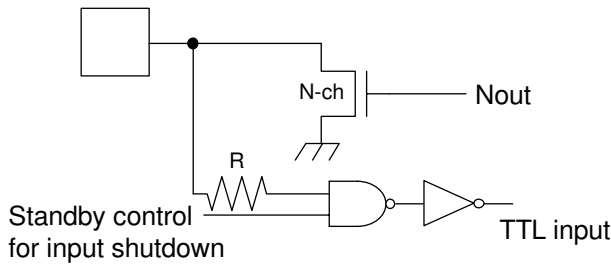
6. I/O Circuit Type

Type	Circuit	Remarks
A	 FCI or Osc disable	High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. $1.0M\Omega$ ■ The amplitude: $1.8V \pm 0.15V$ to operate by the internal supply voltage

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: ■ Feedback resistor = approx. 5.0MΩ ■ GPIO functionality selectable (CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$), Automotive input with input shutdown function and programmable pull-up resistor)
C		CMOS hysteresis input pin

Type	Circuit	Remarks
F		Power supply input protection circuit
G		■ A/D converter ref+ (AVRH)/ref- (AVRL) power supply input pin with protection circuit ■ Without protection circuit against V_{CC} for pins AVRH/AVRL
H		■ CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor
I		■ CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor ■ Analog input

Type	Circuit	Remarks
K		■ CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor ■ Analog input
M		■ CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor
N		■ CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor *: N-channel transistor has slew rate control according to I²C spec, irrespective of usage.

Type	Circuit	Remarks
O	 Standby control for input shutdown TTL input N-ch Nout R	■ Open-drain I/O ■ Output 25mA, $V_{CC} = 2.7V$ ■ TTL input

7. Memory Map

FF:FFF _H	USER ROM* ¹
DE:000 _H	
DD:FFF _H	Reserved
10:000 _H	
0F:C00 _H	Boot-ROM
	Peripheral
0E:900 _H	
	Reserved
01:000 _H	
	ROM/RAM MIRROR
00:800 _H	
	Internal RAM bank0
RAMSTART0* ²	
	Reserved
00:0C0 _H	
	Peripheral
00:038 _H	
00:018 _H	GPR* ³
00:010 _H	DMA
00:00F _H	Reserved
00:000 _H	Peripheral

*1: For details about USER ROM area, see “□USER ROM MEMORY MAP FOR FLASH DEVICES” on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. Ramstart Addresses

Devices	Bank 0 RAM size	RAMSTART0
MB96F653	10KB	00:5A00 _H
MB96F655	16KB	00:4200 _H
MB96F656	24KB	00:2200 _H
MB96F657	28KB	00:1200 _H

9. User ROM Memory Map for Flash Devices

		MB96F653			MB96F655			MB96F656			MB96F657			
CPU mode address	Flash memory mode address	Flash size 64.5KB + 32KB			Flash size 128.5KB + 32KB			Flash size 256.5KB + 32KB			Flash size 384.5KB + 32KB			
FF:FFF _H	3F:FFF _H	SA39 - 64KB			SA39 - 64KB			SA39 - 64KB			SA39 - 64KB		Bank A of Flash A	
FF:000 _H	3F:000 _H	Reserved			SA38 - 64KB			SA38 - 64KB			SA38 - 64KB			
FE:FFF _H	3E:FFF _H						SA37 - 64KB			SA37 - 64KB				
FE:000 _H	3E:000 _H						SA36 - 64KB			SA36 - 64KB				
FD:FFF _H	3D:FFF _H						Reserved			SA35 - 64KB				
FD:000 _H	3D:000 _H							SA34 - 64KB						
FC:FFF _H	3C:FFF _H							Reserved			Reserved			
FC:000 _H	3C:000 _H													
FB:FFF _H	3B:FFF _H													
FB:000 _H	3B:000 _H													
FA:FFF _H	3A:FFF _H													
FA:000 _H	3A:000 _H													
F9:FFF _H		Reserved			Reserved			Reserved			Reserved			
DF:A000 _H														
DF:9FFF _H	1F:9FFF _H		SA4 - 8KB			SA4 - 8KB			SA4 - 8KB			SA4 - 8KB		Bank B of Flash A
DF:8000 _H	1F:8000 _H		SA3 - 8KB			SA3 - 8KB			SA3 - 8KB			SA3 - 8KB		
DF:7FFF _H	1F:7FFF _H		SA2 - 8KB			SA2 - 8KB			SA2 - 8KB			SA2 - 8KB		
DF:6000 _H	1F:6000 _H		SA1 - 8KB			SA1 - 8KB			SA1 - 8KB			SA1 - 8KB		
DF:5FFF _H	1F:5FFF _H		SAS - 512B*			SAS - 512B*			SAS - 512B*			SAS - 512B*		
DF:4000 _H	1F:4000 _H		Reserved			Reserved			Reserved			Reserved		
DF:3FFF _H	1F:3FFF _H													
DF:2000 _H	1F:2000 _H													
DF:1FFF _H	1F:1FFF _H													
DF:0000 _H	1F:0000 _H													
DE:FFF _H		Reserved			Reserved			Reserved			Reserved			
DE:0000 _H														

*: Physical address area of SAS-512B is from DF:0000_H to DF:01FF_H.
Others (from DF:0200_H to DF:1FFF_H) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000_H -DF:01FF_H.
SAS can not be used for E²PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96650		
Pin Number	USART Number	Normal Function
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
56	USART2	SIN2
57		SOT2
58		SCK2
101	USART4	SIN4
102		SOT4
103		SCK4

11. Interrupt Vector Table

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC _H	CALLV0	No	-	CALLV instruction
1	3F8 _H	CALLV1	No	-	CALLV instruction
2	3F4 _H	CALLV2	No	-	CALLV instruction
3	3F0 _H	CALLV3	No	-	CALLV instruction
4	3EC _H	CALLV4	No	-	CALLV instruction
5	3E8 _H	CALLV5	No	-	CALLV instruction
6	3E4 _H	CALLV6	No	-	CALLV instruction
7	3E0 _H	CALLV7	No	-	CALLV instruction
8	3DC _H	RESET	No	-	Reset vector
9	3D8 _H	INT9	No	-	INT9 instruction
10	3D4 _H	EXCEPTION	No	-	Undefined instruction execution
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Clock Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	LVDI	No	16	Low Voltage Detector
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	EXTINT1	Yes	18	External Interrupt 1
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	EXTINT5	Yes	22	External Interrupt 5
23	3A0 _H	EXTINT6	Yes	23	External Interrupt 6
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	EXTINT8	Yes	25	External Interrupt 8
26	394 _H	EXTINT9	Yes	26	External Interrupt 9
27	390 _H	EXTINT10	Yes	27	External Interrupt 10
28	38C _H	EXTINT11	Yes	28	External Interrupt 11
29	388 _H	EXTINT12	Yes	29	External Interrupt 12
30	384 _H	EXTINT13	Yes	30	External Interrupt 13
31	380 _H	EXTINT14	Yes	31	External Interrupt 14
32	37C _H	EXTINT15	Yes	32	External Interrupt 15
33	378 _H	CAN0	No	33	CAN Controller 0
34	374 _H	-	-	34	Reserved
35	370 _H	-	-	35	Reserved
36	36C _H	-	-	36	Reserved
37	368 _H	-	-	37	Reserved
38	364 _H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360 _H	PPG1	Yes	39	Programmable Pulse Generator 1

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	35C _H	PPG2	Yes	40	Programmable Pulse Generator 2
41	358 _H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 _H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350 _H	PPG5	Yes	43	Programmable Pulse Generator 5
44	34C _H	PPG6	Yes	44	Programmable Pulse Generator 6
45	348 _H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344 _H	PPG8	Yes	46	Programmable Pulse Generator 8
47	340 _H	PPG9	Yes	47	Programmable Pulse Generator 9
48	33C _H	PPG10	Yes	48	Programmable Pulse Generator 10
49	338 _H	PPG11	Yes	49	Programmable Pulse Generator 11
50	334 _H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330 _H	PPG13	Yes	51	Programmable Pulse Generator 13
52	32C _H	PPG14	Yes	52	Programmable Pulse Generator 14
53	328 _H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324 _H	-	-	54	Reserved
55	320 _H	-	-	55	Reserved
56	31C _H	-	-	56	Reserved
57	318 _H	-	-	57	Reserved
58	314 _H	RLT0	Yes	58	Reload Timer 0
59	310 _H	RLT1	Yes	59	Reload Timer 1
60	30C _H	RLT2	Yes	60	Reload Timer 2
61	308 _H	RLT3	Yes	61	Reload Timer 3
62	304 _H	-	-	62	Reserved
63	300 _H	-	-	63	Reserved
64	2FC _H	RLT6	Yes	64	Reload Timer 6
65	2F8 _H	ICU0	Yes	65	Input Capture Unit 0
66	2F4 _H	ICU1	Yes	66	Input Capture Unit 1
67	2F0 _H	-	-	67	Reserved
68	2EC _H	-	-	68	Reserved
69	2E8 _H	ICU4	Yes	69	Input Capture Unit 4
70	2E4 _H	ICU5	Yes	70	Input Capture Unit 5
71	2E0 _H	ICU6	Yes	71	Input Capture Unit 6
72	2DC _H	ICU7	Yes	72	Input Capture Unit 7
73	2D8 _H	-	-	73	Reserved
74	2D4 _H	ICU9	Yes	74	Input Capture Unit 9
75	2D0 _H	-	-	75	Reserved
76	2CC _H	-	-	76	Reserved
77	2C8 _H	OCU0	Yes	77	Output Compare Unit 0
78	2C4 _H	OCU1	Yes	78	Output Compare Unit 1
79	2C0 _H	OCU2	Yes	79	Output Compare Unit 2
80	2BC _H	OCU3	Yes	80	Output Compare Unit 3