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MB96670 series is based on Cypress's advanced F<sup>2</sup>MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F<sup>2</sup>MC-16LX family thus allowing for easy migration of F<sup>2</sup>MC-16LX Software to the new F<sup>2</sup>MC-16FX products.

F<sup>2</sup>MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz to 8MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

## Features

### ■ Technology

0.18μm CMOS

### ■ CPU

- F<sup>2</sup>MC-16FX CPU
- Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
- 8-byte instruction queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

### ■ System clock

- On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
- 4MHz to 8MHz crystal oscillator (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 8MHz external clock for devices with fast clock input feature
- 32.768kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
- Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
- The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
- Low Power Consumption - 13 operating modes (different Run, Sleep, Timer, Stop modes)

### ■ On-chip voltage regulator

Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption

### ■ Low voltage detection function

Reset is generated when supply voltage falls below programmable reference voltage

### ■ Code Security

Protects Flash Memory content from unintended read-out

### ■ DMA

Automatic transfer function independent of CPU, can be assigned freely to resources

### ■ Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

### ■ CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1Mbps
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

### ■ USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

### ■ I<sup>2</sup>C

- Up to 400kbps
- Master and Slave functionality, 7-bit and 10-bit addressing



- A/D converter
  - SAR-type
  - 8/10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
  - Range Comparator Function
  - Scan Disable Function
  - ADC Pulse Detection Function
- Source Clock Timers
  - Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- Reload Timers
  - 16-bit wide
  - Prescaler with  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$  of peripheral clock frequency
  - Event count function
- Free-Running Timers
  - Signals an interrupt on overflow
  - Prescaler with  $1$ ,  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$ ,  $1/2^7$ ,  $1/2^8$  of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as  $2 \times 8$ -bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows  $1$ ,  $1/4$ ,  $1/16$ ,  $1/64$  of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
- Stepping Motor Controller
  - Stepping Motor Controller with integrated high current output drivers
  - Four high current outputs for each channel
  - Two synchronized 8/10-bit PWMs per channel
  - Internal prescaling for PWM clock:  $1$ ,  $1/4$ ,  $1/5$ ,  $1/6$ ,  $1/8$ ,  $1/10$ ,  $1/12$ ,  $1/16$  of peripheral clock
  - Dedicated power supply for high current output drivers
- LCD Controller
  - LCD controller with up to  $4\text{COM} \times 24\text{SEG}$
  - Internal or external voltage generation
  - Duty cycle: Selectable from options:  $1/2$ ,  $1/3$  and  $1/4$
  - Fixed  $1/3$  bias
  - Programmable frame period
  - Clock source selectable from four options (main clock, peripheral clock, subclock or RC oscillator clock)
  - Internal divider resistors or external divider resistors
  - On-chip data memory for display
  - LCD display can be operated in Timer Mode
  - Blank display: selectable
  - All SEG, COM and V pins can be switched between general and specialized purposes
- Sound Generator
  - 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
  - PWM clock by internal prescaler:  $1$ ,  $1/2$ ,  $1/4$ ,  $1/8$  of peripheral clock
- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock
- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, can not be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0
- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I2C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor

### ■ Built-in On Chip Debugger (OCD)

- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - Data event: 6 points
  - Event sequencer: 2 levels + reset
- Execution time measurement function
- Trace function: 42 branches
- Security function

### ■ Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the automatic algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase or write

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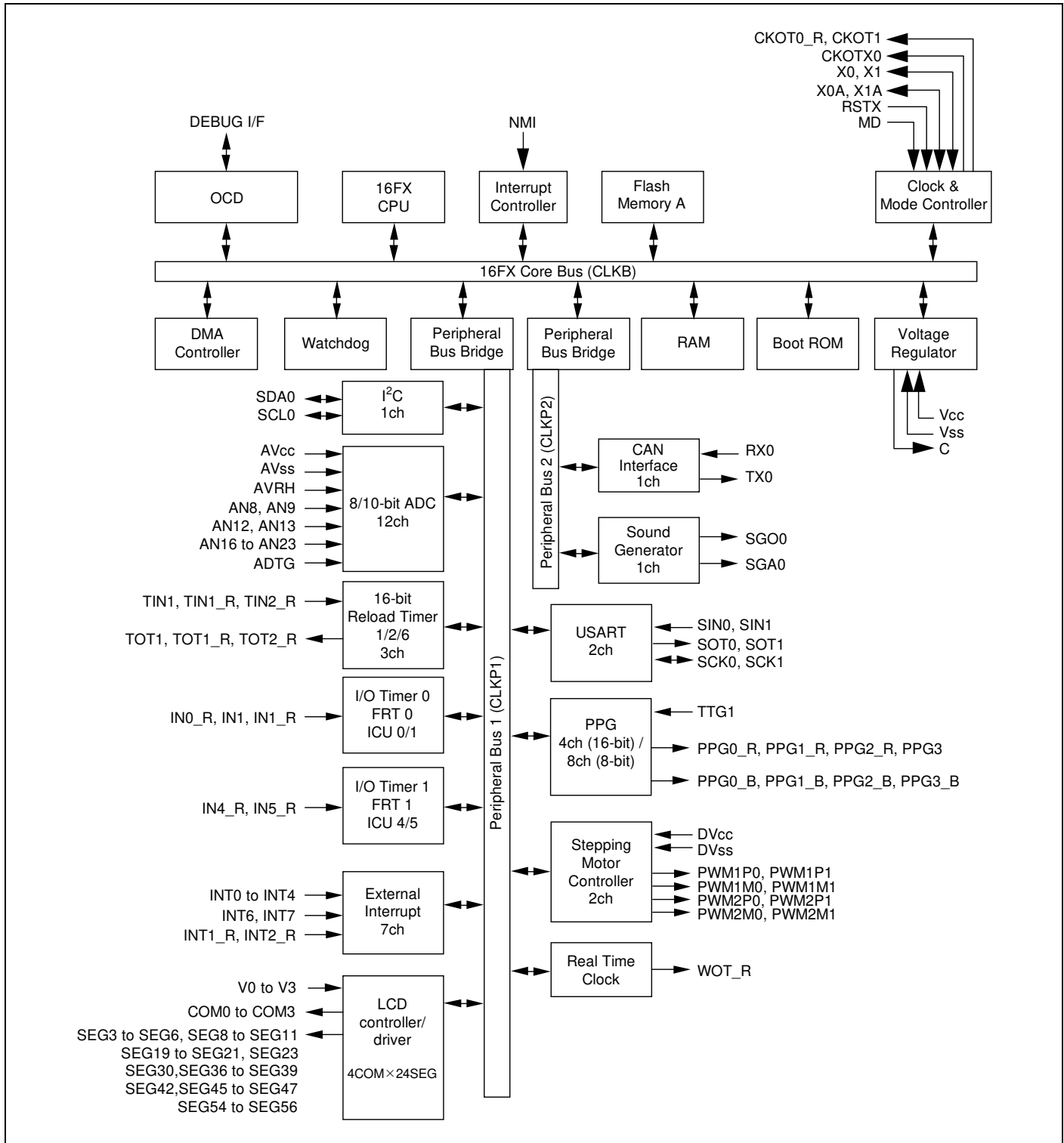
## 1. Product Lineup

Features		MB96670	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
64.5KB + 32KB	4KB	MB96F673R, MB96F673A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB	4KB	MB96F675R, MB96F675A	
Package		LQFP-64 FPT-64P-M23/M24	
DMA		2ch	
USART		2ch	LIN-USART 0/1
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO	No	
I <sup>2</sup> C		1ch	I <sup>2</sup> C 0
8/10-bit A/D Converter		12ch	AN 8/9/12/13/16 to 23
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	Yes	
16-bit Reload Timer (RLT)		3ch	RLT 1/2/6
16-bit Free-Running Timer (FRT)		2ch	FRT 0/1
16-bit Input Capture Unit (ICU)		4ch (2 channels for LIN-USART)	ICU 0/1/4/5 ICU 0/1 for LIN-USART
8/16-bit Programmable Pulse Generator (PPG)		4ch (16-bit) / 8ch (8-bit)	PPG 0 to 3
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
CAN Interface		1ch	CAN 0 32 Message Buffers
Stepping Motor Controller (SMC)		2ch	SMC 0/1
External Interrupts (INT)		7ch	INT 0 to 4/6/7
Non-Maskable Interrupt (NMI)		1ch	
Sound Generator (SG)		1ch	SG 0
LCD Controller		4COM × 24SEG	COM 0 to 3 SEG 3 to 6/8 to 11/ 19 to 21/23/30/36 to 39/42/45 to 47/54 to 56
Real Time Clock (RTC)		1ch	
I/O Ports		48 (Dual clock mode) 50 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

### Note:

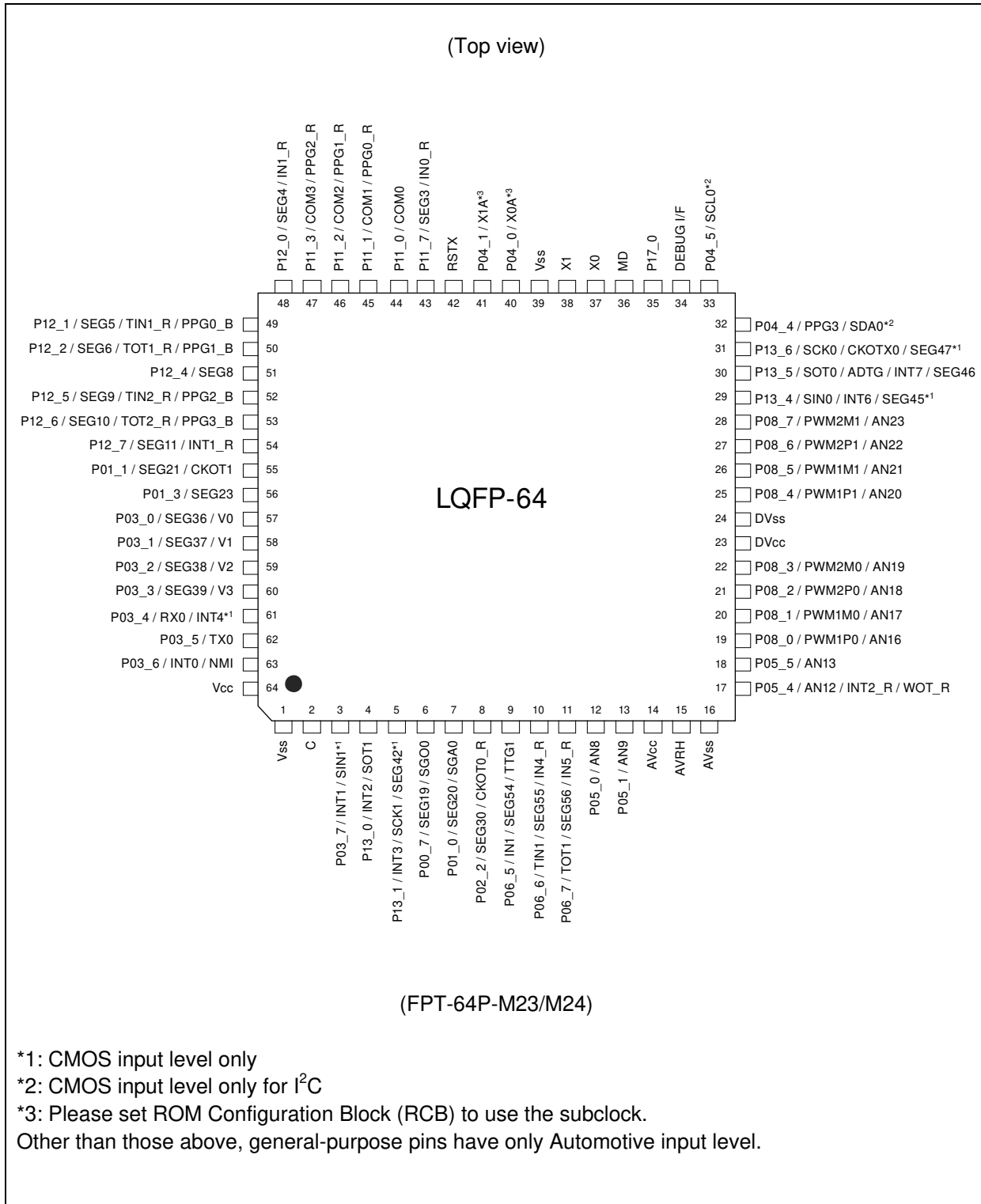
All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.

## 2. Block Diagram





### 3. Pin Assignment



#### 4. Pin Description

Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
COMn	LCD	LCD Common driver pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
DVcc	Supply	SMC pins power supply
DVss	Supply	SMC pins power supply
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PWMn	SMC	SMC PWM high current output pin
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCLn	I <sup>2</sup> C	I <sup>2</sup> C interface n clock I/O input/output pin
SDAn	I <sup>2</sup> C	I <sup>2</sup> C interface n serial data I/O input/output pin
SEGn	LCD	LCD Segment driver pin
SGAn	Sound Generator	Sound Generator amplitude output pin
SGOn	Sound Generator	Sound Generator sound/tone output pin
SINn	USART	USART n serial data input pin
SOTn	USART	USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TINn_R	Reload Timer	Relocated Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TOTn_R	Reload Timer	Relocated Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin

<b>Pin name</b>	<b>Feature</b>	<b>Description</b>
Vn	LCD	LCD voltage reference pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin

**5. Pin Circuit Type**

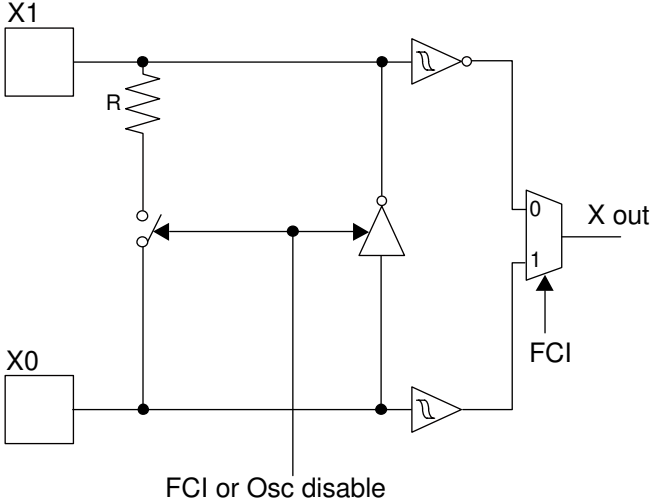
Pin no.	I/O circuit type*	Pin name
1	Supply	Vss
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	P	P13_1 / INT3 / SCK1 / SEG42
6	J	P00_7 / SEG19 / SGO0
7	J	P01_0 / SEG20 / SGA0
8	J	P02_2 / SEG30 / CKOT0_R
9	J	P06_5 / IN1 / SEG54 / TTG1
10	J	P06_6 / TIN1 / SEG55 / IN4_R
11	J	P06_7 / TOT1 / SEG56 / IN5_R
12	K	P05_0 / AN8
13	K	P05_1 / AN9
14	Supply	AVcc
15	G	AVRH
16	Supply	AVss
17	K	P05_4 / AN12 / INT2_R / WOT_R
18	K	P05_5 / AN13
19	R	P08_0 / PWM1P0 / AN16
20	R	P08_1 / PWM1M0 / AN17
21	R	P08_2 / PWM2P0 / AN18
22	R	P08_3 / PWM2M0 / AN19
23	Supply	DVcc
24	Supply	DVss
25	R	P08_4 / PWM1P1 / AN20
26	R	P08_5 / PWM1M1 / AN21
27	R	P08_6 / PWM2P1 / AN22
28	R	P08_7 / PWM2M1 / AN23
29	P	P13_4 / SIN0 / INT6 / SEG45
30	J	P13_5 / SOT0 / ADTG / INT7 / SEG46
31	P	P13_6 / SCK0 / CKOTX0 / SEG47
32	N	P04_4 / PPG3 / SDA0

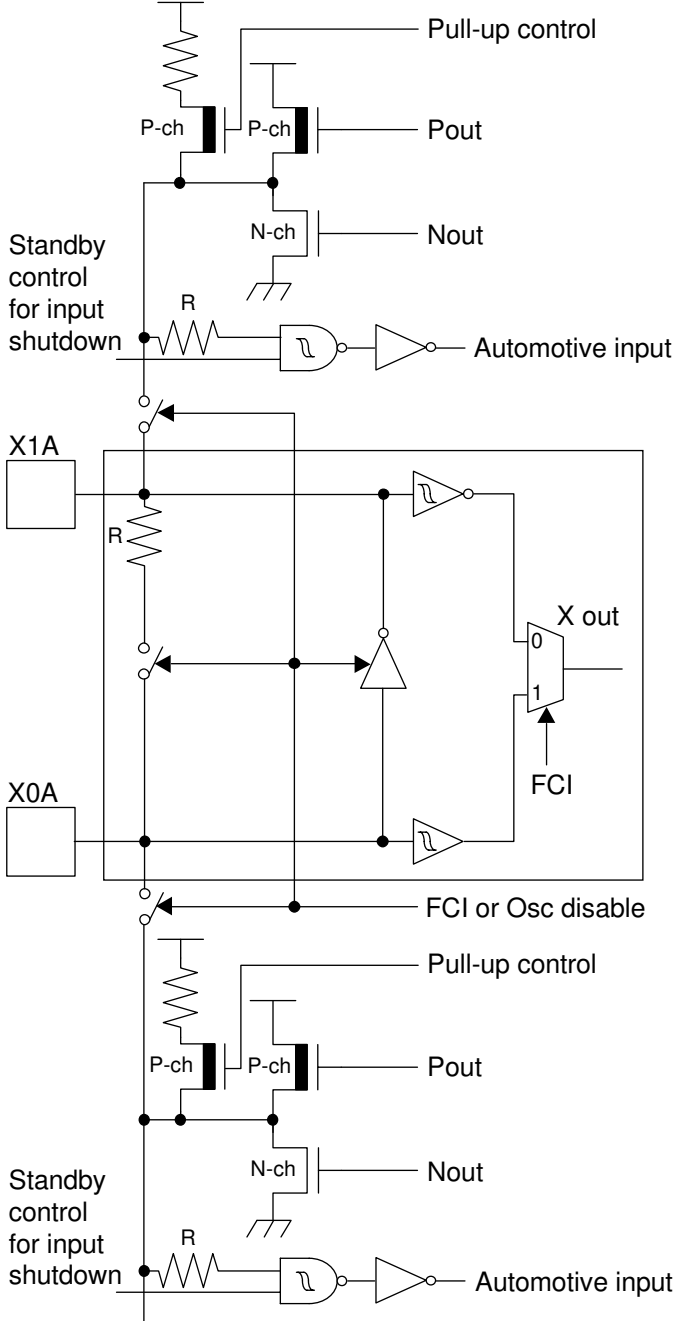
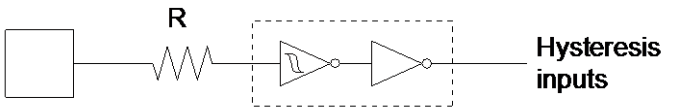
Pin no.	I/O circuit type*	Pin name
33	N	P04_5 / SCL0
34	O	DEBUG I/F
35	H	P17_0
36	C	MD
37	A	X0
38	A	X1
39	Supply	Vss
40	B	P04_0 / X0A
41	B	P04_1 / X1A
42	C	RSTX
43	J	P11_7 / SEG3 / IN0_R
44	J	P11_0 / COM0
45	J	P11_1 / COM1 / PPG0_R
46	J	P11_2 / COM2 / PPG1_R
47	J	P11_3 / COM3 / PPG2_R
48	J	P12_0 / SEG4 / IN1_R
49	J	P12_1 / SEG5 / TIN1_R / PPG0_B
50	J	P12_2 / SEG6 / TOT1_R / PPG1_B
51	J	P12_4 / SEG8
52	J	P12_5 / SEG9 / TIN2_R / PPG2_B
53	J	P12_6 / SEG10 / TOT2_R / PPG3_B
54	J	P12_7 / SEG11 / INT1_R
55	J	P01_1 / SEG21 / CKOT1
56	J	P01_3 / SEG23
57	L	P03_0 / SEG36 / V0
58	L	P03_1 / SEG37 / V1
59	L	P03_2 / SEG38 / V2
60	L	P03_3 / SEG39 / V3
61	M	P03_4 / RX0 / INT4
62	H	P03_5 / TX0
63	H	P03_6 / INT0 / NMI
64	Supply	Vcc

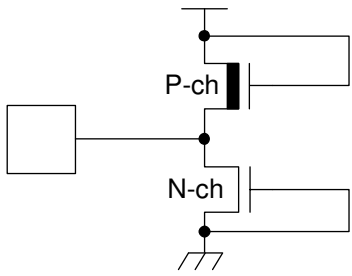
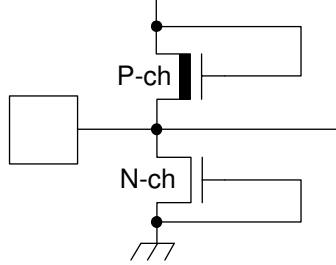
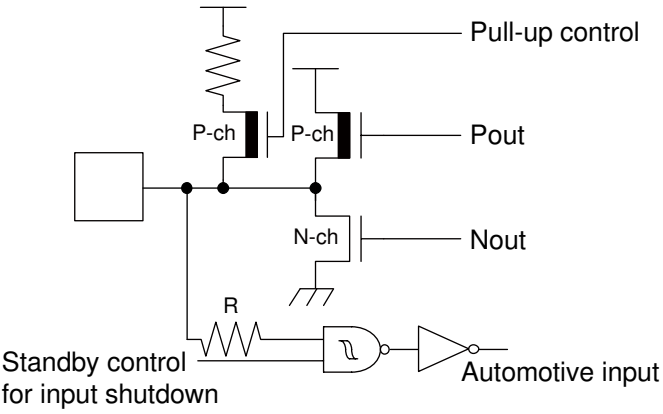
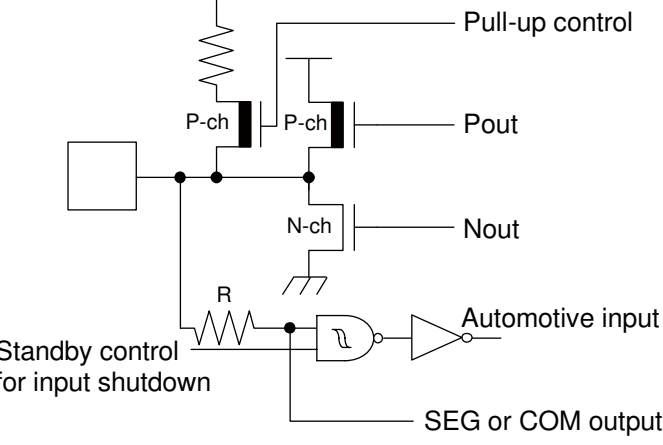
\*: See "I/O CIRCUIT TYPE" for details on the I/O circuit types.

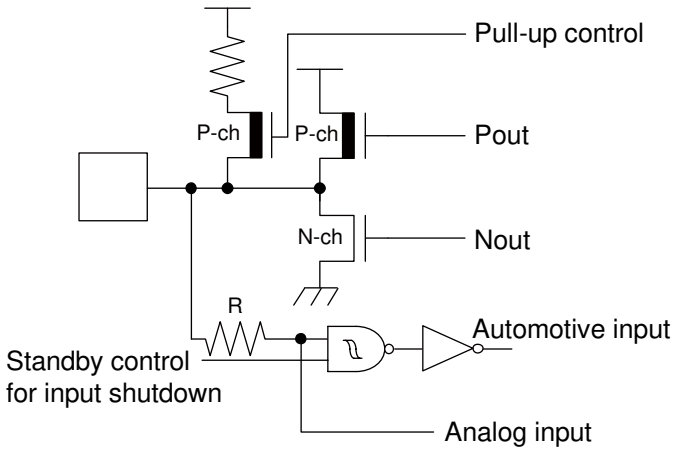
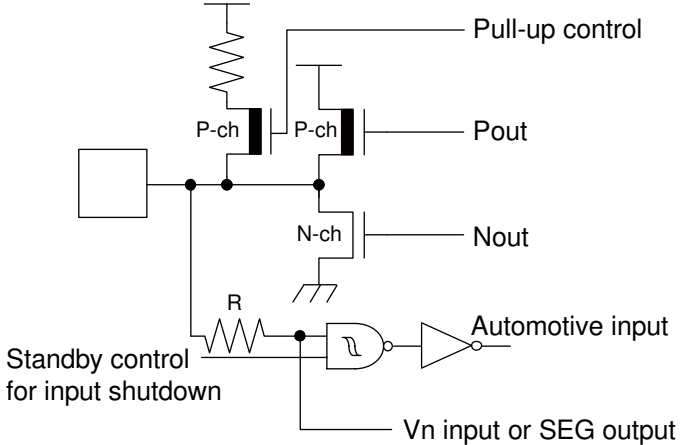
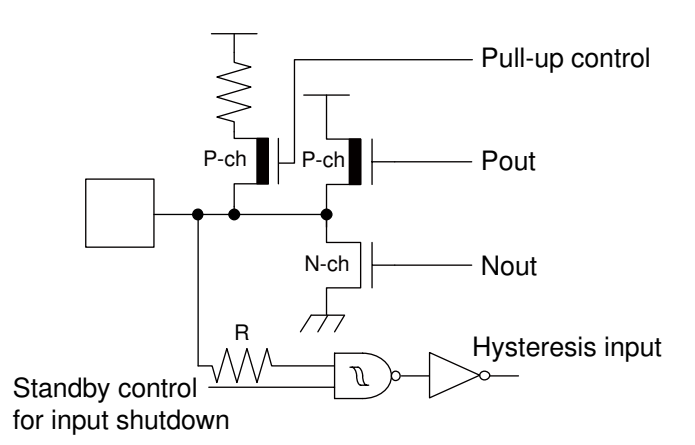


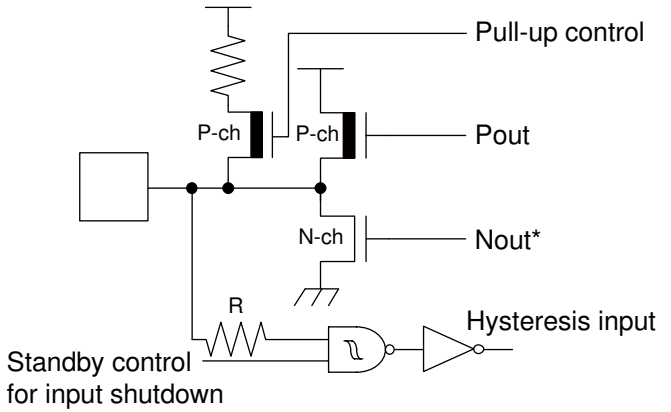
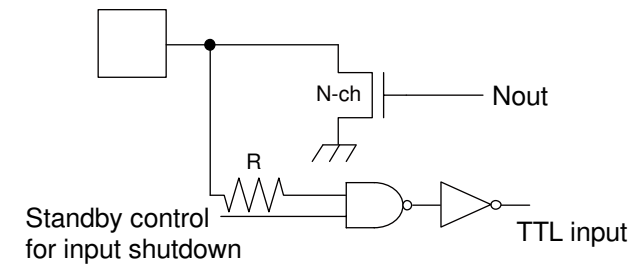
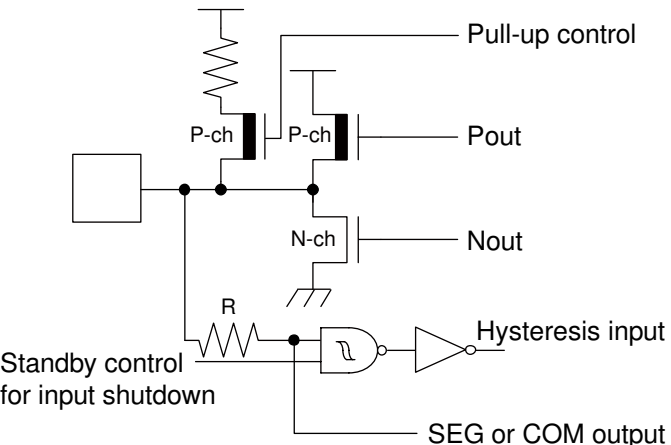
6. I/O Circuit Type

Type	Circuit	Remarks
A		<p>High-speed oscillation circuit:</p> <ul style="list-style-type: none"> <li>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)</li> <li>• Feedback resistor = approx. 1.0MΩ</li> <li>• The amplitude: 1.8V±0.15V to operate by the internal supply voltage</li> </ul>

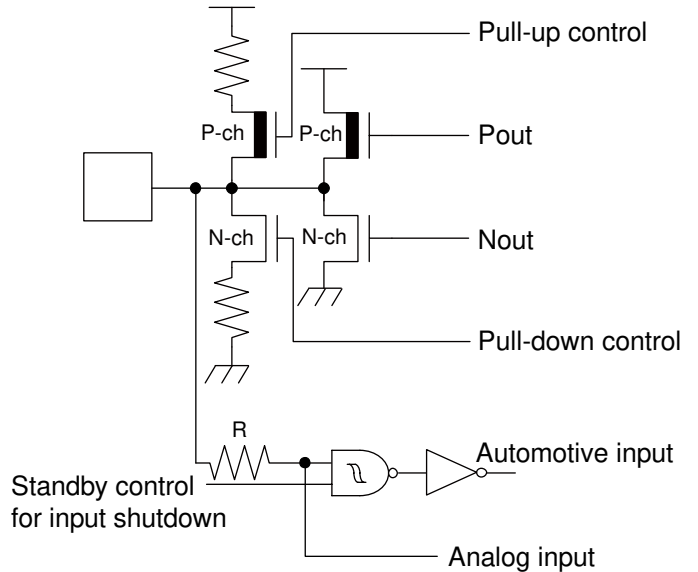
Type	Circuit	Remarks
B	 <p>The diagram for Type B shows a complex input circuit. At the top, a pull-up resistor is connected to a 'Pull-up control' signal. Below it, two P-channel MOSFETs (P-ch) are shown, one labeled 'Pout'. An N-channel MOSFET (N-ch) is labeled 'Nout'. A 'Standby control for input shutdown' signal is connected to a resistor 'R' and an AND gate. The output of the AND gate is an 'Automotive input' signal. Below this, two multiplexers 'X1A' and 'X0A' are shown. 'X1A' has a resistor 'R' and a switch. 'X0A' has a switch. The outputs of these multiplexers are connected to an AND gate, which is then connected to an 'Automotive input' signal. The output of this AND gate is connected to the 'FCI' input of a multiplexer 'X out'. The 'X out' multiplexer has two inputs, '0' and '1', and an output 'X out'. A 'FCI or Osc disable' signal is connected to the 'FCI' input of 'X out'. At the bottom, there is another pull-up control circuit with P-ch and N-ch MOSFETs, and an 'Automotive input' signal.</p>	<p>Low-speed oscillation circuit shared with GPIO functionality:</p> <ul style="list-style-type: none"> <li>• Feedback resistor = approx. 5.0MΩ</li> <li>• GPIO functionality selectable (CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>), Automotive input with input shutdown function and programmable pull-up resistor)</li> </ul>
C	 <p>The diagram for Type C shows a simple circuit with a resistor 'R' connected to a 'Hysteresis inputs' pin. The 'Hysteresis inputs' pin is connected to a hysteresis circuit, which is represented by a dashed box containing two inverters connected in a feedback loop.</p>	<p>CMOS hysteresis input pin</p>

Type	Circuit	Remarks
F		Power supply input protection circuit
G		<ul style="list-style-type: none"> <li>• A/D converter ref+ (AVRH) power supply input pin with protection circuit</li> <li>• Without protection circuit against V<sub>CC</sub> for pins AVRH</li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• Automotive input with input shutdown function</li> <li>• Programmable pull-up resistor</li> </ul>
J		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• Automotive input with input shutdown function</li> <li>• Programmable pull-up resistor</li> <li>• SEG or COM output</li> </ul>

Type	Circuit	Remarks
K		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• Automotive input with input shutdown function</li> <li>• Programmable pull-up resistor</li> <li>• Analog input</li> </ul>
L		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• Automotive input with input shutdown function</li> <li>• Programmable pull-up resistor</li> <li>• Vn input or SEG output</li> </ul>
M		<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• CMOS hysteresis input with input shutdown function</li> <li>• Programmable pull-up resistor</li> </ul>

Type	Circuit	Remarks
N	 <p>The diagram shows a CMOS output stage. A pull-up resistor is connected to the input of a P-channel MOSFET (P-ch). The gate of this P-ch MOSFET is controlled by a 'Pull-up control' signal. The drain of the P-ch MOSFET is connected to the output 'Pout'. The source of the P-ch MOSFET is connected to the gate of an N-channel MOSFET (N-ch). The drain of the N-ch MOSFET is connected to the output 'Nout*'. The source of the N-ch MOSFET is connected to ground. A 'Standby control for input shutdown' signal is connected to the input through a resistor 'R'. This signal also passes through an AND gate and an inverter to become the 'Hysteresis input'.</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 3\text{mA}</math>, <math>I_{OH} = -3\text{mA}</math>)</li> <li>• CMOS hysteresis input with input shutdown function</li> <li>• Programmable pull-up resistor</li> </ul> <p>*: N-channel transistor has slew rate control according to I<sup>2</sup>C spec, irrespective of usage.</p>
O	 <p>The diagram shows an open-drain output stage. The input is connected to the gate of an N-channel MOSFET (N-ch). The drain of the N-ch MOSFET is connected to the output 'Nout'. The source of the N-ch MOSFET is connected to ground. A 'Standby control for input shutdown' signal is connected to the input through a resistor 'R'. This signal also passes through an AND gate and an inverter to become the 'TTL input'.</p>	<ul style="list-style-type: none"> <li>• Open-drain I/O</li> <li>• Output 25mA, <math>V_{CC} = 2.7\text{V}</math></li> <li>• TTL input</li> </ul>
P	 <p>The diagram shows a CMOS output stage similar to Type N. A pull-up resistor is connected to the input of a P-channel MOSFET (P-ch). The gate of this P-ch MOSFET is controlled by a 'Pull-up control' signal. The drain of the P-ch MOSFET is connected to the output 'Pout'. The source of the P-ch MOSFET is connected to the gate of an N-channel MOSFET (N-ch). The drain of the N-ch MOSFET is connected to the output 'Nout'. The source of the N-ch MOSFET is connected to ground. A 'Standby control for input shutdown' signal is connected to the input through a resistor 'R'. This signal also passes through an AND gate and an inverter to become the 'Hysteresis input'. Additionally, the signal after the AND gate is connected to the output 'SEG or COM output'.</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• CMOS hysteresis inputs with input shutdown function</li> <li>• Programmable pull-up resistor</li> <li>• SEG or COM output</li> </ul>



Type	Circuit	Remarks
R	 <p>The diagram shows a CMOS input/output pin. It features a pull-up resistor connected to VDD and a pull-down resistor connected to ground. The output node is driven by a P-channel MOSFET (Pout) and an N-channel MOSFET (Nout). Control signals for the pull-up and pull-down resistors are labeled 'Pull-up control' and 'Pull-down control'. An automotive input section includes a resistor 'R', an AND gate, and an inverter, with inputs for 'Standby control for input shutdown' and 'Analog input'.</p>	<ul style="list-style-type: none"> <li>• CMOS level output (programmable <math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math> and <math>I_{OL} = 30\text{mA}</math>, <math>I_{OH} = -30\text{mA}</math>)</li> <li>• Automotive input with input shutdown function</li> <li>• Programmable pull-up / pull-down resistor</li> <li>• Analog input</li> </ul>

## 7. Memory Map

FF:FFFF <sub>H</sub>	USER ROM*1
DE:0000 <sub>H</sub> DD:FFFF <sub>H</sub>	Reserved
10:0000 <sub>H</sub>	Boot-ROM
0F:C000 <sub>H</sub>	Peripheral
0E:9000 <sub>H</sub>	Reserved
01:0000 <sub>H</sub>	ROM/RAM MIRROR
00:8000 <sub>H</sub>	Internal RAM bank0
RAMSTART0*2	Reserved
00:0C00 <sub>H</sub>	Peripheral
00:0380 <sub>H</sub>	GPR*3
00:0180 <sub>H</sub>	DMA
00:0100 <sub>H</sub>	Reserved
00:00F0 <sub>H</sub>	Reserved
00:0000 <sub>H</sub>	Peripheral

\*1: For details about USER ROM area, see “User ROM Memory Map For Flash Devices” on the following pages.

\*2: For RAMSTART addresses, see the table on the next page.

\*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

**8. RAMSTART Addresses**

<b>Devices</b>	<b>Bank 0 RAM size</b>	<b>RAMSTART0</b>
MB96F673 MB96F675	4KB	00:7200 <sub>H</sub>

**9. User ROM Memory Map For Flash Devices**

CPU mode address	Flash memory mode address	MB96F673	MB96F675	
		Flash size 64.5KB + 32KB	Flash size 128.5KB + 32KB	
FF:FFFFH FF:0000H	3F:FFFFH 3F:0000H	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFFH FE:0000H	3E:FFFFH 3E:0000H	Reserved	SA38 - 64KB	
FD:FFFFH			Reserved	
DF:A000H				
DF:9FFFH DF:8000H	1F:9FFFH 1F:8000H	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFFH DF:6000H	1F:7FFFH 1F:6000H	SA3 - 8KB	SA3 - 8KB	
DF:5FFFH DF:4000H	1F:5FFFH 1F:4000H	SA2 - 8KB	SA2 - 8KB	
DF:3FFFH DF:2000H	1F:3FFFH 1F:2000H	SA1 - 8KB	SA1 - 8KB	
DF:1FFFH DF:0000H	1F:1FFFH 1F:0000H	SAS - 512B*	SAS - 512B*	
DE:FFFFH DE:0000H		Reserved	Reserved	Bank A of Flash A

\*: Physical address area of SAS-512B is from DF:0000H to DF:01FFH.  
Others (from DF:0200H to DF:1FFFH) is mirror area of SAS-512B.  
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000H -DF:01FFH.  
SAS can not be used for E<sup>2</sup>PROM emulation.

## 10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

<b>MB96670</b>		
Pin Number	USART Number	Normal Function
29	USART0	SIN0
30		SOT0
31		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1



## 11. Interrupt Vector Table

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC <sub>H</sub>	CALLV0	No	-	CALLV instruction
1	3F8 <sub>H</sub>	CALLV1	No	-	CALLV instruction
2	3F4 <sub>H</sub>	CALLV2	No	-	CALLV instruction
3	3F0 <sub>H</sub>	CALLV3	No	-	CALLV instruction
4	3EC <sub>H</sub>	CALLV4	No	-	CALLV instruction
5	3E8 <sub>H</sub>	CALLV5	No	-	CALLV instruction
6	3E4 <sub>H</sub>	CALLV6	No	-	CALLV instruction
7	3E0 <sub>H</sub>	CALLV7	No	-	CALLV instruction
8	3DC <sub>H</sub>	RESET	No	-	Reset vector
9	3D8 <sub>H</sub>	INT9	No	-	INT9 instruction
10	3D4 <sub>H</sub>	EXCEPTION	No	-	Undefined instruction execution
11	3D0 <sub>H</sub>	NMI	No	-	Non-Maskable Interrupt
12	3CC <sub>H</sub>	DLY	No	12	Delayed Interrupt
13	3C8 <sub>H</sub>	RC_TIMER	No	13	RC Clock Timer
14	3C4 <sub>H</sub>	MC_TIMER	No	14	Main Clock Timer
15	3C0 <sub>H</sub>	SC_TIMER	No	15	Sub Clock Timer
16	3BC <sub>H</sub>	LVDI	No	16	Low Voltage Detector
17	3B8 <sub>H</sub>	EXTINT0	Yes	17	External Interrupt 0
18	3B4 <sub>H</sub>	EXTINT1	Yes	18	External Interrupt 1
19	3B0 <sub>H</sub>	EXTINT2	Yes	19	External Interrupt 2
20	3AC <sub>H</sub>	EXTINT3	Yes	20	External Interrupt 3
21	3A8 <sub>H</sub>	EXTINT4	Yes	21	External Interrupt 4
22	3A4 <sub>H</sub>	-	-	22	Reserved
23	3A0 <sub>H</sub>	EXTINT6	Yes	23	External Interrupt 6
24	39C <sub>H</sub>	EXTINT7	Yes	24	External Interrupt 7
25	398 <sub>H</sub>	-	-	25	Reserved
26	394 <sub>H</sub>	-	-	26	Reserved
27	390 <sub>H</sub>	-	-	27	Reserved
28	38C <sub>H</sub>	-	-	28	Reserved
29	388 <sub>H</sub>	-	-	29	Reserved
30	384 <sub>H</sub>	-	-	30	Reserved
31	380 <sub>H</sub>	-	-	31	Reserved
32	37C <sub>H</sub>	-	-	32	Reserved
33	378 <sub>H</sub>	CAN0	No	33	CAN Controller 0
34	374 <sub>H</sub>	-	-	34	Reserved
35	370 <sub>H</sub>	-	-	35	Reserved
36	36C <sub>H</sub>	-	-	36	Reserved
37	368 <sub>H</sub>	-	-	37	Reserved
38	364 <sub>H</sub>	PPG0	Yes	38	Programmable Pulse Generator 0
39	360 <sub>H</sub>	PPG1	Yes	39	Programmable Pulse Generator 1

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	35C <sub>H</sub>	PPG2	Yes	40	Programmable Pulse Generator 2
41	358 <sub>H</sub>	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 <sub>H</sub>	-	-	42	Reserved
43	350 <sub>H</sub>	-	-	43	Reserved
44	34C <sub>H</sub>	-	-	44	Reserved
45	348 <sub>H</sub>	-	-	45	Reserved
46	344 <sub>H</sub>	-	-	46	Reserved
47	340 <sub>H</sub>	-	-	47	Reserved
48	33C <sub>H</sub>	-	-	48	Reserved
49	338 <sub>H</sub>	-	-	49	Reserved
50	334 <sub>H</sub>	-	-	50	Reserved
51	330 <sub>H</sub>	-	-	51	Reserved
52	32C <sub>H</sub>	-	-	52	Reserved
53	328 <sub>H</sub>	-	-	53	Reserved
54	324 <sub>H</sub>	-	-	54	Reserved
55	320 <sub>H</sub>	-	-	55	Reserved
56	31C <sub>H</sub>	-	-	56	Reserved
57	318 <sub>H</sub>	-	-	57	Reserved
58	314 <sub>H</sub>	-	-	58	Reserved
59	310 <sub>H</sub>	RLT1	Yes	59	Reload Timer 1
60	30C <sub>H</sub>	RLT2	Yes	60	Reload Timer 2
61	308 <sub>H</sub>	-	-	61	Reserved
62	304 <sub>H</sub>	-	-	62	Reserved
63	300 <sub>H</sub>	-	-	63	Reserved
64	2FC <sub>H</sub>	RLT6	Yes	64	Reload Timer 6
65	2F8 <sub>H</sub>	ICU0	Yes	65	Input Capture Unit 0
66	2F4 <sub>H</sub>	ICU1	Yes	66	Input Capture Unit 1
67	2F0 <sub>H</sub>	-	-	67	Reserved
68	2EC <sub>H</sub>	-	-	68	Reserved
69	2E8 <sub>H</sub>	ICU4	Yes	69	Input Capture Unit 4
70	2E4 <sub>H</sub>	ICU5	Yes	70	Input Capture Unit 5
71	2E0 <sub>H</sub>	-	-	71	Reserved
72	2DC <sub>H</sub>	-	-	72	Reserved
73	2D8 <sub>H</sub>	-	-	73	Reserved
74	2D4 <sub>H</sub>	-	-	74	Reserved
75	2D0 <sub>H</sub>	-	-	75	Reserved
76	2CC <sub>H</sub>	-	-	76	Reserved
77	2C8 <sub>H</sub>	-	-	77	Reserved
78	2C4 <sub>H</sub>	-	-	78	Reserved
79	2C0 <sub>H</sub>	-	-	79	Reserved
80	2BC <sub>H</sub>	-	-	80	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	2B8 <sub>H</sub>	-	-	81	Reserved
82	2B4 <sub>H</sub>	-	-	82	Reserved
83	2B0 <sub>H</sub>	-	-	83	Reserved
84	2AC <sub>H</sub>	-	-	84	Reserved
85	2A8 <sub>H</sub>	-	-	85	Reserved
86	2A4 <sub>H</sub>	-	-	86	Reserved
87	2A0 <sub>H</sub>	-	-	87	Reserved
88	29C <sub>H</sub>	-	-	88	Reserved
89	298 <sub>H</sub>	FRT0	Yes	89	Free-Running Timer 0
90	294 <sub>H</sub>	FRT1	Yes	90	Free-Running Timer 1
91	290 <sub>H</sub>	-	-	91	Reserved
92	28C <sub>H</sub>	-	-	92	Reserved
93	288 <sub>H</sub>	RTC0	No	93	Real Time Clock
94	284 <sub>H</sub>	CAL0	No	94	Clock Calibration Unit
95	280 <sub>H</sub>	SG0	No	95	Sound Generator 0
96	27C <sub>H</sub>	IIC0	Yes	96	I <sup>2</sup> C interface 0
97	278 <sub>H</sub>	-	-	97	Reserved
98	274 <sub>H</sub>	ADC0	Yes	98	A/D Converter 0
99	270 <sub>H</sub>	-	-	99	Reserved
100	26C <sub>H</sub>	-	-	100	Reserved
101	268 <sub>H</sub>	LINR0	Yes	101	LIN USART 0 RX
102	264 <sub>H</sub>	LINT0	Yes	102	LIN USART 0 TX
103	260 <sub>H</sub>	LINR1	Yes	103	LIN USART 1 RX
104	25C <sub>H</sub>	LINT1	Yes	104	LIN USART 1 TX
105	258 <sub>H</sub>	-	-	105	Reserved
106	254 <sub>H</sub>	-	-	106	Reserved
107	250 <sub>H</sub>	-	-	107	Reserved
108	24C <sub>H</sub>	-	-	108	Reserved
109	248 <sub>H</sub>	-	-	109	Reserved
110	244 <sub>H</sub>	-	-	110	Reserved
111	240 <sub>H</sub>	-	-	111	Reserved
112	23C <sub>H</sub>	-	-	112	Reserved
113	238 <sub>H</sub>	-	-	113	Reserved
114	234 <sub>H</sub>	-	-	114	Reserved
115	230 <sub>H</sub>	-	-	115	Reserved
116	22C <sub>H</sub>	-	-	116	Reserved
117	228 <sub>H</sub>	-	-	117	Reserved
118	224 <sub>H</sub>	-	-	118	Reserved
119	220 <sub>H</sub>	-	-	119	Reserved
120	21C <sub>H</sub>	-	-	120	Reserved