



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





The MB9A140NB Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, and Communication Interfaces (UART, CSIO, I²C).

The products which are described in this datasheet are placed into TYPE6 product categories in FM3 Family Peripheral Manual.

Features

32-bit ARM[®] Cortex[®]-M3 Core

- Processor version: r2p1
- Up to 40 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC):
 - 1 NMI (non-maskable interrupt) and
 - 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Dual operation Flash memory
 - Dual Operation Flash memory has the upper bank and the lower bank.
So, this series could implement erase, write and read operations for each bank simultaneously.
 - Main area: Up to 256 Kbytes (Up to 240 Kbytes upper bank + 16 Kbytes lower bank)
 - Work area: 32 Kbytes (lower bank)
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 16 KB
- SRAM1: Up to 16 KB

External Bus Interface^[1]

- Supports SRAM, NOR Flash memory device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 MB
- Supports Address/Data multiplex
- Supports external RDY function
 - [1]: MB9AF141LB, F142LB and F144LB do not support External Bus Interface.

Multi-function Serial Interface (Max 8 channels)

- 4 channels with 16 steps×9-bit FIFO (ch.4 to ch.7), 4 channels without FIFO (ch.0 to ch.3)
- Operation mode is selectable from the followings for each channel.
 - UART
 - CSIO
 - I2C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control^[1]: Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detection functions available (parity errors, framing errors, and overrun errors)
 - [1]: MB9AF141LB, F142LB and F144LB do not support Hardware Flow control.

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

DMA Controller (8 channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 24 channels)
[12-bit A/D Converter]

- Successive Approximation type
- Built-in 2 units
- Conversion time: 2.0 μ s @ 2.7 V to 3.6 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 83 fast general-purpose I/O Ports@100 pin Package
- Some ports are 5 V tolerant I/O.
See Pin Description to confirm the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

HDMI-CEC/Remote Control Receiver (Up to 2 channels)

- HDMI-CEC transmitter
 - Header block automatic transmission by judging Signal free
 - Generating status interrupt by detecting Arbitration lost
 - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
 - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
 - Automatic ACK reply function available
 - Line error detection function available
- Remote control receiver
 - 4 bytes reception buffer
 - Repeat code detection function available

Real-time clock (RTC)

The Real-time clock can count

Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Watch Counter

The Watch counter is used for wake up from sleep and timer mode.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit

- Up to 16 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep Standby RTC and Deep Standby Stop modes.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock : 4 MHz to 48 MHz
- Sub Clock : 32.768 kHz
- Built-in high-speed CR Clock : 4 MHz
- Built-in low-speed CR Clock : 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- External clock failure (clock stop) is detected, reset is asserted.
- External frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Six low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop
- Deep Standby RTC (selectable between keeping the value of RAM and not)
- Deep Standby Stop (selectable between keeping the value of RAM and not)

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM).^[1]
 - [1]: MB9AF141LB/MB, F142LB/MB and F144LB/MB support only SWJ-DP.

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

Wide range voltage: VCC = 1.65 V to 3.6 V

Contents

1. Product Lineup	7
2. Packages	8
3. Pin Assignment	9
4. List of Pin Functions	16
5. I/O Circuit Type	39
6. Handling Precaution	44
6.1 Precautions for Product Design	44
6.2 Precautions for Package Mounting.....	45
6.3 Precautions for Use Environment	46
7. Handling Devices	47
8. Block Diagram	49
9. Memory Size	50
10. Memory Map	50
11. Pin Status in Each CPU State	53
12. Electrical Characteristics	60
12.1 Absolute Maximum Ratings.....	60
12.2 Recommended Operating Conditions.....	61
12.3 DC Characteristics.....	62
12.3.1 Current Rating.....	62
12.3.2 Pin Characteristics	65
12.4 AC Characteristics.....	66
12.4.1 Main Clock Input Characteristics.....	66
12.4.2 Sub Clock Input Characteristics	67
12.4.3 Built-in CR Oscillation Characteristics.....	67
12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)	68
12.4.5 Operating Conditions of Main PLL (In the case of using the built-in High-speed CR for the input clock of the Main PLL)	68
12.4.6 Reset Input Characteristics	69
12.4.7 Power-on Reset Timing.....	69
12.4.8 External Bus Timing	70
12.4.9 Base Timer Input Timing	77
12.4.10 CSIO/UART Timing	78
12.4.11 External Input Timing.....	86
12.4.12 I ² C Timing.....	87
12.4.13 ETM Timing	88
12.4.14 JTAG Timing.....	89
12.5 12-bit A/D Converter.....	90
12.6 Low-Voltage Detection Characteristics.....	93
12.6.1 Low-Voltage Detection Reset.....	93
12.6.2 Interrupt of Low-Voltage Detection.....	94
12.7 Flash Memory Write/Erase Characteristics	95
12.7.1 Write / Erase time.....	95
12.7.2 Erase/write cycles and data hold time	95
12.8 Return Time from Low-Power Consumption Mode.....	96
12.8.1 Return Factor: Interrupt/WKUP	96
12.8.2 Return Factor: Reset.....	98



13. Ordering Information 100
14. Package Dimensions 102
15. Major Changes 111
Document History..... 113

1. Product Lineup

Memory Size

Product name		MB9AF141LB/MB/NB	MB9AF142LB/MB/NB	MB9AF144LB/MB/NB
On-chip Flash memory	Main area	64 KB	128 KB	256 KB
	Work area	32 KB	32 KB	32 KB
On-chip SRAM	SRAM0	8 KB	8 KB	16 KB
	SRAM1	8 KB	8 KB	16 KB
	Total	16 KB	16 KB	32 KB

Function

Product name		MB9AF141LB MB9AF142LB MB9AF144LB	MB9AF141MB MB9AF142MB MB9AF144MB	MB9AF141NB MB9AF142NB MB9AF144NB
Pin count		64	80/96	100/112
CPU		Cortex-M3		
Freq.		40 MHz		
Power supply voltage range		1.65 V to 3.6 V		
DMAC		8ch.		
External Bus Interface		-	Addr: 21-bit (Max) R/W Data: 8-bit (Max) CS: 4 (Max) Support: SRAM, NOR Flash memory	Addr: 25-bit (Max) R/W Data: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR Flash memory
Multi-function Serial Interface (UART/CSIO/I ² C)		8ch. (Max) ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO		
Base Timer (PWC/Reload timer/PWM/PPG)		8ch. (Max)		
Dual Timer		1 unit		
HDMI-CEC/ Remote Control Receiver		2ch. (Max)		
Real-Time Clock		1 unit		
Watch Counter		1 unit		
CRC Accelerator		Yes		
Watchdog timer		1ch. (SW) + 1ch. (HW)		
External Interrupts		8 pins (Max) + NMI × 1	11 pins (Max) + NMI × 1	16 pins (Max) + NMI × 1
I/O ports		51 pins (Max)	66 pins (Max)	83 pins (Max)
12-bit A/D converter		12ch. (2 units)	17ch. (2 units)	24ch. (2 units)
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2ch.		
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug Function		SWJ-DP		SWJ-DP/ETM
Unique ID		Yes		

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use. See 12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics for accuracy of built-in CR.

2. Packages

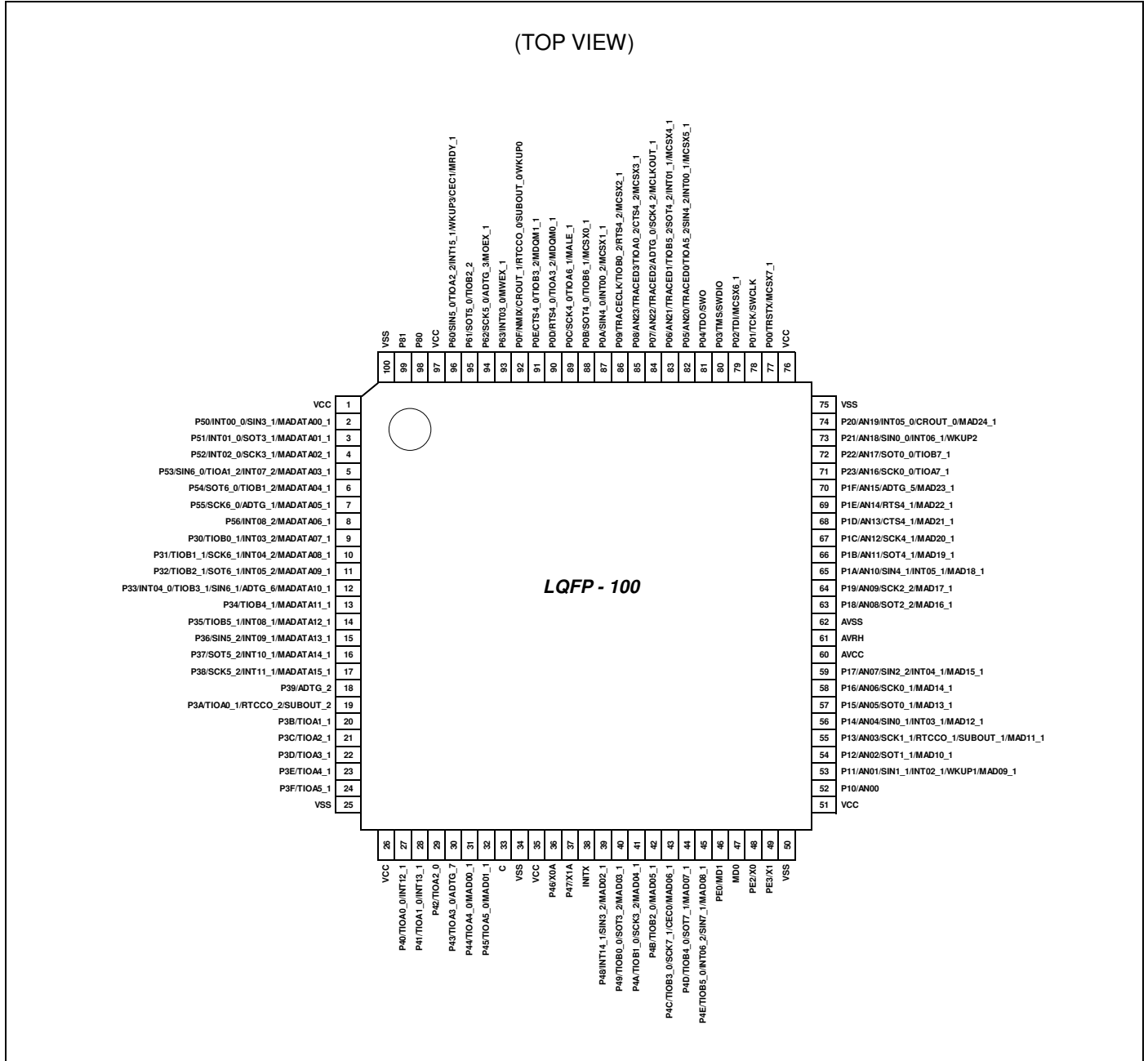
Package	Product name	MB9AF141LB MB9AF142LB MB9AF144LB	MB9AF141MB MB9AF142MB MB9AF144MB	MB9AF141NB MB9AF142NB MB9AF144NB
LQFP: FPT-64P-M38 (0.5mm pitch)		○	-	-
LQFP: FPT-64P-M39 (0.65mm pitch)		○	-	-
QFN: LCC-64P-M24 (0.5mm pitch)		○	-	-
LQFP: FPT-80P-M37 (0.5mm pitch)		-	○	-
LQFP: FPT-80P-M40 (0.65mm pitch)		-	○	-
BGA: BGA-96P-M07 (0.5mm pitch)		-	○	-
LQFP: FPT-100P-M23 (0.5mm pitch)		-	-	○
QFP: FPT-100P-M36 (0.65mm pitch)		-	-	○
BGA: BGA-112P-M04 (0.8mm pitch)		-	-	○

○: Supported

Note: See “14. Package Dimensions” for detailed information on each package.

3. Pin Assignment

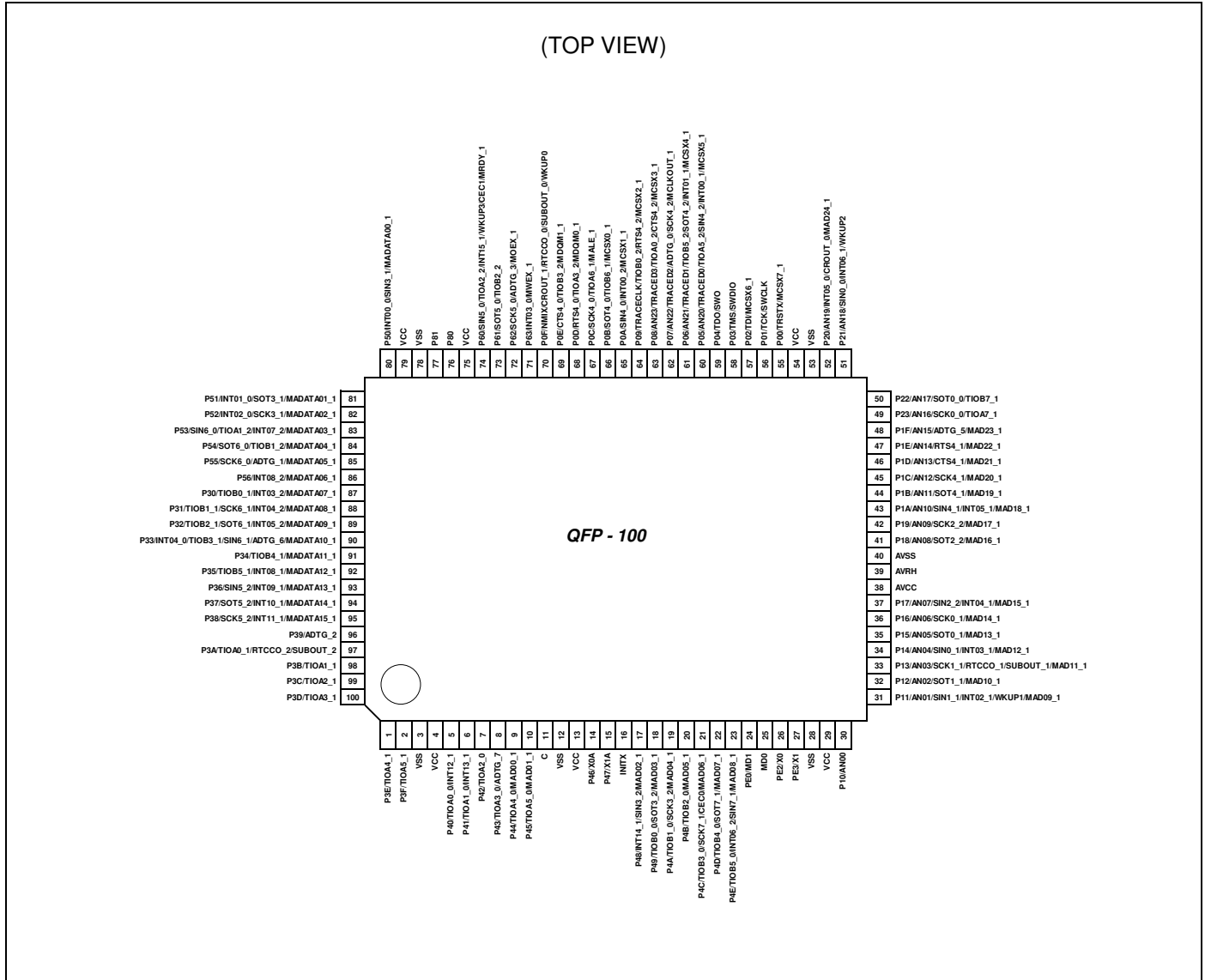
FPT-100P-M23



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

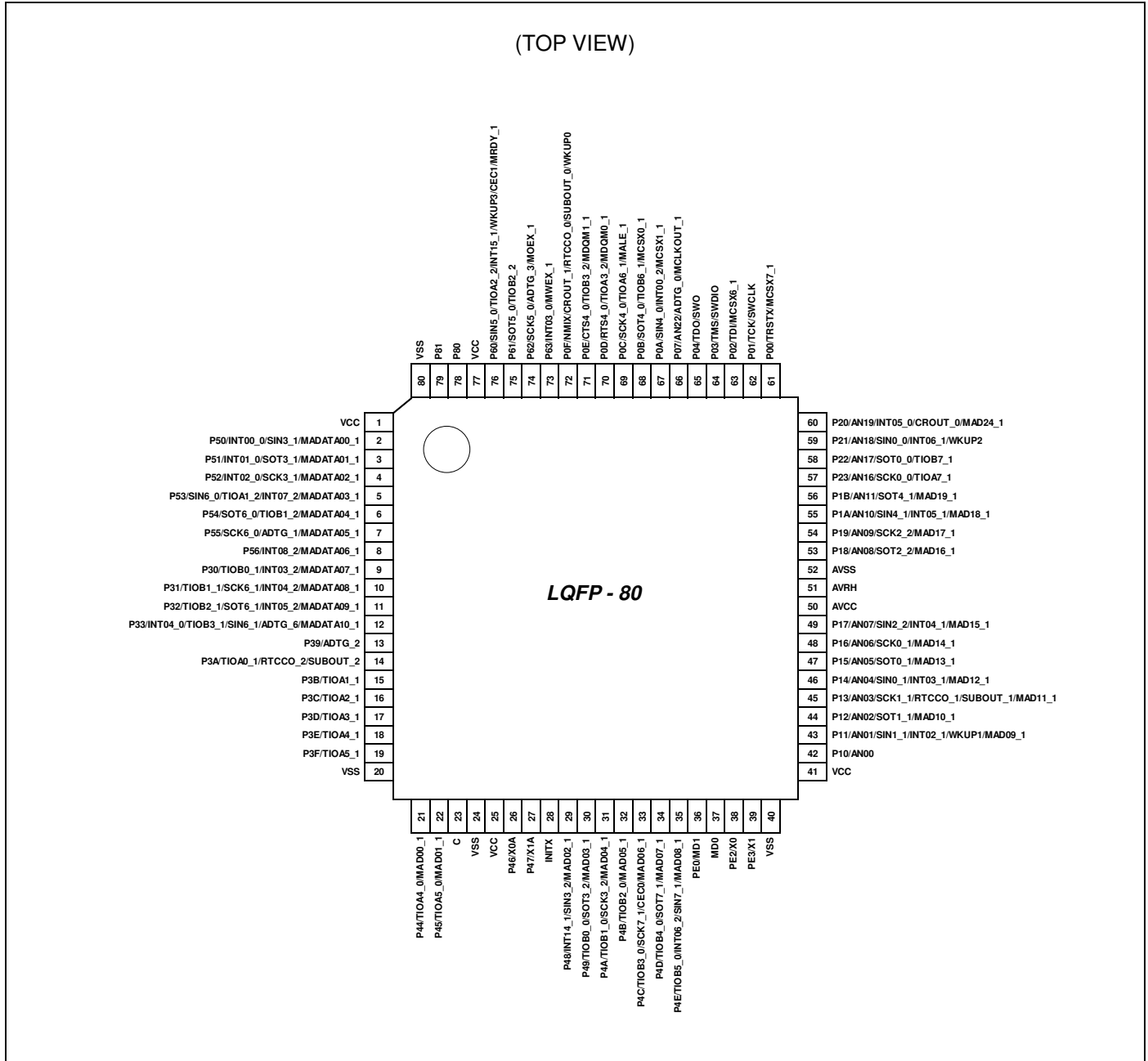
FPT-100P-M36



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

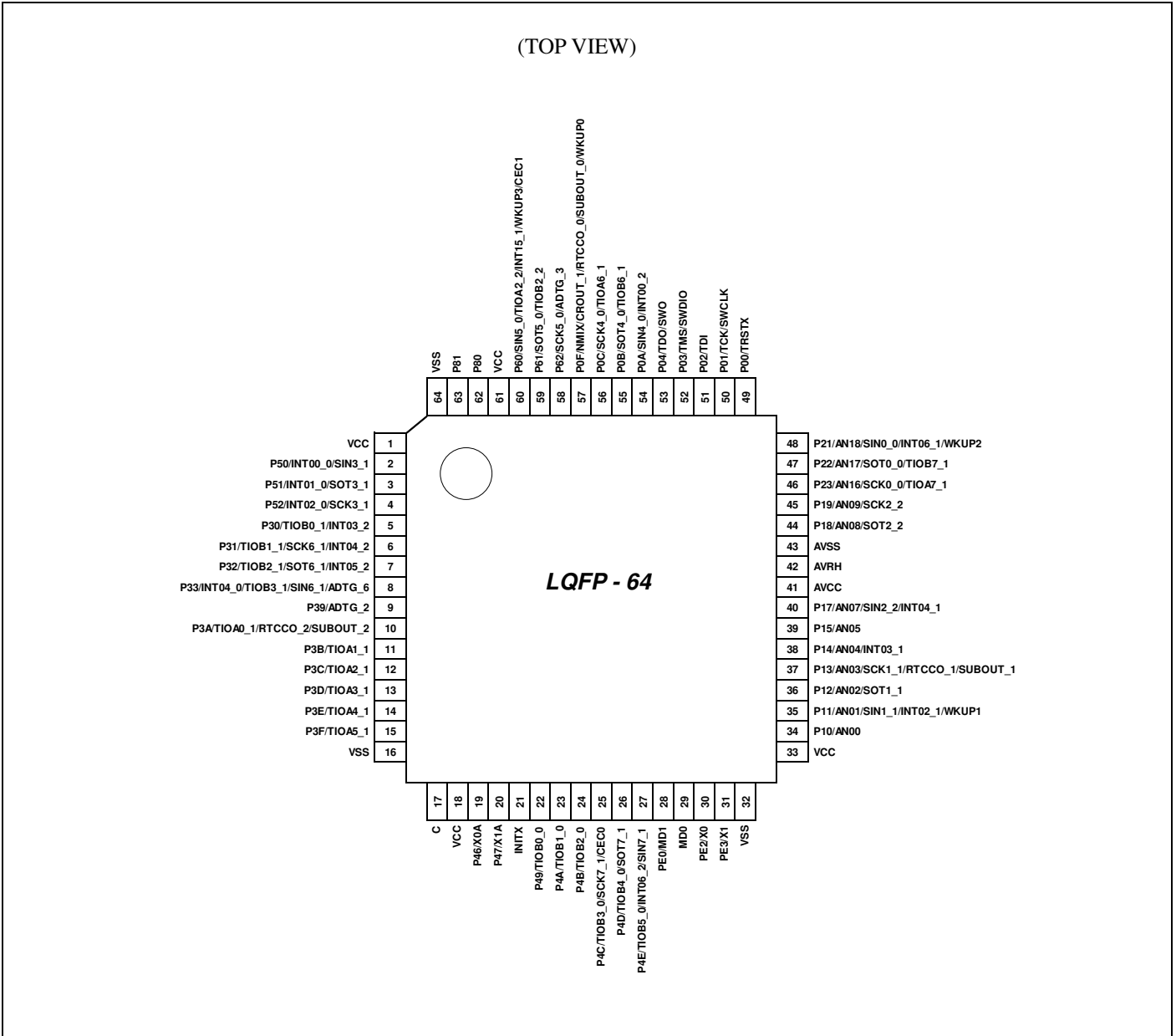
FPT-80P-M37/M40



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

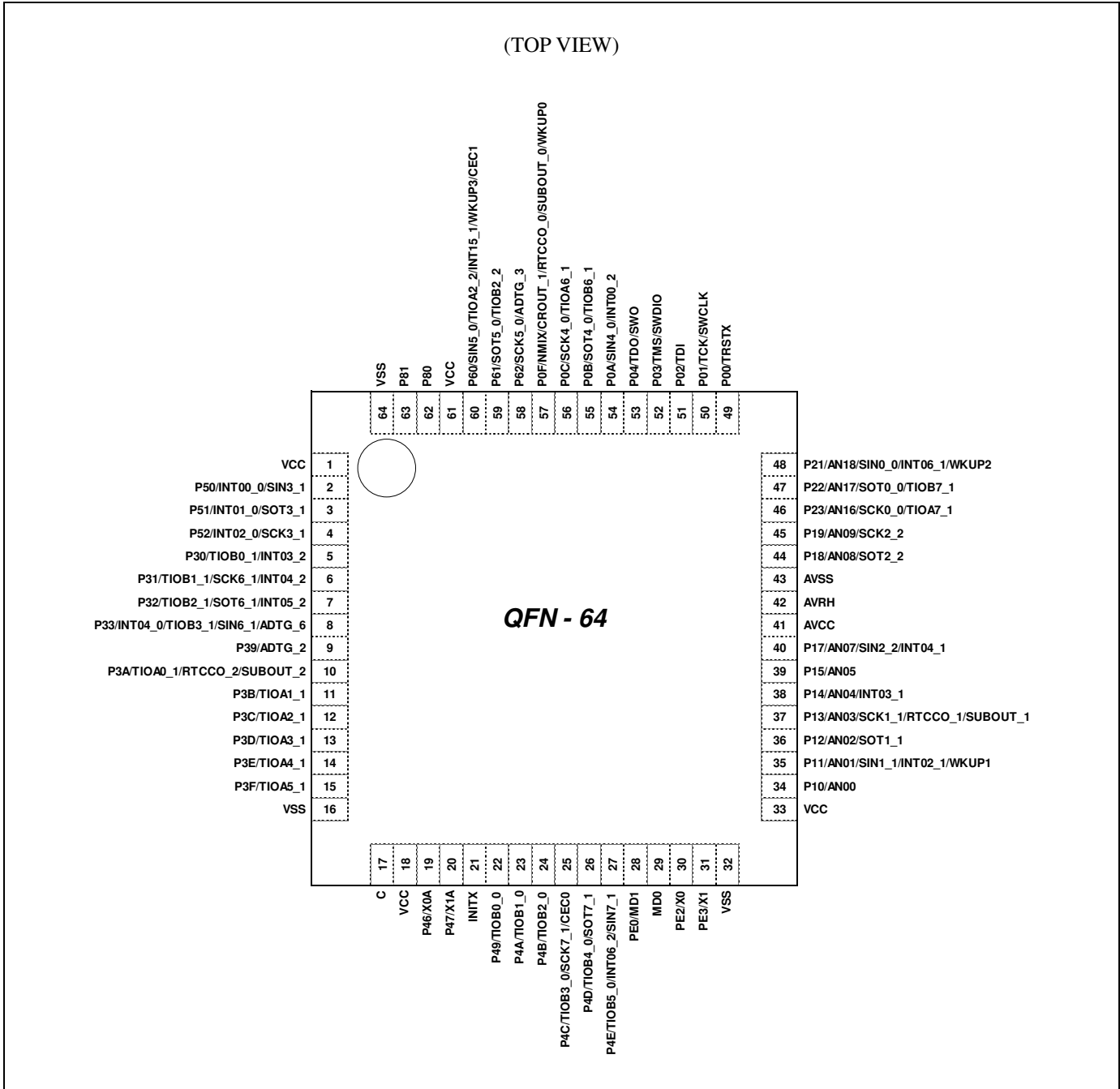
FPT-64P-M38/M39



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LCC-64P- M24

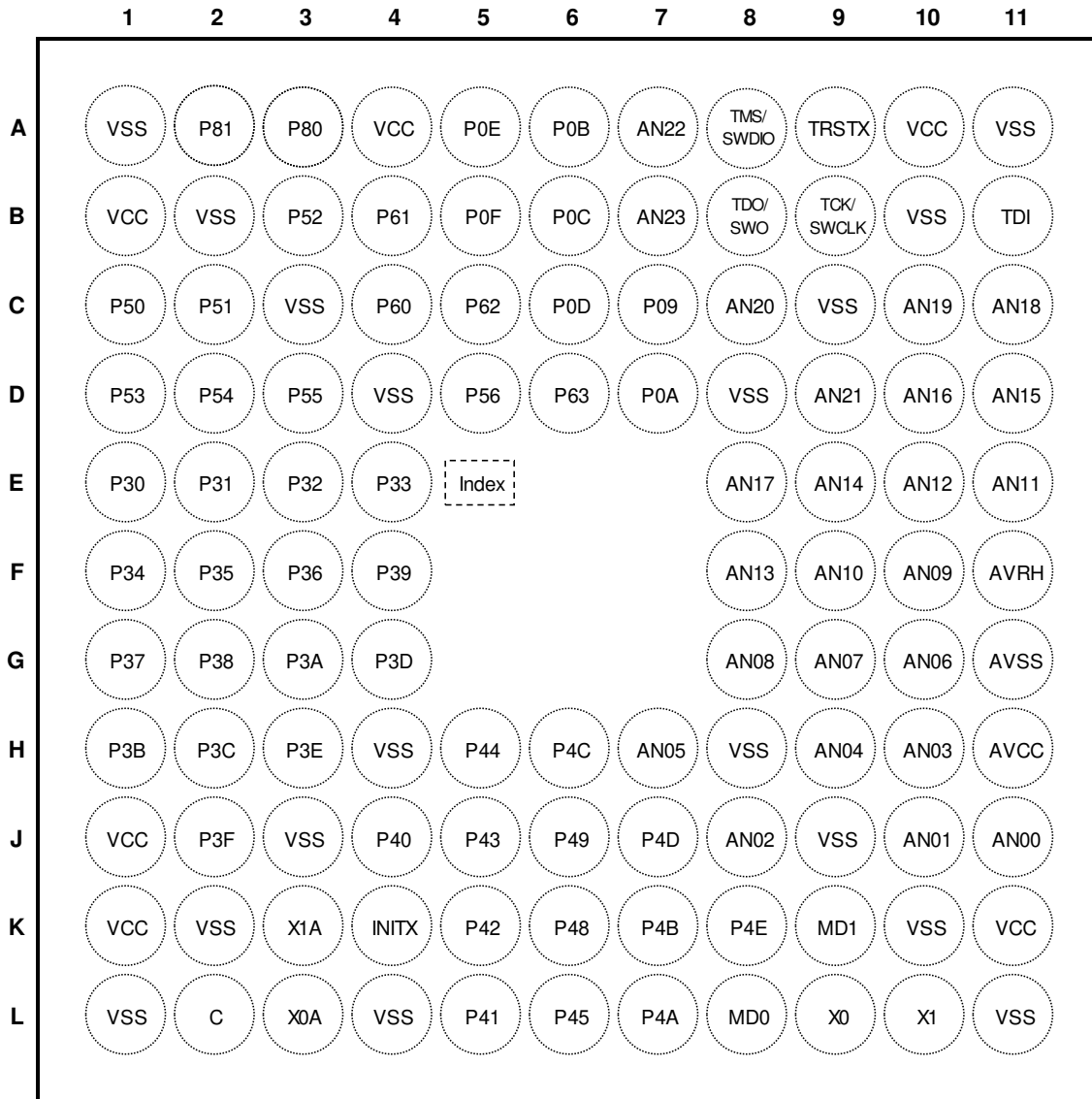


Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

BGA-112P-M04

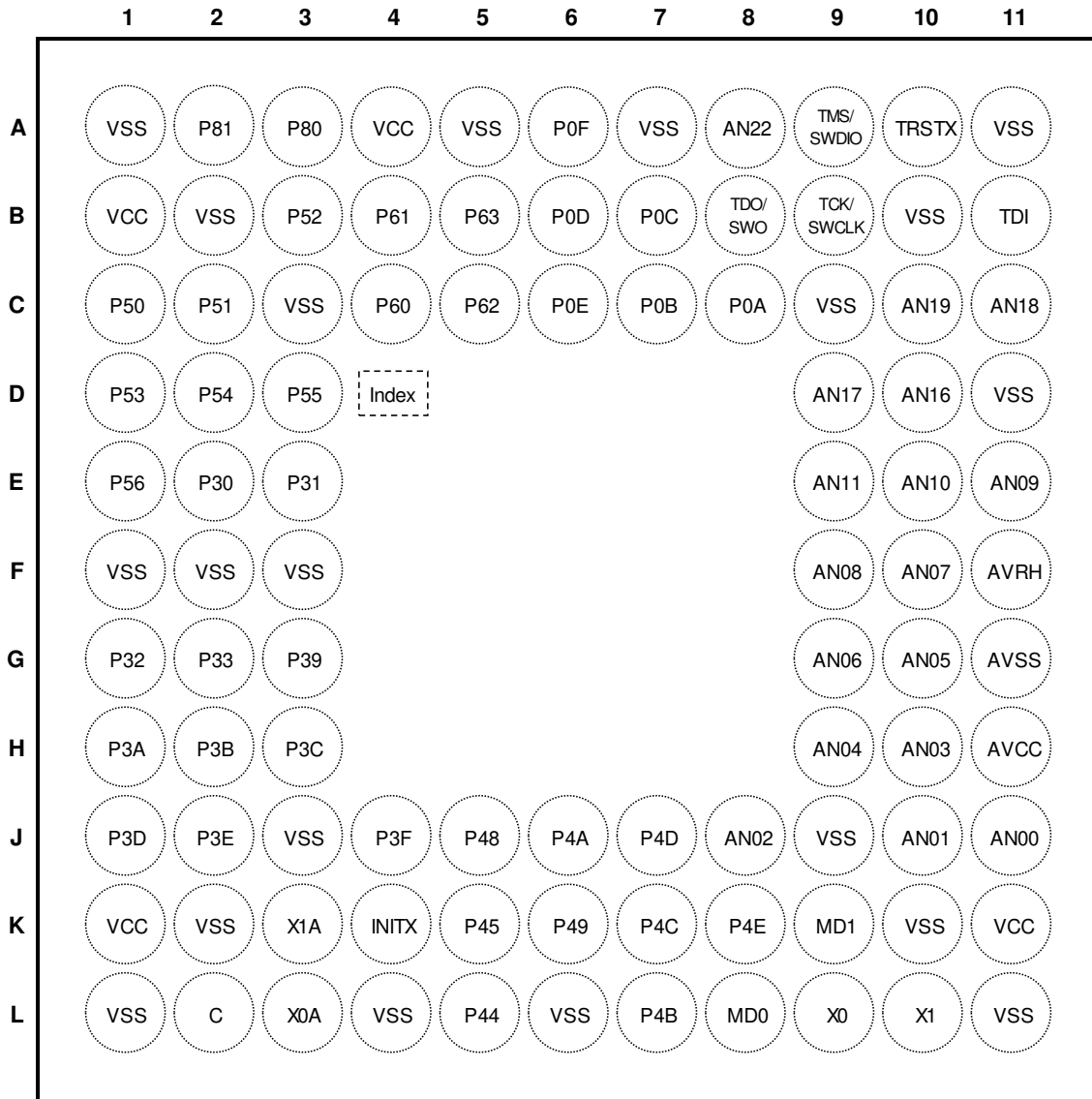
(TOP VIEW)


Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

BGA-96P-M07

(TOP VIEW)



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No						Pin Name	I/O Circuit Type	Pin State Type	
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64				
1	79	B1	1	B1	1	VCC	-		
2	80	C1	2	C1	2	P50	E	L	
						INT00_0			
						SIN3_1			
					-	MADATA00_1			
3	81	C2	3	C2	3	P51	E	L	
						INT01_0			
						SOT3_1 (SDA3_1)			
					-	MADATA01_1			
4	82	B3	4	B3	4	P52	E	L	
						INT02_0			
						SCK3_1 (SCL3_1)			
					-	MADATA02_1			
5	83	D1	5	D1	-	P53	E	L	
									SIN6_0
									TIOA1_2
									INT07_2
						MADATA03_1			
6	84	D2	6	D2	-	P54	E	K	
									SOT6_0 (SDA6_0)
									TIOB1_2
									MADATA04_1
7	85	D3	7	D3	-	P55	E	K	
									SCK6_0 (SCL6_0)
									ADTG_1
									MADATA05_1
8	86	D5	8	E1	-	P56	E	L	
									INT08_2
									MADATA06_1
9	87	E1	9	E2	5	P30	E	L	
						TIOB0_1			
						INT03_2			
						MADATA07_1			
					-				

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
10	88	E2	10	E3	6	P31	E	L
						TIOB1_1		
						SCK6_1 (SCL6_1)		
						INT04_2		
-	-	-	-	-	-	MADATA08_1	-	-
11	89	E3	11	G1	7	P32	E	L
						TIOB2_1		
						SOT6_1 (SDA6_1)		
						INT05_2		
-	-	-	-	-	-	MADATA09_1	-	-
12	90	E4	12	G2	8	P33	E	L
						INT04_0		
						TIOB3_1		
						SIN6_1		
						ADTG_6		
-	-	-	-	-	-	MADATA10_1	-	-
13	91	F1	-	-	-	P34	E	K
						TIOB4_1		
						MADATA11_1		
14	92	F2	-	-	-	P35	E	L
						TIOB5_1		
						INT08_1		
						MADATA12_1		
15	93	F3	-	-	-	P36	E	L
						SIN5_2		
						INT09_1		
						MADATA13_1		
-	-	-	-	F1	-	VSS	-	-
-	-	-	-	F2	-	VSS	-	-
-	-	-	-	F3	-	VSS	-	-
16	94	G1	-	-	-	P37	E	L
						SOT5_2 (SDA5_2)		
						INT10_1		
						MADATA14_1		
17	95	G2	-	-	-	P38	E	L
						SCK5_2 (SCL5_2)		
						INT11_1		
						MADATA15_1		
18	96	F4	13	G3	9	P39	E	K
						ADTG_2		

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
19	97	G3	14	H1	10	P3A	E	K
						TIOA0_1		
						RTCCO_2		
						SUBOUT_2		
20	98	H1	15	H2	11	P3B	E	K
						TIOA1_1		
21	99	H2	16	H3	12	P3C	E	K
						TIOA2_1		
22	100	G4	17	J1	13	P3D	E	K
						TIOA3_1		
-	-	B2	-	B2	-	VSS	-	-
23	1	H3	18	J2	14	P3E	E	K
						TIOA4_1		
24	2	J2	19	J4	15	P3F	E	K
						TIOA5_1		
25	3	L1	20	L1	16	VSS	-	-
26	4	J1	-	-	-	VCC	-	-
27	5	J4	-	-	-	P40	E	L
						TIOA0_0		
						INT12_1		
28	6	L5	-	-	-	P41	E	L
						TIOA1_0		
						INT13_1		
29	7	K5	-	-	-	P42	E	K
						TIOA2_0		
30	8	J5	-	-	-	P43	E	K
						TIOA3_0		
						ADTG_7		
31	9	H5	21	L5	-	P44	E	K
						TIOA4_0		
						MAD00_1		
32	10	L6	22	K5	-	P45	E	K
						TIOA5_0		
						MAD01_1		
-	-	K2	-	K2	-	VSS	-	-
-	-	J3	-	J3	-	VSS	-	-
-	-	H4	-	-	-	VSS	-	-
-	-	-	-	L6	-	VSS	-	-
33	11	L2	23	L2	17	C	-	-
34	12	L4	24	L4	-	VSS	-	-
35	13	K1	25	K1	18	VCC	-	-
36	14	L3	26	L3	19	P46	D	F
						X0A		
37	15	K3	27	K3	20	P47	D	G
						X1A		

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
38	16	K4	28	K4	21	INITX	B	C
39	17	K6	29	J5	-	P48	E	L
						INT14_1		
						SIN3_2		
40	18	J6	30	K6	22	P49	E	K
					-	TIOB0_0		
					-	SOT3_2 (SDA3_2)		
41	19	L7	31	J6	23	P4A	E	K
					-	TIOB1_0		
					-	SCK3_2 (SCL3_2)		
42	20	K7	32	L7	24	P4B	E	K
					-	TIOB2_0		
					-	MAD05_1		
43	21	H6	33	K7	25	P4C	I	S
						TIOB3_0		
						SCK7_1 (SCL7_1)		
						CEC0		
-	MAD06_1							
44	22	J7	34	J7	26	P4D	I	K
						TIOB4_0		
						SOT7_1 (SDA7_1)		
-	MAD07_1							
45	23	K8	35	K8	27	P4E	I	L
						TIOB5_0		
						INT06_2		
						SIN7_1		
-	MAD08_1							
46	24	K9	36	K9	28	MD1	C	E
						PE0		
47	25	L8	37	L8	29	MD0	G	D
48	26	L9	38	L9	30	X0	A	A
						PE2		
49	27	L10	39	L10	31	X1	A	B
						PE3		
50	28	L11	40	L11	32	VSS	-	
51	29	K11	41	K11	33	VCC	-	
52	30	J11	42	J11	34	P10	F	M
						AN00		

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
53	31	J10	43	J10	35	P11	F	R
						AN01		
						SIN1_1		
						INT02_1		
					WKUP1			
-	-	-	-	-	MAD09_1	-	-	
54	32	J8	44	J8	36	P12	F	M
						AN02		
						SOT1_1 (SDA1_1)		
					-	MAD10_1		
-	-	K10	-	K10	-	VSS	-	-
-	-	J9	-	J9	-	VSS	-	-
55	33	H10	45	H10	37	P13	F	M
						AN03		
						SCK1_1 (SCL1_1)		
						RTCCO_1		
					-	SUBOUT_1		
-	-	-	-	-	MAD11_1	-	-	
56	34	H9	46	H9	38	P14	F	N
						AN04		
						INT03_1		
					-	SIN0_1		
-	-	-	-	-	MAD12_1	-	-	
57	35	H7	47	G10	39	P15	F	M
						AN05		
					-	SOT0_1 (SDA0_1)		
-	-	-	-	-	MAD13_1	-	-	
58	36	G10	48	G9	-	P16	F	M
						AN06		
						SCK0_1 (SCL0_1)		
						-		
59	37	G9	49	F10	40	P17	F	N
						AN07		
						SIN2_2		
						INT04_1		
					-	MAD15_1		
60	38	H11	50	H11	41	AVCC	-	-
61	39	F11	51	F11	42	AVRH	-	-
62	40	G11	52	G11	43	AVSS	-	-

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
63	41	G8	53	F9	44	P18	F	M
						AN08		
						SOT2_2 (SDA2_2)		
						MAD16_1		
64	42	F10	54	E11	45	P19	F	M
						AN09		
						SCK2_2 (SCL2_2)		
						MAD17_1		
-	-	H8	-	-	-	VSS	-	-
65	43	F9	55	E10	-	P1A	F	N
						AN10		
						SIN4_1		
						INT05_1		
						MAD18_1		
66	44	E11	56	E9	-	P1B	F	M
						AN11		
						SOT4_1 (SDA4_1)		
						MAD19_1		
67	45	E10	-	-	-	P1C	F	M
						AN12		
						SCK4_1 (SCL4_1)		
						MAD20_1		
68	46	F8	-	-	-	P1D	F	M
						AN13		
						CTS4_1		
						MAD21_1		
69	47	E9	-	-	-	P1E	F	M
						AN14		
						RTS4_1		
						MAD22_1		
70	48	D11	-	-	-	P1F	F	M
						AN15		
						ADTG_5		
						MAD23_1		
-	-	B10	-	B10	-	VSS	-	-
-	-	C9	-	C9	-	VSS	-	-
-	-	-	-	D11	-	VSS	-	-

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
71	49	D10	57	D10	46	P23	F	M
						AN16		
						SCK0_0 (SCL0_0)		
						TIOA7_1		
72	50	E8	58	D9	47	P22	F	M
						AN17		
						SOT0_0 (SDA0_0)		
						TIOB7_1		
73	51	C11	59	C11	48	P21	F	R
						AN18		
						SIN0_0		
						INT06_1		
						WKUP2		
74	52	C10	60	C10	-	P20	F	N
						AN19		
						INT05_0		
						CROUT_0		
						MAD24_1		
75	53	A11	-	A11	-	VSS	-	
76	54	A10	-	-	-	VCC	-	
77	55	A9	61	A10	49	P00	E	J
					-	TRSTX		
78	56	B9	62	B9	50	MCSX7_1	E	J
						P01		
						TCK		
79	57	B11	63	B11	51	P02	E	J
					-	TDI		
					-	MCSX6_1		
80	58	A8	64	A9	52	P03	E	J
						TMS		
						SWDIO		
81	59	B8	65	B8	53	P04	E	J
						TDO		
						SWO		
82	60	C8	-	-	-	P05	F	Q
						AN20		
						TRACED0		
						TIOA5_2		
						SIN4_2		
						INT00_1		
MCSX5_1								

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
-	-	D8	-	-	-	VSS	-	
83	61	D9	-	-	-	P06	F	Q
						AN21		
						TRACED1		
						TIOB5_2		
						SOT4_2 (SDA4_2)		
						INT01_1		
MCSX4_1								
84	62	A7	66	A8	-	P07	F	P
			-	-		AN22		
						ADTG_0		
						MCLKOUT_1		
						TRACED2		
SCK4_2 (SCL4_2)								
-	-	-	-	A7	-	VSS	-	
85	63	B7	-	-	-	P08	F	P
						AN23		
						TRACED3		
						TIOA0_2		
						CTS4_2		
MCSX3_1								
86	64	C7	-	-	-	P09	E	O
						TRACECLK		
						TIOB0_2		
						RTS4_2		
MCSX2_1								
87	65	D7	67	C8	54	P0A	I	L
					SIN4_0			
					INT00_2			
-	-	-	-	-	-	MCSX1_1	-	
88	66	A6	68	C7	55	P0B	I	K
					SOT4_0 (SDA4_0)			
					TIOB6_1			
-	-	-	-	-	-	MCSX0_1	-	
89	67	B6	69	B7	56	P0C	I	K
					SCK4_0 (SCL4_0)			
					TIOA6_1			
-	-	-	-	-	-	MALE_1	-	
-	-	D4	-	-	-	VSS	-	

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
-	-	C3	-	C3	-	VSS	-	
90	68	C6	70	B6	-	P0D	E	K
						RTS4_0		
						TIOA3_2		
						MDQM0_1		
91	69	A5	71	C6	-	P0E	E	K
						CTS4_0		
						TIOB3_2		
						MDQM1_1		
-	-	-	-	A5	-	VSS	-	
92	70	B5	72	A6	57	P0F	E	I
						NMIX		
						CROUT_1		
						RTCCO_0		
						SUBOUT_0		
						WKUP0		
93	71	D6	73	B5	-	P63	E	L
						INT03_0		
						MWEX_1		
94	72	C5	74	C5	58	P62	E	K
						SCK5_0 (SCL5_0)		
					ADTG_3			
					-	MOEX_1		
95	73	B4	75	B4	59	P61	E	K
						SOT5_0 (SDA5_0)		
						TIOB2_2		
96	74	C4	76	C4	60	P60	I	T
						SIN5_0		
						TIOA2_2		
						INT15_1		
						WKUP3		
					CEC1			
					-	MRDY_1		
97	75	A4	77	A4	61	VCC	-	
98	76	A3	78	A3	62	P80	H	H
99	77	A2	79	A2	63	P81	H	H
100	78	A1	80	A1	64	VSS	-	

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Function	Pin Name	Function Description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
ADC	ADTG_0	A/D converter external trigger input pin	84	62	A7	66	A8	-
	ADTG_1		7	85	D3	7	D3	-
	ADTG_2		18	96	F4	13	G3	9
	ADTG_3		94	72	C5	74	C5	58
	ADTG_4		-	-	-	-	-	-
	ADTG_5		70	48	D11	-	-	-
	ADTG_6		12	90	E4	12	G2	8
	ADTG_7		30	8	J5	-	-	-
	ADTG_8		-	-	-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	30	J11	42	J11	34
	AN01		53	31	J10	43	J10	35
	AN02		54	32	J8	44	J8	36
	AN03		55	33	H10	45	H10	37
	AN04		56	34	H9	46	H9	38
	AN05		57	35	H7	47	G10	39
	AN06		58	36	G10	48	G9	-
	AN07		59	37	G9	49	F10	40
	AN08		63	41	G8	53	F9	44
	AN09		64	42	F10	54	E11	45
	AN10		65	43	F9	55	E10	-
	AN11		66	44	E11	56	E9	-
	AN12		67	45	E10	-	-	-
	AN13		68	46	F8	-	-	-
	AN14		69	47	E9	-	-	-
	AN15		70	48	D11	-	-	-
	AN16		71	49	D10	57	D10	46
	AN17		72	50	E8	58	D9	47
	AN18		73	51	C11	59	C11	48
	AN19		74	52	C10	60	C10	-
	AN20		82	60	C8	-	-	-
	AN21		83	61	D9	-	-	-
	AN22		84	62	A7	66	A8	-
	AN23	85	63	B7	-	-	-	