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The MB9A420L Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM® Cortex®-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, DACs and Communication Interfaces (CAN, UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE11 product categories in FM3 Family Peripheral Manual.

Features

32-bit ARM® Cortex®-M3 Core

- Processor version: r2p1
- Up to 40 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and
- 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- 64 Kbytes
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This series contains 4 Kbyte on-chip SRAM memories that is connected to System bus of Cortex-M3 core.

- SRAM1: 4 Kbyte

CAN Interface (Max one channel)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Multi-function Serial Interface (Max four channels)

- 4 channels without FIFO (ch.0, ch.1, ch.3, ch.5)
- Operation mode is selectable from the followings for each channel.
 - UART
 - CSIO
 - LIN
 - I²C

[UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can be changed to 13-bit to 16-bit length)
- LIN break delimiter generation (can be changed to 1-bit to 4-bit length)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

A/D Converter (Max eight channels)

[12-bit A/D Converter]

- Successive Approximation type
 - Conversion time: 0.8 μ s @ 5 V
 - Priority conversion available (priority at 2 levels)
 - Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

D/A Converter (Max one channel)

- R-2R type
- 10-bit resolution

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built-in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
 - Capable of reading pin level directly
 - Built-in the port relocate function
 - Up to 51 high-speed general-purpose I/O Ports@64 pin Package
 - Some ports are 5V tolerant
- See List of Pin Functions and I/O Circuit Type to confirm the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch.
 - Input capture × 3 ch.
 - Output compare × 6 ch.
 - A/D activation compare × 1 ch.
 - Waveform generator × 3 ch.
 - 16-bit PPG timer × 3 ch.
- IGBT mode is contained

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

External Interrupt Controller Unit

- Up to 19 external interrupt input pins @ 64 pin Package
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption modes except RTC, Stop modes.

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in high-speed CR Clock: 4 MHz
- Built-in low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Four low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop

Debug

Serial Wire JTAG Debug Port (SWJ-DP)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

Wide range voltage: VCC = 2.7 V to 5.5 V

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1. Product Lineup

Memory size

Product name		MB9AF421K/L
On-chip Flash memory		64 Kbytes
On-chip SRAM	SRAM1	4 Kbytes

Function

Product name		MB9AF421K	MB9AF421L	
Pin count		48/52	64	
CPU		Cortex-M3	40 MHz	
	Freq.	40 MHz		
Power supply voltage range		2.7 V to 5.5 V		
CAN		1 ch. (Max)		
Multi-function Serial Interface (UART/CSIO/LIN/I ² C)		4 ch. (Max) ch.0, ch.1, ch.3, ch.5: No FIFO (In ch.5, only UART and LIN are available.)	4ch. (Max) ch.0, ch.1, ch.3, ch.5: No FIFO	
Base Timer (PWC/Reload timer/PWM/PPG)		8 ch. (Max)		
MF-Timer	A/D activation compare	1 ch.	1 unit	
	Input capture	3 ch.		
	Free-run timer	3 ch.		
	Output compare	6 ch.		
	Waveform generator	3 ch.		
	PPG (IGBT mode)	3 ch.		
Dual Timer		1 unit		
Real-Time Clock		1 unit		
Watchdog timer		1 ch. (SW) + 1 ch. (HW)		
External Interrupts		14 pins (Max) + NMI × 1	19 pins (Max) + NMI × 1	
I/O ports		36 pins (Max)	51 pins (Max)	
12-bit A/D converter		8 ch. (1 unit)		
10-bit D/A converter		1 ch. (Max)		
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2 ch.		
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug Function		SWJ-DP		
Unique ID		Yes		

Note:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the I/O port according to your function use.
See Electrical Characteristics 4.AC Characteristics (3) Built-in CR Oscillation Characteristics for accuracy of built-in CR.

2. Packages

Package	Product name	MB9AF421K	MB9AF421L
LQFP:	LQA048 (0.5 mm pitch)	○	-
QFN:	WNY048 (0.5 mm pitch)	○	-
LQFP:	LQC052 (0.65 mm pitch)	○	-
LQFP:	LQD064 (0.5 mm pitch)	-	○
LQFP:	LQG064 (0.65 mm pitch)	-	○
QFN:	WNS064 (0.5 mm pitch)	-	○

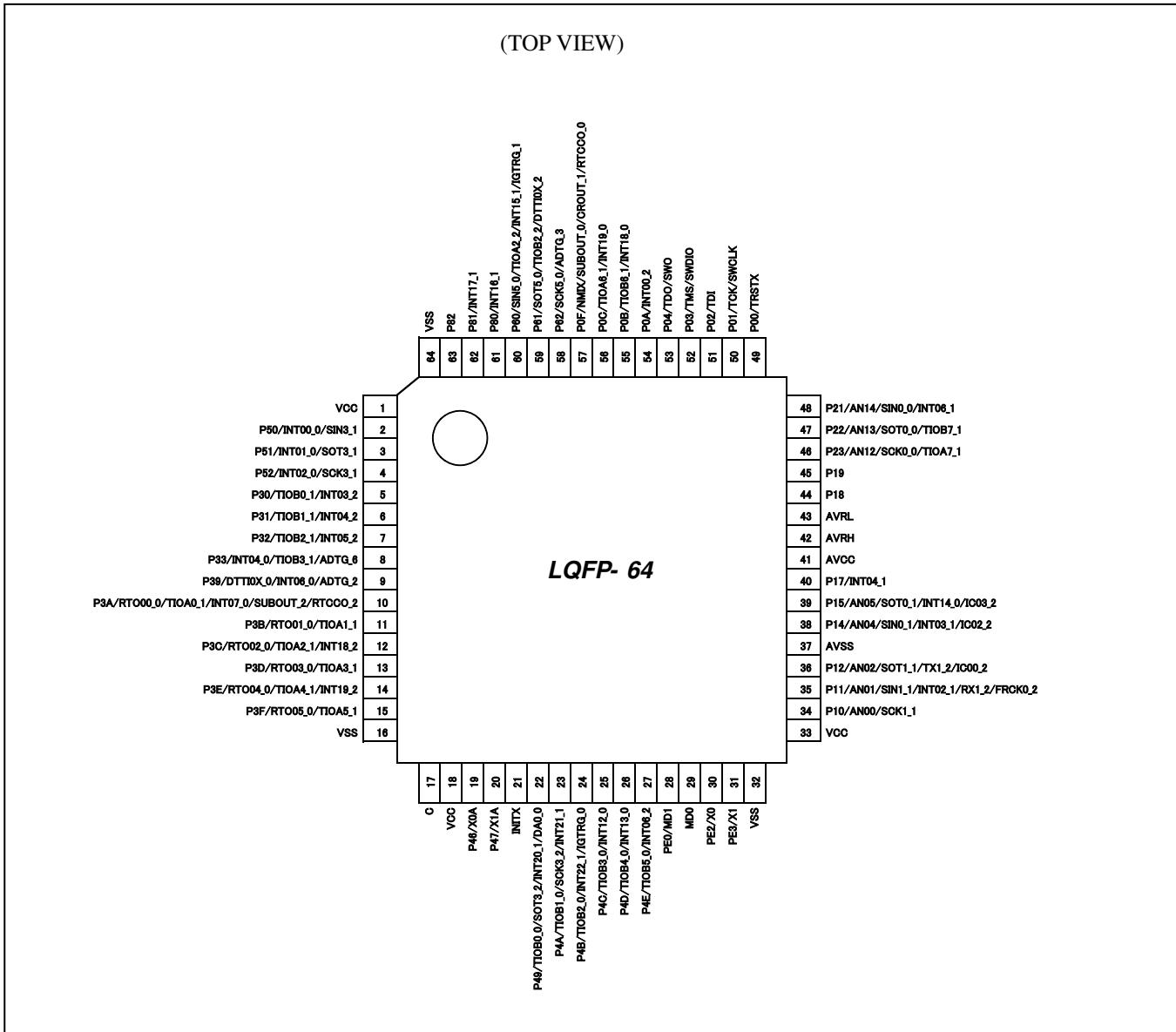
○: Supported

Note:

- See Package Dimensions for detailed information on each package.

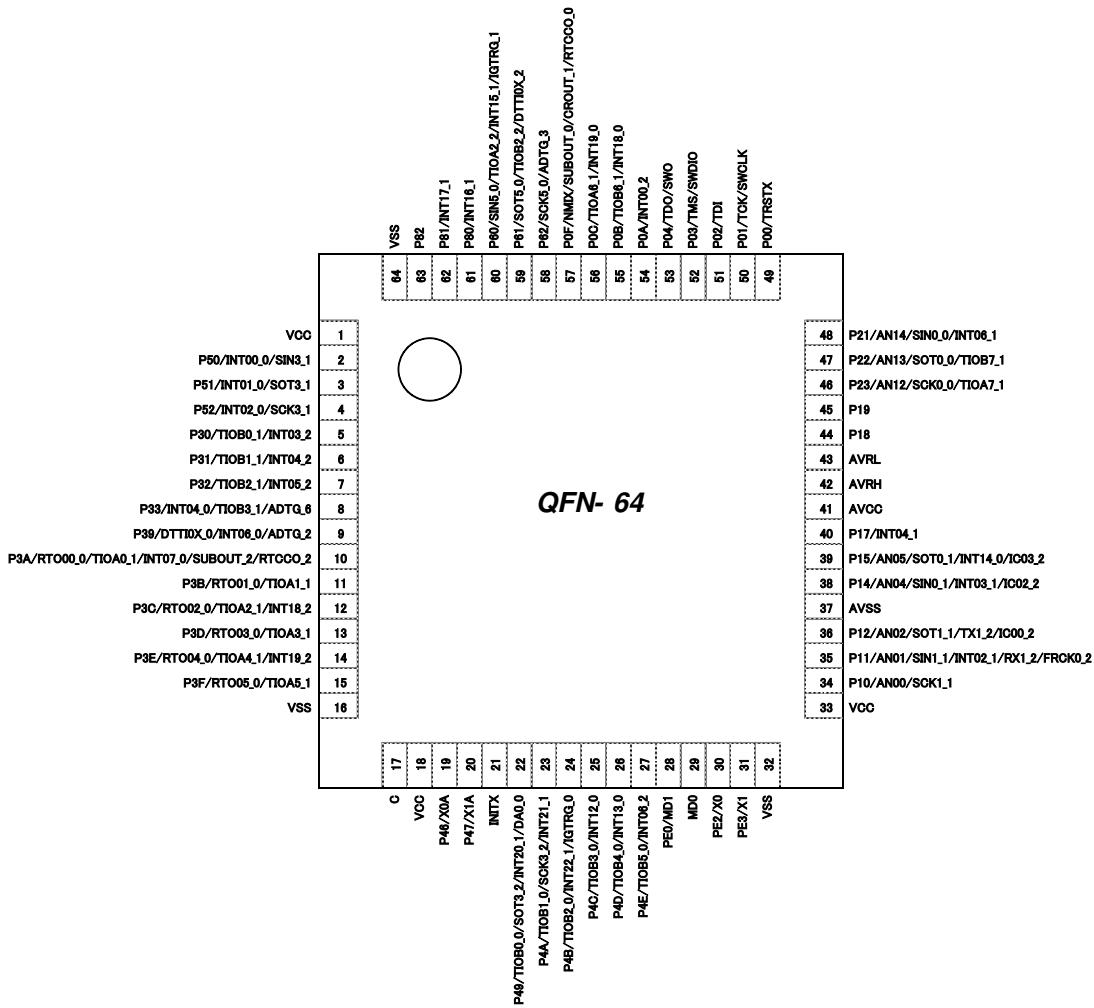
3. Pin Assignment

LQD064/ LQG064

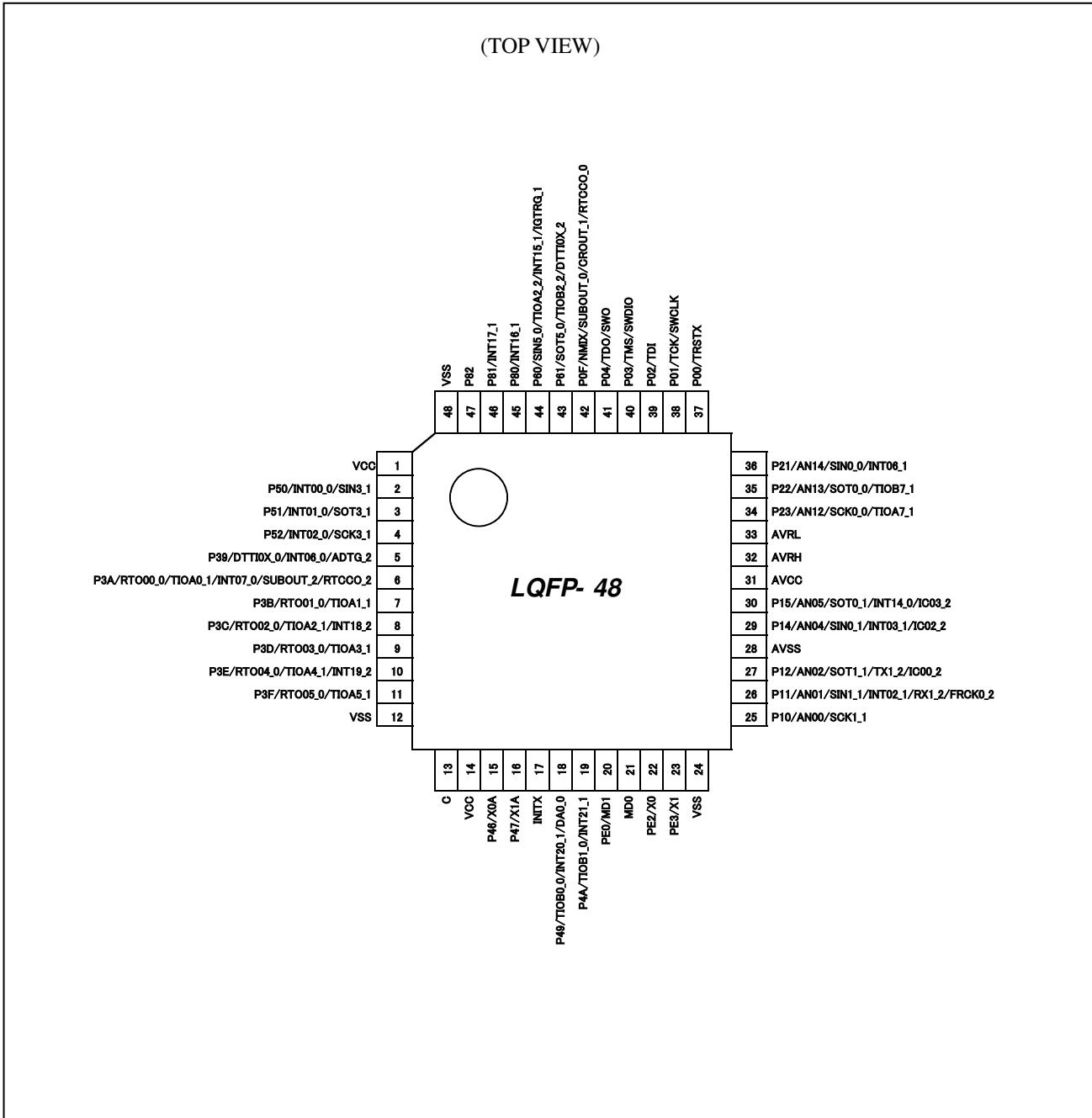


WNS064

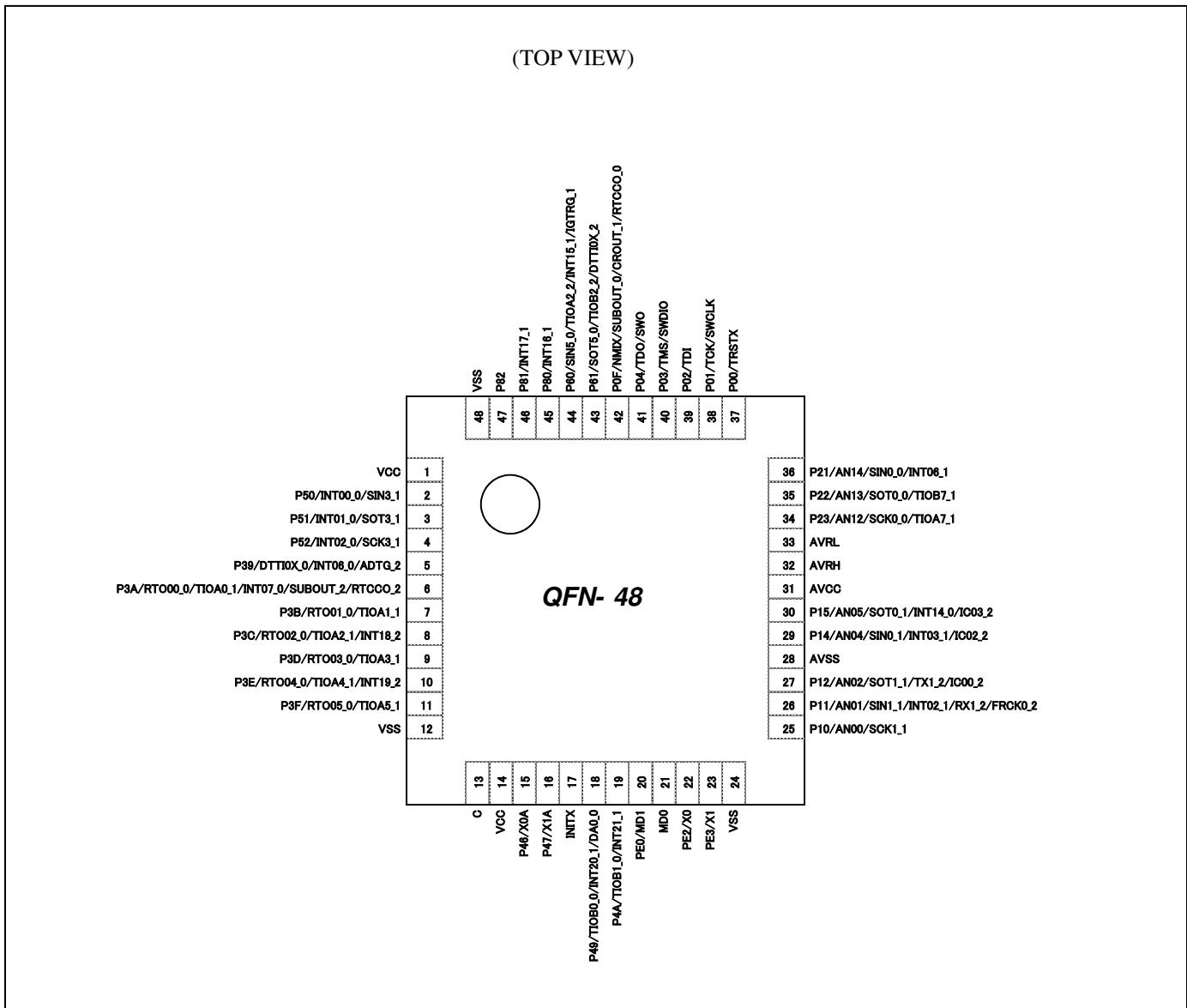
(TOP VIEW)


Note:

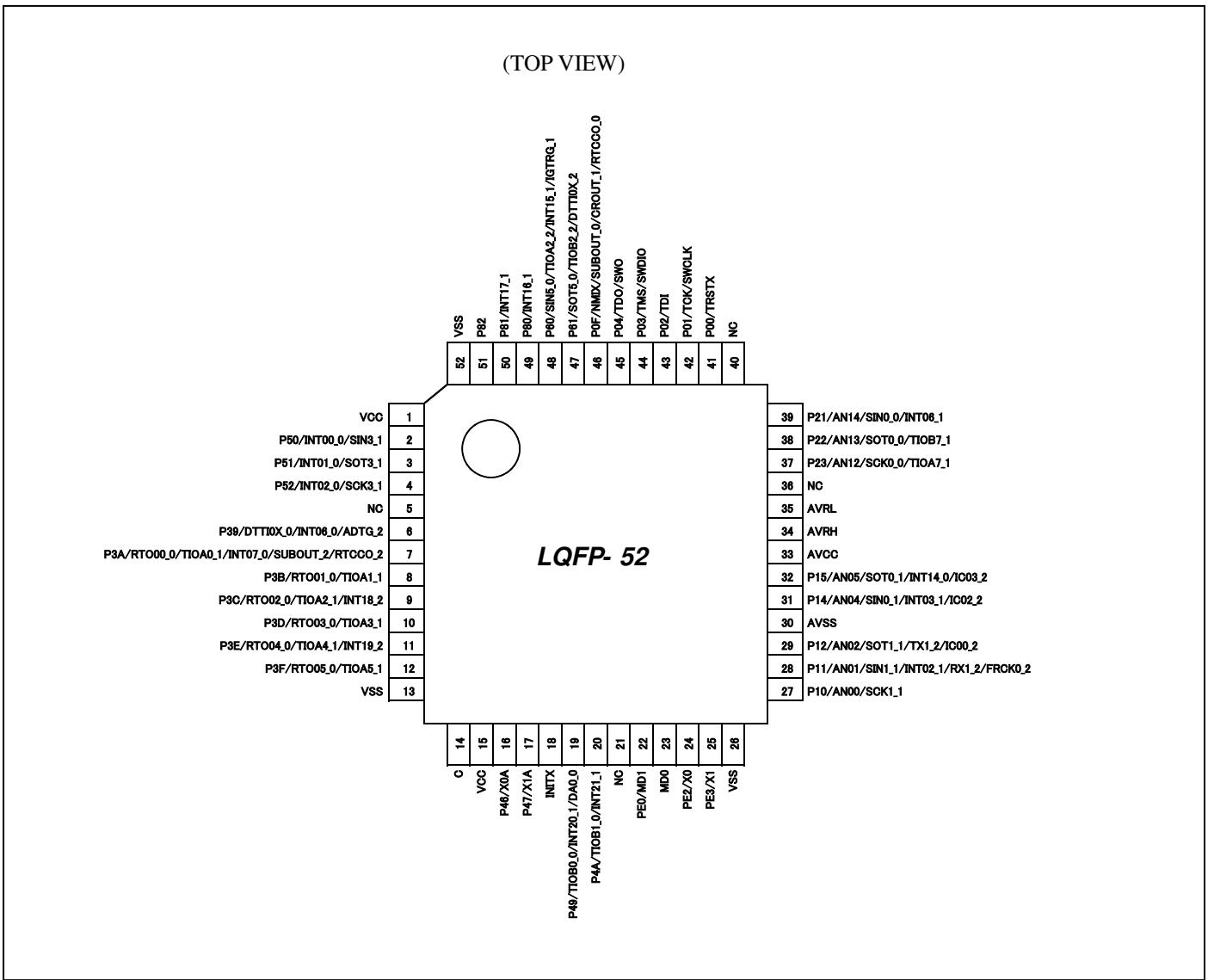
- The number after the underscore ("_) in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LQA048

Note:

- The number after the underscore ("_) in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

WNY048

Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LQC052

Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48			
1	1	1	VCC	H* ¹	K
2	2	2	P50		
			INT00_0		
			SIN3_1		
			P51	H* ²	K
3	3	3	INT01_0		
			SOT3_1 (SDA3_1)		
			P52	H* ²	K
			INT02_0		
4	4	4	SCK3_1 (SCL3_1)		
			P30	E	K
			TIOB0_1		
			INT03_2		
5	-	-	P31	E	K
			TIOB1_1		
			INT04_2		
			P32	E	K
6	-	-	TIOB2_1		
			INT05_2		
			P33	E	K
			INT04_0		
7	-	-	TIOB3_1		
			ADTG_6		
			P39	E	K
			DTTI0X_0		
8	6	5	INT06_0		
			ADTG_2		
			P3A	G	K
			RTO00_0 (PPG00_0)		
10	7	6	TIOA0_1		
			INT07_0		
			SUBOUT_2		
			RTCCO_2		
			P3B	G	J
			RTO01_0 (PPG00_0)		
			TIOA1_1		

Pin No			Pin Name	I/O circuit type	Pin state type	
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48				
12	9	8	P3C	G	K	
			RTO02_0 (PPG02_0)			
			TIOA2_1			
			INT18_2			
13	10	9	P3D	G	J	
			RTO03_0 (PPG02_0)			
			TIOA3_1			
14	11	10	P3E	G	K	
			RTO04_0 (PPG04_0)			
			TIOA4_1			
			INT19_2			
15	12	11	P3F	G	J	
			RTO05_0 (PPG04_0)			
			TIOA5_1			
16	13	12	VSS	-		
17	14	13	C	-		
18	15	14	VCC	-		
19	16	15	P46	D	F	
			X0A			
20	17	16	P47	D	G	
			X1A			
21	18	17	INITX	B	C	
22	19	18	P49	K	K	
			TIOB0_0			
			INT20_1			
			DA0_0			
	-	-	SOT3_2 (SDA3_2)			
23	20	19	P4A	E	K	
			TIOB1_0			
			INT21_1			
	-	-	SCK3_2 (SCL3_2)			
24	-	-	P4B	E	K	
			TIOB2_0			
			INT22_1			
			IGTRG_0			
25	-	-	P4C	E	K	
			TIOB3_0			
			INT12_0			
26	-	-	P4D	E	K	
			TIOB4_0			
			INT13_0			

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48			
27	-	-	P4E	E	K
			TIOB5_0		
			INT06_2		
28	22	20	PE0	C	E
			MD1		
29	23	21	MD0	J	D
30	24	22	PE2	A	A
			X0		
31	25	23	PE3	A	B
			X1		
32	26	24	VSS	-	
33	-	-	VCC	-	
34	27	25	P10	F	L
			AN00		
			SCK1_1 (SCL1_1)		
35	28	26	P11	F	M
			AN01		
			SIN1_1		
			INT02_1		
			RX1_2		
			FRCK0_2		
36	29	27	P12	F	L
			AN02		
			SOT1_1 (SDA1_1)		
			TX1_2		
			IC00_2		
37	30	28	AVSS	-	
38	31	29	P14	F	M
			AN04		
			SIN0_1		
			INT03_1		
			IC02_2		
39	32	30	P15	F	M
			AN05		
			SOT0_1 (SDA0_1)		
			INT14_0		
			IC03_2		
40	-	-	P17	E	K
41	33	31	AVCC	-	
42	34	32	AVRH	-	
43	35	33	AVRL	-	
44	-	-	P18	E	J
45	-	-	P19	E	J

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48			
46	37	34	P23	I ^{*2}	M
			AN12		
			SCK0_0 (SCL0_0)		
			TIOA7_1		
47	38	35	P22	I ^{*2}	M
			AN13		
			SOT0_0 (SDA0_0)		
			TIOB7_1		
48	39	36	P21	I ^{*1}	M
			AN14		
			SIN0_0		
			INT06_1		
49	41	37	P00	E	I
			TRSTX		
50	42	38	P01	E	I
			TCK		
			SWCLK		
51	43	39	P02	E	I
			TDI		
52	44	40	P03	E	I
			TMS		
			SWDIO		
53	45	41	P04	E	I
			TDO		
			SWO		
54	-	-	P0A	E	K
			INT00_2		
55	-	-	P0B	E	K
			TIOB6_1		
			INT18_0		
56	-	-	P0C	E	K
			TIOA6_1		
			INT19_0		
57	46	42	P0F	E	H
			NMIX		
			SUBOUT_0		
			CROUT_1		
			RTCCO_0		
58	-	-	P62	E	J
			SCK5_0 (SCL5_0)		
			ADTG_3		

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48			
59	47	43	P61	E	J
			SOT5_0 (SDA5_0)		
			TIOB2_2		
			DTTI0X_2		
60	48	44	P60	I ^{*2}	K
			SIN5_0		
			TIOA2_2		
			INT15_1		
			IGTRG_1		
61	49	45	P80	L	K
			INT16_1		
62	50	46	P81	L	K
			INT17_1		
63	51	47	P82	L	J
64	52	48	VSS	-	
-	5, 21, 36, 40	-	NC	-	

*1: 5 V tolerant I/O, without PZR function

*2: 5 V tolerant I/O, with PZR function

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
ADC	ADTG_2	A/D converter external trigger input pin	9	6	5
	ADTG_3		58	-	-
	ADTG_6		8	-	-
ANxx	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	34	27	25
	AN01		35	28	26
	AN02		36	29	27
	AN04		38	31	29
	AN05		39	32	30
	AN12		46	37	34
	AN13		47	38	35
	AN14		48	39	36
	TIOA0_1	Base timer ch.0 TIOA pin	10	7	6
	TIOB0_0		22	19	18
	TIOB0_1		5	-	-
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	11	8	7
	TIOB1_0		23	20	19
	TIOB1_1		6	-	-
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	12	9	8
	TIOA2_2		60	48	44
	TIOB2_0	Base timer ch.2 TIOB pin	24	-	-
	TIOB2_1		7	-	-
	TIOB2_2		59	47	43
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	13	10	9
	TIOB3_0		25	-	-
	TIOB3_1		8	-	-
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	14	11	10
	TIOB4_0		26	-	-
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	15	12	11
	TIOB5_0		27	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	56	-	-
	TIOB6_1		55	-	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	46	37	34
	TIOB7_1		47	38	35
Debugger	SWCLK	Serial wire debug interface clock input pin	50	42	38
	SWDIO	Serial wire debug interface data input / output pin	52	44	40
	SWO	Serial wire viewer output pin	53	45	41
	TCK	JTAG test clock input pin	50	42	38
	TDI	JTAG test data input pin	51	43	39
	TDO	JTAG debug data output pin	53	45	41
	TMS	JTAG test mode state input/output pin	52	44	40
	TRSTX	JTAG test reset input pin	49	41	37

Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2
	INT00_2		54	-	-
	INT01_0	External interrupt request 01 input pin	3	3	3
	INT02_0	External interrupt request 02 input pin	4	4	4
	INT02_1		35	28	26
	INT03_1	External interrupt request 03 input pin	38	31	29
	INT03_2		5	-	-
	INT04_0	External interrupt request 04 input pin	8	-	-
	INT04_1		40	-	-
	INT04_2		6	-	-
	INT05_2	External interrupt request 05 input pin	7	-	-
	INT06_0	External interrupt request 06 input pin	9	6	5
	INT06_1		48	39	36
	INT06_2		27	-	-
	INT07_0	External interrupt request 07 input pin	10	7	6
	INT12_0	External interrupt request 12 input pin	25	-	-
	INT13_0	External interrupt request 13 input pin	26	-	-
	INT14_0	External interrupt request 14 input pin	39	32	30
	INT15_1	External interrupt request 15 input pin	60	48	44
	INT16_1	External interrupt request 16 input pin	61	49	45
	INT17_1	External interrupt request 17 input pin	62	50	46
	INT18_0	External interrupt request 18 input pin	55	-	-
	INT18_2		12	9	8
	INT19_0	External interrupt request 19 input pin	56	-	-
	INT19_2		14	11	10
	INT20_1	External interrupt request 20 input pin	22	19	18
	INT21_1	External interrupt request 21 input pin	23	20	19
	INT22_1	External interrupt request 22 input pin	24	-	-
	NMIX	Non-Maskable Interrupt input pin	57	46	42

Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
GPIO	P00	General-purpose I/O port 0	49	41	37
	P01		50	42	38
	P02		51	43	39
	P03		52	44	40
	P04		53	45	41
	P0A		54	-	-
	P0B		55	-	-
	P0C		56	-	-
	P0F		57	46	42
	P10		34	27	25
	P11		35	28	26
	P12		36	29	27
	P14		38	31	29
	P15		39	32	30
GPIO	P17	General-purpose I/O port 1	40	-	-
	P18		44	-	-
	P19		45	-	-
	P21		48	39	36
	P22		47	38	35
	P23		46	37	34
	P30	General-purpose I/O port 3	5	-	-
	P31		6	-	-
	P32		7	-	-
	P33		8	-	-
	P39		9	6	5
	P3A		10	7	6
	P3B		11	8	7
	P3C		12	9	8
	P3D		13	10	9
	P3E		14	11	10
	P3F		15	12	11
	P46	General-purpose I/O port 4	19	16	15
	P47		20	17	16
	P49		22	19	18
	P4A		23	20	19
	P4B		24	-	-
	P4C		25	-	-
	P4D		26	-	-
	P4E		27	-	-
GPIO	P50	General-purpose I/O port 5	2	2	2
	P51		3	3	3
	P52		4	4	4
	P60		60	48	44
	P61	General-purpose I/O port 6	59	47	43
	P62		58	-	-
	P80		61	49	45
GPIO	P81	General-purpose I/O port 8	62	50	46
	P82		63	51	47
	PE0		28	22	20
	PE2	General-purpose I/O port E	30	24	22
	PE3		31	25	23

Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	48	39	36
	SIN0_1		38	31	29
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I ² C (operation mode 4).	47	38	35
	SOT0_1 (SDA0_1)		39	32	30
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I ² C (operation mode 4).	46	37	34
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	35	28	26
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I ² C (operation mode 4).	36	29	27
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I ² C (operation mode 4).	34	27	25
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	2	2
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I ² C (operation mode 4).	3	3	3
	SOT3_2 (SDA3_2)		22	-	-
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation mode 2) and as SCL3 when it is used in an I ² C (operation mode 4).	4	4	4
	SCK3_2 (SCL3_2)		23	-	-

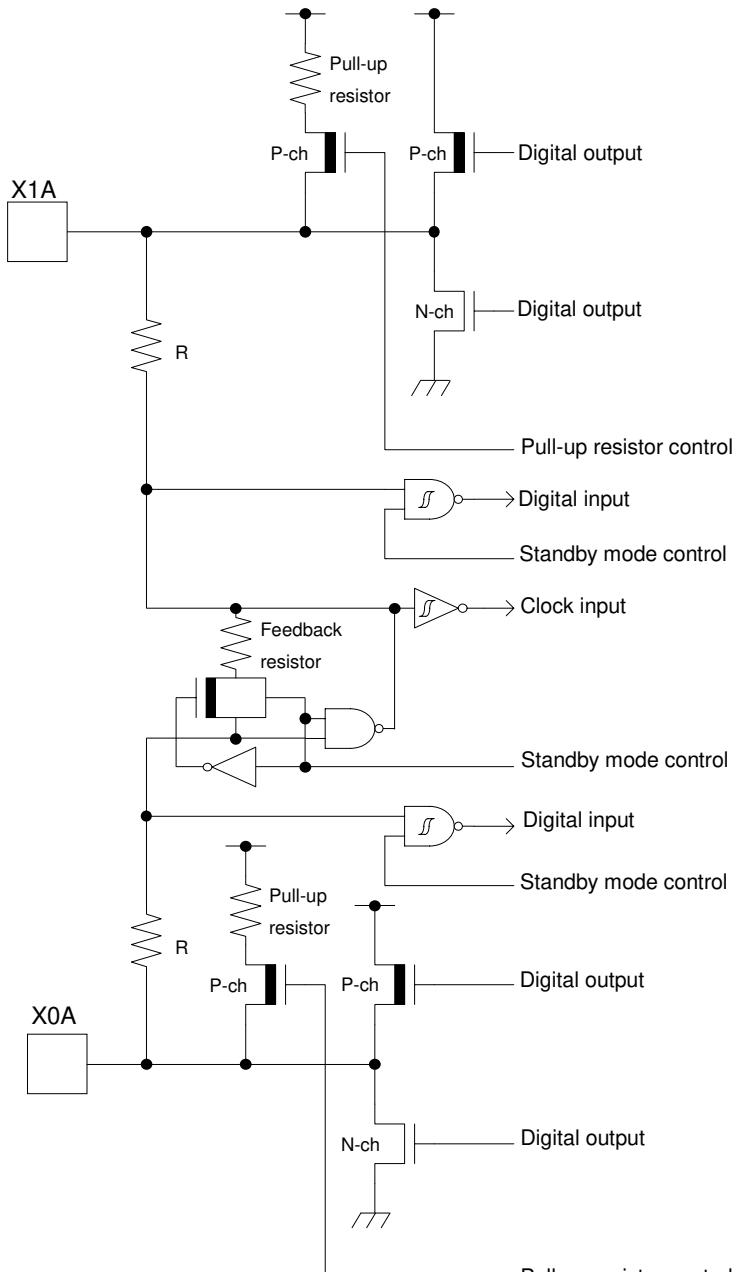
Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	60	48	44
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I ² C (operation mode 4).	59	47	43
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I ² C (operation mode 4).	58	-	-
Multi-function Timer 0	DTT10X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0.	9	6	5
	DTT10X_2		59	47	43
	FRCK0_2	16-bit free-run timer ch.0 external clock input pin	35	28	26
	IC00_2	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	36	29	27
	IC02_2		38	31	29
	IC03_2		39	32	30
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	10	7	6
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	11	8	7
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	12	9	8
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	13	10	9
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	14	11	10
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	15	12	11
	IGTRG_0	PPG IGBT mode external trigger input pin	24	-	-
	IGTRG_1		60	48	44

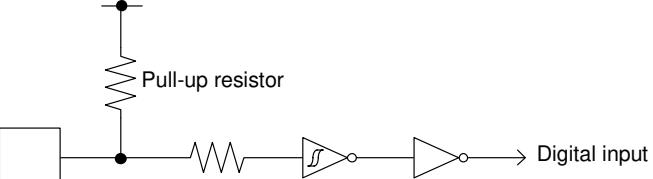
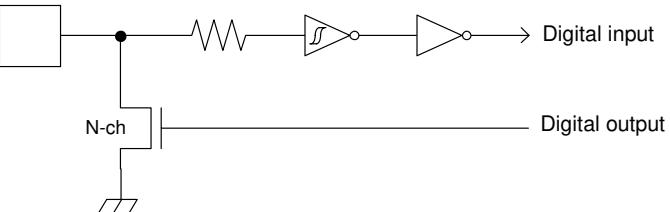
Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
CAN	TX1_2	CAN interface TX output pin	36	29	27
	RX1_2	CAN interface RX input pin	35	28	26
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	57	46	42
	RTCCO_2		10	7	6
	SUBOUT_0	Sub clock output pin	57	46	42
	SUBOUT_2		10	7	6
DAC	DA0_0	D/A converter ch.0 analog output pin	22	19	18
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	21	18	17
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	29	23	21
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	28	22	20
Power	VCC	Power supply Pin	1	1	1
			18	15	14
			33	-	-
GND	VSS	GND Pin	16	13	12
			32	26	24
			64	52	48
Clock	X0	Main clock (oscillation) input pin	30	24	22
	X0A	Sub clock (oscillation) input pin	19	16	15
	X1	Main clock (oscillation) I/O pin	31	25	23
	X1A	Sub clock (oscillation) I/O pin	20	17	16
	CROUT_1	Built-in high-speed CR-osc clock output port	57	46	42
Analog Power	AVCC	A/D converter and D/A converter analog power supply pin	41	33	31
	AVRH	A/D converter analog reference voltage input pin	42	34	32
Analog GND	AVSS	A/D converter and D/A converter GND pin	37	30	28
	AVRL	A/D converter analog reference voltage input pin	43	35	33
C pin	C	Power supply stabilization capacity pin	17	14	13

Note:

- While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.

5. I/O Circuit Type

Type	Circuit	Remarks
A	 <p>The schematic illustrates the internal structure of I/O Type A. It features two parallel paths for X1A and X0A. Each path consists of a resistor R, a feedback resistor, and a complex digital logic section. The logic includes P-ch and N-ch MOS transistors, along with various logic gates (inverter, AND, OR, NOT) for generating digital outputs, controlling pull-up resistors, and managing standby modes.</p>	<p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected.</p> <ul style="list-style-type: none"> • Oscillation feedback resistor : Approximately $1\text{ M}\Omega$ • With Standby mode control <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately $50\text{ k}\Omega$ • $I_{OH} = -4\text{ mA}$, $I_{OL} = 4\text{ mA}$

Type	Circuit	Remarks
B	 <p>Pull-up resistor</p> <p>Digital input</p>	<ul style="list-style-type: none"> CMOS level hysteresis input Pull-up resistor : Approximately 50 kΩ
C	 <p>N-ch</p> <p>Digital output</p> <p>Digital input</p>	<ul style="list-style-type: none"> Open drain output CMOS level hysteresis input