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MB9B110R Series

32-bit ARM® Cortex®-M3 based FM3 Microcontroller

The MB9B110R Series are a highly integrated 32-bit microcontrollers dedicated for embedded controllers with high-performance and competitive cost. These series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I^2C, LIN). The products which are described in this data sheet are placed into TYPE4 product categories in FM3 Family Peripheral Manual.

Features

32-bit ARM Cortex-M3 Core

- Processor version: r2p1
- Up to 144 MHz Frequency Operation
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

- Flash memory

These series are based on two independent on-chip Flash memories.

- MainFlash
  - Up to 512 Kbyte
  - Built-in Flash Accelerator System with 16 Kbyte trace buffer memory
  - The read access to Flash memory can be achieved without wait cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
  - Security function for code protection
- WorkFlash
  - 32 Kbyte
  - Read cycle
  - 4 wait-cycle: the operation frequency more than 72 MHz
  - 2 wait-cycle: the operation frequency more than 40 MHz, and to 72 MHz
  - 0wait-cycle: the operation frequency to 40 MHz
  - Security function is shared with code protection

- SRAM

This Series contain a total of up to 64 Kbyte on-chip SRAM. This is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

  - SRAM0: Up to 32 Kbyte
  - SRAM1: Up to 32 Kbyte

External Bus Interface

- Supports SRAM, NOR and NAND Flash device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size : Up to 256 Mbytes
- Supports Address/Data multiplex
- Supports external RDY input

Multi-function Serial Interface (Max eight channels)

- 4 channels with 16 steps×9-bit FIFO (ch.4-ch.7), 4 channels without FIFO (ch.0-ch.3)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generate (can be changed 13 to 16-bit length)
  - LIN break delimiter generate (can be changed 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard-mode (Max 100 kbps) / Fast-mode (Max 400kbps) supported

DMA Controller (Eight channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32 bit (4 Gbyte)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 16 channels)

- 12-bit A/D Converter
  - Successive Approximation Register type
  - Built-in 3 unit
  - Conversion time: 1.0 µs @ 5 V
  - Priority conversion available (priority at 2 levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up 103 fast general purpose I/O Ports@120 pin Package
- Some pin is 5 V tolerant I/O.
  See4. List of Pin Functions to confirm the corresponding pins.

Multi-function Timer (Max three units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch./unit
- Input capture × 4ch./unit
- Output compare × 6ch./unit
- A/D activating compare × 3ch./unit
- Waveform generator × 3ch./unit
- 16-bit PPG timer × 3ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (Max three channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from power consumption mode.

- Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- Up to 16 external interrupt input pin
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.
This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.
"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power consumption mode except Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.
CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

- Clocks

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timers reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Three power consumption modes supported.

- Sleep
- Timer
- Stop

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Power Supply

- Wide range voltage:
  VCC = 2.7 V to 5.5 V

Table of Contents

1. Product Lineup

Memory Size

Product name		MB9BF112N/R	MB9BF114N/R	MB9BF115N/R	MB9BF116N/R
MainFlash		128 Kbyte	256 Kbyte	384 Kbyte	512 Kbyte
WorkFlash		32 Kbyte	32 Kbyte	32 Kbyte	32 Kbyte
On-chip RAM		16 Kbyte	32 Kbyte	48 Kbyte	64 Kbyte
	SRAM0	8 Kbyte	16 Kbyte	24 Kbyte	32 Kbyte
	SRAM1	8 Kbyte	16 Kbyte	24 Kbyte	32 Kbyte

Function

Product name			MB9BF112N MB9BF114N MB9BF115N MB9BF116N	MB9BF112R MB9BF114R MB9BF115R MB9BF116R
Pin count			100/112	120
CPU			Cortex-M3	
	Freq.		144 MHz	
Power supply voltage range			VCC: 2.7 V to 5.5 V	
DMAC			8ch.	
External Bus Interface			Addr: 25-bit (Max) R/Wdata: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR Flash	Addr: 25-bit (Max) R/Wdata: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR & NAND Flash
MF Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max) ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO	
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)	
MF-Timer	A/D activation compare	3ch.	3 units (Max)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
QPRC			3ch. (Max)	
Dual Timer			1 unit	
Real-Time Clock			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1ch. (SW) + 1ch. (HW)	
External Interrupts			16 pins (Max) + NMI × 1	
I/O ports			83 pins (Max)	103 pins (Max)
12-bit A/D converter			16ch. (3 units)	
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2ch.	
Internal OSC	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP/ETM	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use. See 12.4.3 Internal CR Oscillation Characteristics for accuracy of built-in CR.*

2. Packages

Package \ Product name	MB9BF112N MB9BF114N MB9BF115N MB9BF116N	MB9BF112R MB9BF114R MB9BF115R MB9BF116R
QFP: PQH100 (0.65 mm pitch)	❍	-
LQFP: LQI100-02 (0.5 mm pitch)	❍	-
LQFP: LQM120-02 (0.5 mm pitch)	-	❍
FBGA: LBC112 (0.8 mm pitch)	❍	-

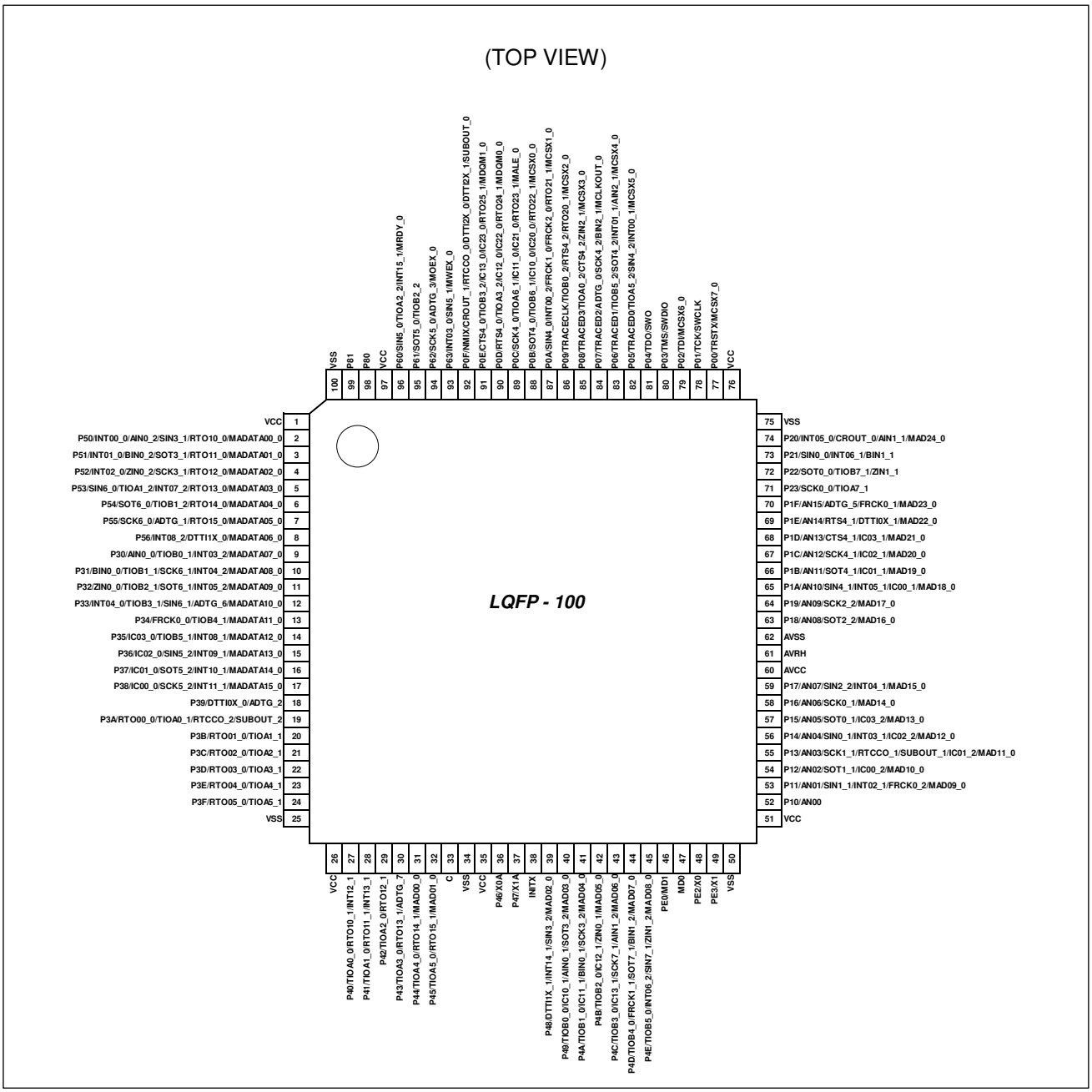
❍: Supported

Note:

- *See 14. Package Dimensions for detailed information on each package.*

3. Pin Assignment

LQI100-02

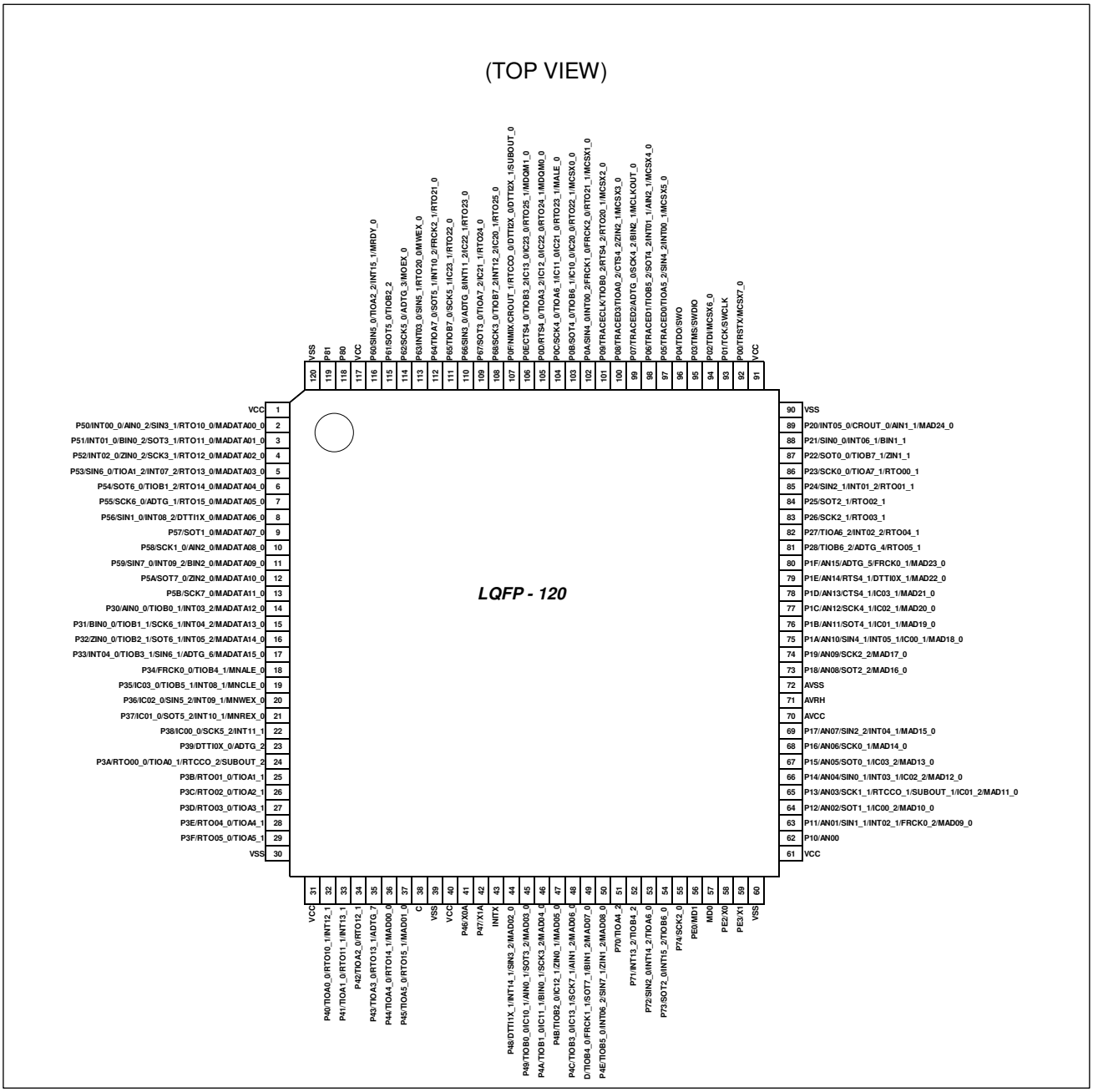


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

LQM120-02

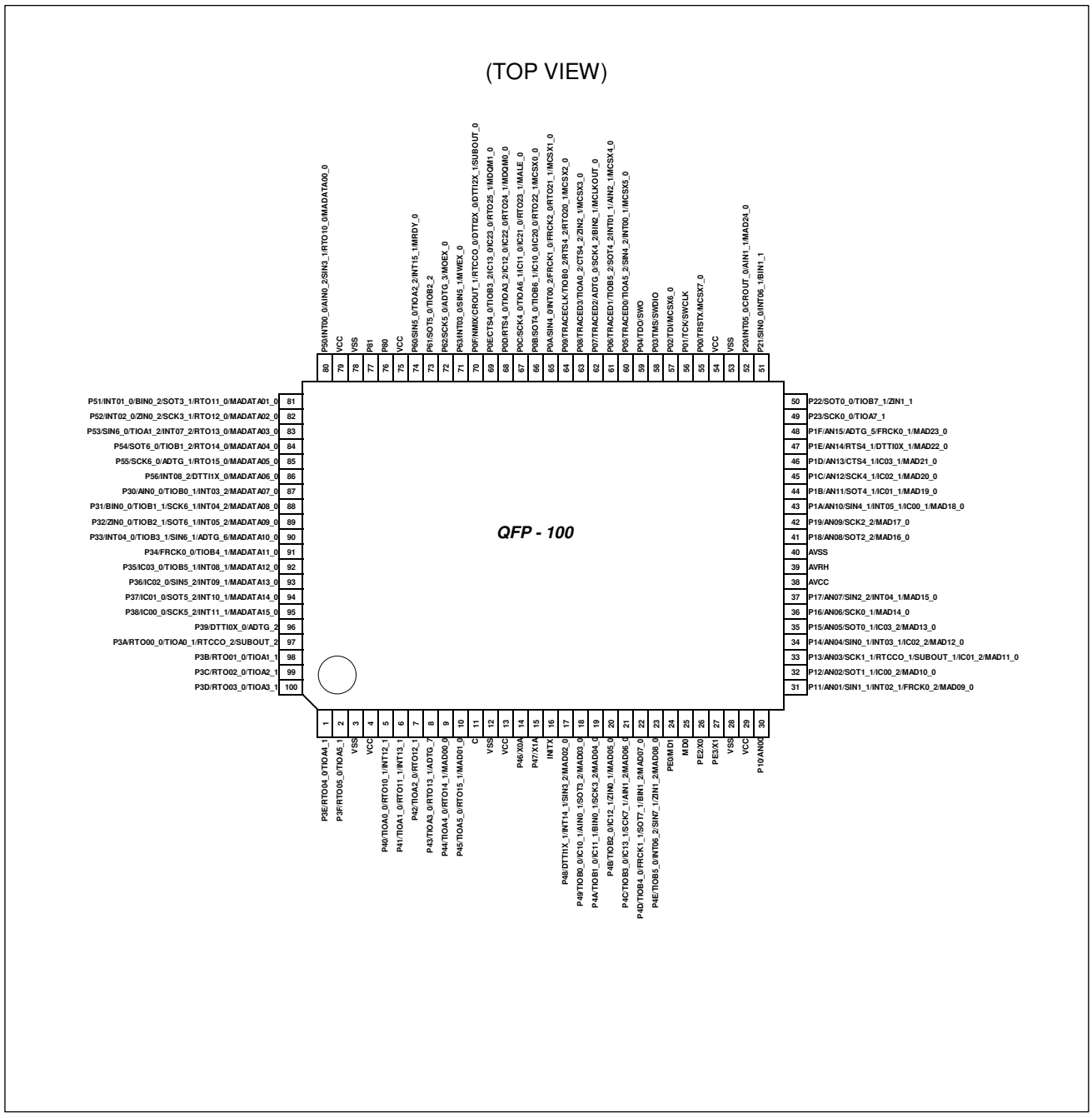


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

PQH100

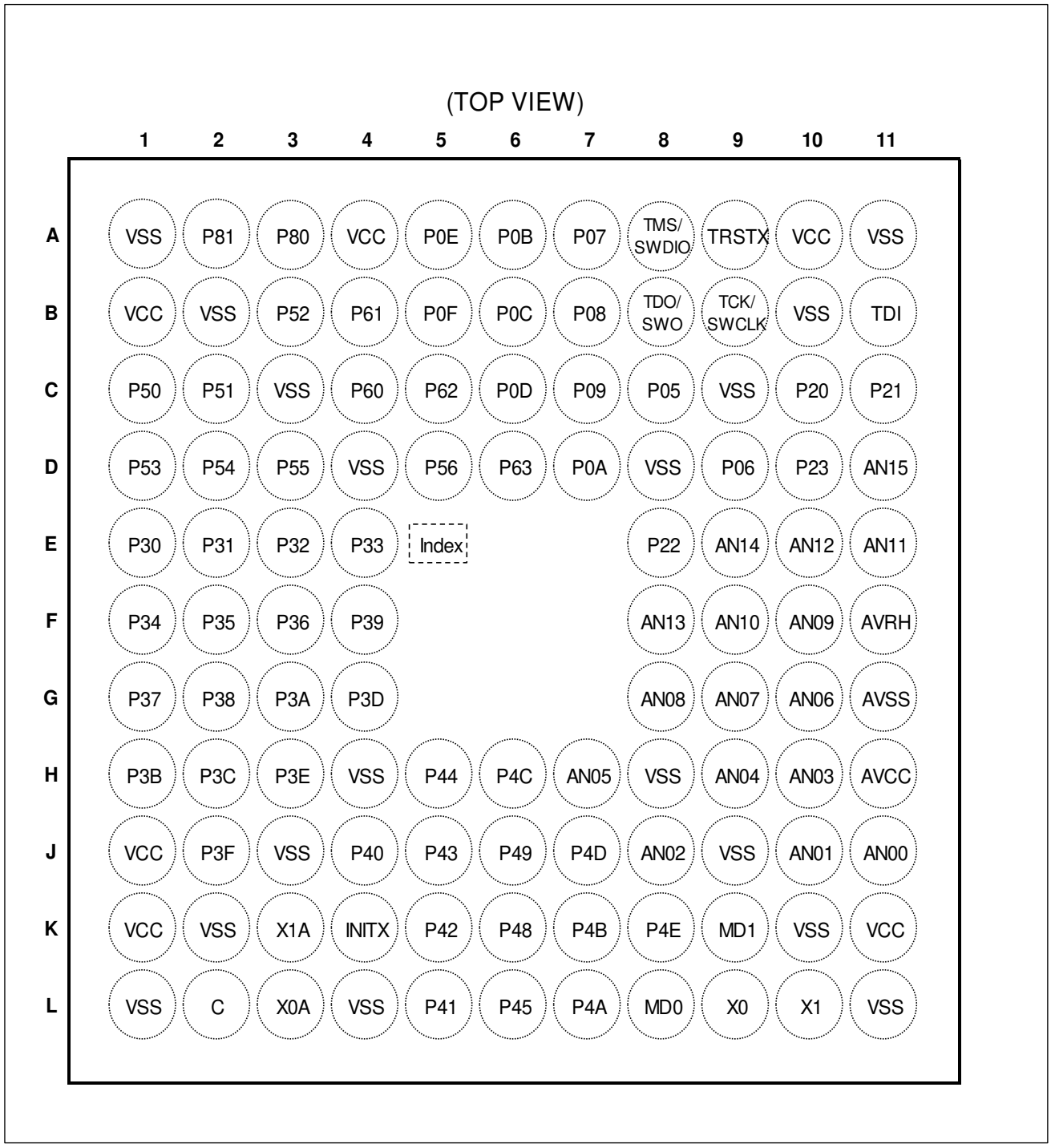


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

LBC112



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*

  Use the extended port function register (EPFR) to select the pin.

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
1	B1	1	79	VCC	-	
2	C1	2	80	P50 INT00_0 AIN0_2 SIN3_1 RTO10_0 (PPG10_0) MADATA00_0	E	H
3	C2	3	81	P51 INT01_0 BIN0_2 SOT3_1 (SDA3_1) RTO11_0 (PPG10_0) MADATA01_0	E	H
4	B3	4	82	P52 INT02_0 ZIN0_2 SCK3_1 (SCL3_1) RTO12_0 (PPG12_0) MADATA02_0	E	H
5	D1	5	83	P53 SIN6_0 TIOA1_2 INT07_2 RTO13_0 (PPG12_0) MADATA03_0	E	H
6	D2	6	84	P54 SOT6_0 (SDA6_0) TIOB1_2 RTO14_0 (PPG14_0) MADATA04_0	E	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
7	D3	7	85	P55 SCK6_0 (SCL6_0) ADTG_1 RTO15_0 (PPG14_0) MADATA05_0	E	I
8	D5	8	86	P56 INT08_2 DTTI1X_0 MADATA06_0	E	H
-	-		-	SIN1_0 (120pin only)		
-	-	9	-	P57 SOT1_0 (SDA1_0) MADATA07_0	E	I
-	-	10	-	P58 SCK1_0 (SCL1_0) AIN2_0 MADATA08_0	E	I
-	-	11	-	P59 SIN7_0 INT09_2 BIN2_0 MADATA09_0	E	H
-	-	12	-	P5A SOT7_0 (SDA7_0) ZIN2_0 MADATA10_0	E	I
-	-	13	-	P5B SCK7_0 (SCL7_0) MADATA11_0	E	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
9	E1	14	87	P30 AIN0_0 TIOB0_1 INT03_2	E	H
		-		MADATA07_0 (100pin only)		
-	-	14	-	MADATA12_0 (120pin only)		
10	E2	15	88	P31 BIN0_0 TIOB1_1 SCK6_1 (SCL6_1) INT04_2	E	H
		-		MADATA08_0 (100pin only)		
-	-	15	-	MADATA13_0 (120pin only)		
11	E3	16	89	P32 ZIN0_0 TIOB2_1 SOT6_1 (SDA6_1) INT05_2	E	H
		-		MADATA09_0 (100pin only)		
-	-	16	-	MADATA14_0 (120pin only)		
12	E4	17	90	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6	E	H
		-		MADATA10_0 (100pin only)		
-	-	17	-	MADATA15_0 (120pin only)		
13	F1	18	91	P34 FRCK0_0 TIOB4_1	E	I
		-		MADATA11_0 (100pin only)		
-	-	18	-	MNALE_0 (120pin only)		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
14	F2	19	92	P35 IC03_0 TIOB5_1 INT08_1	E	H
		-		MADATA12_0 (100pin only)		
-	-	19	-	MNCLE_0 (120pin only)		
15	F3	20	93	P36 IC02_0 SIN5_2 INT09_1	E	H
		-		MADATA13_0 (100pin only)		
-	-	20	-	MNWEX_0 (120pin only)		
16	G1	21	94	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1	E	H
		-		MADATA14_0 (100pin only)		
-	-	21	-	MNREX_0 (120pin only)		
17	G2	22	95	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	H
		-		MADATA15_0 (100pin only)		
18	F4	23	96	P39 DTTI0X_0 ADTG_2	E	I
19	G3	24	97	P3A RTO00_0 (PPG00_0) TIOA0_1 RTCCO_2 SUBOUT_2	G	I
-	B2	-	-	VSS	-	

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
20	H1	25	98	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	H2	26	99	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	G4	27	100	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
23	H3	28	1	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	J2	29	2	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	L1	30	3	VSS	-	
26	J1	31	4	VCC	-	
27	J4	32	5	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	H
28	L5	33	6	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1	G	H
29	K5	34	7	P42 TIOA2_0 RTO12_1 (PPG12_1)	G	I
30	J5	35	8	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7	G	I
-	K2	-	-	VSS	-	
-	J3	-	-	VSS	-	
-	H4	-	-	VSS	-	

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
31	H5	36	9	P44 TIOA4_0 RTO14_1 (PPG14_1) MAD00_0	G	I
32	L6	37	10	P45 TIOA5_0 RTO15_1 (PPG14_1) MAD01_0	G	I
33	L2	38	11	C	-	
34	L4	39	12	VSS	-	
35	K1	40	13	VCC	-	
36	L3	41	14	P46 X0A	D	M
37	K3	42	15	P47 X1A	D	N
38	K4	43	16	INITX	B	C
39	K6	44	17	P48 DTTI1X_1 INT14_1 SIN3_2 MAD02_0	E	H
40	J6	45	18	P49 TIOB0_0 IC10_1 AIN0_1 SOT3_2 (SDA3_2) MAD03_0	E	I
41	L7	46	19	P4A TIOB1_0 IC11_1 BIN0_1 SCK3_2 (SCL3_2) MAD04_0	E	I
42	K7	47	20	P4B TIOB2_0 IC12_1 ZIN0_1 MAD05_0	E	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
43	H6	48	21	P4C TIOB3_0 IC13_1 SCK7_1 (SCL7_1) AIN1_2 MAD06_0	I*	I
44	J7	49	22	P4D TIOB4_0 FRCK1_1 SOT7_1 (SDA7_1) BIN1_2 MAD07_0	I*	I
45	K8	50	23	P4E TIOB5_0 INT06_2 SIN7_1 ZIN1_2 MAD08_0	I*	H
-	-	51	-	P70 TIOA4_2	E	I
-	-	52	-	P71 INT13_2 TIOB4_2	E	H
-	-	53	-	P72 SIN2_0 INT14_2 TIOA6_0	E	H
-	-	54	-	P73 SOT2_0 (SDA2_0) INT15_2 TIOB6_0	E	H
-	-	55	-	P74 SCK2_0 (SCL2_0)	E	I
46	K9	56	24	PE0 MD1	C	P
47	L8	57	25	MD0	J	D

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
48	L9	58	26	PE2	A	A
				X0		
49	L10	59	27	PE3	A	B
				X1		
50	L11	60	28	VSS	-	
51	K11	61	29	VCC	-	
52	J11	62	30	P10	F	K
				AN00		
53	J10	63	31	P11	F	L
				AN01		
				SIN1_1		
				INT02_1		
				FRCK0_2		
				MAD09_0		
-	K10	-	-	VSS	-	
-	J9	-	-	VSS	-	
54	J8	64	32	P12	F	K
				AN02		
				SOT1_1 (SDA1_1)		
				IC00_2		
				MAD10_0		
55	H10	65	33	P13	F	K
				AN03		
				SCK1_1 (SCL1_1)		
				RTCCO_1		
				SUBOUT_1		
				IC01_2		
				MAD11_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
56	H9	66	34	P14	F	L
				AN04		
				SIN0_1		
				INT03_1		
				IC02_2		
				MAD12_0		
57	H7	67	35	P15	F	K
				AN05		
				SOT0_1 (SDA0_1)		
				IC03_2		
				MAD13_0		
58	G10	68	36	P16	F	K
				AN06		
				SCK0_1 (SCL0_1)		
				MAD14_0		
59	G9	69	37	P17	F	L
				AN07		
				SIN2_2		
				INT04_1		
				MAD15_0		
60	H11	70	38	AVCC	-	
61	F11	71	39	AVRH	-	
62	G11	72	40	AVSS	-	
63	G8	73	41	P18	F	K
				AN08		
				SOT2_2 (SDA2_2)		
				MAD16_0		
64	F10	74	42	P19	F	K
				AN09		
				SCK2_2 (SCL2_2)		
				MAD17_0		
65	F9	75	43	P1A	F	L
				AN10		
				SIN4_1		
				INT05_1		
				IC00_1		
				MAD18_0		
-	H8	-	-	VSS	-	

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
66	E11	76	44	P1B AN11 SOT4_1 (SDA4_1) IC01_1 MAD19_0	F	K
67	E10	77	45	P1C AN12 SCK4_1 (SCL4_1) IC02_1 MAD20_0	F	K
68	F8	78	46	P1D AN13 CTS4_1 IC03_1 MAD21_0	F	K
69	E9	79	47	P1E AN14 RTS4_1 DTTI0X_1 MAD22_0	F	K
70	D11	80	48	P1F AN15 ADTG_5 FRCK0_1 MAD23_0	F	K
-	-	81	-	P28 TIOB6_2 ADTG_4 RTO05_1 (PPG04_1)	E	I
-	-	82	-	P27 TIOA6_2 INT02_2 RTO04_1 (PPG04_1)	E	H
-	-	83	-	P26 SCK2_1 (SCL2_1) RTO03_1 (PPG02_1)	E	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
-	-	84	-	P25 SOT2_1 (SDA2_1) RTO02_1 (PPG02_1)	E	I
-	B10	-	-	VSS	-	
-	C9	-	-	VSS	-	
-	-	85	-	P24 SIN2_1 INT01_2 RTO01_1 (PPG00_1)	E	H
71	D10	86	49	P23 SCK0_0 (SCL0_0) TIOA7_1	E	I
-	-		-	RTO00_1 (PPG00_1)		
72	E8	87	50	P22 SOT0_0 (SDA0_0) TIOB7_1 ZIN1_1	E	I
73	C11	88	51	P21 SIN0_0 INT06_1 BIN1_1	E	H
74	C10	89	52	P20 INT05_0 CROUT_0 AIN1_1 MAD24_0	E	H
75	A11	90	53	VSS	-	
76	A10	91	54	VCC	-	
77	A9	92	55	P00 TRSTX MCSX7_0	E	E
78	B9	93	56	P01 TCK SWCLK	E	E

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
79	B11	94	57	P02 TDI MCSX6_0	E	E
80	A8	95	58	P03 TMS SWDIO	E	E
81	B8	96	59	P04 TDO SWO	E	E
82	C8	97	60	P05 TRACED0 TIOA5_2 SIN4_2 INT00_1 MCSX5_0	E	F
-	D8	-	-	VSS	-	
83	D9	98	61	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 AIN2_1 MCSX4_0	E	F
84	A7	99	62	P07 TRACED2 ADTG_0 SCK4_2 (SCL4_2) BIN2_1 MCLKOUT_0	E	G
85	B7	100	63	P08 TRACED3 TIOA0_2 CTS4_2 ZIN2_1 MCSX3_0	E	G
86	C7	101	64	P09 TRACECLK TIOB0_2 RTS4_2 RTO20_1 (PPG20_1) MCSX2_0	E	G

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
87	D7	102	65	P0A SIN4_0 INT00_2 FRCK1_0 FRCK2_0 RTO21_1 (PPG20_1) MCSX1_0	I*	H
88	A6	103	66	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 IC20_0 RTO22_1 (PPG22_1) MCSX0_0	I*	I
89	B6	104	67	P0C SCK4_0 (SCL4_0) TIOA6_1 IC11_0 IC21_0 RTO23_1 MALE_0	I*	I
90	C6	105	68	P0D RTS4_0 TIOA3_2 IC12_0 IC22_0 RTO24_1 (PPG24_1) MDQM0_0	E	I
91	A5	106	69	P0E CTS4_0 TIOB3_2 IC13_0 IC23_0 RTO25_1 (PPG24_1) MDQM1_0	E	I
-	D4	-	-	VSS	-	
-	C3	-	-	VSS	-	