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The MB9B120M Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM<sup>®</sup> Cortex<sup>®</sup>-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, DACs and Communication Interfaces (UART, CSIO, I<sup>2</sup>C, LIN).

The products which are described in this data sheet are placed into TYPE9 product categories in FM3 Family Peripheral Manual.

## Features

### 32-bit ARM<sup>®</sup> Cortex<sup>®</sup>-M3 Core

- Processor version: r2p1
- Up to 72 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

### On-chip Memories

#### [Flash memory]

- Dual operation Flash memory
  - Dual Operation Flash memory has the upper bank and the lower bank.  
So, this series could implement erase, write and read operations for each bank simultaneously.
  - Main area: Up to 256 Kbytes (Up to 240 Kbytes upper bank + 16 Kbytes lower bank)
  - Work area: 32 Kbytes (lower bank)
- Read cycle: 0 wait-cycle
- Security function for code protection

#### [SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 16 Kbytes
- SRAM1: Up to 16 Kbytes

### Multi-function Serial Interface (Max eight channels)

- 4 channels with 16 stepsx9-bit FIFO (ch.0/1/3/4), 4 channels without FIFO (ch.2/5/6/7)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I<sup>2</sup>C

#### [UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission/reception by CTS/RTS (only ch.4)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

#### [CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

#### [LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can be changed to 13 to 16-bit length)
- LIN break delimiter generation (can be changed to 1 to 4-bit length)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

#### [I<sup>2</sup>C]

- Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported

## DMA Controller (Eight channels)

The DMA controller has an independent bus from the CPU, so the CPU and the DMA controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

## A/D Converter (Max 26 channels)

### [12-bit A/D Converter]

- Successive Approximation type
- Built-in 2 units
- Conversion time: 0.8 $\mu$ s @ 5V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

## D/A Converter (Max two channels)

- R-2R type
- 10-bit resolution

## Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

## General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port relocate function
- Up to 65 high-speed general-purpose I/O ports @ 80 pin package
- Some ports are 5V tolerant.  
See "List of Pin Functions" and "I/O Circuit Type" to confirm the corresponding pins.

## Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

## Quadrature Position/Revolution Counter (QPRC) (Max two channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use as the up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

## Multi-Function Timer

The multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch./unit
- Input capture × 4ch./unit
- Output compare × 6ch./unit
- A/D activation compare × 2ch./unit
- Waveform generator × 3ch./unit
- 16-bit PPG timer × 3ch./unit

The following functions can be used to achieve motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D converter activate function
- DTIF (motor emergency stop) interrupt function

## Real-Time Clock (RTC)

The real-time clock can count

Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

## Watch Counter

The watch counter is used for wake up from the Sleep and Timer mode.

Interval timer: up to 64s (Max) @ Sub Clock: 32.768 kHz

## External Interrupt Controller Unit

- Up to 23 external interrupt input pins @ 80 pin Package
- Include one non-maskable interrupt (NMI) input pin

## Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a “Hardware” watchdog and a “Software” watchdog.

The “Hardware” watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the “Hardware” watchdog is active in any low-power consumption modes except RTC, Stop, Deep Standby RTC, Deep Standby Stop modes.

## CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

## Clock and Reset

### [Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillator, and Main PLL).

- Main Clock : 4 MHz to 48 MHz
- Sub Clock : 32.768 kHz
- Built-in High-speed CR Clock : 4 MHz
- Built-in Low-speed CR Clock : 100 kHz
- Main PLL Clock

### [Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

## Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

### Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

### Low-Power Consumption Mode

Six low-power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep Standby RTC (selectable between keeping the value of RAM and not)
- Deep Standby Stop (selectable between keeping the value of RAM and not)

### Debug

Serial Wire JTAG Debug Port (SWJ-DP)

### Unique ID

Unique value of the device (41-bit) is set.

### Power Supply

- Wide range voltage:  
VCC = 2.7V to 5.5V

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## 1. Product Lineup

### Memory Size

Product Name		MB9BF121K/L/M	MB9BF122K/L/M	MB9BF124K/L/M
On-chip Flash memory	Main area	64 Kbytes	128 Kbytes	256 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	8 Kbytes	8 Kbytes	16 Kbytes
	SRAM1	8 Kbytes	8 Kbytes	16 Kbytes
	Total	16 Kbytes	16 Kbytes	32 Kbytes

### Function

Product Name		MB9BF121K MB9BF122K MB9BF124K	MB9BF121L MB9BF122L MB9BF124L	MB9BF121M MB9BF122M MB9BF124M
Pin count		48	64	80/96
CPU		Cortex-M3		
Freq.		72 MHz		
Power supply voltage range		2.7 V to 5.5 V		
DMAC		8ch.		
Multi-function Serial Interface (UART/CSIO/LIN/I <sup>2</sup> C)		4ch. (Max) ch.0/1/3: FIFO ch.5: No FIFO (In ch.1/5, only UART and LIN are available.)	8ch. (Max) ch.0/1/3/4 FIFO ch.2/5/6/7: No FIFO (In ch.1, only UART and LIN are available.)	
Base Timer (PWC/Reload timer/PWM/PPG)		8ch. (Max)		
MF Timer	A/D activation compare	2ch.		
	Input capture	4ch.*		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
QPRC		1ch.	2ch. (Max)	
Dual Timer		1 unit		
Real-Time Clock		1 unit		
Watch Counter		1 unit		
CRC Accelerator		Yes		
Watchdog Timer		1ch. (SW) + 1ch. (HW)		
External Interrupts		14 pins (Max) + NMI x 1	19 pins (Max) + NMI x 1	23 pins (Max) + NMI x 1
I/O ports		35 pins (Max)	50 pins (Max)	60 pins (Max)
12-bit A/D converter		14ch. (2 units)	23ch. (2 units)	26ch. (2 units)
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2ch.		
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug Function		SWJ-DP		
Unique ID		Yes		

\*: The external input channel which can be used is shown as follows.

- ch.0 to ch.3 : MB9BF121M/F122M/F124M
- ch.0, ch.2, ch.3 : MB9BF121K/F122K/F124K, MB9BF121L/F122L/F124L

**Note:** All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.

It is necessary to use the port relocate function of the I/O port according to your function use.

See "12 Electrical Characteristics 12.4 AC Characteristics 12.4.3 Built-in CR Oscillation Characteristics" for the accuracy of the built-in CR.



## 2. Packages

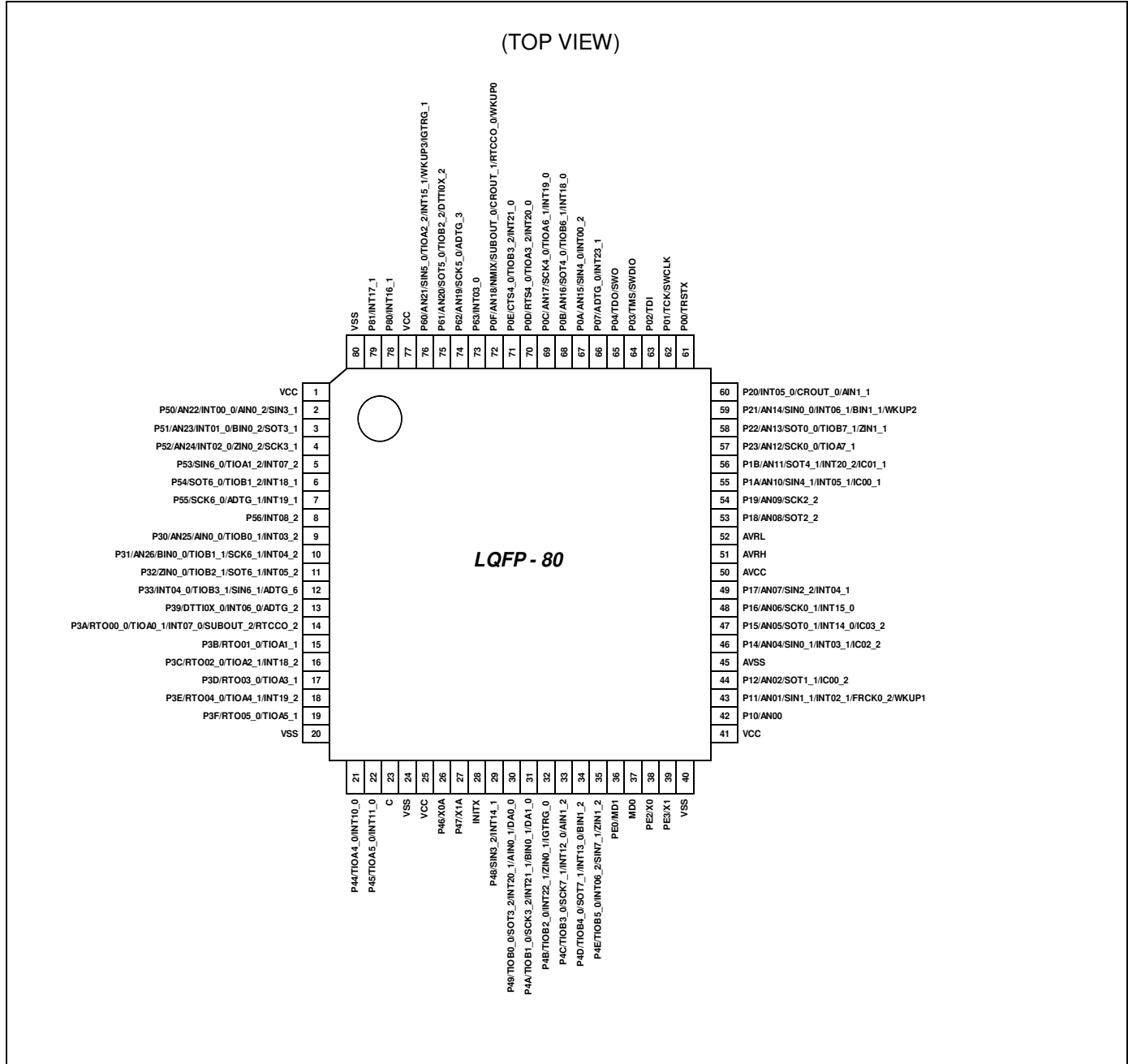
Package	Product name	MB9BF121K MB9BF122K MB9BF124K	MB9BF121L MB9BF122L MB9BF124L	MB9BF121M MB9BF122M MB9BF124M
LQFP: FPT-48P-M49 (0.5mm pitch)		○	-	-
QFN: LCC-48P-M73 (0.5mm pitch)		○	-	-
LQFP: FPT-64P-M38 (0.5mm pitch)		-	○	-
LQFP: FPT-64P-M39 (0.65mm pitch)		-	○	-
QFP: LCC-64P-M24 (0.5mm pitch)		-	○	-
LQFP: FPT-80P-M37 (0.5mm pitch)		-	-	○
LQFP: FPT-80P-M40 (0.65mm pitch)		-	-	○
BGA: BGA-96P-M07 (0.5mm pitch)		-	-	○

○: Supported

**Note:** See "Package Dimensions" for detailed information on each package

### 3. Pin Assignment

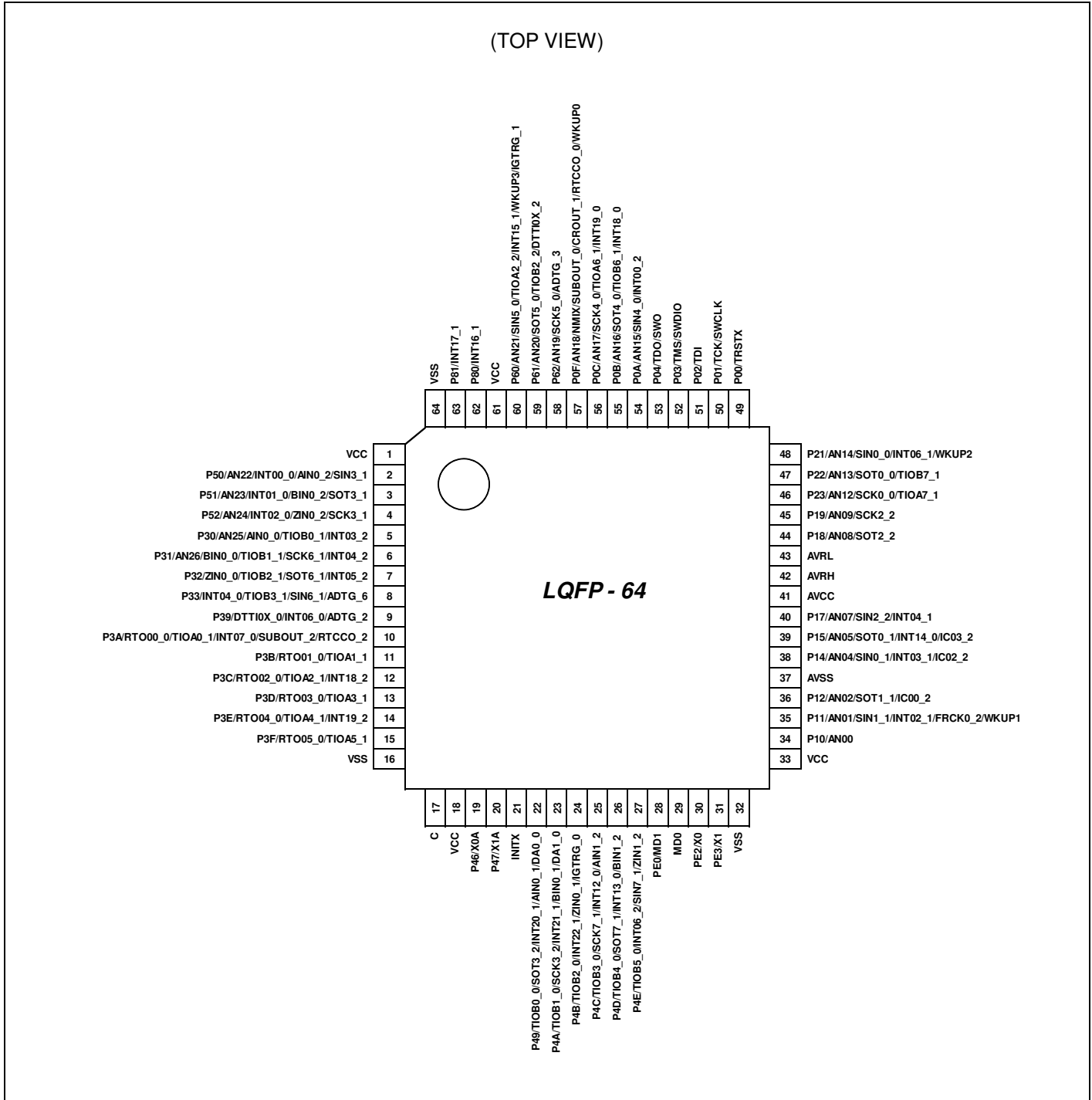
#### FPT-80-M37/M40



**Note:**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

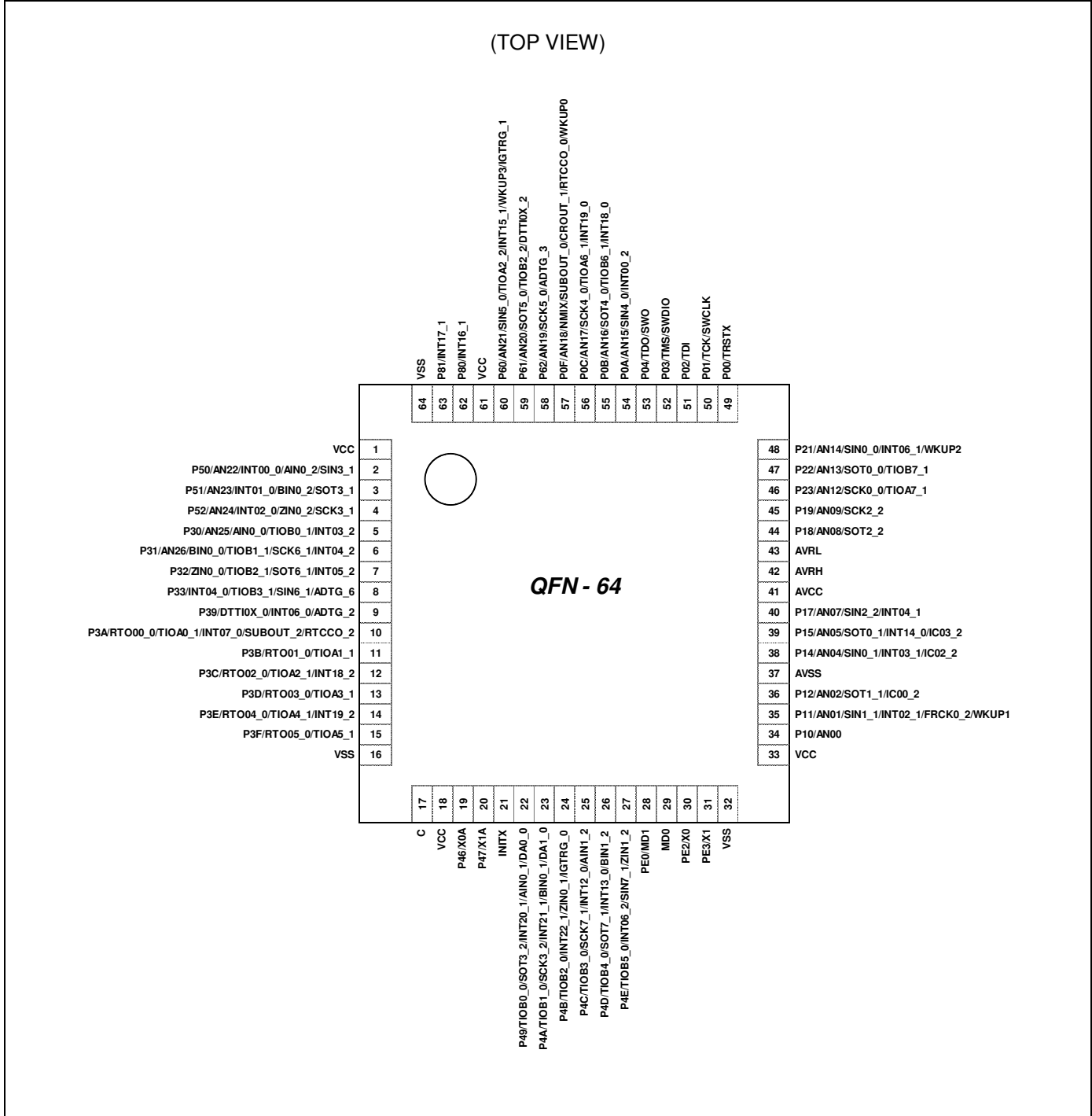
## FPT-64P-M38/M39



**Note:**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

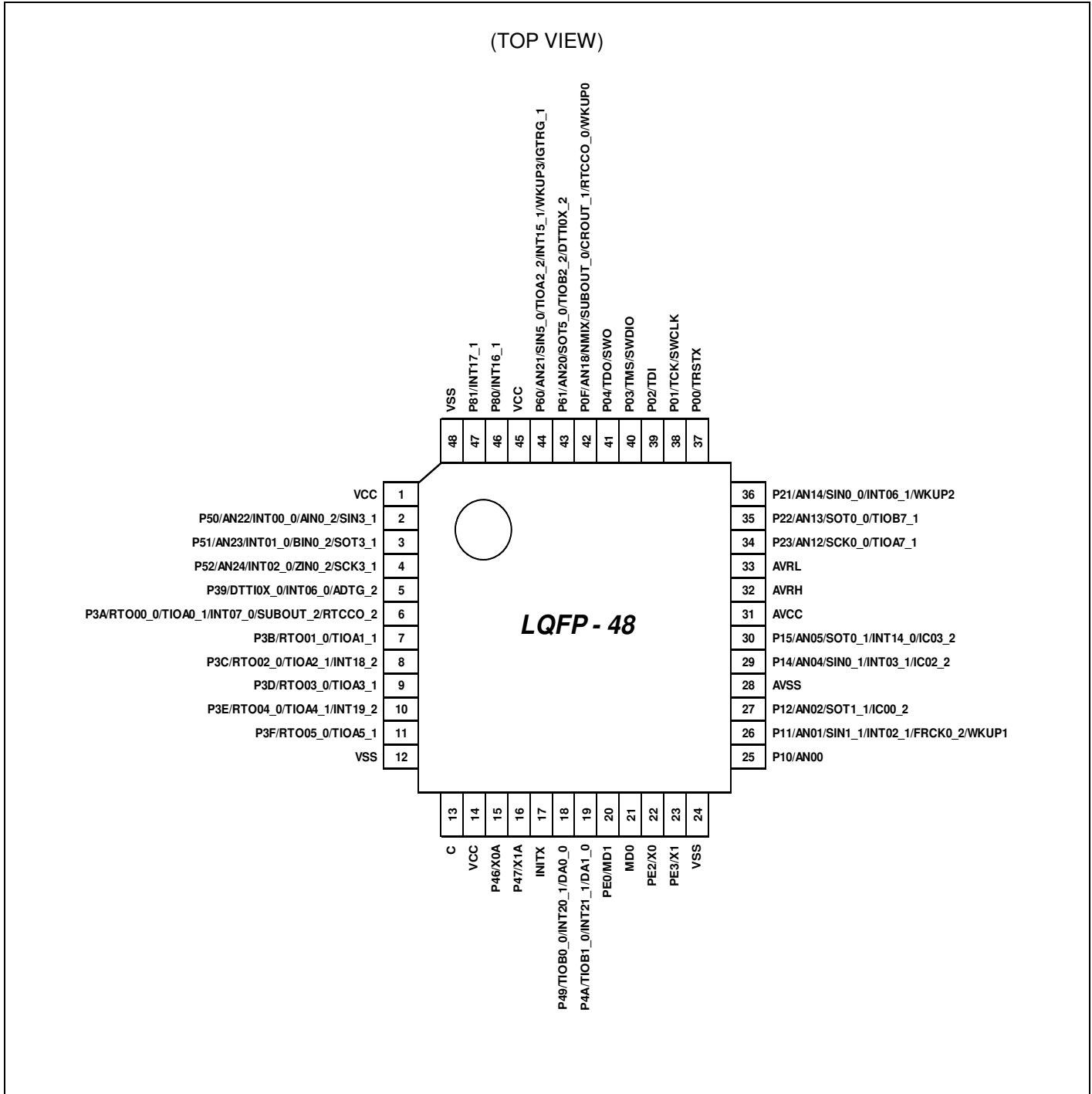
LCC-64P-M24



**Note:**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

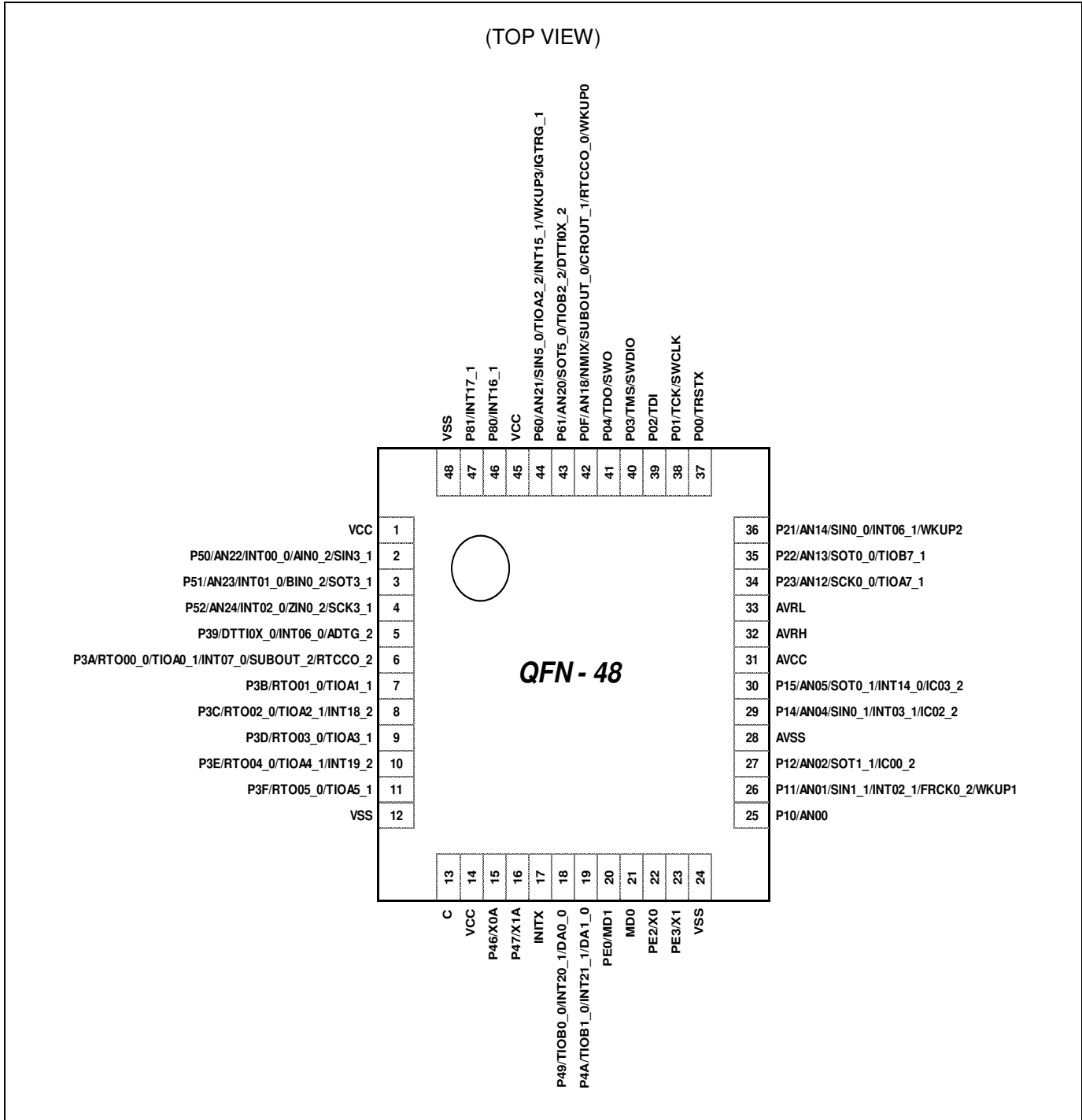
FPT-48P-M49



**Note:**

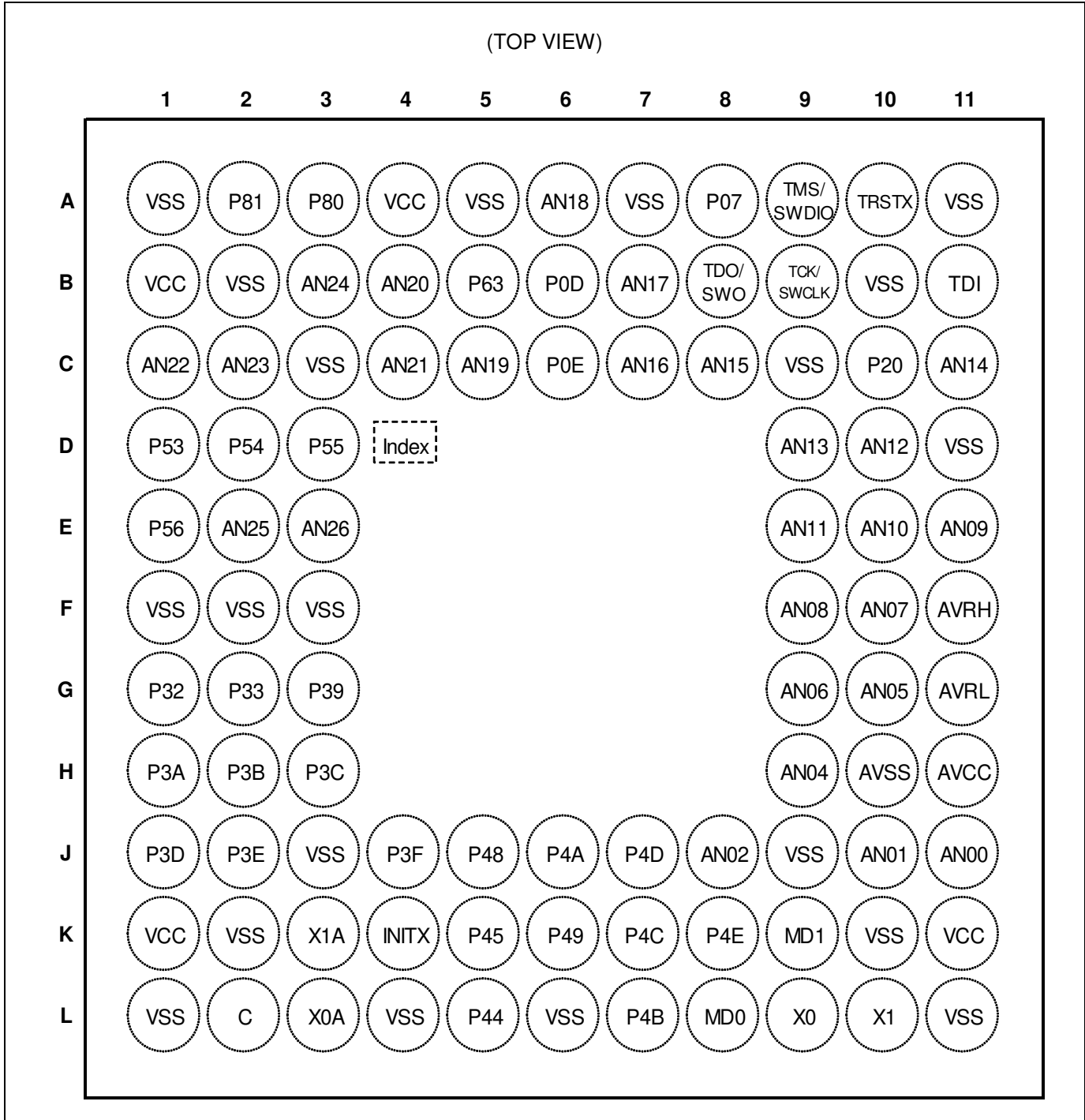
The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LCC-48P-M73



**Note:**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

**BGA-96P-M07**

**Note:**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

#### 4. List of Pin Functions

##### List of pin numbers

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
1	B1	1	1	VCC	-	
2	C1	2	2	P50	F	N
				INT00_0		
				AIN0_2		
				SIN3_1		
3	C2	3	3	AN22	F	N
				P51		
				INT01_0		
				BIN0_2		
4	B3	4	4	SOT3_1 (SDA3_1)	F	N
				AN23		
				P52		
				INT02_0		
5	D1	-	-	ZIN0_2	F	N
				SCK3_1 (SCL3_1)		
				AN24		
				P53		
6	D2	-	-	SIN6_0	E	L
				TIOA1_2		
				INT07_2		
				P54		
7	D3	-	-	SOT6_0 (SDA6_0)	E	L
				TIOB1_2		
				INT18_1		
				P55		
8	E1	-	-	SCK6_0 (SCL6_0)	E	L
				ADTG_1		
				INT19_1		
				P56		
9	E2	5	-	INT08_2	E	L
				P30		
				AIN0_0		
				TIOB0_1		
10	E3	6	-	INT03_2	F	N
				AN25		
				P31		
				BIN0_0		
				TIOB1_1		
				SCK6_1 (SCL6_1)		
INT04_2						
				AN26		



Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
11	G1	7	-	P32	E	L
				ZIN0_0		
				TIOB2_1		
				SOT6_1 (SDA6_1)		
				INT05_2		
12	G2	8	-	P33	E	L
				INT04_0		
				TIOB3_1		
				SIN6_1		
				ADTG_6		
13	G3	9	5	P39	E	L
				DTTIOX_0		
				INT06_0		
				ADTG_2		
14	H1	10	6	P3A	G	L
				RTO00_0 (PPG00_0)		
				TIOA0_1		
				INT07_0		
				SUBOUT_2		
RTCCO_2						
15	H2	11	7	P3B	G	K
				RTO01_0 (PPG00_0)		
				TIOA1_1		
16	H3	12	8	P3C	G	L
				RTO02_0 (PPG02_0)		
				TIOA2_1		
				INT18_2		
17	J1	13	9	P3D	G	K
				RTO03_0 (PPG02_0)		
				TIOA3_1		
18	J2	14	10	P3E	G	L
				RTO04_0 (PPG04_0)		
				TIOA4_1		
				INT19_2		
19	J4	15	11	P3F	G	K
				RTO05_0 (PPG04_0)		
				TIOA5_1		
20	L1	16	12	VSS	-	
21	L5	-	-	P44	G	L
				TIOA4_0		
				INT10_0		
22	K5	-	-	P45	G	L
				TIOA5_0		
				INT11_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
23	L2	17	13	C	-	
24	L4	-	-	VSS	-	
25	K1	18	14	VCC	-	
26	L3	19	15	P46	D	F
				X0A		
27	K3	20	16	P47	D	G
				X1A		
28	K4	21	17	INITX	B	C
29	J5	-	-	P48	E	L
				INT14_1		
				SIN3_2		
30	K6	22	18	P49	L	L
				TIOB0_0		
				INT20_1		
			DA0_0			
			-	SOT3_2 (SDA3_2)		
-	AIN0_1					
31	J6	23	19	P4A	L	L
				TIOB1_0		
				INT21_1		
			DA1_0			
			-	SCK3_2 (SCL3_2)		
-	BIN0_1					
32	L7	24	-	P4B	E	L
				TIOB2_0		
				INT22_1		
				IGTRG_0		
				ZIN0_1		
33	K7	25	-	P4C	I*	L
				TIOB3_0		
				SCK7_1 (SCL7_1)		
				INT12_0		
				AIN1_2		
34	J7	26	-	P4D	I*	L
				TIOB4_0		
				SOT7_1 (SDA7_1)		
				INT13_0		
				BIN1_2		
35	K8	27	-	P4E	I*	L
				TIOB5_0		
				INT06_2		
				SIN7_1		
				ZIN1_2		
36	K9	28	20	MD1	C	E
				PE0		
37	L8	29	21	MD0	K	D

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
38	L9	30	22	X0	A	A
				PE2		
39	L10	31	23	X1	A	B
				PE3		
40	L11	32	24	VSS	-	
41	K11	33	-	VCC	-	
42	J11	34	25	P10	F	M
				AN00		
43	J10	35	26	P11	F	N
				AN01		
				SIN1_1		
				INT02_1		
				FRCK0_2		
WKUP1						
44	J8	36	27	P12	F	M
				AN02		
				SOT1_1 (SDA1_1)		
				IC00_2		
45	H10	37	28	AVSS	-	
46	H9	38	29	P14	F	N
				AN04		
				INT03_1		
				IC02_2		
SIN0_1						
47	G10	39	30	P15	F	N
				AN05		
				IC03_2		
				SOT0_1 (SDA0_1)		
INT14_0						
48	G9	-	-	P16	F	N
				AN06		
				SCK0_1 (SCL0_1)		
				INT15_0		
49	F10	40	-	P17	F	N
				AN07		
				SIN2_2		
				INT04_1		
50	H11	41	31	AVCC	-	
51	F11	42	32	AVRH	-	
52	G11	43	33	AVRL	-	
53	F9	44	-	P18	F	M
				AN08		
				SOT2_2 (SDA2_2)		
54	E11	45	-	P19	F	M
				AN09		
				SCK2_2 (SCL2_2)		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
55	E10	-	-	P1A	F	N
				AN10		
				SIN4_1		
				INT05_1		
56	E9	-	-	IC00_1	F	N
				P1B		
				AN11		
				SOT4_1 (SDA4_1)		
57	D10	46	34	IC01_1	F	M
				INT20_2		
				P23		
				SCK0_0 (SCL0_0)		
58	D9	47	35	TIOA7_1	F	M
				AN12		
		-	-	SOT0_0 (SDA0_0)		
				TIOB7_1		
59	C11	48	36	AN13	F	N
				ZIN1_1		
				P21		
				SIN0_0		
				INT06_1		
60	C10	-	-	WKUP2	E	N
				BIN1_1		
				AN14		
				P20		
61	A10	49	37	INT05_0	E	J
				TRSTX		
				CROUT_0		
62	B9	50	38	AIN1_1	E	J
				P01		
				TCK		
63	B11	51	39	SWCLK	E	J
				P02		
				TDI		
64	A9	52	40	P03	E	J
				TMS		
				SWDIO		
65	B8	53	41	P04	E	J
				TDO		
				SWO		
66	A8	-	-	P07	E	L
				ADTG_0		
				INT23_1		
67	C8	54	-	P0A	J*	N
				SIN4_0		
				INT00_2		
				AN15		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
68	C7	55	-	P0B	J*	N
				SOT4_0 (SDA4_0)		
				TIOB6_1		
				AN16		
				INT18_0		
69	B7	56	-	P0C	J*	N
				SCK4_0 (SCL4_0)		
				TIOA6_1		
				INT19_0		
				AN17		
70	B6	-	-	P0D	E	L
				RTS4_0		
				TIOA3_2		
				INT20_0		
71	C6	-	-	P0E	E	L
				CTS4_0		
				TIOB3_2		
				INT21_0		
72	A6	57	42	P0F	F	I
				NMIX		
				SUBOUT_0		
				CROUT_1		
				RTCCO_0		
				WKUP0		
				AN18		
73	B5	-	-	P63	E	L
				INT03_0		
74	C5	58	-	P62	F	M
				SCK5_0 (SCL5_0)		
				ADTG_3		
				AN19		
75	B4	59	43	P61	F	M
				SOT5_0 (SDA5_0)		
				TIOB2_2		
				DTTIOX_2		
				AN20		
76	C4	60	44	P60	J*	N
				SIN5_0		
				TIOA2_2		
				INT15_1		
				WKUP3		
				IGTRG_1		
				AN21		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
77	A4	61	45	VCC	-	
78	A3	62	46	P80	H	H
				INT16_1		
79	A2	63	47	P81	H	H
				INT17_1		
80	A1	64	48	VSS	-	
-	A5, A7, A11, B2, B10, C3, C9, F1, F2, F3, J3, J9, K2, K10, L6	-	-	VSS	-	

\*: 5 V tolerant I/O

**List of functions**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
ADC	ADTG_0	A/D converter external trigger input pin	66	A8	-	-
	ADTG_1		7	D3	-	-
	ADTG_2		13	G3	9	5
	ADTG_3		74	C5	58	-
	ADTG_6		12	G2	8	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	42	J11	34	25
	AN01		43	J10	35	26
	AN02		44	J8	36	27
	AN04		46	H9	38	29
	AN05		47	G10	39	30
	AN06		48	G9	-	-
	AN07		49	F10	40	-
	AN08		53	F9	44	-
	AN09		54	E11	45	-
	AN10		55	E10	-	-
	AN11		56	E9	-	-
	AN12		57	D10	46	34
	AN13		58	D9	47	35
	AN14		59	C11	48	36
	AN15		67	C8	54	-
	AN16		68	C7	55	-
	AN17		69	B7	56	-
	AN18		72	A6	57	42
	AN19		74	C5	58	-
	AN20		75	B4	59	43
	AN21		76	C4	60	44
AN22	2		C1	2	2	
AN23	3		C2	3	3	
AN24	4		B3	4	4	
AN25	9		E2	5	-	
AN26	10		E3	6	-	
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	14	H1	10	6
	TIOB0_0	Base timer ch.0 TIOB pin	30	K6	22	18
	TIOB0_1		9	E2	5	-
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	15	H2	11	7
	TIOA1_2		5	D1	-	-
	TIOB1_0	Base timer ch.1 TIOB pin	31	J6	23	19
	TIOB1_1		10	E3	6	-
TIOB1_2	6	D2	-	-		
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	16	H3	12	8
	TIOA2_2		76	C4	60	44
	TIOB2_0	Base timer ch.2 TIOB pin	32	L7	24	-
	TIOB2_1		11	G1	7	-
	TIOB2_2		75	B4	59	43
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	17	J1	13	9
	TIOA3_2		70	B6	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	33	K7	25	-
	TIOB3_1		12	G2	8	-
	TIOB3_2		71	C6	-	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	21	L5	-	-
	TIOA4_1		18	J2	14	10
	TIOB4_0	Base timer ch.4 TIOB pin	34	J7	26	-

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	22	K5	-	-
	TIOA5_1		19	J4	15	11
	TIOB5_0	Base timer ch.5 TIOB pin	35	K8	27	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	69	B7	56	-
	TIOB6_1	Base timer ch.6 TIOB pin	68	C7	55	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	57	D10	46	34
	TIOB7_1	Base timer ch.7 TIOB pin	58	D9	47	35
Debugger	SWCLK	Serial wire debug interface clock input pin	62	B9	50	38
	SWDIO	Serial wire debug interface data input / output pin	64	A9	52	40
	SWO	Serial wire viewer output pin	65	B8	53	41
	TCK	J-TAG test clock input pin	62	B9	50	38
	TDI	J-TAG test data input pin	63	B11	51	39
	TDO	J-TAG debug data output pin	65	B8	53	41
	TMS	J-TAG test mode state input/output pin	64	A9	52	40
TRSTX	J-TAG test reset input pin	61	A10	49	37	



Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
External Interrupt	INT00_0	External interrupt request 00 input pin	2	C1	2	2
	INT00_2		67	C8	54	-
	INT01_0	External interrupt request 01 input pin	3	C2	3	3
	INT02_0	External interrupt request 02 input pin	4	B3	4	4
	INT02_1		43	J10	35	26
	INT03_0	External interrupt request 03 input pin	73	B5	-	-
	INT03_1		46	H9	38	29
	INT03_2		9	E2	5	-
	INT04_0	External interrupt request 04 input pin	12	G2	8	-
	INT04_1		49	F10	40	-
	INT04_2		10	E3	6	-
	INT05_0	External interrupt request 05 input pin	60	P20	-	-
	INT05_1		55	E10	-	-
	INT05_2		11	G1	7	-
	INT06_0	External interrupt request 06 input pin	13	G3	9	5
	INT06_1		59	C11	48	36
	INT06_2		35	K8	27	-
	INT07_0	External interrupt request 07 input pin	14	H1	10	6
	INT07_2		5	D1	-	-
	INT08_2	External interrupt request 08 input pin	8	E1	-	-
	INT10_0	External interrupt request 10 input pin	21	L5	-	-
	INT11_0	External interrupt request 11 input pin	22	K5	-	-
	INT12_0	External interrupt request 12 input pin	33	K7	25	-
	INT13_0	External interrupt request 13 input pin	34	J7	26	-
	INT14_0	External interrupt request 14 input pin	47	G10	39	30
	INT14_1		29	J5	-	-
	INT15_0	External interrupt request 15 input pin	48	G9	-	-
	INT15_1		76	C4	60	44
	INT16_1	External interrupt request 16 input pin	78	A3	62	46
	INT17_1	External interrupt request 17 input pin	79	A2	63	47
	INT18_0	External interrupt request 18 input pin	68	C7	55	-
	INT18_1		6	D2	-	-
	INT18_2		16	H3	12	8
INT19_0	External interrupt request 19 input pin	59	C11	56	-	
INT19_1		7	D3	-	-	
INT19_2		18	J2	14	10	
INT20_0	External interrupt request 20 input pin	70	B6	-	-	
INT20_1		30	K6	22	18	
INT20_2		56	E9	-	-	
INT21_0	External interrupt request 21 input pin	71	C6	-	-	
INT21_1		31	J6	23	19	
INT22_1	External interrupt request 22 input pin	32	L7	24	-	
INT23_1	External interrupt request 23 input pin	66	A8	-	-	
NMIX	Non-Maskable Interrupt input pin	72	A6	57	42	

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
GPIO	P00	General-purpose I/O port 0	61	A10	49	37
	P01		62	B9	50	38
	P02		63	B11	51	39
	P03		64	A9	52	40
	P04		65	B8	53	41
	P07		66	A8	-	-
	P0A		67	C8	54	-
	P0B		68	C7	55	-
	P0C		69	B7	56	-
	P0D		70	B6	-	-
	P0E		71	C6	-	-
	P0F		72	A6	57	42
	P10	42	General-purpose I/O port 1	J11	34	25
	P11	43		J10	35	26
	P12	44		J8	36	27
	P14	46		H9	38	29
	P15	47		G10	39	30
	P16	48		G9	-	-
	P17	49		F10	40	-
	P18	53		F9	44	-
	P19	54		E11	45	-
	P1A	55		E10	-	-
	P1B	56	E9	-	-	
	P20	60	General-purpose I/O port 2	C10	-	-
	P21	59		C11	48	36
	P22	58		D9	47	35
	P23	57		D10	46	34
	P30	9	General-purpose I/O port 3	E2	5	-
	P31	10		E3	6	-
	P32	11		G1	7	-
	P33	12		G2	8	-
	P39	13		G3	9	5
	P3A	14		H1	10	6
	P3B	15		H2	11	7
	P3C	16		H3	12	8
	P3D	17		J1	13	9
P3E	18	J2		14	10	
P3F	19	J4	15	11		