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MB9B400A Series

32-bit Arm® Cortex®-M3 FM3 Microcontroller

The MB9B400A Series are a highly integrated 32-bit microcontroller that target for high-performance and cost-sensitive embedded control applications.
The MB9B400A Series are based on the Arm® Cortex®-M3 Processor and on-chip Flash memory and SRAM, and peripheral functions, including Motor Control Timers, ADCs and Communication Interfaces (CAN, UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE0 product categories in "FM3 Family Peripheral Manual".

Features

32-bit Arm® Cortex®-M3 Core

- Processor version: r2p0
- Up to 80 MHz Frequency Operation
- Memory Protection Unit (MPU): improve the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Up to 512 Kbyte
- Read cycle: 0wait-cycle@up to 60 MHz, 2wait-cycle* above
  *: Instruction pre-fetch buffer is included. So when CPU access continuously, it becomes 0wait-cycle
- Security function for code protection

[SRAM]

This series contain a total of up to 64 Kbyte on-chip SRAM. This is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 32 Kbyte
- SRAM1: Up to 32 Kbyte

CAN Interface (Max. 2 channels)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Multi-function Serial Interface (Max. 8 channels)

- 4 channels with 16steps × 9bit FIFO (ch.4-ch.7), 4 channels without FIFO (ch.0-ch.3)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I²C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control: Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13-16bit length)
- LIN break delimiter generate (can be changed 1-4bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I²C]

- Standard-mode (Max.100 kbps) / Fast-mode (Max.400 kbps) supported

External Bus Interface

- Supports SRAM, NOR& NAND Flash device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 Mbytes

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32 bit(4 Gbyte)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max. 16 channels)

[12-bit A/D Converter]

- Successive Approximation Register type
- Built-in 3 unit
- Conversion time: 1.0 µs@5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

Base Timer (Max. 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

Multi-function Timer (Max. 2 units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 3 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max. 2 units)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (Two 32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from sleep mode.

- Interval timer: up to 64 s (Max)@ Sub Clock: 32.768 kHz

Watch dog Timer (2 channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, "Hardware" watchdog is active in any low-power consumption modes except STOP mode.

External Interrupt Controller Unit

- Up to 16 external vectors
- Include one non-maskable interrupt (NMI)

General Purpose I/O Port
This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O Ports@120pin Package

CRC (Cyclic Redundancy Check) Accelerator
The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]
Five clock sources (2 ext. osc, 2 CR osc, and Main PLL) that are dynamically selectable.

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in high-speed CR Clock: 4 MHz
- Built-in low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pins
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock supervisor reset

Clock Super Visor (CSV)
Clocks generated by CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low Voltage Detector (LVD)
This series include 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage has been set, Low Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode
Three low-power consumption modes supported.

- SLEEP
- TIMER
- STOP

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Power Supply

- VCC = 2.7 V to 5.5 V: Correspond to the wide range voltage.

Contents

1. Product Lineup

Memory size

Product device	MB9BF404NA/RA	MB9BF405NA/RA	MB9BF406NA/RA
On-chip Flash memory	256 Kbyte	384 Kbyte	512 Kbyte
On-chip SRAM	32 Kbyte	48 Kbyte	64 Kbyte

Function

Product device			MB9BF404NA MB9BF405NA MB9BF406NA	MB9BF404RA MB9BF405RA MB9BF406RA
Pin count			100	120
CPU			Cortex-M3	
	Freq.		80 MHz	
Power supply voltage range			2.7 V to 5.5 V	
CAN Interface			2 ch(Max)	
DMAC			8 ch	
External Bus Interface			Addr: 25-bit (Max.) Data: 8-/16-bit CS: 5(Max.) Support: SRAM, NOR Flash	Addr: 25-bit (Max.) Data: 8-/16-bit CS: 8(Max.) Support: SRAM, NOR & NAND Flash
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8 ch (Max.)	
Base Timer (PWC/ Reload timer/PWM/PPG)			8 ch (Max.)	
MF-Timer	A/D activation compare	3 ch.	2 units (Max.)	
	Input capture	4 ch.		
	Free-run timer	3 ch.		
	Output compare	6 ch.		
	Waveform generator	3 ch.		
	PPG	3 ch.		
QPRC			2 ch (Max.)	
Dual Timer			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1 ch(SW) + 1 ch(HW)	
External Interrupts			16 pins (Max.)+ NMI × 1	
I/O ports			80 pins (Max.)	100 pins (Max.)
12-bit A/D converter			16 ch (3 units)	
CSV (Clock Super Visor)			Yes	
LVD (Low Voltage Detector)			2 ch	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP/ETM	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use.*
  See "Electrical Characteristics 12.4 AC Characteristics (12.4.3) Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

2. Packages

Package / Product name	MB9BF404NA MB9BF405NA MB9BF406NA	MB9BF404RA MB9BF405RA MB9BF406RA
LQFP: LQI100 (0.5 mm pitch)	❍	-
LQFP: LQM120 (0.5 mm pitch)	-	❍
BGA: LBC112 (0.8 mm pitch)	❍	-

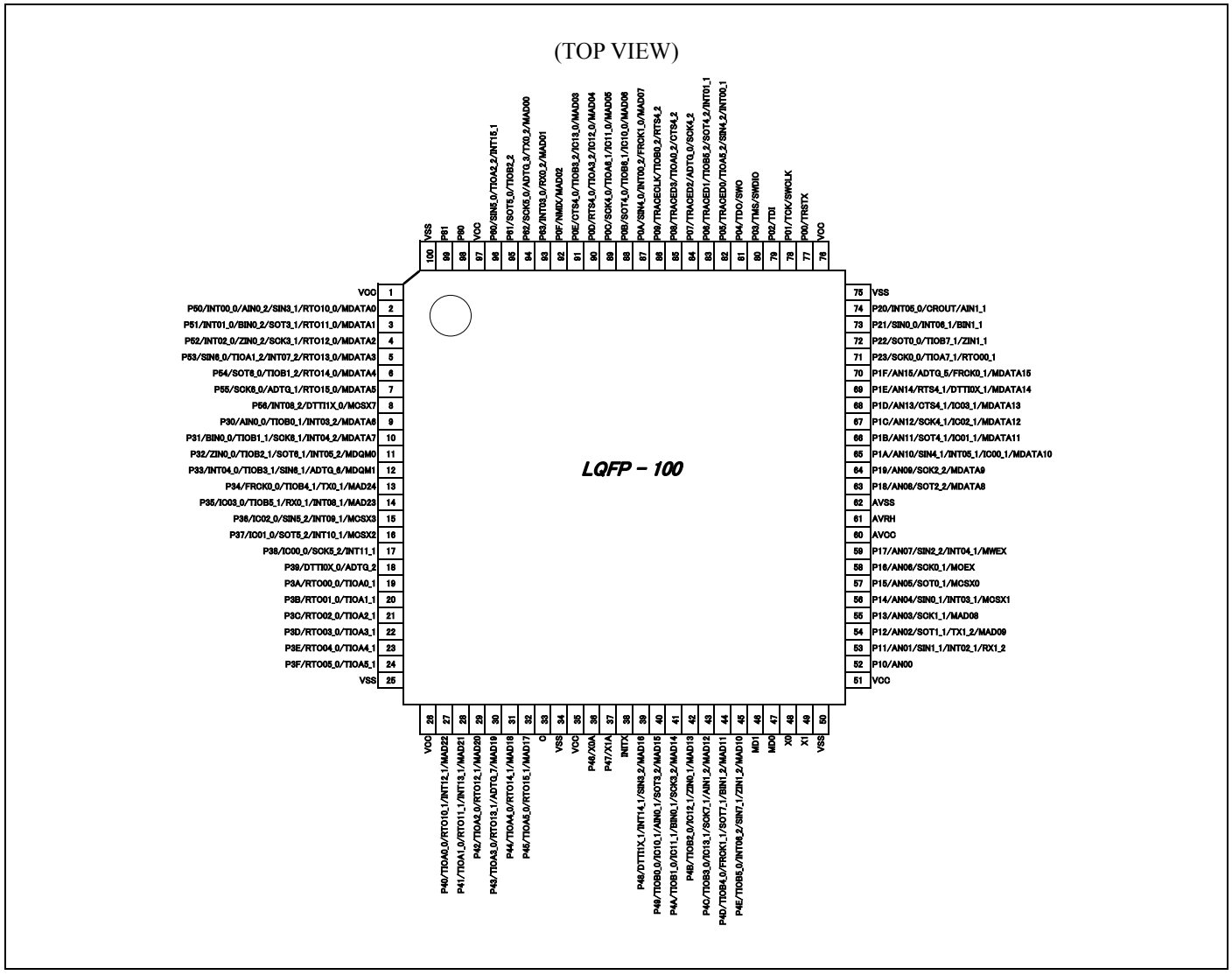
❍: Supported

Note:

- *Refer to "Package Dimensions" for detailed information on each package.*

3. Pin Assignment

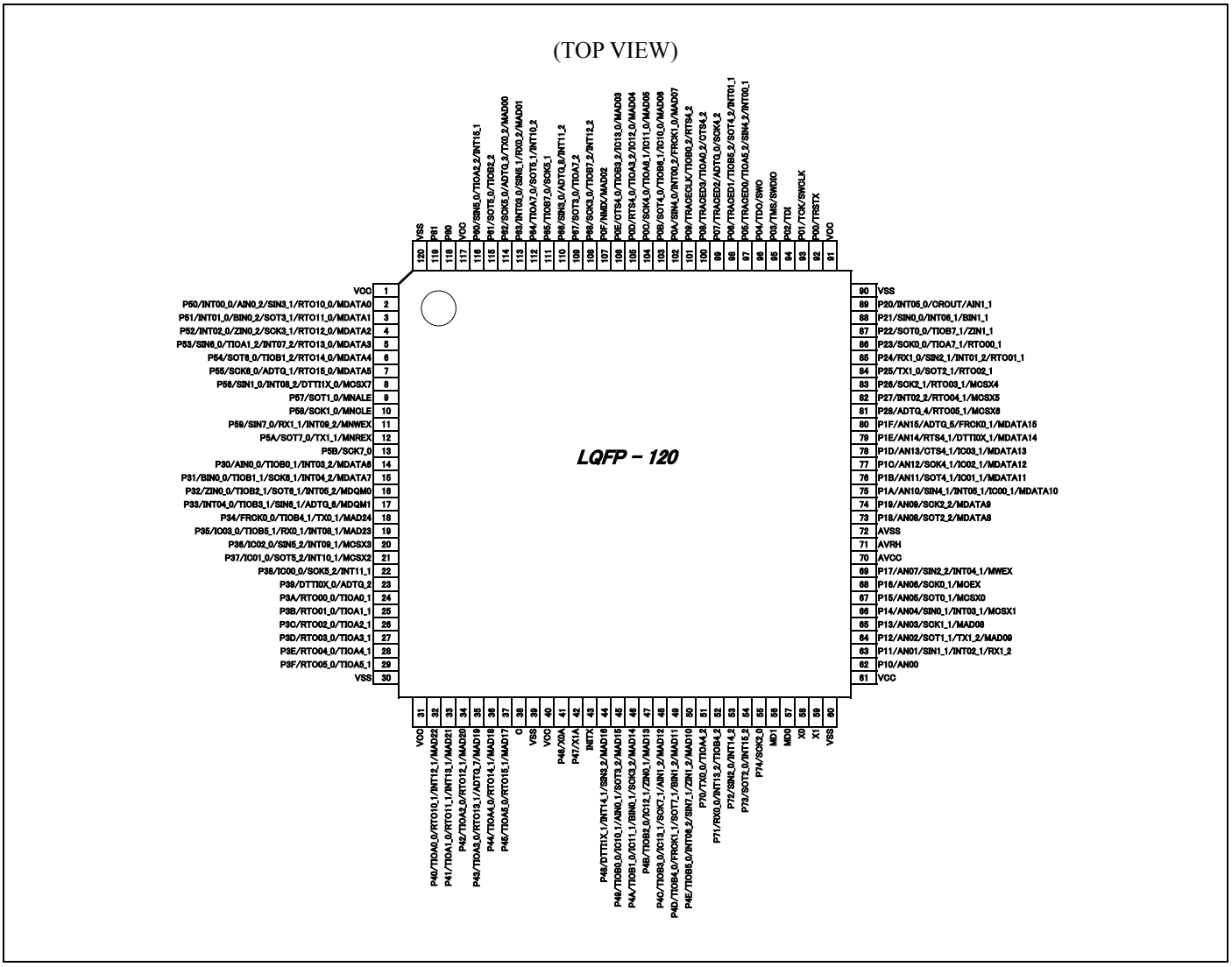
LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

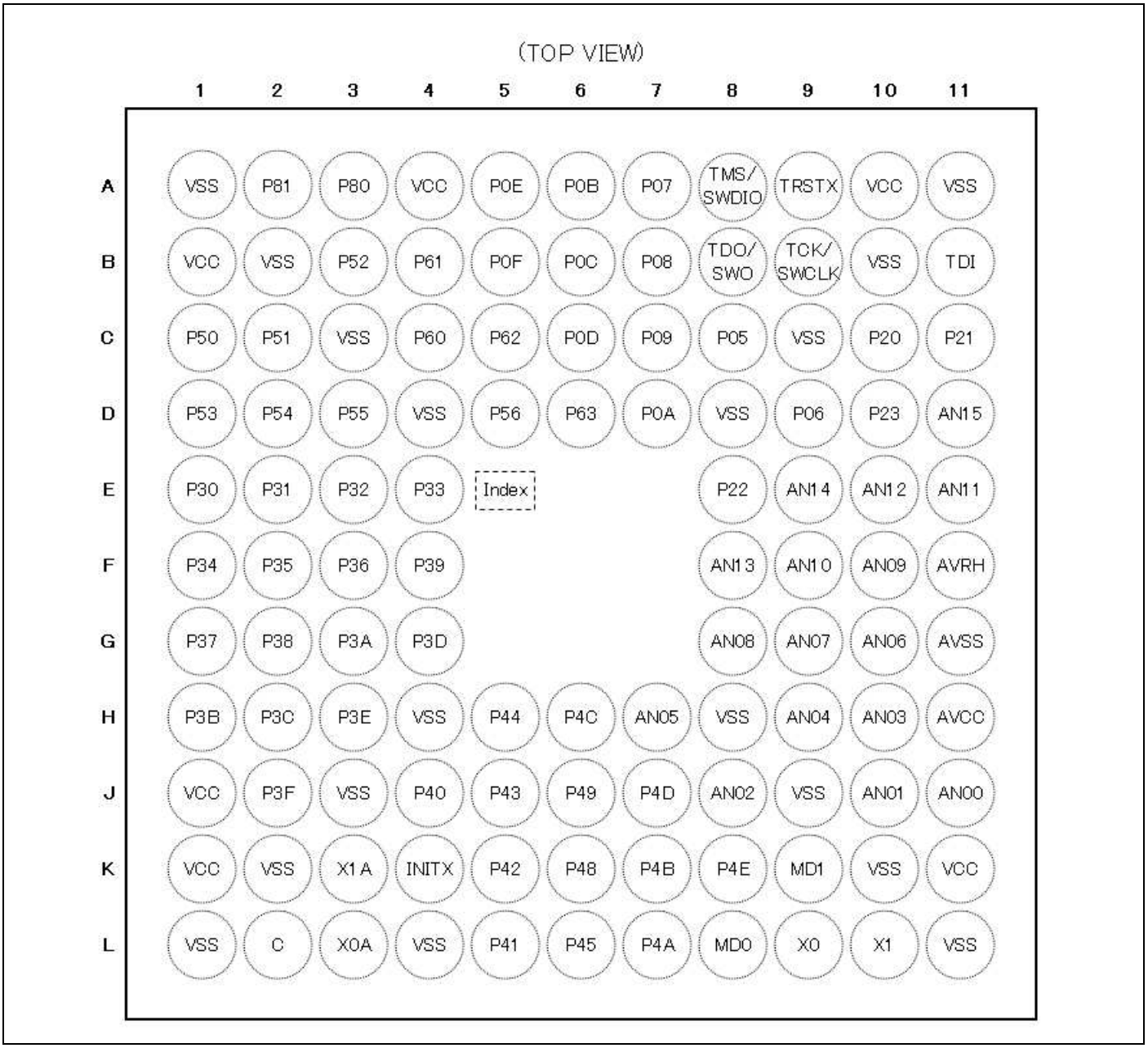
LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LBC112



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
1	B1	1	VCC	-	
2	C1	2	P50 INT00_0 AIN0_2 SIN3_1 RTO10_0 (PPG10_0) MDATA0	E	H
3	C2	3	P51 INT01_0 BIN0_2 SOT3_1 (SDA3_1) RTO11_0 (PPG10_0) MDATA1	E	H
4	B3	4	P52 INT02_0 ZIN0_2 SCK3_1 (SCL3_1) RTO12_0 (PPG12_0) MDATA2	E	H
5	D1	5	P53 SIN6_0 TIOA1_2 INT07_2 RTO13_0 (PPG12_0) MDATA3	E	H
6	D2	6	P54 SOT6_0 (SDA6_0) TIOB1_2 RTO14_0 (PPG14_0) MDATA4	E	I

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
7	D3	7	P55 SCK6_0 (SCL6_0) ADTG_1 RTO15_0 (PPG14_0) MDATA5	E	I
8	D5	8	P56 SIN1_0 (120pin only) INT08_2 DTTI1X_0 MCSX7	E	H
-	-	9	P57 SOT1_0 (SDA1_0) MNALE	E	I
-	-	10	P58 SCK1_0 (SCL1_0) MNCLE	E	I
-	-	11	P59 SIN7_0 RX1_1 INT09_2 MNWEX	E	H
-	-	12	P5A SOT7_0 (SDA7_0) TX1_1 MNREX	E	I
-	-	13	P5B SCK7_0 (SCL7_0)	E	I
9	E1	14	P30 AIN0_0 TIOB0_1 INT03_2 MDATA6	E	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
10	E2	15	P31 BIN0_0 TIOB1_1 SCK6_1 (SCL6_1) INT04_2 MDATA7	E	H
11	E3	16	P32 ZIN0_0 TIOB2_1 SOT6_1 (SDA6_1) INT05_2 MDQM0	E	H
12	E4	17	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6 MDQM1	E	H
13	F1	18	P34 FRCK0_0 TIOB4_1 TX0_1 MAD24	E	I
14	F2	19	P35 IC03_0 TIOB5_1 RX0_1 INT08_1 MAD23	E	H
15	F3	20	P36 IC02_0 SIN5_2 INT09_1 MCSX3	E	H
16	G1	21	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1 MCSX2	E	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
17	G2	22	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	H
18	F4	23	P39 DTTI0X_0 ADTG_2	E	I
19	G3	24	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
-	B2	-	VSS	-	
20	H1	25	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	H2	26	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	G4	27	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
23	H3	28	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	J2	29	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	L1	30	VSS	-	
26	J1	31	VCC	-	
27	J4	32	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1 MAD22	G	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
28	L5	33	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 MAD21	G	H
29	K5	34	P42 TIOA2_0 RTO12_1 (PPG12_1) MAD20	G	I
30	J5	35	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7 MAD19	G	I
-	K2	-	VSS	-	
-	J3	-	VSS	-	
-	H4	-	VSS	-	
31	H5	36	P44 TIOA4_0 RTO14_1 (PPG14_1) MAD18	G	I
32	L6	37	P45 TIOA5_0 RTO15_1 (PPG14_1) MAD17	G	I
33	L2	38	C	-	
34	L4	39	VSS	-	
35	K1	40	VCC	-	
36	L3	41	P46 X0A	D	M
37	K3	42	P47 X1A	D	N
38	K4	43	INITX	B	C
39	K6	44	P48 DTTI1X_1 INT14_1 SIN3_2 MAD16	E	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
40	J6	45	P49 TIOB0_0 IC10_1 AIN0_1 SOT3_2 (SDA3_2) MAD15	E	I
41	L7	46	P4A TIOB1_0 IC11_1 BIN0_1 SCK3_2 (SCL3_2) MAD14	E	I
42	K7	47	P4B TIOB2_0 IC12_1 ZIN0_1 MAD13	E	I
43	H6	48	P4C TIOB3_0 IC13_1 SCK7_1 (SCL7_1) AIN1_2 MAD12	E	I
44	J7	49	P4D TIOB4_0 FRCK1_1 SOT7_1 (SDA7_1) BIN1_2 MAD11	E	I
45	K8	50	P4E TIOB5_0 INT06_2 SIN7_1 ZIN1_2 MAD10	E	H
-	-	51	P70 TX0_0 TIOA4_2	E	I

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
-	-	52	P71 RX0_0 INT13_2 TIOB4_2	E	H
-	-	53	P72 SIN2_0 INT14_2	E	H
-	-	54	P73 SOT2_0 (SDA2_0) INT15_2	E	H
-	-	55	P74 SCK2_0 (SCL2_0)	E	I
46	K9	56	MD1	C	D
47	L8	57	MD0	C	D
48	L9	58	X0	A	A
49	L10	59	X1	A	B
50	L11	60	VSS	-	
51	K11	61	VCC	-	
52	J11	62	P10 AN00	F	K
53	J10	63	P11 AN01 SIN1_1 INT02_1 RX1_2	F	L
-	K10	-	VSS	-	
-	J9	-	VSS	-	
54	J8	64	P12 AN02 SOT1_1 (SDA1_1) TX1_2 MAD09	F	K
55	H10	65	P13 AN03 SCK1_1 (SCL1_1) MAD08	F	K

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
56	H9	66	P14 AN04 SIN0_1 INT03_1 MCSX1	F	L
57	H7	67	P15 AN05 SOT0_1 (SDA0_1) MCSX0	F	K
58	G10	68	P16 AN06 SCK0_1 (SCL0_1) MOEX	F	K
59	G9	69	P17 AN07 SIN2_2 INT04_1 MWEX	F	L
60	H11	70	AVCC	-	
61	F11	71	AVRH	-	
62	G11	72	AVSS	-	
63	G8	73	P18 AN08 SOT2_2 (SDA2_2) MDATA8	F	K
64	F10	74	P19 AN09 SCK2_2 (SCL2_2) MDATA9	F	K
65	F9	75	P1A AN10 SIN4_1 INT05_1 IC00_1 MDATA10	F	L
-	H8	-	VSS	-	

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
66	E11	76	P1B AN11 SOT4_1 (SDA4_1) IC01_1 MDATA11	F	K
67	E10	77	P1C AN12 SCK4_1 (SCL4_1) IC02_1 MDATA12	F	K
68	F8	78	P1D AN13 CTS4_1 IC03_1 MDATA13	F	K
69	E9	79	P1E AN14 RTS4_1 DTTI0X_1 MDATA14	F	K
70	D11	80	P1F AN15 ADTG_5 FRCK0_1 MDATA15	F	K
-	-	81	P28 ADTG_4 RTO05_1 (PPG04_1) MCSX6	E	I
-	-	82	P27 INT02_2 RTO04_1 (PPG04_1) MCSX5	E	H
-	-	83	P26 SCK2_1 (SCL2_1) RTO03_1 (PPG02_1) MCSX4	E	I

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
-	-	84	P25 TX1_0 SOT2_1 (SDA2_1) RTO02_1 (PPG02_1)	E	I
-	B10	-	VSS	-	
-	C9	-	VSS	-	
-	-	85	P24 RX1_0 SIN2_1 INT01_2 RTO01_1 (PPG00_1)	E	H
71	D10	86	P23 SCK0_0 (SCL0_0) TIOA7_1 RTO00_1 (PPG00_1)	E	I
72	E8	87	P22 SOT0_0 (SDA0_0) TIOB7_1 ZIN1_1	E	I
73	C11	88	P21 SIN0_0 INT06_1 BIN1_1	E	H
74	C10	89	P20 INT05_0 CROUT AIN1_1	E	H
75	A11	90	VSS	-	
76	A10	91	VCC	-	
77	A9	92	P00 TRSTX	E	E
78	B9	93	P01 TCK SWCLK	E	E
79	B11	94	P02 TDI	E	E

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
80	A8	95	P03 TMS SWDIO	E	E
81	B8	96	P04 TDO SWO	E	E
82	C8	97	P05 TRACED0 TIOA5_2 SIN4_2 INT00_1	E	F
-	D8	-	VSS	-	
83	D9	98	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1	E	F
84	A7	99	P07 TRACED2 ADTG_0 SCK4_2 (SCL4_2)	E	G
85	B7	100	P08 TRACED3 TIOA0_2 CTS4_2	E	G
86	C7	101	P09 TRACECLK TIOB0_2 RTS4_2	E	G
87	D7	102	P0A SIN4_0 INT00_2 FRCK1_0 MAD07	E	H
88	A6	103	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 MAD06	E	I

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
89	B6	104	P0C SCK4_0 (SCL4_0) TIOA6_1 IC11_0 MAD05	E	I
90	C6	105	P0D RTS4_0 TIOA3_2 IC12_0 MAD04	E	I
91	A5	106	P0E CTS4_0 TIOB3_2 IC13_0 MAD03	E	I
-	D4	-	VSS	-	
-	C3	-	VSS	-	
92	B5	107	P0F NMIX MAD02	E	J
-	-	108	P68 SCK3_0 (SCL3_0) TIOB7_2 INT12_2	E	H
-	-	109	P67 SOT3_0 (SDA3_0) TIOA7_2	E	I
-	-	110	P66 SIN3_0 ADTG_8 INT11_2	E	H
-	-	111	P65 TIOB7_0 SCK5_1 (SCL5_1)	E	I
-	-	112	P64 TIOA7_0 SOT5_1 (SDA5_1) INT10_2	E	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
93	D6	113	P63	E	H
			INT03_0		
			RX0_2		
			MAD01		
-	-		SIN5_1		
94	C5	114	P62	E	I
			SCK5_0 (SCL5_0)		
			ADTG_3		
			TX0_2		
			MAD00		
95	B4	115	P61	E	I
			SOT5_0 (SDA5_0)		
			TIOB2_2		
96	C4	116	P60	E	H
			SIN5_0		
			TIOA2_2		
			INT15_1		
97	A4	117	VCC	-	
98	A3	118	P80	H	O
99	A2	119	P81	H	O
100	A1	120	VSS	-	

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
ADC	ADTG_0	A/D converter external trigger input pin.	84	A7	99
	ADTG_1		7	D3	7
	ADTG_2		18	F4	23
	ADTG_3		94	C5	114
	ADTG_4		-	-	81
	ADTG_5		70	D11	80
	ADTG_6		12	E4	17
	ADTG_7		30	J5	35
	ADTG_8		-	-	110
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	J11	62
	AN01		53	J10	63
	AN02		54	J8	64
	AN03		55	H10	65
	AN04		56	H9	66
	AN05		57	H7	67
	AN06		58	G10	68
	AN07		59	G9	69
	AN08		63	G8	73
	AN09		64	F10	74
	AN10		65	F9	75
	AN11		66	E11	76
	AN12		67	E10	77
	AN13		68	F8	78
	AN14		69	E9	79
	AN15		70	D11	80
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin.	27	J4	32
	TIOA0_1		19	G3	24
	TIOA0_2		85	B7	100
	TIOB0_0	Base timer ch.0 TIOB pin.	40	J6	45
	TIOB0_1		9	E1	14
	TIOB0_2		86	C7	101
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin.	28	L5	33
	TIOA1_1		20	H1	25
	TIOA1_2		5	D1	5
	TIOB1_0	Base timer ch.1 TIOB pin.	41	L7	46
	TIOB1_1		10	E2	15
	TIOB1_2		6	D2	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin.	29	K5	34
	TIOA2_1		21	H2	26
	TIOA2_2		96	C4	116
	TIOB2_0	Base timer ch.2 TIOB pin.	42	K7	47
	TIOB2_1		11	E3	16
	TIOB2_2		95	B4	115