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MB9B560R Series

32-bit ARM® Cortex®-M4F FM4 Microcontroller

Devices in the MB9B560R Series are highly integrated 32-bit microcontrollers with high performance and competitive cost.

This series is based on the ARM® Cortex®-M4F Processor with on-chip Flash memory and SRAM. The series has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (USB, CAN, UART, CSIO, I²C, LIN).

Features

32-bit ARM® Cortex®-M4F Core

- Processor version: r0p1
- Up to 160 MHz Frequency Operation
- FPU built-in
- Support DSP instruction
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

These series are based on two independent on-chip Flash memories.

- MainFlash memory
  - Up to 1024 Kbytes
  - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
  - The read access to Flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
  - Security function for code protection
- WorkFlash memory
  - 32 Kbytes
  - Read cycle:
    - 6wait-cycle: the operation frequency more than 120 MHz, and up to 160 MHz
    - 4wait-cycle: the operation frequency more than 72 MHz, and up to 120 MHz
    - 2wait-cycle: the operation frequency more than 40 MHz, and up to 72 MHz
    - 0wait-cycle: the operation frequency up to 40 MHz
  - Security function is shared with code protection

[SRAM]

This is composed of three independent SRAMs (SRAM0, SRAM1, and SRAM2). SRAM0 is connected to I-code bus and D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to System bus of Cortex-M4F core.

- SRAM0: Up to 64 Kbytes
- SRAM1: Up to 32 Kbytes
- SRAM2: Up to 32 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND Flash, and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum Access size: 256M byte
- Supports Address/Data multiplex
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note**: It is necessary to prepare the dedicated software library to use the scramble function.

USB Interface

USB interface is composed of Device and Host.

[USB device]

- USB2.0 Full-Speed supported
- Max 6 Endpoint supported
  - Endpoint 0 is control transfer
  - Endpoint 1, 2 can be selected Bulk-transfer, Interrupt-transfer or Isochronous-transfer
  - Endpoint 3 to 5 can select Bulk-transfer or Interrupt-transfer
  - Endpoint 1 to 5 comprise Double Buffer
  - The size of each endpoint is according to the follows.
    - Endpoint 0, 2 to 5: 64 bytes
    - Endpoint 1: 256 bytes

[USB host]

- USB2.0 Full/Low-speed supported
- Bulk-transfer, interrupt-transfer and Isochronous-transfer support
- USB Device connected/dis-connected automatically detect
- IN/OUT token handshake packet automatically
- Max 256-byte packet-length supported
- Wake-up function supported

CAN Interface (Max two channels)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Multi-function Serial Interface (Max eight channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)
  - Supports high-speed SPI (ch.4 and ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported
  - Fast-mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported

DMA Controller (Eight channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 24 channels) [12-bit A/D Converter]

- Successive Approximation type
- Built-in 3 units
- Conversion time: 0.5 µs @ 5 V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

D/A Converter (Max two channels)

- R-2R type
- 12-bit resolution

Base Timer (Max eight channels)
Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port
This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O ports @ 120 pin Package
- Some pin is 5 V tolerant I/O.

See 4. Pin Description and 5. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max two units)
The Multi-function timer is composed of the following blocks.

Minimum resolution: 6.25 ns

- 16-bit free-run timer × 3 ch./unit
- Input capture × 4 ch./unit
- Output compare × 6 ch./unit
- A/D activation compare × 6 ch./unit
- Waveform generator × 3 ch./unit
- 16-bit PPG timer × 3 ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)
The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (Max two channels)
The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN, and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)
The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter
The Watch counter is used for wake up from the low-power consumption mode. It is possible to select the main clock, sub clock, built-in high-speed CR clock or built-in low-speed CR clock as the clock source.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit
- External interrupt input pin: Max 16 pins
- Include one non-maskable interrupt (NMI)

Watchdog Timer (two channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP.

CRC (Cyclic Redundancy Check) Accelerator
The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

SD Card Interface
It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

Clock and Reset

- Clocks

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

  - Main clock: 4 MHz to 48 MHz
  - Sub Clock: 32.768 kHz
  - High-speed internal CR Clock: 4 MHz
  - Low-speed internal CR Clock: 100 kHz
  - Main PLL Clock

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timers reset
  - Low voltage detector reset
  - Clock supervisor reset

Clock Super Visor (CSV)
Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)
This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode
Six low-power consumption modes are supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

VBAT
The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Unique ID
Unique value of the device (41-bit) is set.

Power Supply
Three Power Supplies

- Wide range voltage:
  VCC = 2.7 V to 5.5 V
- Power supply for USB I/O:
  USBVCC = 3.0 V to 3.6 V (when USB is used)
  = 2.7 V to 5.5 V (when GPIO is used)
- Power supply for VBAT:
  VBAT = 2.7 V to 5.5 V

Contents

1. Product Lineup

Memory Size

Product name		MB9BF566M/N/R	MB9BF567M/N/R	MB9BF568M/N/R
MainFlash memory		512 Kbytes	768 Kbytes	1024 Kbytes
WorkFlash memory		32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM		64 Kbytes	96 Kbytes	128 Kbytes
	SRAM0	32 Kbytes	48 Kbytes	64 Kbytes
	SRAM1	16 Kbytes	24 Kbytes	32 Kbytes
	SRAM1	16 Kbytes	24 Kbytes	32 Kbytes

Function

Product name			MB9BF566M MB9BF567M MB9BF568M	MB9BF566N MB9BF567N MB9BF568N	MB9BF566R MB9BF567R MB9BF568R
Pin count			80	100/112	120/144
CPU			Cortex-M4F, MPU, NVIC 128ch.		
	Freq.		160 MHz		
Power supply voltage range			2.7 V to 5.5 V		
USB2.0 (Device/Host)			1ch.		
CAN			2ch. (Max)		
DMAC			8ch.		
DSTC			128ch.		
External Bus Interface			Addr:19-bit (Max), R/W data: 8-bit (Max), CS:5 (Max), SRAM, NOR Flash	Addr:25-bit (Max), R/W data: 8-/16-bit (Max), CS:9 (Max), SRAM, NOR Flash, SDRAM	Addr:25-bit (Max), R/W data: 8-/16-bit (Max), CS:9 (Max), SRAM, NOR Flash, NAND Flash, SDRAM
Multi-function Serial Interface (UART/CSIO/LIN/I²C)			8ch. (Max)		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF Timer	A/D activation compare	6ch.	2 units (Max)		
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
SD Card Interface			1 unit		
QPRC			2ch. (Max)		
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog Timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			16 pins (Max) + NMI × 1		
I/O Ports			63 pins (Max)	80 pins (Max)	100 pins (Max)
12-bit A/D Converter			16ch. (3 units)	24ch. (3 units)	
12-bit D/A Converter			2 units (Max)		
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SWJ-DP/ETM		
Unique ID			Yes		

Notes:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See "12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics" for accuracy of built-in CR.*

2. Packages

Product Name Package	MB9BF566M MB9BF567M MB9BF568M	MB9BF566N MB9BF567N MB9BF568N	MB9BF566R MB9BF567R MB9BF568R
LQFP: LQH080 (0.5 mm pitch)	○	-	-
LQFP: LQJ080 (0.65 mm pitch)	○	-	-
QFP: PQH100 (0.65 mm pitch)	-	○	-
LQFP: LQI100 (0.5 mm pitch)	-	○	-
LQFP: LQM120 (0.5 mm pitch)	-	-	○
BGA: LDC112 (0.5 mm pitch)	-	○	-
BGA: LDC144 (0.5 mm pitch)	-	-	○

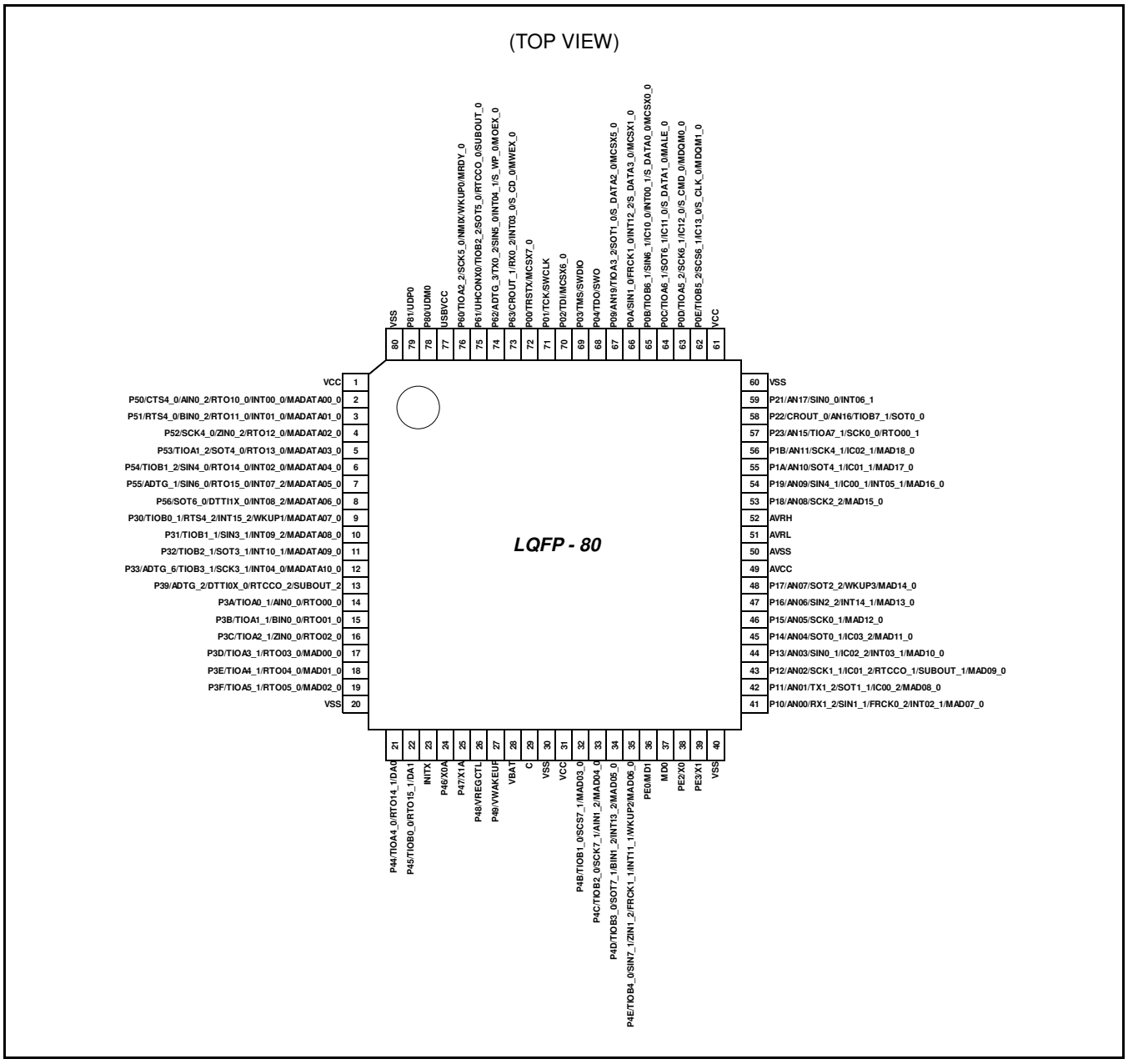
❍: Supported

Note:

- *See 14. Package Dimensions for detailed information on each package.*

3. Pin Assignment

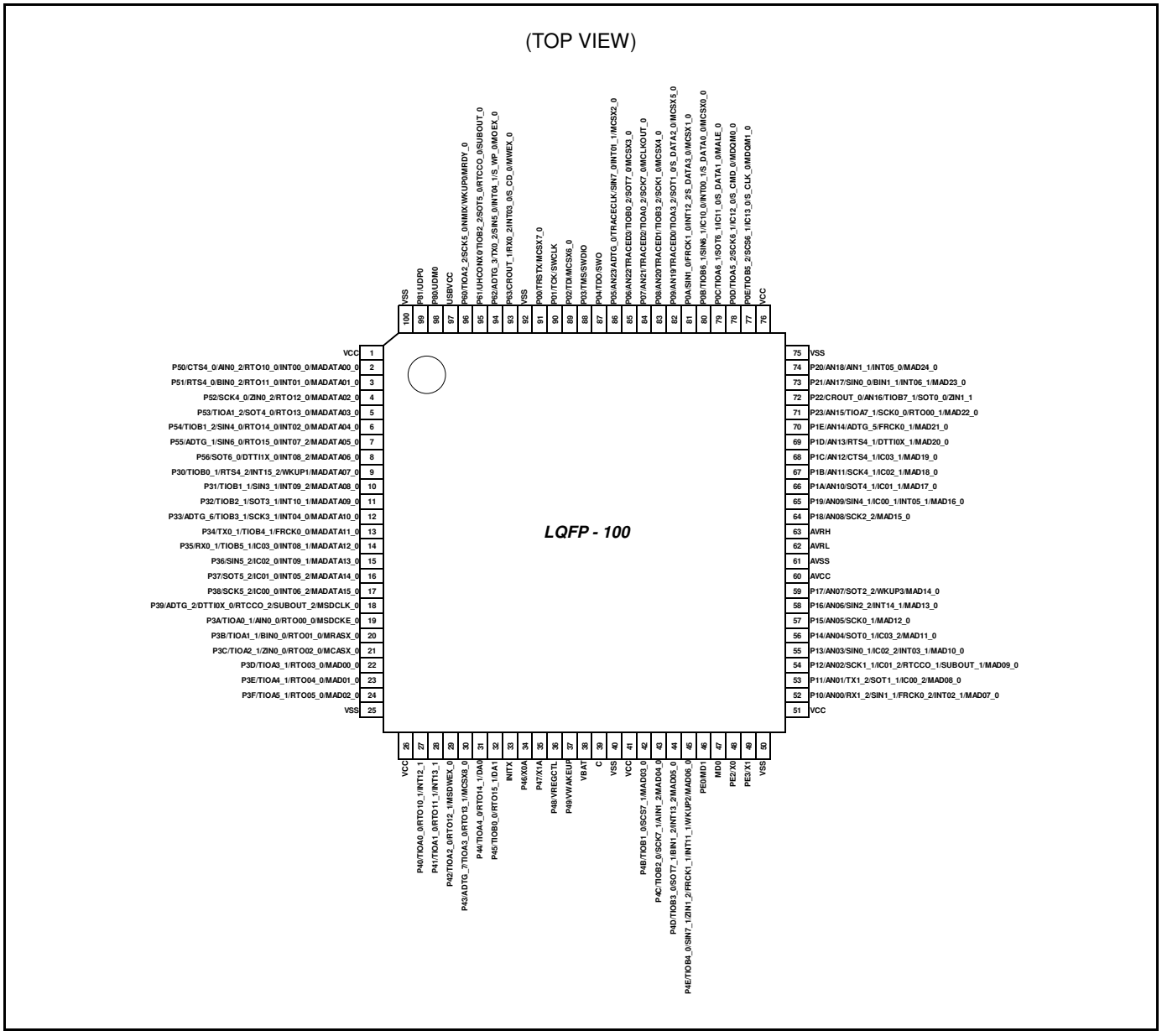
LQH080/LQJ080



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

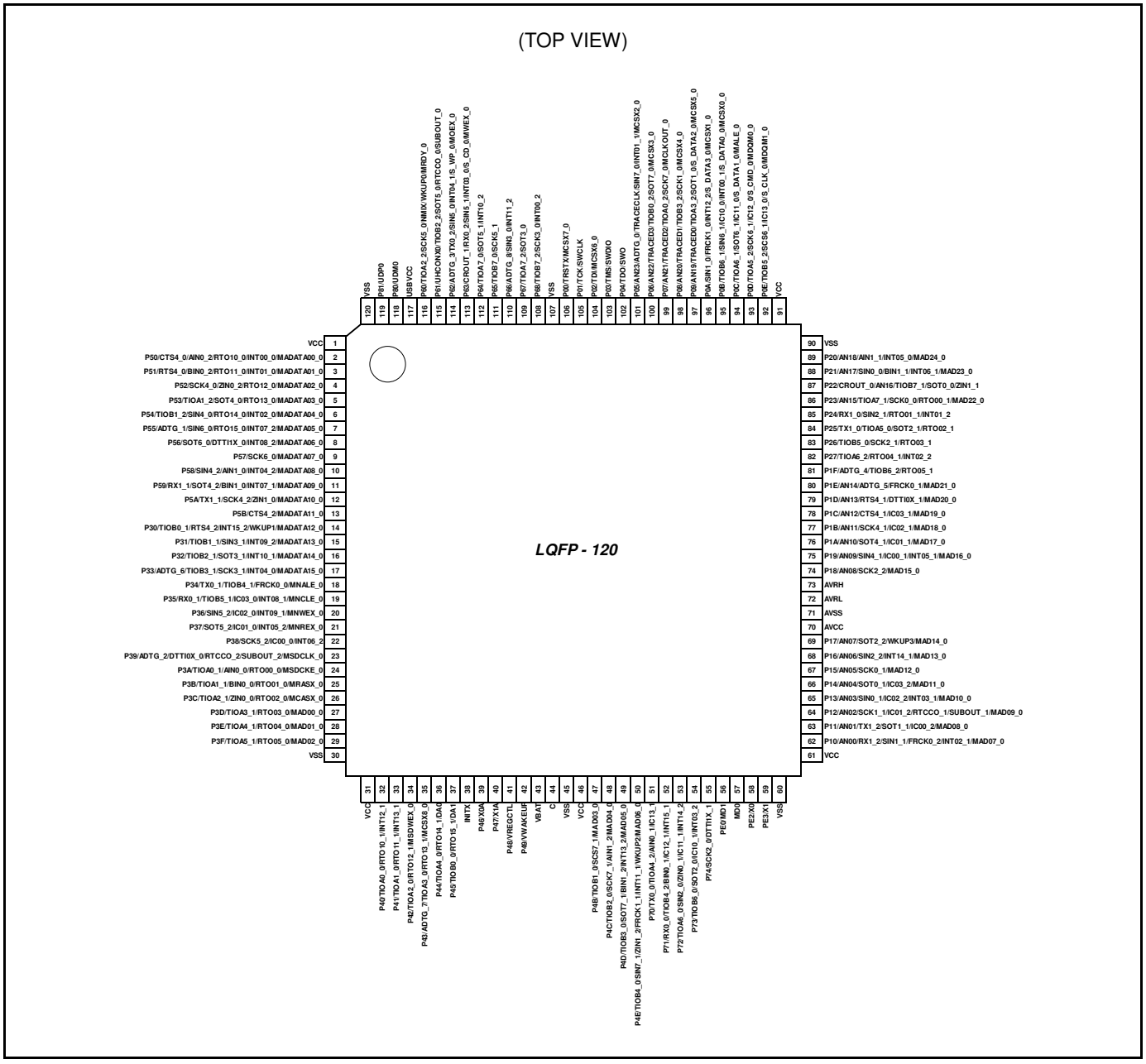
LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

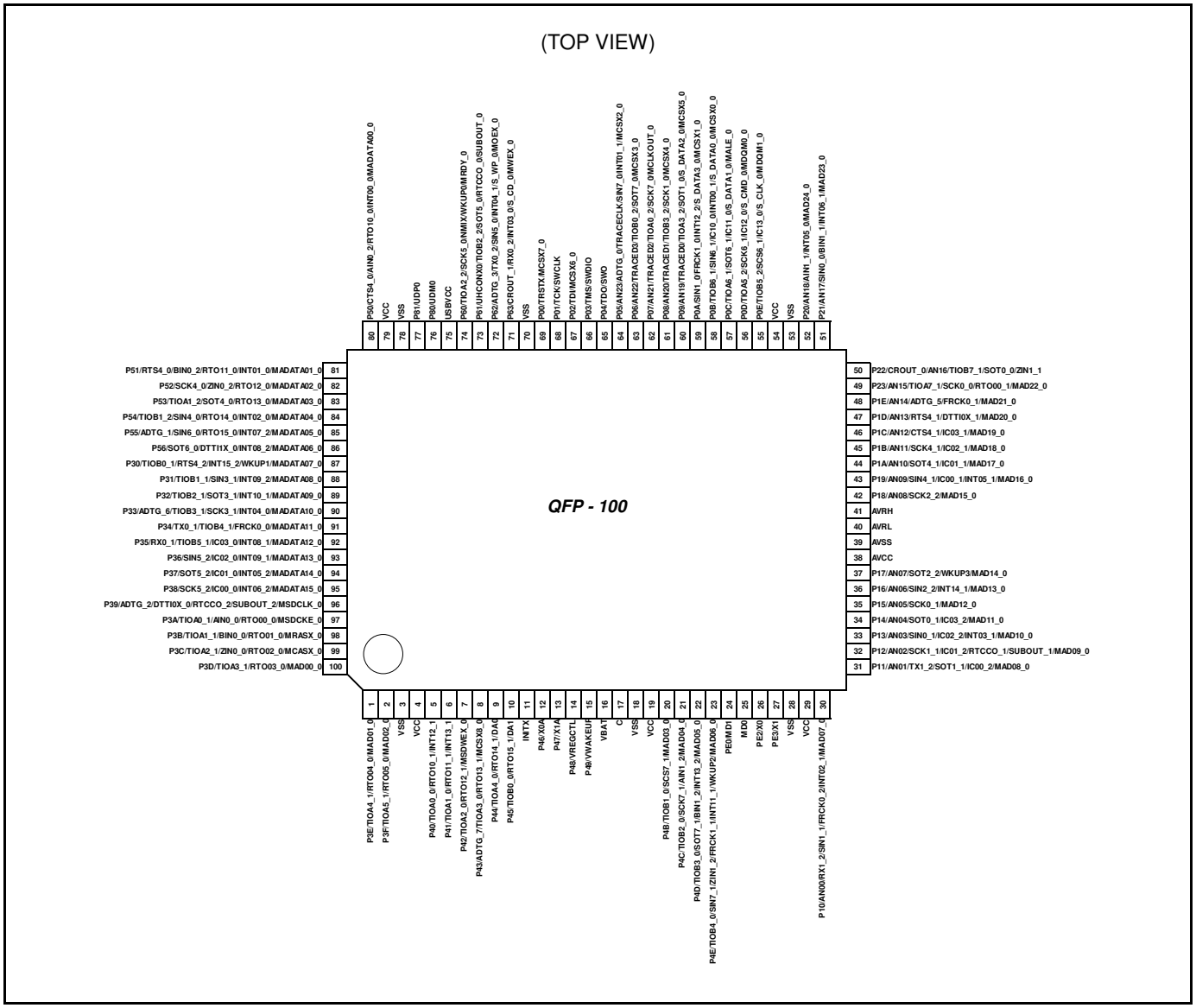
LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

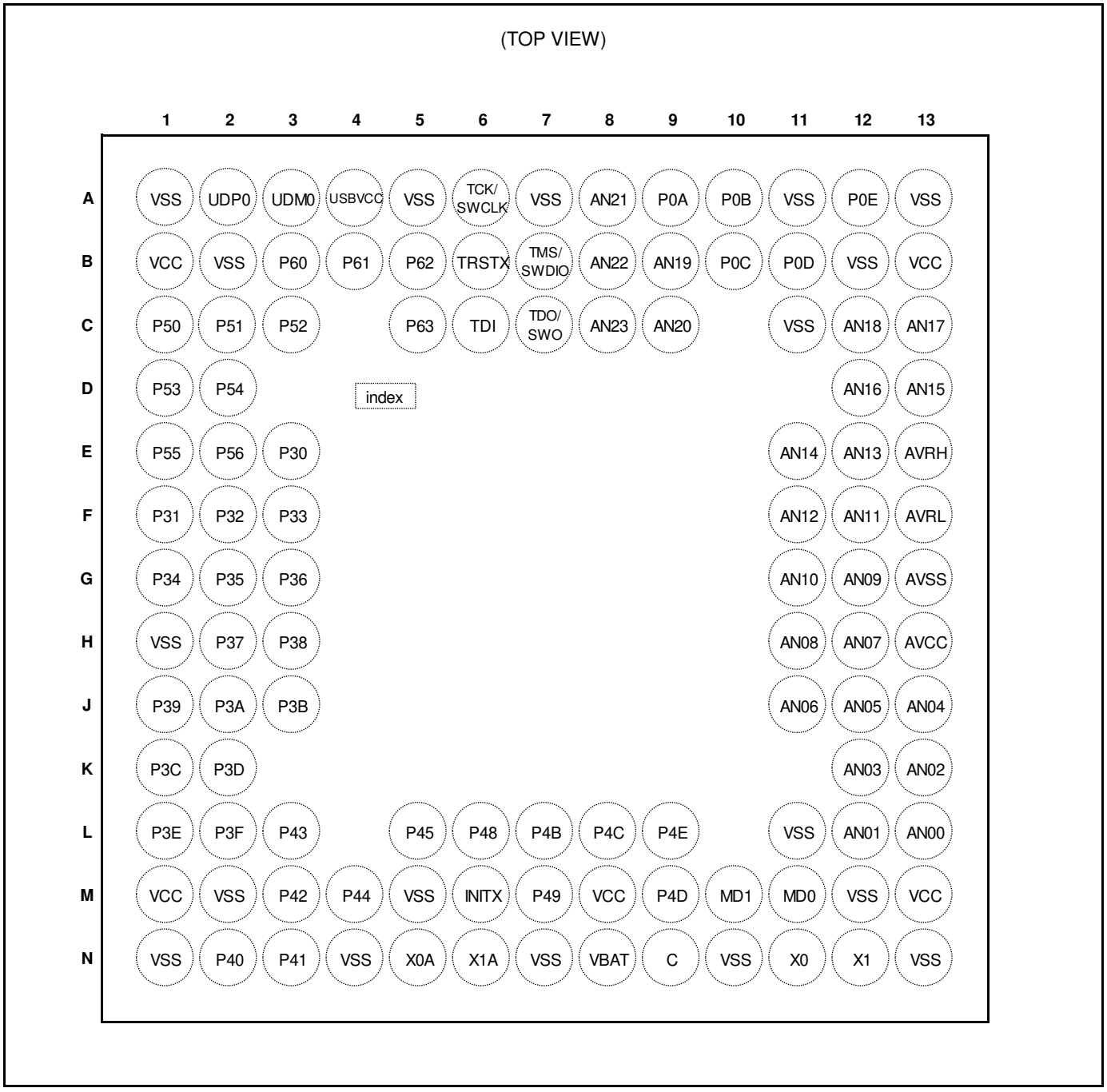
PQH100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

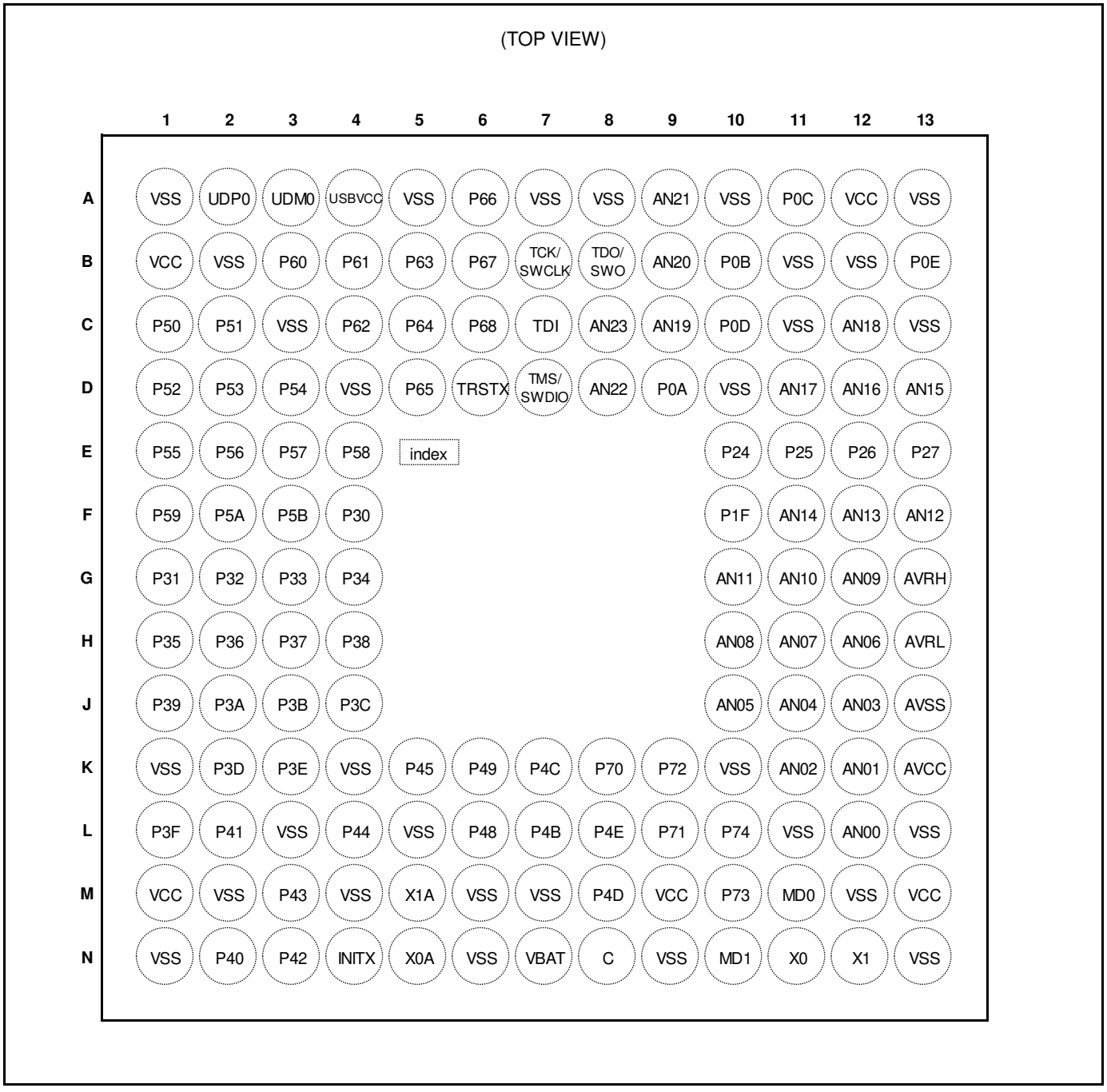
LDC112



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LDC144



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. Pin Description

4.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
1	1	1	79	B1	B1	VCC	-	-
2	2	2	80	C1	C1	P50 CTS4_0 AIN0_2 RTO10_0 (PPG10_0) INT00_0 MADATA00_0	E	K
3	3	3	81	C2	C2	P51 RTS4_0 BIN0_2 RTO11_0 (PPG10_0) INT01_0 MADATA01_0	E	K
4	4	4	82	C3	D1	P52 SCK4_0 (SCL4_0) ZIN0_2 RTO12_0 (PPG12_0) MADATA02_0	E	I
5	5	5	83	D1	D2	P53 TIOA1_2 SOT4_0 (SDA4_0) RTO13_0 (PPG12_0) MADATA03_0	E	I
6	6	6	84	D2	D3	P54 TIOB1_2 SIN4_0 RTO14_0 (PPG14_0) INT02_0 MADATA04_0	E	K

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
7	7	7	85	E1	E1	P55 ADTG_1 SIN6_0 RTO15_0 (PPG14_0) INT07_2 MADATA05_0	E	K
8	8	8	86	E2	E2	P56 SOT6_0 (SDA6_0) DTTI1X_0 INT08_2 MADATA06_0	E	K
9	-	-	-	-	E3	P57 SCK6_0 (SCL6_0) MADATA07_0	E	I
10	-	-	-	-	E4	P58 SIN4_2 AIN1_0 INT04_2 MADATA08_0	E	K
11	-	-	-	-	F1	P59 RX1_1 SOT4_2 (SDA4_2) BIN1_0 INT07_1 MADATA09_0	E	K
12	-	-	-	-	F2	P5A TX1_1 SCK4_2 (SCL4_2) ZIN1_0 MADATA10_0	E	I
13	-	-	-	-	F3	P5B CTS4_2 MADATA11_0	E	I
14	9	9	87	E3	F4	P30 TIOB0_1 RTS4_2 INT15_2 WKUP1	E	Q
-					-	MADATA07_0		
14	-	-	-	-	F4	MADATA12_0		

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
15	10	10	88	F1	G1	P31 TIOB1_1 SIN3_1 INT09_2	I	K
-					-	MADATA08_0		
15	-	-	-	-	G1	MADATA13_0		
16	11	11	89	F2	G2	P32 TIOB2_1 SOT3_1 (SDA3_1) INT10_1	N	K
-					-	MADATA09_0		
16	-	-	-	-	G2	MADATA14_0		
17	12	12	90	F3	G3	P33 ADTG_6 TIOB3_1 SCK3_1 (SCL3_1) INT04_0	N	K
-					-	MADATA10_0		
17	-	-	-	-	G3	MADATA15_0		
18	13	-	91	G1	G4	P34 TX0_1 TIOB4_1 FRCK0_0	E	I
-					-	MADATA11_0		
18	-	-	-	-	G4	MNALE_0		
19	14	-	92	G2	H1	P35 RX0_1 TIOB5_1 IC03_0 INT08_1	E	K
-					-	MADATA12_0		
19	-	-	-	-	H1	MNCLE_0		
20	15	-	93	G3	H2	P36 SIN5_2 IC02_0 INT09_1	E	K
-					-	MADATA13_0		
20	-	-	-	-	H2	MNWEX_0		
21	16	-	94	H2	H3	P37 SOT5_2 (SDA5_2) IC01_0 INT05_2	E	K
-					-	MADATA14_0		
21	-	-	-	-	H3	MNREX_0		

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
22	17	-	95	H3	H4	P38	E	K
						SCK5_2 (SCL5_2)		
						IC00_0		
						INT06_2		
-					-	MADATA15_0		
23	18	13	96	J1	J1	P39	L	I
						ADTG_2		
						DTTI0X_0		
						RTCCO_2		
						SUBOUT_2		
		-				MSDCLK_0		
24	19	14	97	J2	J2	P3A	G	I
						TIOA0_1		
						AIN0_0		
						RTO00_0 (PPG00_0)		
		-				MSDCKE_0		
25	20	15	98	J3	J3	P3B	G	I
						TIOA1_1		
						BIN0_0		
						RTO01_0 (PPG00_0)		
		-				MRASX_0		
26	21	16	99	K1	J4	P3C	G	I
						TIOA2_1		
						ZIN0_0		
						RTO02_0 (PPG02_0)		
		-				MCASX_0		
27	22	17	100	K2	K2	P3D	G	I
						TIOA3_1		
						RTO03_0 (PPG02_0)		
						MAD00_0		
28	23	18	1	L1	K3	P3E	G	I
						TIOA4_1		
						RTO04_0 (PPG04_0)		
						MAD01_0		
29	24	19	2	L2	L1	P3F	G	I
						TIOA5_1		
						RTO05_0 (PPG04_0)		
						MAD02_0		
30	25	20	3	N1	N1	VSS	-	-
31	26	-	4	M1	M1	VCC	-	-

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
32	27	-	5	N2	N2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	6	N3	L2	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1	G	K
34	29	-	7	M3	N3	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0	G	I
35	30	-	8	L3	M3	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0	G	I
36	31	21	9	M4	L4	P44 TIOA4_0 RTO14_1 (PPG14_1) DA0	R	J
37	32	22	10	L5	K5	P45 TIOB0_0 RTO15_1 (PPG14_1) DA1	R	J
38	33	23	11	M6	N4	INITX	B	C
39	34	24	12	N5	N5	P46 X0A	P	S
40	35	25	13	N6	M5	P47 X1A	Q	T
41	36	26	14	L6	L6	P48 VREGCTL	O	U
42	37	27	15	M7	K6	P49 VWAKEUP	O	U
43	38	28	16	N8	N7	VBAT	-	-
44	39	29	17	N9	N8	C	-	-
45	40	30	18	N10	N9	VSS	-	-
46	41	31	19	M8	M9	VCC	-	-
47	42	32	20	L7	L7	P4B TIOB1_0 SCS7_1 MAD03_0	E	I

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
48	43	33	21	L8	K7	P4C TIOB2_0 SCK7_1 (SCL7_1) AIN1_2 MAD04_0	N	I
49	44	34	22	M9	M8	P4D TIOB3_0 SOT7_1 (SDA7_1) BIN1_2 INT13_2 MAD05_0	N	K
50	45	35	23	L9	L8	P4E TIOB4_0 SIN7_1 ZIN1_2 FRCK1_1 INT11_1 WKUP2 MAD06_0	I	Q
51	-	-	-	-	K8	P70 TX0_0 TIOA4_2 AIN0_1 IC13_1	E	I
52	-	-	-	-	L9	P71 RX0_0 TIOB4_2 BIN0_1 IC12_1 INT15_1	E	K
53	-	-	-	-	K9	P72 TIOA6_0 SIN2_0 ZIN0_1 IC11_1 INT14_2	E	K
54	-	-	-	-	M10	P73 TIOB6_0 SOT2_0 (SDA2_0) IC10_1 INT03_2	E	K
55	-	-	-	-	L10	P74 SCK2_0 (SCL2_0) DTTI1X_1	E	I

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
56	46	36	24	M10	N10	PE0 MD1	C	E
57	47	37	25	M11	M11	MD0	J	D
58	48	38	26	N11	N11	PE2 X0	A	A
59	49	39	27	N12	N12	PE3 X1	A	B
60	50	40	28	N13	N13	VSS	-	-
61	51	-	29	M13	M13	VCC	-	-
62	52	41	30	L13	L12	P10 AN00 RX1_2 SIN1_1 FRCK0_2 INT02_1 MAD07_0	F	M
63	53	42	31	L12	K12	P11 AN01 TX1_2 SOT1_1 (SDA1_1) IC00_2 MAD08_0	F	L
64	54	43	32	K13	K11	P12 AN02 SCK1_1 (SCL1_1) IC01_2 RTCCO_1 SUBOUT_1 MAD09_0	F	L
65	55	44	33	K12	J12	P13 AN03 SIN0_1 IC02_2 INT03_1 MAD10_0	F	M
66	56	45	34	J13	J11	P14 AN04 SOT0_1 (SDA0_1) IC03_2 MAD11_0	F	L
67	57	46	35	J12	J10	P15 AN05 SCK0_1 (SCL0_1) MAD12_0	F	L

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
68	58	47	36	J11	H12	P16 AN06 SIN2_2 INT14_1 MAD13_0	F	M
69	59	48	37	H12	H11	P17 AN07 SOT2_2 (SDA2_2) WKUP3 MAD14_0	F	P
70	60	49	38	H13	K13	AVCC	-	-
71	61	50	39	G13	J13	AVSS	-	-
72	62	51	40	F13	H13	AVRL	-	-
73	63	52	41	E13	G13	AVRH	-	-
74	64	53	42	H11	H10	P18 AN08 SCK2_2 (SCL2_2) MAD15_0	F	L
75	65	54	43	G12	G12	P19 AN09 SIN4_1 IC00_1 INT05_1 MAD16_0	F	M
76	66	55	44	G11	G11	P1A AN10 SOT4_1 (SDA4_1) IC01_1 MAD17_0	M	L
77	67	56	45	F12	G10	P1B AN11 SCK4_1 (SCL4_1) IC02_1 MAD18_0	M	L
78	68	-	46	F11	F13	P1C AN12 CTS4_1 IC03_1 MAD19_0	F	L
79	69	-	47	E12	F12	P1D AN13 RTS4_1 DTTI0X_1 MAD20_0	F	L

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
80	70	-	48	E11	F11	P1E AN14 ADTG_5 FRCK0_1 MAD21_0	F	L
81	-	-	-	-	F10	P1F ADTG_4 TIOB6_2 RTO05_1 (PPG04_1)	E	I
82	-	-	-	-	E13	P27 TIOA6_2 RTO04_1 (PPG04_1) INT02_2	E	K
83	-	-	-	-	E12	P26 TIOB5_0 SCK2_1 (SCL2_1) RTO03_1 (PPG02_1)	E	I
84	-	-	-	-	E11	P25 TX1_0 TIOA5_0 SOT2_1 (SDA2_1) RTO02_1 (PPG02_1)	E	I
85	-	-	-	-	E10	P24 RX1_0 SIN2_1 RTO01_1 (PPG00_1) INT01_2	E	K
86	71	57 -	49	D13	D13	P23 AN15 TIOA7_1 SCK0_0 (SCL0_0) RTO00_1 (PPG00_1) MAD22_0	F	L

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
87	72	58	50	D12	D12	P22 CROUT_0 AN16 TIOB7_1 SOT0_0 (SDA0_0)	F	L
		-				ZIN1_1		
88	73	59	51	C13	D11	P21 AN17 SIN0_0 BIN1_1 INT06_1 MAD23_0	F	M
		-						
		59						
		-						
89	74	-	52	C12	C12	P20 AN18 AIN1_1 INT05_0 MAD24_0	F	M
90	75	60	53	A13	A13	VSS	-	-
91	76	61	54	B13	A12	VCC	-	-
92	77	62	55	A12	B13	P0E TIOB5_2 SCS6_1 IC13_0 S_CLK_0 MDQM1_0	L	I
93	78	63	56	B11	C10	P0D TIOA5_2 SCK6_1 (SCL6_1) IC12_0 S_CMD_0 MDQM0_0	L	I
94	79	64	57	B10	A11	P0C TIOA6_1 SOT6_1 (SDA6_1) IC11_0 S_DATA1_0 MALE_0	L	I
95	80	65	58	A10	B10	P0B TIOB6_1 SIN6_1 IC10_0 INT00_1 S_DATA0_0 MCSX0_0	L	K

Pin No						Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
96	81	66	59	A9	D9	P0A SIN1_0 FRCK1_0 INT12_2 S_DATA3_0 MCSX1_0	L	K
97	82	67 - 67	60	B9	C9	P09 AN19 TRACED0 TIOA3_2 SOT1_0 (SDA1_0) S_DATA2_0 MCSX5_0	M	N
98	83	-	61	C9	B9	P08 AN20 TRACED1 TIOB3_2 SCK1_0 (SCL1_0) MCSX4_0	F	N
99	84	-	62	A8	A9	P07 AN21 TRACED2 TIOA0_2 SCK7_0 (SCL7_0) MCLKOUT_0	F	N
100	85	-	63	B8	D8	P06 AN22 TRACED3 TIOB0_2 SOT7_0 (SDA7_0) MCSX3_0	F	N
101	86	-	64	C8	C8	P05 AN23 ADTG_0 TRACECLK SIN7_0 INT01_1 MCSX2_0	F	O
102	87	68	65	C7	B8	P04 TDO SWO	E	G
103	88	69	66	B7	D7	P03 TMS SWDIO	E	G