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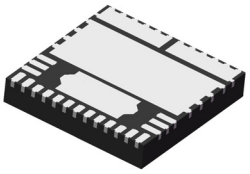
Document Number: MC06XS4200
Rev. 4.0, 4/2014

Dual 24 V, 6.0 mOhm High-side Switch

06XS4200

High-side Switch



FK SUFFIX (PB-FREE)
98ASA00428D
23 PIN PQFN (12 X12 mm)

The 06XS4200 device is part of a 24 V dual high-side switch product family with integrated control and a high number of protective and diagnostic functions. It has been designed for truck, bus, and industrial applications. The low $R_{DS(on)}$ channels (<6.0 mOhm) can control different load types; bulbs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit serial peripheral interface (SPI), allowing easy integration into existing applications.

Both channels can be controlled individually by external/internal clock-signals or by direct inputs. Using the internal clock allows fully autonomous device operation. Programmable output voltage slew rates (individually programmable) help improve EMC performance. To avoid shutting off the device during inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Switching current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a fail-safe operation mode, but remains operational, controllable, and protected. This device is powered using SMARTMOS technology.

Features

- Two fully-protected 6.0 mOhm (@ 25 °C) high-side switches
- Up to 9.0 A steady-state current per channel
- Separate bulb and DC motor latched overcurrent handling
- Parallel output operating mode with improved switching synchronization
- Individually programmable internal/external PWM clock signals (switching frequency, duty cycle, slew rate, switch-on time-shift)
- Overcurrent, short-circuit, and overtemperature protection with programmable auto-retry functions
- Accurate temperature and current sensing (high/low sensing ratios/offset compensation)
- OpenLoad detection (channel in OFF and ON state), also for LED applications (7.0 mA typ.)
- Normal operating range: 8.0 - 36 V, extended range: 6.0 - 58 V, 3.3 V and 5.0 V compatible 16-bit SPI port for device control, configuration, and diagnostics at rates up to 8.0 MHz

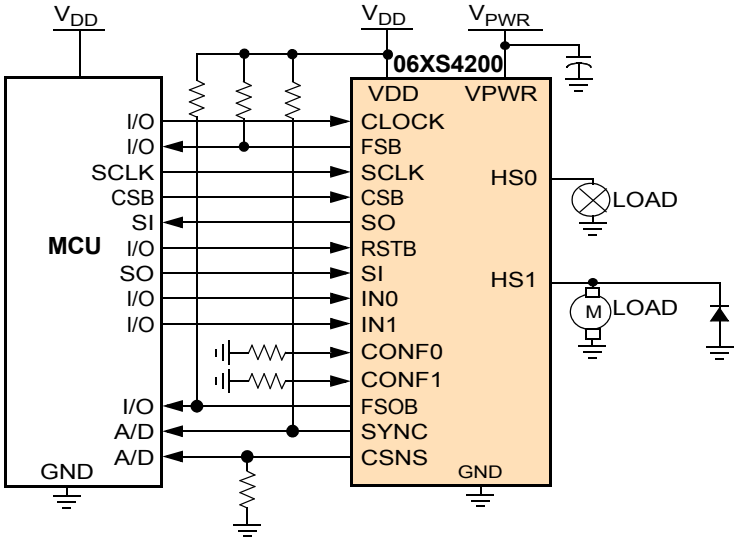


Figure 1. Simplified Application Diagram

*This document contains certain information on a product under development.
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ORDERABLE PARTS

Table 1. Orderable Part Variations

Part Number		MC06XS4200FK	MC06XS4200BFK
Notes		(1)	(1), (2)
Temperature (T_A)		-40 to 125 °C	
Package		23 PQFN	
V_{PWR} (V) Reverse Battery at 25 °C		-28	-32
I_{OUT_LEAK} min (µA) $V_{HS,OFF}$ = V_{PWR} = 24 V		-40	-120
V_{CL} (V)	Min	-35	-38
	Max	-24	-32
Δt_{RF_01} (µs)	Min	-60	-90
	Max	60	90
$I_{OLD(ON)}$ min (mA) CSNS_ratio bit = 0	Min	200.0	135.0
Δt(DLY) (µs) SR[1:0] = 00	Min	-21	-25
	Max	21	25
Δt(DLY) (µs) SR[1:0] = 01	Min	-41	-50
	Max	41	50
SYNC output signal delay for SR[1:0] = 00 (µs)	Min	46	50
	Max	155	160
SYNC output signal delay for SR[1:0] = 01 (µs)	Min	55	80
	Max	280	320
$I_{\_LOAD\_ERR\_SYS}$ (mA) typ		15	-22

Notes

1. Bit D4 of RETRY_s Serial Input register
   MC06XS4200FK = 0
   MC06XS4200BFK = CONF_SPI_s
   Setting bit D4 to 0 (CONF_SPI_s = 0) will configure the overcurrent profile as the CONF pin.
   Setting bit D4 to 1 (CONF_SPI_s = 1) will configure the overcurrent profile as the opposite of CONF pin.
2. The overcurrent profile can be configured through the SPI in the RETRY_s register. If CONF_SPI_s bit is set to 0, the overcurrent profile is selected on the CONF input pin, otherwise it is the opposite. After device reset, the overcurrent profile is defined by the CONF input pin. The SPI-SO CONF bit reporting shall combine external hardware configuration and SPI settings.

INTERNAL BLOCK DIAGRAM

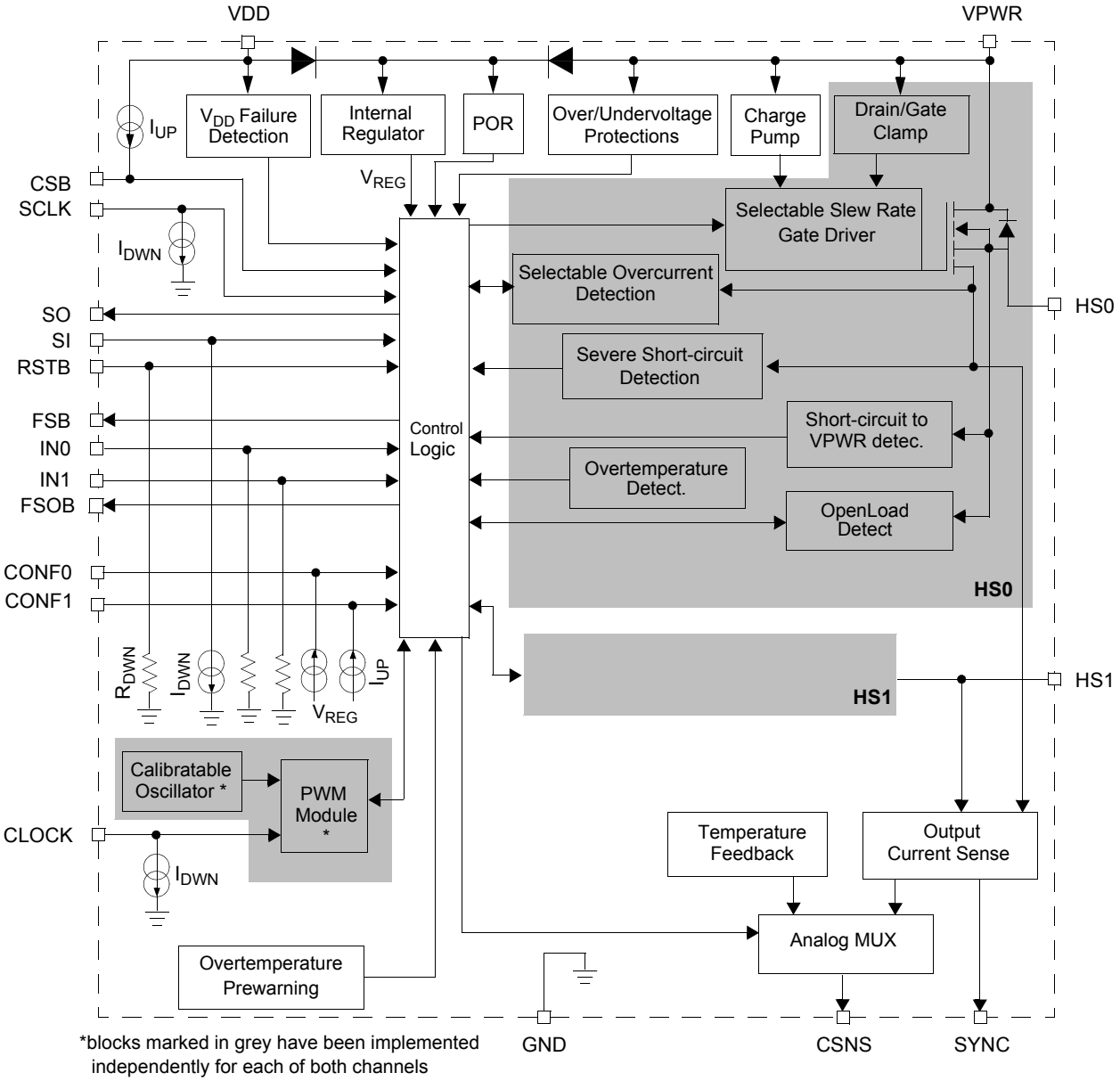

Figure 2. Internal Block Diagram

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PIN CONNECTIONS

Transparent Top View

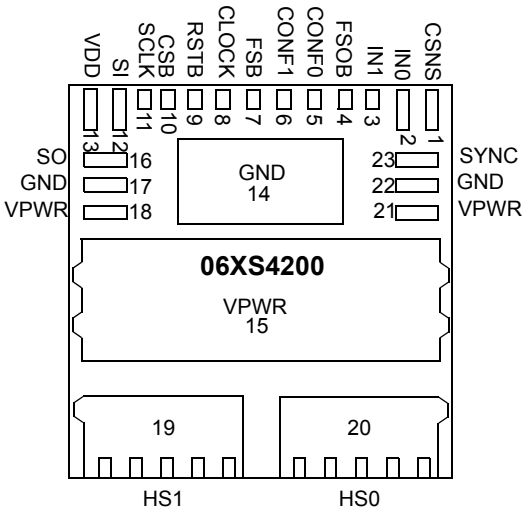

Figure 3. Device Pin Assignments

Table 2. 06XS4200 Pin Assignments

The function of each pin is described in the section Functional Description

Pin Number	Pin Name	Function	Formal Name	Definition
1	CSNS	Output	Output Current/ Temperature Monitoring	This pin either outputs a current proportional to the channel's output current or a voltage proportional to the temperature of the GND pin (pin 14). Selection between current and temperature sensing, as well as setting the current sensing sensitivity are performed through the SPI interface. An external pull-down resistor must be connected between CSNS and GND.
2 3	IN0 IN1	Input	Direct Inputs	The IN[0:1] input pins are used to directly control the switching state of both switches and consequently the voltage on the HS0:HS1 output pins. The pins are connected to GND by internal pull-down resistors
4	FSOB	Output	Fail-safe Output (Active Low)	FSOB is asserted (active-low) upon entering Fail-safe mode (see Functional Description) This open-drain output requires an external pull-up resistor to V_{PWR}
5 6	CONF0 CONF1	Input	Configuration Input	The CONF[0:1] input pins are used to select the appropriate overcurrent detection profile (bulb/DC motor) for each of both channels. CONF requires a pull-down resistor to GND.
7	FSB	Output	Fault Status (Active Low)	This open-drain output pin (external pull-up resistor to V_{DD} required) is set when the device enters Fault mode (see Fault Mode)
8	CLOCK	Input	PWM Clock	The clock input gives the time-base when the device is operated in external clock/internal PWM mode. This pin has an internal pull-down current source.
9	RSTB	Input	Reset	This input pin is used to initialize the device's configuration - and fault registers. Reset puts the device in Sleep mode (low current consumption) provided it is not stimulated by direct input signals.This pin is connected to GND by an internal pull-down resistor.
10	CSB	Input	Chip Select (Active Low)	This input pin is connected to the SPI chip-select output of an external µ-controller. CSB is internally pulled up to V_{DD} by a current source I_{UP}.

Table 2. 06XS4200 Pin Assignments (continued)

The function of each pin is described in the section Functional Description

Pin Number	Pin Name	Function	Formal Name	Definition
11	SCLK	Input	Serial Clock	This input pin is to be connected to an external SPI Clock signal. The SCLK pin is internally connected to a pull-down current source I_{DWN}
12	SI	Input	Serial Input	This input pin receives the SPI input data from an external device (microcontroller or another extreme switch device in case of daisy-chaining). The SI pin is internally connected to a pull-down current source I_{DWN}
13	VDD	Power	Digital Drain Voltage	This is the positive supply pin of the SPI interface.
16	SO	Output	Serial Output	This output pin transmits SPI data to an external device (external microcontroller or the SI pin of the next SPI device in case of daisy-chaining). The pin doesn't require external pull-up or pull-down resistors, but a series resistor is recommended to limit current consumption in case of GND disconnection
14, 17, 22	GND	Ground	Ground	These pins, internally connected, are the ground pins for the logic - and analog circuitry. It is recommended to also connect these pins on the PCB.
15,18,21	VPWR	Power	Positive Power Supply	These pins, internally connected, supply both the device's power and control circuitry (except the SPI port). The drain of both internal MOSFET switches is connected to them. Pin 15 is the device's primary thermal pad.
19 20	HS1 HS0	Output	Power Switch Outputs	Output pins of the switches, to be connected to the load.
23	SYNC	Output	Output Current Monitoring Synchronization	This output pin is asserted (active low) when the Current Sense (CS) output signal is within the specified accuracy range. Reading the SYNC pin allows the external microprocessor to synchronize to the device when operating in autonomous operating mode. SYNC is open-drain and requires a pull-up resistor to V_{DD}.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Parameter	Symbol	Maximum ratings	Unit
ELECTRICAL RATINGS			
VPWR Supply Voltage Range	V_{PWR}		V
Load Dump at 25 °C (500 ms)		58	
Reverse Battery at 25 °C			
06XS4200		-28	
06XS4200B		-32	
Fast Negative Transient Pulses (ISO 7637-2 pulse #1, V_{PWR} = 14 V & Ri = 10 Ohm)		-60	
VDD Supply Voltage Range	V_{DD}	-0.3 to 5.5	V
Voltage on Input pins[3] (except IN[0:1]) and Output pins[4](except HS[0:1])	$V_{MAX,LOGIC}$[3]	-0.3 to 5.5	V
Voltage on Fail-safe Output (FSOB)	V_{FSO}	-0.3 to 58	V
Voltage on SO pin	V_{SO}	-0.3 to V_{DD}+0.3	V
Voltage (continuous, max. allowable) on IN[0:1] Inputs	$V_{IN,MAX}$	58	V
Voltage (continuous, max. allowable) on output pins (HS [0:1])	$V_{HS[0:1]}$		V
06XS4200		-28 to 58	
06XS4200B		-32 to 58	
Rated Continuous Output Current per channel[5]	$I_{HS[0:1]}$	9.0	A
Maximum allowable energy dissipation per channel and two parallel channels, single-pulse method[6]	$E_{CL[0:1]\_SING}$	250	mJ
ESD Voltage[7]			V
Human Body Model (HBM) for HS[0:1], VPWR and GND	V_{ESD1}	±8000	
Human Body Model (HBM) for other pins	V_{ESD2}	±2000	
Charge Device Model (CDM)			
Package Corner pins (1, 13, 19, 20)	V_{ESD3}	±750	
All Other pins	V_{ESD4}	±500	

Notes:

3. Concerned Input pins are: CONF[0:1], RSTB, SI, SCLK, Clock, and CSB.
4. Concerned Output pins are: CSNS, SYNC, and FSB.
5. Output current rating valid as long as maximum junction temperature is not exceeded. For computation of the maximum allowable output current, the thermal resistance of the package & the underlying heatsink must be taken into account
6. Single pulse Energy dissipation, Single-pulse short-circuit method (L_L = 0.5 mH, R = 48 mOhm, V_{PWR} = 28 V, T_J = 150 °C initial).
7. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ohm), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).

Table 3. Maximum Ratings *(continued)*

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Parameter	Symbol	Maximum ratings	Unit
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance / Junction to Case	$R_{\theta JC}$	<1.0	°C/W
Reflow Peak Temperature on device pins during soldering[8], [9]	T_{SOLDER}	260	°C

Notes:

8. 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device. MSL level is specified later.
9. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
SUPPLY ELECTRICAL CHARACTERISTICS					
Supply Voltage Range:	V_{PWR}				
Full Specification compliant		8.0	24	36	V
Extended Mode[10]		6.0	–	58	
V_{PWR} Supply Current, device in wake-up mode, channel On, OpenLoad Outputs in ON-state, HS[0:1] open, IN[0:1] > V_{IH}	$I_{PWR(ON)}$	–	6.5	8.0	mA
V_{PWR} Supply Current, device in wake-up mode (Standby), channel Off OpenLoad in OFF-state Detection Disabled, HS[0:1] shorted to ground with V_{DD} = 5.5 V and RSTB > V_{WAKE}	$I_{PWR(SBY)}$	–	6.5	8.0	mA
Sleep State Supply Current	$I_{PWR(SLEEP)}$				µA
V_{PWR} = 24 V, RSTB = IN[0:1] < V_{WAKE}, HS[0:1] connected to ground					
T_A = 25 °C		–	3.0	10.0	
T_A = 125 °C		–	–	60.0	
V_{DD} Supply Voltage	$V_{DD(ON)}$	3.0	–	5.5	V
V_{DD} Supply Current at V_{DD} = 5.5 V	$I_{DD(ON)}$				mA
No SPI Communication		–	–	2.2	
8.0 MHz SPI Communication[11]		–	5.0	–	
V_{DD} Sleep State Current at V_{DD} = 5.5 V with or without V_{PWR}	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage Shutdown Threshold	$V_{PWR(OV)}$	39	42	45.5	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Shutdown Threshold[12]	$V_{PWR(UV)}$	5.0	–	6.0	V
V_{PWR} Power-On-Reset (POR) Voltage Threshold[12]	$V_{PWR(POR)}$	2.2	2.6	4.0	V
V_{DD} Power-On-Reset (POR) Voltage Threshold[12]	$V_{DD(POR)}$	1.5	2.0	2.5	V
V_{DD} Supply Failure Voltage Threshold (assumed V_{PWR} > $V_{PWR(UV)}$)	$V_{DD(FAIL)}$	2.2	2.5	2.8	V

Notes

10. In extended mode, availability of several device functions (channel control, value of $R_{DS(ON)}$, overtemperature protection) is guaranteed, but compliance with the specified values in this document is not. Below 6.0 V, the device is only protected from overheating (thermal shutdown). Above $V_{PWR(OV)}$, the channels can only be turned ON when the overvoltage detection function has been disabled.
11. Typical value guaranteed per design.
12. When the device recovers from undervoltage and returns to normal mode (6.0 V < V_{PWR} < 58 V) before the end of the auto-retry period (see Auto-retry), the device performs normally. When V_{PWR} drops below $V_{PWR(UV)}$, undervoltage is detected (see Undervoltage Fault (Latchable Fault) and EMC Performances).

Table 4. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1)					
ON-Resistance, Drain-to-Source (I_{HS} = 3.0 A, T_J = 25 °C) CSNS_ratio = 0	$R_{DS(ON)25}$				
V_{PWR} = 8.0 V		–	–	6.0	mΩ
V_{PWR} = 28 V		–	–	6.0	
V_{PWR} = 36 V		–	–	6.0	
ON-Resistance, Drain-to-Source (I_{HS} = 3.0 A,T_J = 150 °C) CSNS_ratio = 0	$R_{DS(ON)150}$				
V_{PWR} = 8.0 V		–	–	12	mΩ
V_{PWR} = 28 V		–	–	12	
V_{PWR} = 36 V		–	–	12	
ON-Resistance, Drain-to-Source difference from one channel to the other in parallel mode (I_{HS} = 1.0 A,T_J = 150 °C) CSNS_ratio = X	$\Delta R_{DS(ON)150}$	-0.7	–	+0.7	mΩ
ON-Resistance, Source-Drain (I_{HS} = -3.0 A, T_J = 150 °C, V_{PWR} = -24 V)	$R_{SD(ON)150}$	–	–	12	mΩ
Max. detectable wiring length (2.5 mm²) for severe short-circuit detection (see Severe Short-circuit Fault (latchable fault)):	L_{SHORT}				
High slew rate selected		14	48	80	cm
Medium slew rate selected:		30	100	170	
Low slew rate selected:		60	200	340	
Overcurrent Detection thresholds with CSNS_ratio bit = 0 (CSR0)	$I_{\_OCH1\_0}$	90.0	110.0	128.3	A
	$I_{\_OCH2\_0}$	58.3	70.0	81.7	
	$I_{\_OCM1\_0}$	36.1	43.3	50.6	
	$I_{\_OCM2\_0}$	22.2	26.7	31.1	
	$I_{\_OCL1\_0}$	15.0	18.0	21.0	
	$I_{\_OCL2\_0}$	10.0	12.0	14.0	
	$I_{\_OCL3\_0}$	5.0	6.0	7.0	
Overcurrent Detection thresholds with CSNS_ratio bit = 1(CSR1)	$I_{\_OCH1\_1}$	30.6	36.7	42.8	A
	$I_{\_OCH2\_1}$	19.4	23.3	27.2	
	$I_{\_OCM1\_1}$	12.0	14.4	16.9	
	$I_{\_OCM2\_1}$	7.4	8.9	10.4	
	$I_{\_OCL1\_1}$	5.0	6.0	7.0	
	$I_{\_OCL2\_1}$	3.3	4.0	4.7	
	$I_{\_OCL3\_1}$	1.6	2.0	2.4	
Output (HS[x]) leakage Current in sleep state (positive value = outgoing)	I_{OUT_LEAK}				µA
06XS4200					
$V_{HS,OFF}$ = 0 V ($V_{HS,OFF}$ = output voltage in OFF state)		–	–	+16	
$V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 24 V)		-40.0	–	+5.0	
06XS4200B					
$V_{HS,OFF}$ = 0 V ($V_{HS,OFF}$ = output voltage in OFF state)		–	–	+16	
$V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 24 V)		-120	–	+5.0	
$V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 36 V)		-1400	–	+5.0	

Table 4. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)					
Output biasing current in off-state (positive value = outgoing) 06XS4200B with OL_OFF disabled (worst case V_{PWR} = 36 V, $V_{HS,OFF}$ = 34 V)	I_{OUT_OFF}				µA
Fast slew rate selected		-770	-620	-460	
Medium slew rate selected		-520	-420	-310	
Slow slew rate selected		-390	-315	-240	
With OL_OFF disabled and ECU ground disconnected (V_{PWR} = 32 V)		0.0	–	1000	
Switch Turn-on threshold for supply overvoltage (V_{PWR} -GND)	$V_{D\_GND(CLAMP)}$	58	–	66	V
Switch turn-on threshold for drain-source overvoltage (@ I_{HS} = 100 mA)	$V_{DS(CLAMP)}$	58	–	66	V
Switch turn-on threshold for Drain-Source overvoltage difference from one channel to the other in parallel mode (@ I_{HS} = 100 mA)	$\Delta V_{DS(CLAMP)}$	-2.0	–	+2.0	V
Current Sensing Ratio[13]					–
CSNS_ratio bit = 0 (high-current mode)	C_{SR0}	–	1/5000	–	
CSNS_ratio bit = 1 (low-current mode)	C_{SR1}	–	1/1666.6	–	
Minimum measurable load current with compensated error[14] < 35%	$I_{\_LOAD\_MIN}$	–	–	175	mA
CSNS leakage current in OFF state (CSNSx_en = 0, CSNS_ratio bit_x = 0)	I_{CSR_LEAK}	-4.0	–	+4.0	µA
Systematic offset error (see Current Sense Errors)	$I_{\_LOAD\_ERR\_SYS}$				mA
06XS4200		–	15	–	
06XS4200B		–	-22	–	
Random offset error	$I_{\_LOAD\_ERR\_RAND}$	-360	–	360	mA
CSNS pin current sourcing capability, absolute upper limit	$I_{CSNS,MAX}$	5.15	–	–	mA
E_{SR0} Output Current Sensing Error (%, uncompensated[15]) at output Current level (Sense ratio C_{SR0} selected):	E_{SR0_ERR}				%
T_J = -40 °C					
9.0 A		-13	–	13	
4.5 A		-12	–	12	
2.25 A		-17	–	17	
1.13 A		-31	–	31	
T_J = 125 °C					
9.0 A		-10	–	10	
4.5 A		-9.0	–	9.0	
2.25 A		-12	–	12	
1.13 A		-19	–	19	
T_J = 25 to 125 °C					
9.0 A		-10	–	10	
4.5 A		-9.0	–	9.0	
2.25 A		-12	–	12	
1.13 A		-22	–	22	

Table 4. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)					
E_{SR0} Output Current Sensing Error (%, after offset compensation(14)) at output Current level (Sense ratio C_{SR0} selected):	E_{SR0_ERR}(Comp)				%
T_J = -40 °C					
9.0 A		-10	–	10	
4.5 A		-10	–	10	
2.25 A		-10	–	10	
1.13 A		-10	–	10	
T_J = 125 °C					
9.0 A		-9.0	–	9.0	
4.5 A		-8.0	–	8.0	
2.25 A		-9.0	–	9.0	
1.13 A		-9.0	–	9.0	
T_J = 25 to 125 °C					
9.0 A		-9.0	–	9.0	
4.5 A		-8.0	–	8.0	
2.25 A		-9.0	–	9.0	
1.13 A		-9.0	–	9.0	
E_{SR1} Output Current Sensing Error (%, uncompensated (15)) at output Current level (Sense ratio C_{SR1} selected):	E_{SR1_ERR}				%
T_J = -40 °C					
2.25 A		-16	–	16	
T_J = 125 °C					
2.25 A		-12	–	12	
T_J = 25 to 125 °C					
2.25 A		-12	–	12	

Notes:

13. Current Sense Ratio C_{SRX} = I_{CSNS} / ($I_{HS[x]}$ + $I_{\_LOAD\_ERR\_SYS}$)
14. See note (15), but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and Use of Offset Compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration
15. E_{SRX_ERR} = (I_{CSNS_MEAS} / I_{CSNS_MODEL}) - 1, with I_{CSNS_MODEL} = (I(HS[x]) + $I_{\_LOAD\_ERR\_SYS}$) * C_{SRX} , ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current Sense Error Model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRX} - $I_{\_LOAD\_ERR\_SYS}$

Table 4. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)					
E_{SR1} Output Current Sensing Error (% after offset compensation[16]) at output Current level (Sense ratio C_{SR1} selected):	E_{SR1_ERR}(Comp)				%
T_J = -40 °C					
2.25 A		-10	–	10	
0.75 A		-11	–	11	
0.375 A		-18	–	18	
0.225 A		-29	–	29	
T_J = 125 °C					
2.25 A		-8.0	–	8.0	
0.75 A		-10	–	10	
0.375 A		-12	–	12	
0.225 A		-16	–	16	
T_J = 25 to 125 °C					
2.25 A		-8.0	–	8.0	
0.75 A		-10	–	10	
0.375 A		-13	–	13	
0.225 A		-21	–	21	
E_{SR0} Output Current Sensing Error in parallel mode (%, uncompensated[17]) at outputs Current level (Sense ratio C_{SR0} selected):	$E_{SR0\_ERR\_PAR}$				%
T_J = -40 °C					
9.0 A		-10	–	10	
4.5 A		-11	–	11	
T_J = 125 °C					
9.0 A		-8.0	–	8.0	
4.5 A		-8.0	–	8.0	
T_J = 25 to 125 °C					
9.0 A		-8.0	–	8.0	
4.5 A		-8.0	–	8.0	
Current Sense Clamping Voltage (condition: R(CSNS) > 10 kOhm)	$V_{CL(CSNS)}$	5.5	–	7.5	V
OpenLoad detection Current threshold in OFF state [18]	$I_{OLD(OFF)}$	30	–	100	µA
OpenLoad Fault Detection Voltage Threshold [18]	$V_{OLD(THRES)}$	4.0	–	5.5	V

Notes:

16. See note [17], but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and Use of Offset Compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration.
17. E_{SRX_ERR} = (I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRX} , ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current Sense Error Model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRX} - $I_{\_LOAD\_ERR\_SYS}$
18. Minimum required value of OpenLoad impedance for detection of OpenLoad in OFF-state: 200 kΩ.($V_{OLD(THRES)}$ = V_{HS} @ $I_{OLD(OFF)}$)

Table 4. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)					
OpenLoad detection Current threshold in ON state (see OpenLoad Detection In On State (OL_ON)):	$I_{OLD(ON)}$				mA
CSNS_ratio bit = 0					
06XS4200		200.0	500.0	999.9	
06XS4200B		135.0	500.0	999.9	
CSNS_ratio bit = 1 (fast slew rate SR[1:0] = 10 mandatory for this function)		5.0	7.0	10	
Time period of the periodically activated OpenLoad in ON state detection for CSNS_ratio bit = 1	t_{OLLED}	105	150	195	ms
Output Shorted-to-V_{PWR} Detection Voltage Threshold (channel in OFF state)	$V_{OSD(THRES)}$	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V
Switch turn-on threshold for Negative Output Voltages (protects against negative transients) - (measured at I_{OUT} = 100 mA, Channel in OFF state)	V_{CL}				V
06XS4200		-35	–	-24	
06XS4200B		-38	–	-32	
Switch turn-on threshold for Negative Output Voltages difference from one channel to the other in parallel mode - (measured at I_{OUT} = 100 mA, Channel in OFF state)	ΔV_{CL}	-2.0	–	+2.0	V
Switching State (On/Off) discrimination thresholds	V_{HS_TH}	0.45*V_{PWR}	0.5*V_{PWR}	0.55*V_{PWR}	V
Shutdown temperature (Power MOSFET junction; 6.0 V < V_{PWR} < 58 V)	T_{SD}	160	175	190	°C
ELECTRICAL CHARACTERISTICS OF THE CONTROL INTERFACE PINS					
Logic Input Voltage, High[19]	V_{IH}	2.0	–	5.5	V
Logic Input Voltage, Low[19]	V_{IL}	-0.3	–	0.8	V
Wake-up Threshold Voltage (IN[0:1] and RSTB)[20]	V_{WAKE}	1.0	–	2.2	V
Internal Pull-down Current Source (on Inputs: CLOCK, SCLK and SI)[21]	I_{DWN}	5.0	–	20	µA
Internal Pull-up Current Source (input CSB)[22]	I_{UP_CSB}	5.0	–	20	µA
Internal Pull-up Current Source (input CONF[0:1])[23]	I_{UP_CONF}	25	–	100	µA
Capacitance of SO, FSB and FSOB pins in Tri-state	C_{SO}	–	–	20	pF
Internal Pull-down Resistance (RSTB and IN[0:1])	R_{DWN}	125	250	500	kΩ
Input Capacitance[24]	C_{IN}	–	4.0	12	pF

Notes

19. High and low voltage ranges apply to SI, CSB, SCLK, RSTB, IN[0:1] and CLOCK input signals. The IN[0:1] signals may be derived from V_{PWR} and can tolerate voltages up to 58 V.
20. Voltage above which the device wakes up
21. Valid for $V_{SI} \geq 0.8$ V and $V_{SCLK} \geq 0.8$ V and $V_{CLOCK} \geq 0.8$ V.
22. Valid for $V_{CSB} \leq 2.0$ V. CSB has an internal pull-up current source derived from V_{DD}
23. Pins CONF[0:1] are connected to an internal current source, derived from an internal voltage regulator (V_{REG} ~ 3.0 V).
24. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CONF[0:1], and CLOCK pins. This parameter is guaranteed by the manufacturing process but is not tested in production.

Table 4. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE CONTROL INTERFACE PINS (CONTINUED)					
SO High-state Output Voltage (I_{OH} = 1.0 mA)	V_{SOH}	V_{DD}-0.4	–	–	V
SYNC, SO, FSOB and FSB Low-state Output Voltage (I_{OL} = -1.0 mA)	V_{SOL}	–	–	0.4	V
SYNC, SO, CSNS, FSOB and FSB Tri-state Leakage Current: (0 V < V(SO) < V_{DD}, or V(FS) or V(SYNC) = 5.5 V, or V(FSO) = 36 V or V(CSNS) = 0 V)	$I_{SO(LEAK)}$	-2.0	0	2.0	µA
CONF[0:1]: Required values of the External Pull-down Resistor	R_{CONF}				kΩ
Lighting applications		1.0	–	10	
DC motor applications		50	–	Infinite	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
OUTPUT VOLTAGE SWITCHING CHARACTERISTICS					
Rising and falling edge medium slew rate (SR[1:0] = 00)(25)	SR_{R_00}				V/µs
V_{PWR} = 16 V	SR_{F_00}	0.164	–	0.65	
V_{PWR} = 28 V		0.28	–	0.79	
V_{PWR} = 36 V		0.34	–	0.90	
Rising edge low slew rate (SR[1:0] = 01)(25)	SR_{R_01}				V/µs
V_{PWR} = 16 V	SR_{F_01}	0.081	–	0.32	
V_{PWR} = 28 V		0.14	–	0.395	
V_{PWR} = 36 V		0.17	–	0.45	
Rising edge high slew rate / SR[1:0] = 10)(25)	SR_{R_10}				V/µs
V_{PWR} = 16 V	SR_{F_10}	0.29	–	1.30	
V_{PWR} = 28 V		0.55	–	1.58	
V_{PWR} = 36 V		0.68	–	1.80	
Rising/Falling edge slew rate matching per channel	SR_R/SR_F				
16 V < V_{PWR} < 36 V		0.75	–	1.2	
Edge slew rate difference from one channel to the other in parallel mode(25)	ΔSR				
16 V < V_{PWR} < 36 V					V/µs
SR[1:0] = 00		-0.1	0.0	+0.1	
SR[1:0] = 01		-0.06	0.0	+0.06	
SR[1:0] = 10		-0.14	0.0	+0.14	
Output Turn-ON and Turn-OFF Delays (medium slew rate: SR[1:0] = 00)(26)	t_{DLY_00}				µs
16 V < V_{PWR} < 36 V		39	-	145	
Output Turn-ON and Turn-OFF Delays (low slew rate / SR[1:0] = 01)(26)	t_{DLY_01}				µs
16 V < V_{PWR} < 36 V		50	-	280	
Output Turn-ON and Turn-OFF Delays (high slew rate / SR[1:0] = 10)(26)	t_{DLY_10}				µs
16 V < V_{PWR} < 36 V		22	-	80	
Turn-ON and Turn-OFF Delay time matching per channel ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)	Δt_{RF_00}				µs
f_{PWM} = 400 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 00		-25	0.0	25	
Turn-ON and Turn-OFF Delay time matching per channel ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)	Δt_{RF_01}				µs
f_{PWM} = 200 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 01					
06XS4200		-60	0.0	60	
06XS4200B		-90	0.0	90	

Notes

25. Rising and Falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 Ω resistive load (see Figure 4).
26. Turn-on delay time measured as delay between a rising edge of the channel control signal (IN[0:1] = 1) and the associated rising edge of the output voltage up to: $V_{HS[0:1]} = V_{PWR} / 2$ (where R_L = 5.0 Ω). Turn-OFF delay time is measured as time between a falling edge of the channel control signal (IN[0:1] = 0) and the associated falling edge of the output voltage up to the instant at which: $V_{HS[0:1]} = V_{PWR} / 2$ (R_L = 10.0 Ohm.

Table 5. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (CONTINUED)					
Turn-ON and Turn-OFF Delay time matching per channel ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) f_{PWM} = 1.0 kHz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 10	Δt_{RF_10}	-13	0.0	13	µs
Delay time difference from one channel to the other in parallel mode[27] 16 V < V_{PWR} < 36 V SR[1:0] = 00 06XS4200 06XS4200B SR[1:0] = 01 06XS4200 06XS4200B SR[1:0] = 10	$\Delta t_{(DLY)}$	 -21 -25 -41 -50 -12	 0.0 0.0 0.0 0.0 0.0	 21 25 41 50 12	µs
Fault Detection Delay Time[28]	t_{FAULT}	–	5.0	8.0	µs
Output Shutdown Delay Time[29]	t_{DETECT}	–	12.0	17	µs
Current sense output settling Time for SR[1:0] = 00 (medium slew rate) [30] 16 V < V_{PWR} < 36 V	$t_{CSNSVAL\_00}$	0.0	-	200	µs
Current sense output settling Time for SR[1:0] = 01(low slew rate)[30] 16 V < V_{PWR} < 36 V	$t_{CSNSVAL\_01}$	0.0	-	315	µs
Current sense output settling Time for SR[1:0] = 10 (high slew rate)[30] 16 V < V_{PWR} < 36 V	$t_{CSNSVAL\_10}$	0.0	-	165	µs
SYNC output signal delay for SR[1:0] = 00 (medium SR) [30] 06XS4200 06XS4200B	$t_{SYNCVAL\_00}$	 46 50	 - -	 155 160	µs
SYNC output signal delay for SR[1:0] = 01 (low SR)[30] 06XS4200 06XS4200B	$t_{SYNCVAL\_01}$	 55 80	 - -	 280 320	µs
SYNC output signal delay for SR[1:0] = 10 (high SR) [30]	$t_{SYNCVAL\_10}$	22	-	80	µs
Recommended sync_to_read delay SR[1:0] = 00 (medium slew rate) [30]	$t_{SYNREAD\_00}$	0.0	-	200	µs
Recommended sync_to_read delay SR[1:0] = 01 (low slew rate) [30]	$t_{SYNREAD\_01}$	0.0	-	200	µs
Recommended sync_to_read delay SR[1:0] = 10 (high slew rate) [30]	$t_{SYNREAD\_10}$	0.0	-	200	µs
Upper overcurrent threshold duration	t_{OCH1} t_{OCH2}	6.0 12.0	8.6 17.2	11.2 22.4	ms

Notes:

27. Rising and Falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 Ω resistive load (see Figure 4).
28. Time required to detect and report the fault to the FSB pin.
29. Time required to switch off the channel after detection of overtemperature (OT), overcurrent (OC), SC or UV error (time measured between start of the negative edge on the FSB pin and the falling edge on the output voltage until V(HS[0:1)) = 50% of V_{PWR}
30. Settling time (= $t_{CSNSVAL\_XX}$), SYNC output signal delay (= $t_{SYNCVAL\_XX}$) and Read-out delay (= $t_{SYNREAD\_XX}$) are defined for a stepped load current (100 mA< I(LOAD)<IOCLx A FOR CSNS_RATIO_S = 1, AND 300 mA< I(LOAD)<IOCLx A_0 FOR CSNS_RATIO_S = 0). (see Figure 9 and Output Current Monitoring (CSNS)).

Table 5. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (CONTINUED)					
Medium overcurrent threshold duration (CONF = 0; Lighting Profile)	t_{OCM1_L} t_{OCM2_L}	48 96	67 137	87 178	ms
Medium overcurrent threshold duration (CONF = 1; DC motor Profile)	t_{OCM1_M} t_{OCM2_M}	150 301	214 429	278 557	ms
FREQUENCY & PWM DUTY CYCLE RANGES [31](protections fully operational, see Protective Functions)					
Switching Frequency range - Direct Inputs	$f_{CONTROL}$	0.0	–	1000	Hz
Switching Frequency range - External clock with internal PWM (recommended)	f_{PWM_EXT}	20	–	1000	Hz
Switching Frequency range - Internal clock with internal PWM (recommended)	f_{PWM_INT}	60	–	1000	Hz
Duty Cycle range	$R_{CONTROL}$	0.0	–	100	%

Notes:

31. In Direct Input mode, the lower frequency limit is 0 Hz with RSTB = 5.0 V and 4.0 Hz with RSTB = 0 V. Duty-cycle applies to instants at which V_{HS} = 50 % V_{PWR}. For low duty-cycle values, the effective value also depends on the value of the selected slew rate.

Table 5. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
AVAILABILITY DIAGNOSTIC FUNCTIONS OVER DUTY-CYCLE AND SWITCHING FREQUENCY (PROTECTIONS & DIAGNOSTICS BOTH FULLY OPERATIONAL, SEE DIAGNOSTIC FEATURES FOR THE EXACT BOUNDARY VALUES)					
Available Duty Cycle Range, f_{PWM} = 1.0 kHz high slew rate, PWM mode(32)	$R_{PWM\_1K\_H}$				%
OL_OFF		0.0	–	62	
OL_ON		35	–	100	
OS		0.0	–	90	
Available Duty Cycle Range, f_{PWM} = 400 Hz, medium slew rate, PWM mode(32)	$R_{PWM\_400\_M}$				%
OL_OFF		0.0	–	81	
OL_ON		21	–	100	
OS		0.0	–	88	
Available Duty Cycle Range, f_{PWM} = 400 Hz, high slew rate, PWM mode(32)	$R_{PWM\_400\_H}$				%
OL_OFF		0.0	–	84	
OL_ON		14	–	100	
OS		0.0	–	95	
Available Duty Cycle Range, f_{PWM} = 200 Hz, low slew rate mode, PWM mode(32)	$R_{PWM\_200\_L}$				%
OL_OFF		0.0	–	86	
OL_ON		15	–	100	
OS		0.0	–	93	
Available Duty Cycle Range, f_{PWM} = 200 Hz, medium slew rate, PWM mode(32)	$R_{PWM\_200\_M}$				%
OL_OFF		0.0	–	90	
OL_ON		11	–	100	
OS		0.0	–	94	
Available Duty Cycle Range, f_{PWM} = 100 Hz in low slew rate, PWM mode(32)	$R_{PWM\_100\_L}$				%
OL_OFF		0.0	–	93	
OL_ON		8.0	–	100	
OS		0.0	–	96	
Deviation of the internal clock PWM frequency after Calibration(33)	$A_{FPWM(CAL)}$	-10	–	+10	%
Default output frequency when using an uncalibrated oscillator	$f_{PWM(0)}$	280	400	520	Hz
Minimal required Low Time during Calibration of the Internal Clock through CSB	$t_{CSB(MIN)}$	1.0	1.5	2.0	µs
Maximal allowed Low Time during Calibration of the Internal Clock through CSB	$t_{CSB(MAX)}$	70	100	130	µs
Recommended external Clock Frequency Range (external clock/PWM Module)	f_{CLOCK}	15	–	512	kHz
Upper detection threshold for external clock frequency monitoring	$f_{CLOCK(MAX)}$	512	730	930	kHz
Lower detection threshold for external clock frequency monitoring	$f_{CLOCK(MIN)}$	5.0	7.0	10	kHz

Notes

32. Actually, the device can be operated outside the specified duty cycle and frequency ranges (basic protective functions OC, SC, UV, OV, OT remain active) but the availability of the diagnostic functions OL_ON, OL_OFF, OS is affected.
33. Values guaranteed from 60 Hz to 1.0 kHz (recommended switching frequency range for internal clock operation).

Table 5. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
TIMING: SPI PORT, IN[0]/ IN[1] SIGNALS & AUTORETRY					
Required Low time allowing delatching or triggering sleep mode (direct input mode)	t_{IN}	175	250	325	ms
Watchdog Timeout for entering Fail-safe Mode due to loss of SPI contact(34)	t_{WDTO}	217	310	400	ms
Auto-Retry Repetition Period (when activated):					ms
Auto_period bits = 00	t_{AUTO_00}	105	150	195	
Auto_period bits = 01	t_{AUTO_01}	52.5	75	97.5	
Auto_period bits = 10	t_{AUTO_10}	26.2	37.5	47.8	
Auto_period bits = 11	t_{AUTO_11}	13.1	17.7	24.4	
GND PIN TEMPERATURE SENSING FUNCTION					
Thermal Prewarning Detection Threshold(35)	T_{OTWAR}	110	125	140	°C
Temperature Sensing output voltage @ T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)	T_{FEED}	918	1078	1238	mV
Gain Temperature Sensing output @ T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)(35)	DT_{FEED}	10.7	11.1	11.5	mV/°C
Temperature Sensing Error, range [-40 °C, 150 °C], default(35)	T_{FEED_ERROR}	-15	–	+15	°C
Temperature Sensing Error, [-40 °C, 150 °C] after 1 point calibration @ 25 °C(35)	$T_{FEED\_ERROR\_CAL}$	-5.0	–	+5.0	°C

Notes

34. Only when the WD_dis bit set to logic [0] (default). Watchdog timeout defined from the rising edge on RST to rising edge HS[0,1]
35. Values were obtained by lab characterization.

Table 5. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
SPI INTERFACE ELECTRICAL CHARACTERISTICS(36)					
Maximum Operating Frequency of the Serial Peripheral Interface (SPI)(37)	f_{SPI}	–	–	8.0	MHz
Required Low-state Duration for reset RSTB(38)	t_{WRSTB}	10	–	–	µs
Required duration from the Rising to the Falling Edge of CSB (Required Setup Time)(39)	t_{CSB}	1.0	–	–	µs
Rising Edge of RSTB to Falling Edge of CSB (Required Setup Time)(39)	t_{ENBL}	5.0	–	–	µs
Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)(39)	t_{LEAD}	500	–	–	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Setup lag Time)(39)	t_{LAG}	60	–	–	ns
Required High-state Duration of SCLK (Required Setup Time)(39)	t_{WSCLKh}	50	–	–	ns
Required Low-state Duration of SCLK (Required Setup Time)(39)	t_{WSCLKl}	50	–	–	ns
SI to Falling Edge of SCLK (Required Setup Time)(40)	$t_{SI(SU)}$	15	–	–	ns
Falling Edge of SCLK to SI (Required hold Time of the SI signal)(40)	$t_{SI(H)}$	30	–	–	ns
SO Rise Time C_L = 80 pF	t_{RSO}	–	–	20	ns
SO Fall Time C_L = 80 pF	t_{FSO}	–	–	20	ns
SI, CSB, SCLK, Max. Rise Time allowing operation at f_{SPI} = 8.0 MHz(40)	t_{RSI}	–	–	11	ns
SI, CSB, SCLK, Max. Fall Time allowing operation at f_{SPI} = 8.0 MHz(40)	t_{FSI}	–	–	11	ns
Time from Rising Edge of SCLK to reach a valid level at the SO pin(41)	t_{VALID}	–	–	44	ns
Time from Falling Edge of CSB to reach low-impedance on SO (access time)(42)	t_{SOEN}	–	–	30	ns
Time from Rising Edge of CSB to reach high-impedance on SO pin (turn off time)	t_{SODIS}			30	ns

Notes:

36. Parameters guaranteed by design. It is recommended to tie unused SPI-pins to GND by resistors 1.0 k <R <10 k
37. For clock frequencies > 4.0 MHz, series resistors on the SPI pins should preferably be removed. Otherwise, 470 pF ($V_{MAX.}$ > 40 V) ceramic speed-up capacitors in parallel with the >8.0 kΩ input resistors are required on pins SCLK, SI, SO, CS
38. RSTB low duration is defined as the minimum time required to switch off the channel when previously put ON in SPI mode (direct inputs inactive).
39. Minimum setup time required for the device is the minimum required time that the microcontroller must wait or remain in a given state.
40. Rise and Fall time of incoming SI, CSB, and SCLK signals.
41. Time required for output data to be available for use at SO, measured with a 80 pF capacitive load.
42. Time required for output data to be terminated at SO measured without a series resistor connected CSB.

TIMING DIAGRAMS

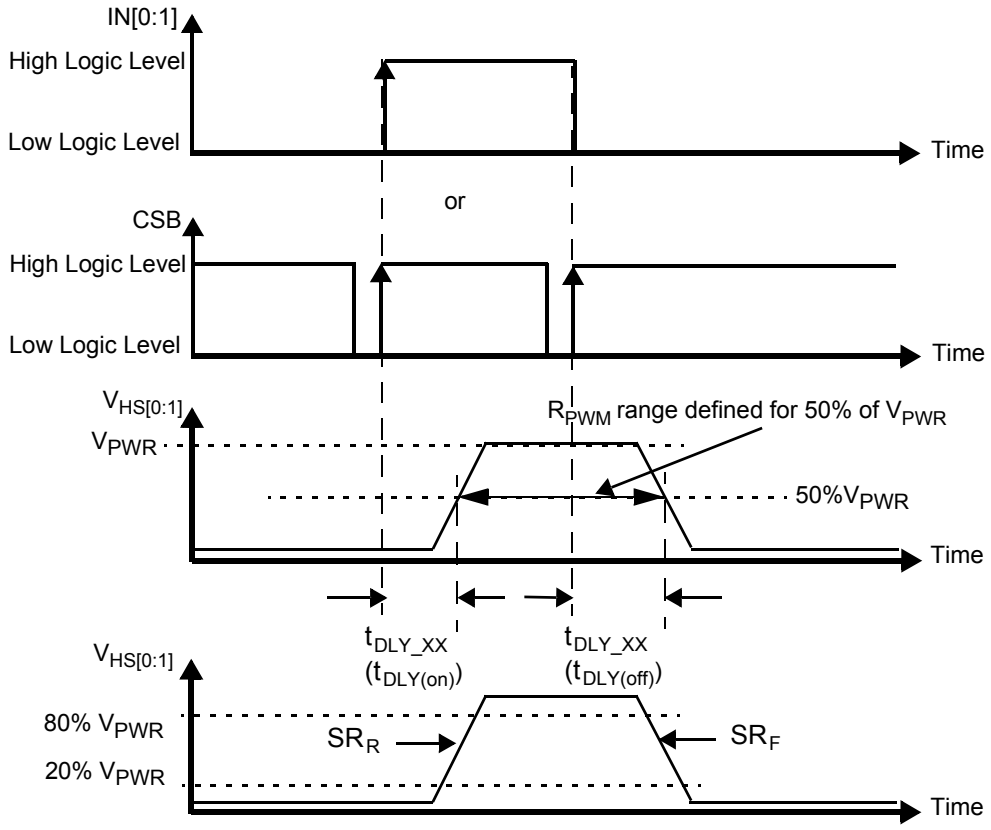

Figure 4. Output Voltage Slew Rate and Delay

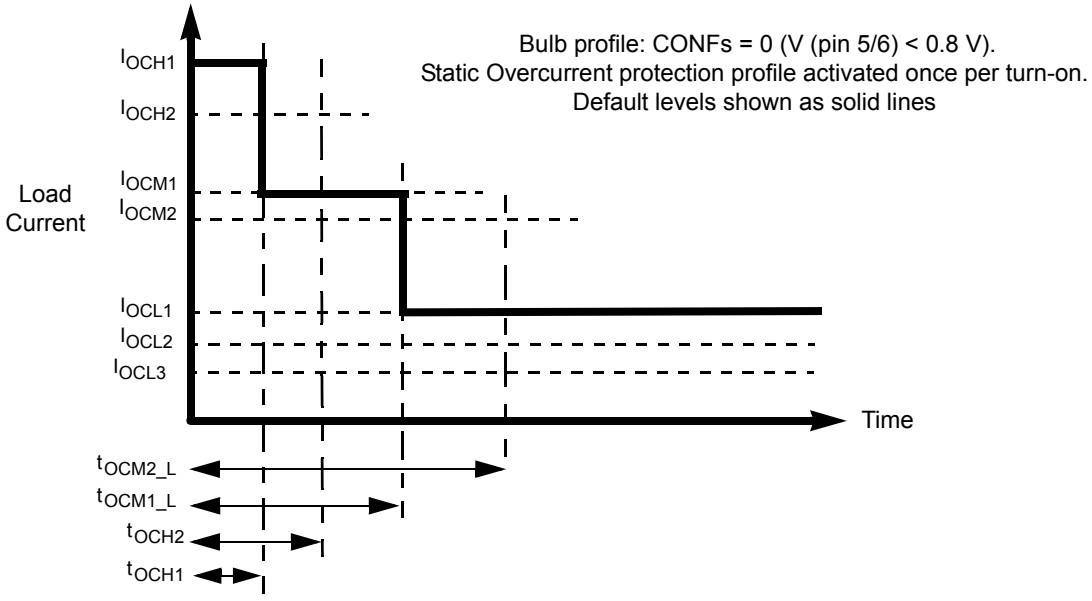

Figure 5. Overcurrent Protection Profile for Bulb Applications

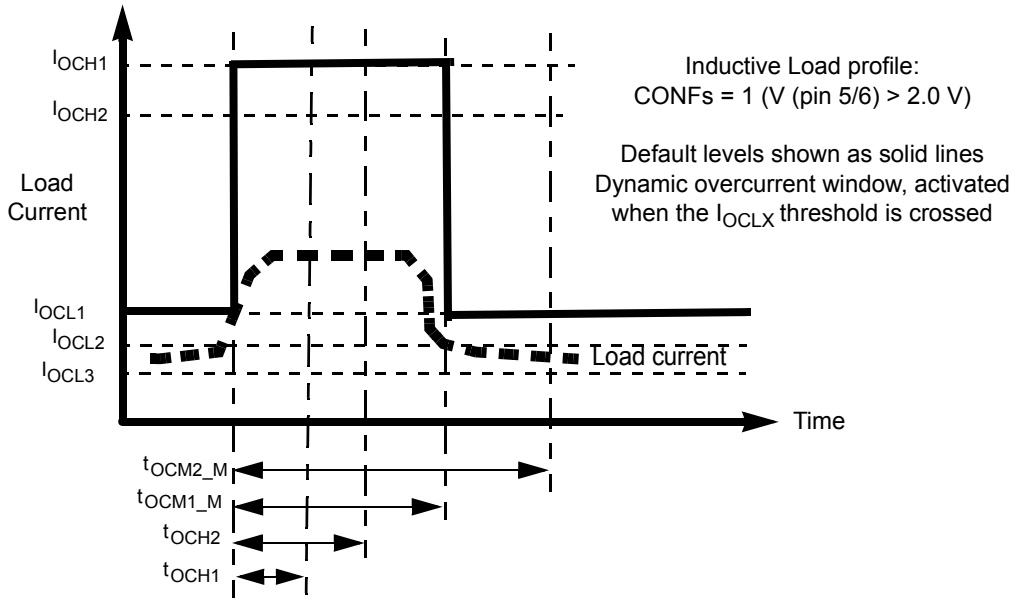

Figure 6. Overcurrent Protection Profile for Applications with Inductive Loads (DC motors, solenoids)

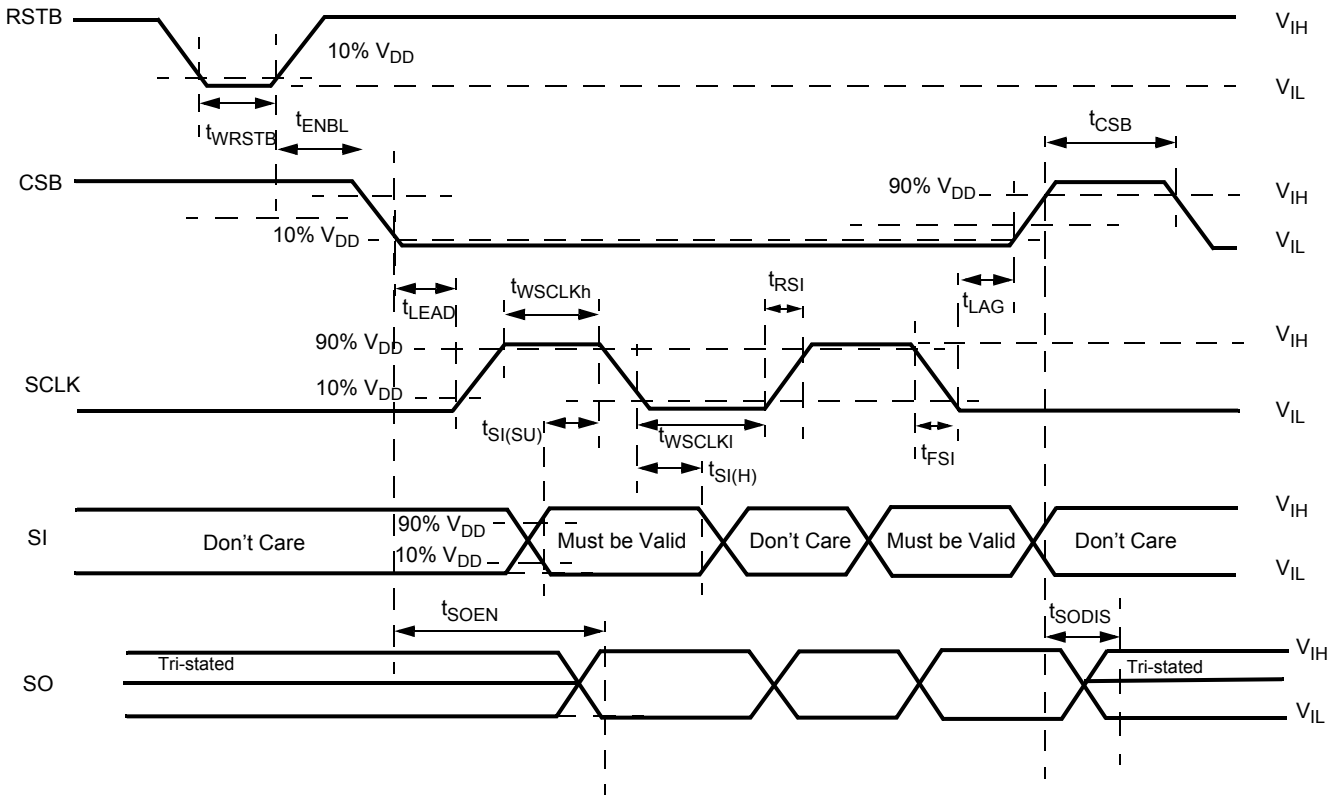

Figure 7. Timing Requirements During SPI Communication

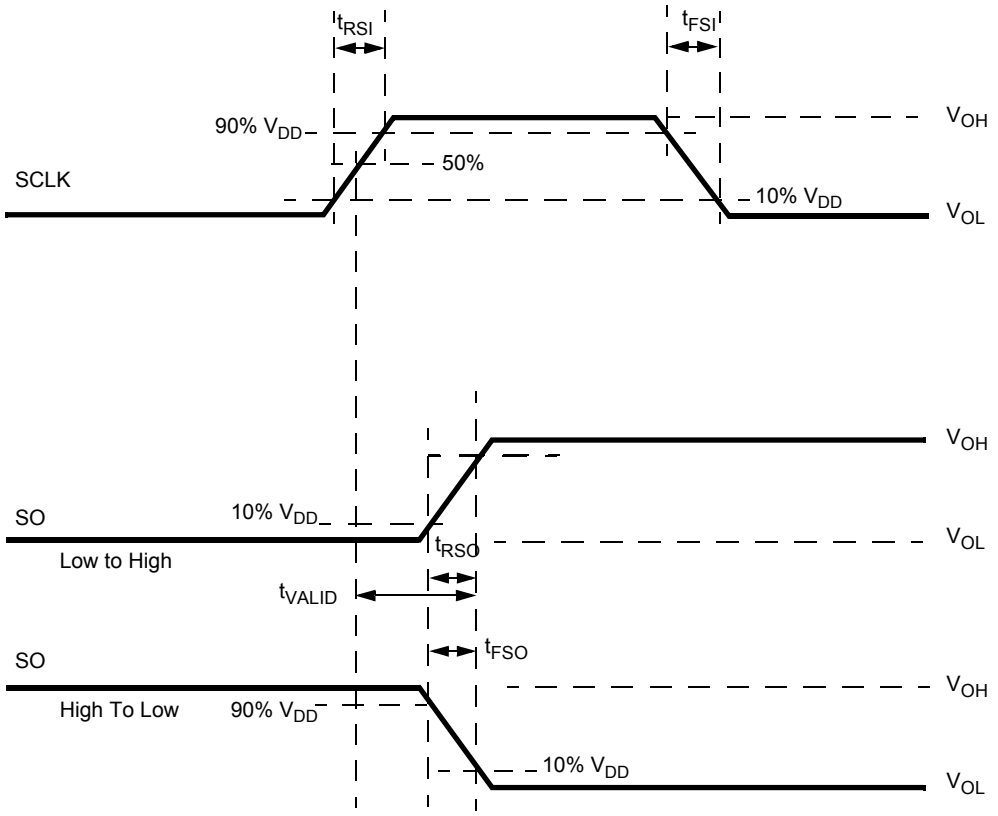

Figure 8. Timing Diagram for Serial Output (SO) Data Communication

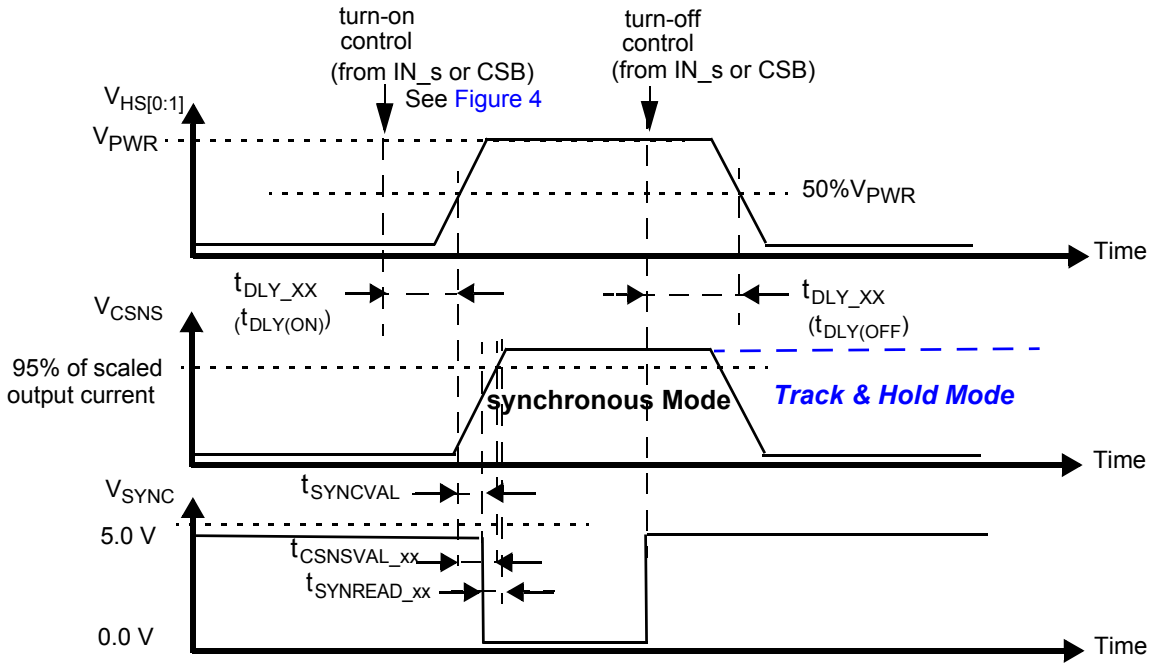

Figure 9. Synchronous & Track-and-Hold Current Sensing Modes: Associated Delay & Settling Times

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 06XS4200 is a two-channel, 24 V high-side switch with integrated control and diagnostics designed for truck, bus, and industrial applications. The device provides a high number of protective functions. Both low $R_{DS(on)}$ channels (< 6.0 mOhm) can independently drive various load types like light bulbs, solenoid actuators, or DC motors. Device control and diagnostics are configured through a 16-bit SPI port with daisy chain capability.

Independently programmable output voltage slew rates allow satisfying electromagnetic compatibility (EMC) requirements.

Both channels can independently be operated in several different switching modes: internal clock, internal PWM mode (fully autonomous operation), external clock, and direct control switching mode.

Current sensing with an adjustable ratio is available on both channels, allowing both high-current (bulbs) and low-current (LED) monitoring. By activating the Track & Hold mode, current monitoring can be performed during the switch-Off phase. This allows random access to the current sense functionality. A patented offset compensation technique further enhances current sense accuracy.

To avoid turning off during inrush current, while being able to monitor it, the device features a dynamic overcurrent threshold profile. For bulbs, this profile is a stair function with stages of which the height and width are programmable through the SPI port. DC motors can be protected from overheating by activating a specific window-shaped overcurrent profile that allows stall currents of limited duration.

Whenever communication with the external micro-controller is lost, the device enters Fail-safe Operation mode, but remains operational, controllable and protected.

PIN ASSIGNMENT AND FUNCTIONS

Functions and register bits that are implemented independently for both channels have extension "_s". Max. ratings of the pins are given in Table 3.

OUTPUT CURRENT MONITORING (CSNS)

The CSNS pin allows independent current monitoring of channel 0 or channel 1 up to the steady-state overcurrent threshold. It can also be used to sense the device temperature. The different functions are selected by setting bits CSNS1_en and CSNS0_en to the appropriate value (Table 12). When the CSNS pin is sensed during switch-off in the (optional) track & hold mode, it outputs the scaled value of the load current as it was just before turn-Off. When several devices share the same pull-down resistor, the CSNS pins of unused devices must be tri-stated. This is accomplished by setting CSNS0_en = 0 and CSNS1_en = 0 in the GCR register. Settling time ($t_{CSNSVAL\_XX}$) is defined as the time between the instant at the middle of the output voltage's rising edge (HS[0:1] = 50% of V_{PWR}), and the instant at which the voltage on the CSNS-pin has settled to ±5.0% of its final value. Anytime an overcurrent window is active, the CSNS pin is disabled (see Overcurrent Detection on Resistive and Inductive Loads). The current and temperature sensing functions are unavailable in Fail-safe mode and in Normal mode when operating without the V_{DD} supply voltage. In order to generate a voltage output, a pull-down resistor is required (R(CSNS) = 1.0 kOhm typ. and 470 < R(CSNS) < 10 k). When the current sense resistor connected to the CSNS pin is disconnected, the CSNS voltage is clamped to $V_{CL(CSNS)}$. The CSNS pin can source currents up to about 5.6 mA.

CURRENT SENSE SYNCHRONIZATION (SYNC)

To synchronize current sensing with an external process, the SYNC signal can be connected to a digital input of an external MCU. SYNC is asserted logic low when the current sense signal is accurate and ready to be read. The current sense signal on the CSNS pin has the specified accuracy $t_{SYNREAD\_XX}$ seconds after the falling edge on the SYNC pin (Figure 9) and remains valid until a rising edge is generated. The rising edge that is generated by the SYNC pin at the turn-OFF instant (internal or external) may also be used to implement synchronization with the external MCU. Parameter $t_{SYNCVAL\_XX}$ is defined as the time between the instant at the middle of the output-voltage rising edge (HS[0:1] = 50% of V_{PWR}), and the instant at which the voltage on the SYNC-pin drops below 0.4 V (V_{SOL}). The SYNC pins of different devices can be connected together to save micro-controller input channels. However, in this configuration, the CSNS function of only one device should be active at a time. Otherwise, the MCU does not determine the origin of the SYNC signal. The SYNC pin is open drain and requires an external pull-up resistor to V_{DD}.

DIRECT CONTROL INPUTS (IN0 AND IN1)

The IN[0:1] pins allow direct control of both channels. A logic [0] level turns off the channel and a logic[1] level turns it on (Channel Control in Normal Mode). When the device is in Sleep mode, a transition from logic 0 to logic 1 on any of these pins wake it up (Sleep Mode). If it is desired to automatically turn on the channels after a transition to Fail-safe mode, inputs IN[0] and IN[1] must be externally connected to the VPWR pin by a pull-up resistor (e.g. 10 kOhm typ.). However, this prevents the device from going