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# Dual 6.0 mOhm High Side Switch

The 06XSD200 device is part of a 36 V dual high side switch product family with integrated control and a high number of protective and diagnostic functions. It has been designed for industrial applications. The low  $R_{DS(ON)}$  channels ( $<6.0\text{ m}\Omega$ ) can control different load types; bulbs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit serial peripheral interface (SPI), allowing easy integration into existing applications.

Both channels can be controlled individually by external/internal clock-signals or by direct inputs. Using the internal clock allows fully autonomous device operation. Programmable output voltage slew rates (individually programmable) help improve EMC performance. To avoid shutting off the device during inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Switching current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a fail-safe operation mode, but remains operational, controllable, and protected.

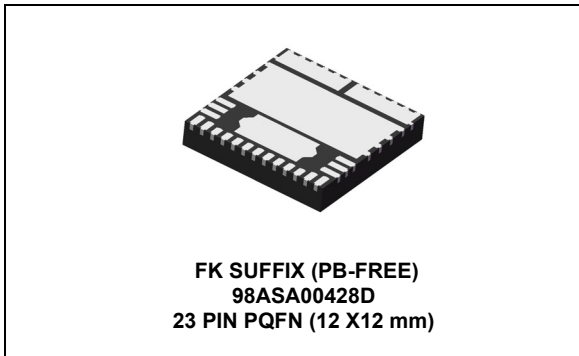
This device is powered by SMARTMOS technology.

### Features

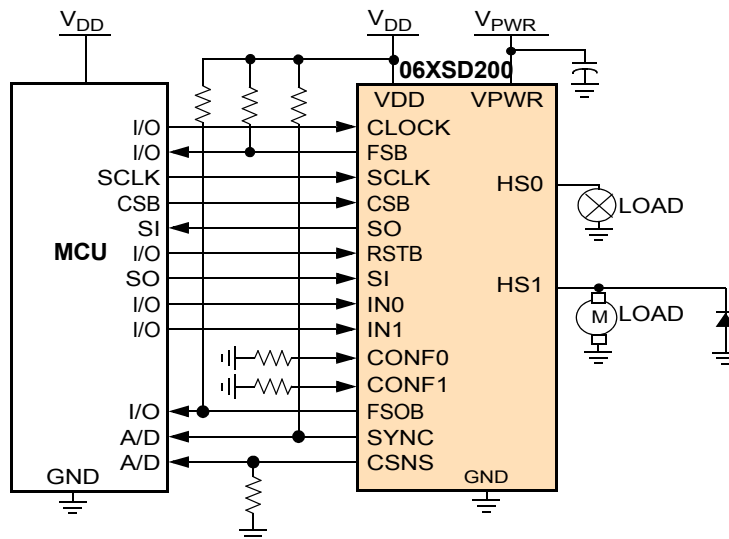
- Normal operating range: 8.0 - 36 V, extended range: 6.0 - 58 V, 3.3 V and 5.0 V compatible 16-bit SPI port for device control, configuration, and diagnostics at rates up to 8.0 MHz
- Two fully-protected 6.0 m $\Omega$  (@ 25 °C) high side switches
- Up to 9.0 A steady-state current per channel
- Separate bulb and DC motor latched overcurrent handling
- Parallel output operating mode with improved switching synchronization
- Individually programmable internal/external PWM clock signals (switching frequency, duty cycle, slew rate, switch-on time-shift)
- Overcurrent, short-circuit, and overtemperature protection with programmable auto-retry functions
- Accurate temperature and current sensing (high/low sensing ratios/offset compensation)
- OpenLoad detection (channel in OFF and ON state), also for LED applications (7.0 mA typ.)

**06XSD200**

**HIGH SIDE SWITCH**



| ORDERING INFORMATION |                                     |         |
|----------------------|-------------------------------------|---------|
| Device               | Temperature Range (T <sub>A</sub> ) | Package |
| MC06XSD200FK         | -40 to 125 °C                       | 23 PQFN |



**Figure 1. Simplified Application Diagram**

\*This document contains certain information on a product under development. Freescale reserves the right to change or discontinue this product without notice

### INTERNAL BLOCK DIAGRAM

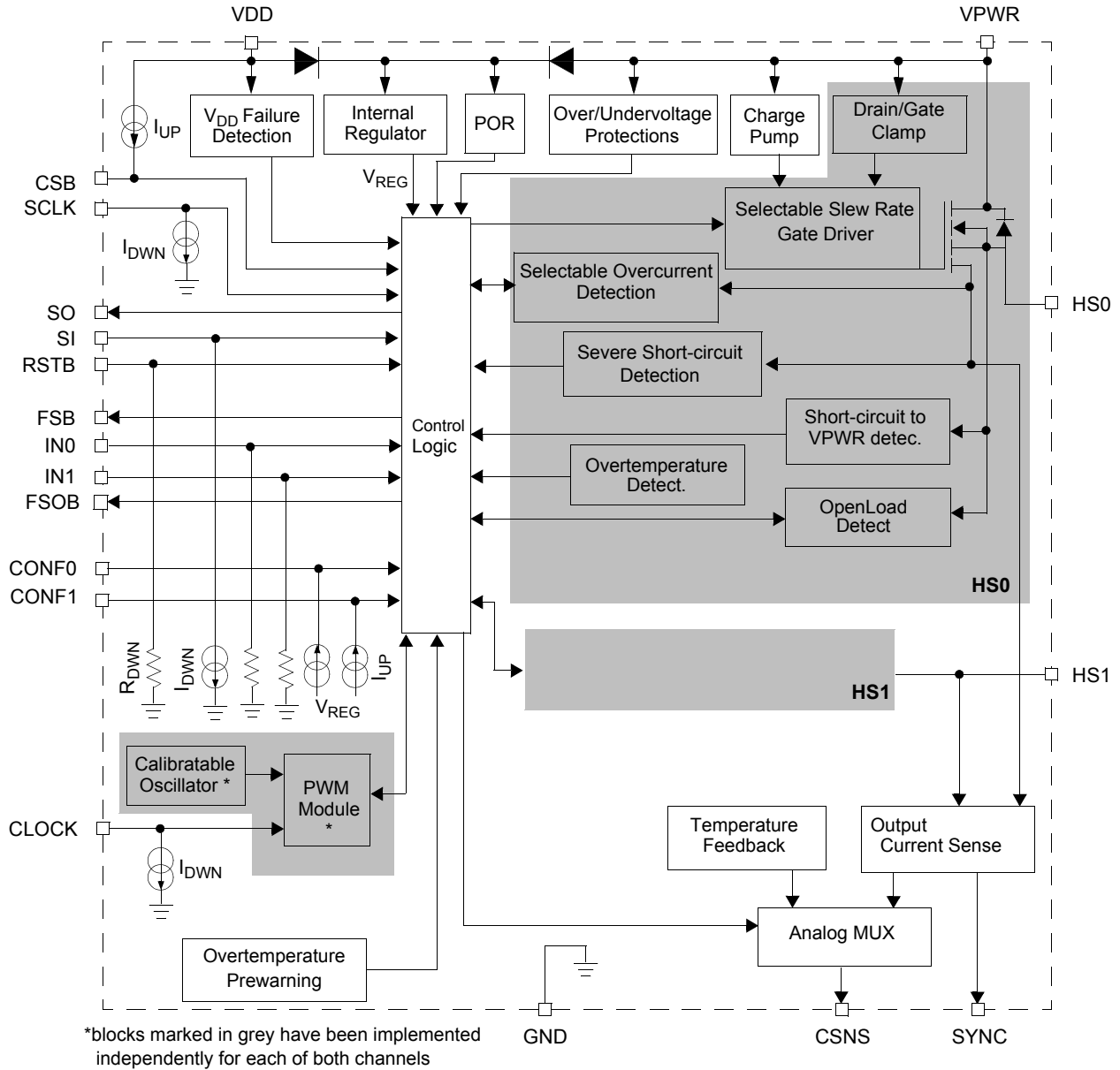


Figure 2. Internal Block Diagram

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## PIN CONNECTIONS

### Transparent Top View

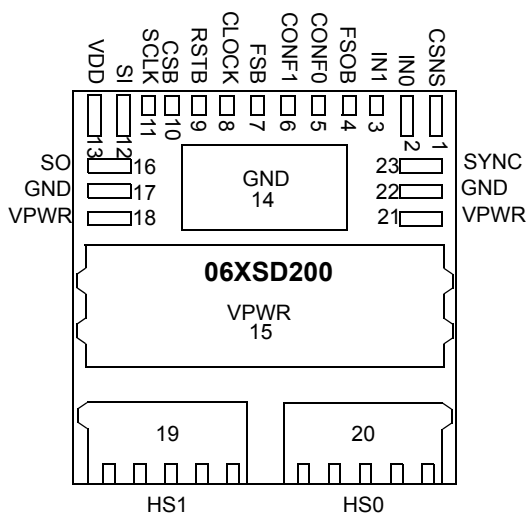


Figure 3. Device Pin Assignments

Table 1. 06XSD200 Pin Assignments

The function of each pin is described in the section [Functional Description](#)

| Pin Number | Pin Name       | Function | Formal Name                                  | Definition   |
|------------|----------------|----------|--|--|
| 1          | CSNS           | Output   | Output Current/<br>Temperature<br>Monitoring | This pin either outputs a current proportional to the channel's output current or a voltage proportional to the temperature of the GND pin (pin 14). Selection between current and temperature sensing, as well as setting the current sensing sensitivity are performed through the SPI interface. An external pull-down resistor must be connected between CSNS and GND. |
| 2<br>3     | IN0<br>IN1     | Input    | Direct Inputs                                | The IN[0:1] input pins are used to directly control the switching state of both switches and consequently the voltage on the HS0:HS1 output pins. The pins are connected to GND by internal pull-down resistors  |
| 4          | FSOB           | Output   | Fail-safe Output<br>(Active Low)             | FSOB is asserted (active-low) upon entering Fail-safe mode (see <a href="#">Functional Description</a> ) This open-drain output requires an external pull-up resistor to VPWR  |
| 5<br>6     | CONF0<br>CONF1 | Input    | Configuration Input                          | The CONF[0:1] input pins are used to select the appropriate overcurrent detection profile (bulb/DC motor) for each of both channels. CONF requires a pull-down resistor to GND.  |
| 7          | FSB            | Output   | Fault Status<br>(Active Low)                 | This open-drain output pin (external pull-up resistor to VDD required) is set when the device enters Fault mode (see <a href="#">Fault Mode</a> )  |
| 8          | CLOCK          | Input    | PWM Clock                                    | The clock input gives the time-base when the device is operated in external clock/internal PWM mode.<br><br>This pin has an internal pull-down current source.   |
| 9          | RSTB           | Input    | Reset  | This input pin is used to initialize the device's configuration - and fault registers. Reset puts the device in Sleep mode (low current consumption) provided it is not stimulated by direct input signals. This pin is connected to GND by an internal pull-down resistor.  |
| 10         | CSB            | Input    | Chip Select<br>(Active Low)                  | This input pin is connected to the SPI chip-select output of an external $\mu$ -controller. CSB is internally pulled up to VDD by a current source I <sub>UP</sub> .   |

**Table 1. 06XSD200 Pin Assignments (continued)**

 The function of each pin is described in the section [Functional Description](#)

| Pin Number | Pin Name   | Function | Formal Name                               | Definition  |
|------------|------------|----------|---|---|
| 11         | SCLK       | Input    | Serial Clock                              | This input pin is to be connected to an external SPI Clock signal. The SCLK pin is internally connected to a pull-down current source $I_{DWN}$   |
| 12         | SI         | Input    | Serial Input                              | This input pin receives the SPI input data from an external device (microcontroller or another extreme switch device in case of daisy-chaining). The SI pin is internally connected to a pull-down current source $I_{DWN}$   |
| 13         | VDD        | Power    | Digital Drain Voltage                     | This is the positive supply pin of the SPI interface.   |
| 16         | SO         | Output   | Serial Output                             | This output pin transmits SPI data to an external device (external microcontroller or the SI pin of the next SPI device in case of daisy-chaining). The pin doesn't require external pull-up or pull-down resistors, but a series resistor is recommended to limit current consumption in case of GND disconnection           |
| 14, 17, 22 | GND        | Ground   | Ground                                    | These pins, internally connected, are the ground pins for the logic - and analog circuitry. It is recommended to also connect these pins on the PCB.  |
| 15,18,21   | VPWR       | Power    | Positive Power Supply                     | These pins, internally connected, supply both the device's power and control circuitry (except the SPI port). The drain of both internal MOSFET switches is connected to them. Pin 15 is the device's primary thermal pad.  |
| 19<br>20   | HS1<br>HS0 | Output   | Power Switch Outputs                      | Output pins of the switches, to be connected to the load.   |
| 23         | SYNC       | Output   | Output Current Monitoring Synchronization | This output pin is asserted (active low) when the Current Sense (CS) output signal is within the specified accuracy range. Reading the SYNC pin allows the external microprocessor to synchronize to the device when operating in autonomous operating mode. SYNC is open-drain and requires a pull-up resistor to $V_{DD}$ . |

## ELECTRICAL CHARACTERISTICS

### MAXIMUM RATINGS

**Table 2. Maximum Ratings**

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

| Parameter   | Symbol   | Maximum ratings                                    | Unit |
|---|--|--|------|
| <b>ELECTRICAL RATINGS</b>   |  |  |      |
| VPWR Supply Voltage Range<br>Voltage Transient at 25 °C (500 ms)<br>Reverse Voltage at 25 °C<br>Fast Negative Transient Pulses (ISO 7637-2 pulse #1, $V_{PWR}=14V$ & $R_i=10\Omega$ )                         | $V_{PWR}$  | 58<br>-32<br>-60                                   | V    |
| VDD Supply Voltage Range  | $V_{DD}$   | -0.3 to 5.5  | V    |
| Voltage on Input pins <sup>(1)</sup> (except IN[0:1]) and Output pins <sup>(2)</sup> (except HS[0:1])   | $V_{MAX,LOGIC}$ <sup>(1)</sup>                       | -0.3 to 5.5  | V    |
| Voltage on Fail-safe Output (FSOB)  | $V_{FSO}$  | -0.3 to 58   | V    |
| Voltage on SO pin   | $V_{SO}$   | -0.3 to $V_{DD}+0.3$                               | V    |
| Voltage (continuous, max. allowable) on IN[0:1] Inputs  | $V_{IN,MAX}$   | 58   | V    |
| Voltage (continuous, max. allowable) on output pins (HS [0:1]),   | $V_{HS[0:1]}$  | -32 to 58  | V    |
| Rated Continuous Output Current per channel <sup>(3)</sup>  | $I_{HS[0:1]}$  | 9.0  | A    |
| Maximum allowable energy dissipation per channel and two parallel channels, single-pulse method <sup>(4)</sup>  | $E_{CL[0:1]_SING}$                                   | 250  | mJ   |
| ESD Voltage <sup>(5)</sup><br>Human Body Model (HBM) for HS[0:1], VPWR and GND<br>Human Body Model (HBM) for other pins<br>Charge Device Model (CDM)<br>Package Corner pins (1, 13, 19, 20)<br>All Other pins | $V_{ESD1}$<br>$V_{ESD2}$<br>$V_{ESD3}$<br>$V_{ESD4}$ | $\pm 8000$<br>$\pm 2000$<br>$\pm 750$<br>$\pm 500$ | V    |

Notes:

1. Concerned Input pins are: CONF[0:1], RSTB, SI, SCLK, Clock, and CSB.
2. Concerned Output pins are: CSNS, SYNC, and FSB.
3. Output current rating valid as long as maximum junction temperature is not exceeded. For computation of the maximum allowable output current, the thermal resistance of the package & the underlying heatsink must be taken into account
4. Single pulse Energy dissipation, Single-pulse short-circuit method ( $L_L = 0.5$  mH,  $R = 48$  m $\Omega$ ,  $V_{PWR} = 28$  V,  $T_J = 150$  °C initial).
5. ESD testing is performed in accordance with the Human Body Model (HBM) ( $C_{ZAP} = 100$  pF,  $R_{ZAP} = 1500$   $\Omega$ ), and the Charge Device Model (CDM), Robotic ( $C_{ZAP} = 4.0$  pF).

**Table 2. Maximum Ratings (continued)**

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

| Parameter   | Symbol          | Maximum ratings | Unit |
|---|-----------------|-----------------|------|
| <b>THERMAL RATINGS</b>  |                 |                 |      |
| Operating Temperature <sup>(6)</sup>  |                 |                 | °C   |
| Ambient   | $T_A$           | -40 to 125      |      |
| Junction  | $T_J$           | -40 to 150      |      |
| Storage Temperature   | $T_{STG}$       | -55 to 150      | °C   |
| Thermal Resistance / Junction to Case                                       | $R_{\theta JC}$ | <1.0            | °C/W |
| Reflow Peak Temperature on device pins during soldering <sup>(7), (8)</sup> | $T_{SOLDER}$    | 260             | °C   |

**Notes:**

6. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
7. 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device. MSL level is specified later.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.



### STATIC ELECTRICAL CHARACTERISTICS

**Table 3. Static Electrical Characteristics**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| parameter   | Symbol           | Min        | Typ      | Max          | Unit          |
|---|------------------|------------|----------|--------------|---------------|
| <b>SUPPLY ELECTRICAL CHARACTERISTICS</b>  |                  |            |          |              |               |
| Supply Voltage Range:<br>Full Specification compliant<br>Extended Mode <sup>(9)</sup>   | $V_{PWR}$        | 8.0<br>6.0 | –<br>–   | 36<br>58     | V             |
| $V_{PWR}$ Supply Current, device in wake-up mode, channel On, OpenLoad<br>Outputs in ON-state, HS[0:1] open, IN[0:1] > $V_{IH}$   | $I_{PWR(ON)}$    | –          | 6.5      | 8.0          | mA            |
| $V_{PWR}$ Supply Current, device in wake-up mode (Standby), channel Off<br>OpenLoad in OFF-state Detection Disabled, HS[0:1] shorted to<br>ground with $V_{DD} = 5.5\text{ V}$ and $\text{RSTB} > V_{WAKE}$ | $I_{PWR(SBY)}$   | –          | 6.5      | 8.0          | mA            |
| Sleep State Supply Current<br>$V_{PWR} = 24\text{ V}$ , $\text{RSTB} = \text{IN}[0:1] < V_{WAKE}$ , HS[0:1] connected to ground<br>$T_A = 25\text{ }^\circ\text{C}$<br>$T_A = 125\text{ }^\circ\text{C}$    | $I_{PWR(SLEEP)}$ | –<br>–     | 3.0<br>– | 10.0<br>60.0 | $\mu\text{A}$ |
| $V_{DD}$ Supply Voltage   | $V_{DD(ON)}$     | 3.0        | –        | 5.5          | V             |
| $V_{DD}$ Supply Current at $V_{DD} = 5.5\text{ V}$<br>No SPI Communication<br>8.0 MHz SPI Communication <sup>(10)</sup>   | $I_{DD(ON)}$     | –<br>–     | –<br>5.0 | 2.2<br>–     | mA            |
| $V_{DD}$ Sleep State Current at $V_{DD} = 5.5\text{ V}$ with or without $V_{PWR}$   | $I_{DD(SLEEP)}$  | –          | –        | 5.0          | $\mu\text{A}$ |
| Overvoltage Shutdown Threshold  | $V_{PWR(OV)}$    | 39         | 42       | 45.5         | V             |
| Overvoltage Shutdown Hysteresis   | $V_{PWR(OVHYS)}$ | 0.2        | 0.8      | 1.5          | V             |
| Undervoltage Shutdown Threshold <sup>(11)</sup>   | $V_{PWR(UV)}$    | 5.0        | –        | 6.0          | V             |
| $V_{PWR}$ Power-On-Reset (POR) Voltage Threshold <sup>(11)</sup>  | $V_{PWR(POR)}$   | 2.2        | 2.6      | 4.0          | V             |
| $V_{DD}$ Power-On-Reset (POR) Voltage Threshold <sup>(11)</sup>   | $V_{DD(POR)}$    | 1.5        | 2.0      | 2.5          | V             |
| $V_{DD}$ Supply Failure Voltage Threshold (assumed $V_{PWR} > V_{PWR(UV)}$ )  | $V_{DD(FAIL)}$   | 2.2        | 2.5      | 2.8          | V             |

**Notes**

9. In extended mode, availability of several device functions (channel control, value of  $R_{DS(ON)}$ , overtemperature protection) is guaranteed, but compliance with the specified values in this document is not. Below 6.0 V, the device is only protected from overheating (thermal shutdown). Above  $V_{PWR(OV)}$ , the channels can only be turned ON when the overvoltage detection function has been disabled.
10. Typical value guaranteed per design.
11. When the device recovers from undervoltage and returns to normal mode ( $6.0\text{ V} < V_{PWR} < 58\text{ V}$ ) before the end of the auto-retry period (see [Auto-retry](#)), the device performs normally. When  $V_{PWR}$  drops below  $V_{PWR(UV)}$ , undervoltage is detected (see [Undervoltage Fault \(Latchable Fault\)](#) and [EMC Performances](#)).

**Table 3. Static Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| parameter  | Symbol  | Min   | Typ  | Max  | Unit          |
|--|---|---|--|--|---------------|
| <b>ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1)</b>  |   |   |  |  |               |
| ON-Resistance, Drain-to-Source ( $I_{HS} = 3.0\text{ A}$ , $T_J = 25\text{ }^\circ\text{C}$ )<br>CSNS_ratio = 0<br>$V_{PWR} = 8.0\text{ V}$<br>$V_{PWR} = 28\text{ V}$<br>$V_{PWR} = 36\text{ V}$  | $R_{DS(ON)25}$  | –   | –  | 6.0  | m $\Omega$    |
| ON-Resistance, Drain-to-Source ( $I_{HS} = 3.0\text{ A}$ , $T_J = 150\text{ }^\circ\text{C}$ )<br>CSNS_ratio = 0<br>$V_{PWR} = 8.0\text{ V}$<br>$V_{PWR} = 28\text{ V}$<br>$V_{PWR} = 36\text{ V}$   | $R_{DS(ON)150}$   | –   | –  | 12   | m $\Omega$    |
| ON-Resistance, Drain-to-Source difference from one channel to the other in parallel mode ( $I_{HS} = 1.0\text{ A}$ , $T_J = 150\text{ }^\circ\text{C}$ ) CSNS_ratio = X  | $\Delta R_{DS(ON)150}$  | -0.7  | –  | +0.7   | m $\Omega$    |
| ON-Resistance, Source-Drain ( $I_{HS} = -3.0\text{ A}$ , $T_J = 150\text{ }^\circ\text{C}$ , $V_{PWR} = -24\text{ V}$ )  | $R_{SD(ON)150}$   | –   | –  | 12   | m $\Omega$    |
| Max. detectable wiring length (2.5 mm <sup>2</sup> ) for severe short-circuit detection (see <a href="#">Severe Short-circuit Fault (latchable fault)</a> ):<br>High slew rate selected<br>Medium slew rate selected:<br>Low slew rate selected:   | $L_{SHORT}$   | 14<br>30<br>60                                      | 48<br>100<br>200                                     | 80<br>170<br>340                                     | cm            |
| Overcurrent Detection thresholds with CSNS_ratio bit = 0 (CSR0)  | $I_{OCH1\_0}$<br>$I_{OCH2\_0}$<br>$I_{OCM1\_0}$<br>$I_{OCM2\_0}$<br>$I_{OCL1\_0}$<br>$I_{OCL2\_0}$<br>$I_{OCL3\_0}$ | 90.0<br>58.3<br>36.1<br>22.2<br>15.0<br>10.0<br>5.0 | 110.0<br>70.0<br>43.3<br>26.7<br>18.0<br>12.0<br>6.0 | 128.3<br>81.7<br>50.6<br>31.1<br>21.0<br>14.0<br>7.0 | A             |
| Overcurrent Detection thresholds with CSNS_ratio bit = 1 (CSR1)  | $I_{OCH1\_1}$<br>$I_{OCH2\_1}$<br>$I_{OCM1\_1}$<br>$I_{OCM2\_1}$<br>$I_{OCL1\_1}$<br>$I_{OCL2\_1}$<br>$I_{OCL3\_1}$ | 30.6<br>19.4<br>12.0<br>7.4<br>5.0<br>3.3<br>1.6    | 36.7<br>23.3<br>14.4<br>8.9<br>6.0<br>4.0<br>2.0     | 42.8<br>27.2<br>16.9<br>10.4<br>7.0<br>4.7<br>2.4    | A             |
| Output (HS[x]) leakage Current in sleep state (positive value = outgoing)<br>$V_{HS,OFF} = 0\text{ V}$ ( $V_{HS,OFF}$ = output voltage in OFF state)<br>$V_{HS,OFF} = V_{PWR}$ , device in sleep state ( $V_{PWR} = 24\text{ V}$ )<br>$V_{HS,OFF} = V_{PWR}$ , device in sleep state ( $V_{PWR} = 36\text{ V}$ ) | $I_{OUT\_LEAK}$   | –<br>-120<br>-1400                                  | –<br>–<br>–  | +16<br>+5.0<br>+5.0                                  | $\mu\text{A}$ |
| Switch Turn-on threshold for supply overvoltage ( $V_{PWR}$ -GND)  | $V_{D\_GND(CLAMP)}$   | 58  | –  | 66   | V             |
| Switch turn-on threshold for drain-source overvoltage (@ $I_{HS} = 100\text{ mA}$ )  | $V_{DS(CLAMP)}$   | 58  | –  | 66   | V             |
| Switch turn-on threshold for Drain-Source overvoltage difference from one channel to the other in parallel mode (@ $I_{HS} = 100\text{ mA}$ )  | $\Delta V_{DS(CLAMP)}$  | -2.0  | –  | +2.0   | V             |

**Table 3. Static Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| parameter   | Symbol                | Min  | Typ      | Max  | Unit          |
|---|-----------------------|------|----------|------|---------------|
| <b>ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)</b>   |                       |      |          |      |               |
| Current Sensing Ratio <sup>(12)</sup>   |                       |      |          |      | –             |
| CSNS_ratio bit = 0 (high-current mode)  | $C_{SR0}$             | –    | 1/5000   | –    |               |
| CSNS_ratio bit = 1 (low-current mode)   | $C_{SR1}$             | –    | 1/1666.6 | –    |               |
| Minimum measurable load current with compensated error <sup>(13)</sup> < 35%  | $I_{LOAD\_MIN}$       | –    | –        | 175  | mA            |
| CSNS leakage current in OFF state ( $CSNSx\_en = 0$ , $CSNS\_ratio$ bit_x = 0)  | $I_{CSR\_LEAK}$       | -4.0 | –        | +4.0 | $\mu\text{A}$ |
| Systematic offset error (see <a href="#">Current Sense Errors</a> )   | $I_{LOAD\_ERR\_SYS}$  | –    | -22      | –    | mA            |
| Random offset error   | $I_{LOAD\_ERR\_RAND}$ | -360 | –        | 360  | mA            |
| CSNS pin current sourcing capability, absolute upper limit  | $I_{CSNS\_MAX}$       | 5.15 | –        | –    | mA            |
| $E_{SR0}$ Output Current Sensing Error (% , uncompensated <sup>(14)</sup> ) at output Current level (Sense ratio $C_{SR0}$ selected): | $E_{SR0\_ERR}$        |      |          |      | %             |
| $T_J = -40\text{ }^\circ\text{C}$   |                       |      |          |      |               |
| 9.0 A   |                       | -13  | –        | 13   |               |
| 4.5 A   |                       | -12  | –        | 12   |               |
| 2.25 A  |                       | -17  | –        | 17   |               |
| 1.13 A  |                       | -31  | –        | 31   |               |
| $T_J = 125\text{ }^\circ\text{C}$   |                       |      |          |      |               |
| 9.0 A   |                       | -10  | –        | 10   |               |
| 4.5 A   |                       | -9.0 | –        | 9.0  |               |
| 2.25 A  |                       | -12  | –        | 12   |               |
| 1.13 A  |                       | -19  | –        | 19   |               |
| $T_J = 25\text{ to }125\text{ }^\circ\text{C}$  |                       |      |          |      |               |
| 9.0 A   |                       | -10  | –        | 10   |               |
| 4.5 A   |                       | -9.0 | –        | 9.0  |               |
| 2.25 A  |                       | -12  | –        | 12   |               |
| 1.13 A  |                       | -22  | –        | 22   |               |

Notes:

12. Current Sense Ratio  $C_{SRx} = I_{CSNS} / (I_{HS[x]} + I_{LOAD\_ERR\_SYS})$
13. See note (14), but with  $I_{CSNS\_MEAS}$  obtained after compensation of  $I_{LOAD\_ERR\_RAND}$  (see [Activation and Use of Offset Compensation](#)). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration
14.  $E_{SRx\_ERR} = (I_{CSNS\_MEAS} / I_{CSNS\_MODEL}) - 1$ , with  $I_{CSNS\_MODEL} = (I_{HS[x]} + I_{LOAD\_ERR\_SYS}) * C_{SRx}$ , ( $I_{LOAD\_ERR\_SYS}$  defined above, see section [Current Sense Error Model](#)). With this model, load current becomes:  $I_{HS[x]} = I_{CSNS} / C_{SRx} - I_{LOAD\_ERR\_SYS}$

**Table 3. Static Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| parameter   | Symbol               | Min | Typ | Max | Unit |
|---|----------------------|-----|-----|-----|------|
| <b>ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)</b>   |                      |     |     |     |      |
| $E_{SR0}$ Output Current Sensing Error (% , after offset compensation <sup>(15)</sup> ) at output Current level (Sense ratio $C_{SR0}$ selected):<br>$T_J = -40\text{ }^\circ\text{C}$<br>9.0 A<br>4.5 A<br>2.25 A<br>1.13 A<br>$T_J = 125\text{ }^\circ\text{C}$<br>9.0 A<br>4.5 A<br>2.25 A<br>1.13 A<br>$T_J = 25\text{ to }125\text{ }^\circ\text{C}$<br>9.0 A<br>4.5 A<br>2.25 A<br>1.13 A | $E_{SR0\_ERR(Comp)}$ |     |     |     | %    |
| $E_{SR1}$ Output Current Sensing Error (% , uncompensated <sup>(16)</sup> ) at output Current level (Sense ratio $C_{SR1}$ selected):<br>$T_J = -40\text{ }^\circ\text{C}$<br>2.25 A<br>$T_J = 125\text{ }^\circ\text{C}$<br>2.25 A<br>$T_J = 25\text{ to }125\text{ }^\circ\text{C}$<br>2.25 A   | $E_{SR1\_ERR}$       |     |     |     | %    |

**Notes:**

- See note <sup>(14)</sup>, but with  $I_{CSNS\_MEAS}$  obtained after compensation of  $I_{LOAD\_ERR\_RAND}$  (see [Activation and Use of Offset Compensation](#)). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration
- $E_{SRx\_ERR} = (I_{CSNS\_MEAS} / I_{CSNS\_MODEL}) - 1$ , with  $I_{CSNS\_MODEL} = (I(HS[x]) + I_{LOAD\_ERR\_SYS}) * C_{SRx}$ , ( $I_{LOAD\_ERR\_SYS}$  defined above, see section [Current Sense Error Model](#)). With this model, load current becomes:  $I(HS[x]) = I_{CSNS} / C_{SRx} - I_{LOAD\_ERR\_SYS}$

**Table 3. Static Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| parameter   | Symbol               | Min  | Typ | Max | Unit |
|---|----------------------|------|-----|-----|------|
| <b>ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)</b>   |                      |      |     |     |      |
| $E_{SR1}$ Output Current Sensing Error (% after offset compensation <sup>(17)</sup> ) at output Current level (Sense ratio $C_{SR1}$ selected):         | $E_{SR1\_ERR(Comp)}$ |      |     |     | %    |
| $T_J = -40\text{ }^\circ\text{C}$   |                      |      |     |     |      |
| 2.25 A  |                      | -10  | –   | 10  |      |
| 0.75 A  |                      | -11  | –   | 11  |      |
| 0.375 A   |                      | -18  | –   | 18  |      |
| 0.225 A   |                      | -29  | –   | 29  |      |
| $T_J = 125\text{ }^\circ\text{C}$   |                      |      |     |     |      |
| 2.25 A  |                      | -8.0 | –   | 8.0 |      |
| 0.75 A  |                      | -10  | –   | 10  |      |
| 0.375 A   |                      | -12  | –   | 12  |      |
| 0.225 A   |                      | -16  | –   | 16  |      |
| $T_J = 25\text{ to }125\text{ }^\circ\text{C}$  |                      |      |     |     |      |
| 2.25 A  |                      | -8.0 | –   | 8.0 |      |
| 0.75 A  |                      | -10  | –   | 10  |      |
| 0.375 A   |                      | -13  | –   | 13  |      |
| 0.225 A   |                      | -21  | –   | 21  |      |
| $E_{SR0}$ Output Current Sensing Error in parallel mode (% , uncompensated <sup>(18)</sup> ) at outputs Current level (Sense ratio $C_{SR0}$ selected): | $E_{SR0\_ERR\_PAR}$  |      |     |     | %    |
| $T_J = -40\text{ }^\circ\text{C}$   |                      |      |     |     |      |
| 9.0 A (per channel)   |                      | -10  | –   | 10  |      |
| 4.5 A (per channel)   |                      | -11  | –   | 11  |      |
| $T_J = 125\text{ }^\circ\text{C}$   |                      |      |     |     |      |
| 9.0 A (per channel)   |                      | -8.0 | –   | 8.0 |      |
| 4.5 A (per channel)   |                      | -8.0 | –   | 8.0 |      |
| $T_J = 25\text{ to }125\text{ }^\circ\text{C}$  |                      |      |     |     |      |
| 9.0 A (per channel)   |                      | -8.0 | –   | 8.0 |      |
| 4.5 A (per channel)   |                      | -8.0 | –   | 8.0 |      |

Notes:

- See note <sup>(18)</sup>, but with  $I_{CSNS\_MEAS}$  obtained after compensation of  $I_{LOAD\_ERR\_RAND}$  (see [Activation and Use of Offset Compensation](#)). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration.
- $E_{SRx\_ERR} = (I_{CSNS\_MEAS} / I_{CSNS\_MODEL}) - 1$ , with  $I_{CSNS\_MODEL} = (I(HS[x]) + I_{LOAD\_ERR\_SYS}) * C_{SRx}$ , ( $I_{LOAD\_ERR\_SYS}$  defined above, see section [Current Sense Error Model](#)). With this model, load current becomes:  $I(HS[x]) = I_{CSNS} / C_{SRx} - I_{LOAD\_ERR\_SYS}$

**Table 3. Static Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| parameter  | Symbol                         | Min                  | Typ                 | Max                  | Unit             |
|--|--------------------------------|----------------------|---------------------|----------------------|------------------|
| <b>ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)</b>  |                                |                      |                     |                      |                  |
| Current Sense Clamping Voltage (condition: $R(\text{CSNS}) > 10\text{ k}\Omega$ )  | $V_{CL(\text{CSNS})}$          | 5.5                  | –                   | 7.5                  | V                |
| OpenLoad detection Current threshold in OFF state <sup>(19)</sup>  | $I_{\text{OLD}(\text{OFF})}$   | 30                   | –                   | 100                  | $\mu\text{A}$    |
| OpenLoad Fault Detection Voltage Threshold <sup>(19)</sup>   | $V_{\text{OLD}(\text{THRES})}$ | 4.0                  | –                   | 5.5                  | V                |
| OpenLoad detection Current threshold in ON state (see <a href="#">OpenLoad Detection In On State (OL_ON)</a> ):<br>CSNS_ratio bit = 0<br>CSNS_ratio bit = 1 (fast slew rate $\text{SR}[1:0] = 10$ mandatory for this function) | $I_{\text{OLD}(\text{ON})}$    | 135<br>5.0           | 500.0<br>7.0        | 999.9<br>10          | mA               |
| Time period of the periodically activated OpenLoad in ON state detection for CSNS_ratio bit = 1  | $t_{\text{OLLED}}$             | 105                  | 150                 | 195                  | ms               |
| Output Shorted-to- $V_{PWR}$ Detection Voltage Threshold (channel in OFF state)  | $V_{\text{OSD}(\text{THRES})}$ | $V_{PWR}-1.2$        | $V_{PWR}-0.8$       | $V_{PWR}-0.4$        | V                |
| Switch turn-on threshold for Negative Output Voltages (protects against negative transients) - (measured at $I_{\text{OUT}} = 100\text{ mA}$ , Channel in OFF state)   | $V_{\text{CL}}$                | -38                  | –                   | -32                  | V                |
| Switch turn-on threshold for Negative Output Voltages difference from one channel to the other in parallel mode - (measured at $I_{\text{OUT}} = 100\text{ mA}$ , Channel in OFF state)  | $\Delta V_{\text{CL}}$         | -2.0                 | –                   | +2.0                 | V                |
| Switching State (On/Off) discrimination thresholds   | $V_{\text{HS\_TH}}$            | $0.45 \cdot V_{PWR}$ | $0.5 \cdot V_{PWR}$ | $0.55 \cdot V_{PWR}$ | V                |
| Shutdown temperature (Power MOSFET junction; $6.0\text{ V} < V_{PWR} < 58\text{ V}$ )  | $T_{\text{SD}}$                | 160                  | 175                 | 190                  | $^\circ\text{C}$ |

Notes:

19. Minimum required value of OpenLoad impedance for detection of OpenLoad in OFF-state:  $200\text{ k}\Omega$ . ( $V_{\text{OLD}(\text{THRES})} = V_{\text{HS}} @ I_{\text{OLD}(\text{OFF})}$ )



**Table 3. Static Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| parameter   | Symbol         | Min  | Typ | Max | Unit          |
|---|----------------|------|-----|-----|---------------|
| <b>ELECTRICAL CHARACTERISTICS OF THE CONTROL INTERFACE PINS</b>                   |                |      |     |     |               |
| Logic Input Voltage, High <sup>(20)</sup>   | $V_{IH}$       | 2.0  | –   | 5.5 | V             |
| Logic Input Voltage, Low <sup>(20)</sup>  | $V_{IL}$       | -0.3 | –   | 0.8 | V             |
| Wake-up Threshold Voltage (IN[0:1] and RSTB) <sup>(21)</sup>                      | $V_{WAKE}$     | 1.0  | –   | 2.2 | V             |
| Internal Pull-down Current Source (on Inputs: CLOCK, SCLK and SI) <sup>(22)</sup> | $I_{DWN}$      | 5.0  | –   | 20  | $\mu\text{A}$ |
| Internal Pull-up Current Source (input CSB) <sup>(23)</sup>                       | $I_{UP\_CSB}$  | 5.0  | –   | 20  | $\mu\text{A}$ |
| Internal Pull-up Current Source (input CONF[0:1]) <sup>(24)</sup>                 | $I_{UP\_CONF}$ | 25   | –   | 100 | $\mu\text{A}$ |
| Capacitance of SO, FSB and FSOB pins in Tri-state                                 | $C_{SO}$       | –    | –   | 20  | pF            |
| Internal Pull-down Resistance (RSTB and IN[0:1])                                  | $R_{DWN}$      | 125  | 250 | 500 | k $\Omega$    |
| Input Capacitance <sup>(25)</sup>   | $C_{IN}$       | –    | 4.0 | 12  | pF            |

**ELECTRICAL CHARACTERISTICS OF THE CONTROL INTERFACE PINS (CONTINUED)**

|   |                       |              |   |          |               |
|---|-----------------------|--------------|---|----------|---------------|
| SO High-state Output Voltage<br>( $I_{OH} = 1.0\text{ mA}$ )  | $V_{SOH}$             | $V_{DD}-0.4$ | – | –        | V             |
| SYNC, SO, FSOB and FSB Low-state Output Voltage<br>( $I_{OL} = -1.0\text{ mA}$ )  | $V_{SOL}$             | –            | – | 0.4      | V             |
| SYNC, SO, CSNS, FSOB and FSB Tri-state Leakage Current:<br>( $0\text{ V} < V(\text{SO}) < V_{DD}$ , or $V(\text{FS})$ or $V(\text{SYNC}) = 5.5\text{ V}$ , or $V(\text{FSO}) = 36\text{ V}$<br>or $V(\text{CSNS}) = 0\text{ V}$ ) | $I_{SO(\text{LEAK})}$ | -2.0         | 0 | 2.0      | $\mu\text{A}$ |
| CONF[0:1]: Required values of the External Pull-down Resistor   | $R_{CONF}$            |              |   |          | k $\Omega$    |
| Lighting applications   |                       | 1.0          | – | 10       |               |
| DC motor applications   |                       | 50           | – | Infinite |               |

Notes

20. High and low voltage ranges apply to SI, CSB, SCLK, RSTB, IN[0:1] and CLOCK input signals. The IN[0:1] signals may be derived from  $V_{PWR}$  and can tolerate voltages up to 58 V.
21. Voltage above which the device wakes up
22. Valid for  $V_{SI} \geq 0.8\text{ V}$  and  $V_{SCLK} \geq 0.8\text{ V}$  and  $V_{CLOCK} \geq 0.8\text{ V}$ .
23. Valid for  $V_{CSB} \leq 2.0\text{ V}$ . CSB has an internal pull-up current source derived from  $V_{DD}$
24. Pins CONF[0:1] are connected to an internal current source, derived from an internal voltage regulator ( $V_{REG} \sim 3.0\text{ V}$ ).
25. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CONF[0:1], and CLOCK pins. This parameter is guaranteed by the manufacturing process but is not tested in production.

### DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 4. Dynamic Electrical Characteristics**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| Parameter  | Symbol                                   | Min                    | Typ               | Max                    | Unit             |
|--|--|------------------------|-------------------|------------------------|------------------|
| <b>OUTPUT VOLTAGE SWITCHING CHARACTERISTICS</b>  |  |                        |                   |                        |                  |
| Rising and falling edge medium slew rate (SR[1:0] = 00) <sup>(26)</sup><br>$V_{PWR} = 16\text{ V}$<br>$V_{PWR} = 28\text{ V}$<br>$V_{PWR} = 36\text{ V}$   | SR <sub>R_00</sub><br>SR <sub>F_00</sub> | 0.164<br>0.28<br>0.34  | –<br>–<br>–       | 0.65<br>0.79<br>0.90   | V/ $\mu\text{s}$ |
| Rising edge low slew rate (SR[1:0] = 01) <sup>(26)</sup><br>$V_{PWR} = 16\text{ V}$<br>$V_{PWR} = 28\text{ V}$<br>$V_{PWR} = 36\text{ V}$  | SR <sub>R_01</sub><br>SR <sub>F_01</sub> | 0.081<br>0.14<br>0.17  | –<br>–<br>–       | 0.32<br>0.395<br>0.45  | V/ $\mu\text{s}$ |
| Rising edge high slew rate / SR[1:0] = 10) <sup>(26)</sup><br>$V_{PWR} = 16\text{ V}$<br>$V_{PWR} = 28\text{ V}$<br>$V_{PWR} = 36\text{ V}$  | SR <sub>R_10</sub><br>SR <sub>F_10</sub> | 0.29<br>0.55<br>0.68   | –<br>–<br>–       | 1.30<br>1.58<br>1.80   | V/ $\mu\text{s}$ |
| Rising/Falling edge slew rate matching per channel<br>$16\text{ V} < V_{PWR} < 36\text{ V}$  | SR <sub>R</sub> /SR <sub>F</sub>         | 0.65                   | –                 | 1.35                   |                  |
| Edge slew rate difference from one channel to the other in parallel mode <sup>(26)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$<br>SR[1:0] = 00<br>SR[1:0] = 01<br>SR[1:0] = 10  | $\Delta\text{SR}$                        | -0.12<br>-0.06<br>-0.2 | 0.0<br>0.0<br>0.0 | +0.12<br>+0.06<br>+0.2 | V/ $\mu\text{s}$ |
| Output Turn-ON and Turn-OFF Delays (medium slew rate: SR[1:0] = 00) <sup>(27)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$   | t <sub>DLY_00</sub>                      | 30                     | -                 | 160                    | $\mu\text{s}$    |
| Output Turn-ON and Turn-OFF Delays (low slew rate / SR[1:0] = 01) <sup>(27)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$   | t <sub>DLY_01</sub>                      | 50                     | -                 | 300                    | $\mu\text{s}$    |
| Output Turn-ON and Turn-OFF Delays (high slew rate / SR[1:0] = 10) <sup>(27)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$  | t <sub>DLY_10</sub>                      | 15                     | -                 | 80                     | $\mu\text{s}$    |
| Turn-ON and Turn-OFF Delay time matching per channel (t <sub>DLY(ON)</sub> - t <sub>DLY(OFF)</sub> )<br>f <sub>PWM</sub> = 400 Hz, $16\text{ V} < V_{PWR} < 36\text{ V}$ , duty cycle on IN[x] = 50 %, SR[1:0] = 00  | $\Delta t_{RF_00}$                       | -25                    | 0.0               | 25                     | $\mu\text{s}$    |
| Turn-ON and Turn-OFF Delay time matching per channel (t <sub>DLY(ON)</sub> - t <sub>DLY(OFF)</sub> )<br>f <sub>PWM</sub> = 200 Hz, $16\text{ V} < V_{PWR} < 36\text{ V}$ , duty cycle on IN[x] = 50 %, SR[1:0] = 01  | $\Delta t_{RF_01}$                       | -90                    | 0.0               | 90                     | $\mu\text{s}$    |
| Turn-ON and Turn-OFF Delay time matching per channel (t <sub>DLY(ON)</sub> - t <sub>DLY(OFF)</sub> )<br>f <sub>PWM</sub> = 1.0 kHz, $16\text{ V} < V_{PWR} < 36\text{ V}$ , duty cycle on IN[x] = 50 %, SR[1:0] = 10   | $\Delta t_{RF_10}$                       | -13                    | 0.0               | 13                     | $\mu\text{s}$    |
| <b>Notes</b>   |  |                        |                   |                        |                  |
| 26. Rising and Falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 $\Omega$ resistive load (see Figure 4).  |  |                        |                   |                        |                  |
| 27. Turn-on delay time measured as delay between a rising edge of the channel control signal (IN[0:1] = 1) and the associated rising edge of the output voltage up to: $V_{HS[0:1]} = V_{PWR} / 2$ (where $R_L = 5.0\text{ }\Omega$ ). Turn-OFF delay time is measured as time between a falling edge of the channel control signal (IN[0:1] = 0) and the associated falling edge of the output voltage up to the instant at which: $V_{HS[0:1]} = V_{PWR} / 2$ ( $R_L = 10.0\text{ }\Omega$ ) |  |                        |                   |                        |                  |

**Table 4. Dynamic Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| Parameter   | Symbol                         | Min               | Typ               | Max            | Unit          |
|---|--------------------------------|-------------------|-------------------|----------------|---------------|
| <b>SWITCHING CHARACTERISTICS (CONTINUED)</b>  |                                |                   |                   |                |               |
| Delay time difference from one channel to the other in parallel mode <sup>(28)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$<br>SR[1:0] = 00<br>SR[1:0] = 01<br>SR[1:0] = 10 | $\Delta t_{(DLY)}$             | -25<br>-50<br>-12 | 0.0<br>0.0<br>0.0 | 25<br>50<br>12 | $\mu\text{s}$ |
| Fault Detection Delay Time <sup>(29)</sup>  | $t_{FAULT}$                    | -                 | 5.0               | 8.0            | $\mu\text{s}$ |
| Output Shutdown Delay Time <sup>(30)</sup>  | $t_{DETECT}$                   | -                 | 12.0              | 17             | $\mu\text{s}$ |
| Current sense output settling Time for SR[1:0] = 00 (medium slew rate)<br>$V_{PWR} = 28\text{ V}$ <sup>(31)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$ <sup>(31)</sup>    | $t_{CSNSVAL\_00}$              | -<br>0.0          | 104<br>-          | -<br>250       | $\mu\text{s}$ |
| Current sense output settling Time for SR[1:0] = 01 (low slew rate)<br>$V_{PWR} = 28\text{ V}$ <sup>(31)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$ <sup>(31)</sup>       | $t_{CSNSVAL\_01}$              | -<br>0.0          | 167<br>-          | -<br>355       | $\mu\text{s}$ |
| Current sense output settling Time for SR[1:0] = 10 (high slew rate)<br>$V_{PWR} = 28\text{ V}$ <sup>(31)</sup><br>$16\text{ V} < V_{PWR} < 36\text{ V}$ <sup>(31)</sup>      | $t_{CSNSVAL\_10}$              | -<br>0.0          | 76<br>-           | -<br>210       | $\mu\text{s}$ |
| SYNC output signal delay for SR[1:0] = 00 (medium SR) <sup>(31)</sup>   | $t_{SYNCVAL\_00}$              | 50                | -                 | 160            | $\mu\text{s}$ |
| SYNC output signal delay for SR[1:0] = 01 (low SR) <sup>(31)</sup>  | $t_{SYNCVAL\_01}$              | 80                | -                 | 320            | $\mu\text{s}$ |
| SYNC output signal delay for SR[1:0] = 10 (high SR) <sup>(31)</sup>   | $t_{SYNCVAL\_10}$              | 22                | -                 | 80             | $\mu\text{s}$ |
| Recommended sync_to_read delay SR[1:0] = 00 (medium slew rate) <sup>(31)</sup>  | $t_{SYNREAD\_00}$              | 0.0               | -                 | 200            | $\mu\text{s}$ |
| Recommended sync_to_read delay SR[1:0] = 01 (low slew rate) <sup>(31)</sup>   | $t_{SYNREAD\_01}$              | 0.0               | -                 | 300            | $\mu\text{s}$ |
| Recommended sync_to_read delay SR[1:0] = 10 (high slew rate) <sup>(31)</sup>  | $t_{SYNREAD\_10}$              | 0.0               | -                 | 200            | $\mu\text{s}$ |
| Upper overcurrent threshold duration  | $t_{OCH1}$<br>$t_{OCH2}$       | 6.0<br>12.0       | 8.6<br>17.2       | 11.2<br>22.4   | ms            |
| Medium overcurrent threshold duration (CONF = 0; Lighting Profile)  | $t_{OCM1\_L}$<br>$t_{OCM2\_L}$ | 48<br>96          | 67<br>137         | 87<br>178      | ms            |
| Medium overcurrent threshold duration (CONF = 1; DC motor Profile)  | $t_{OCM1\_M}$<br>$t_{OCM2\_M}$ | 150<br>301        | 214<br>429        | 278<br>557     | ms            |

**FREQUENCY & PWM DUTY CYCLE RANGES** <sup>(32)</sup> (protections fully operational, see [Protective Functions](#))

|  |                |     |   |      |    |
|--|----------------|-----|---|------|----|
| Switching Frequency range - Direct Inputs                                  | $f_{CONTROL}$  | 0.0 | - | 1000 | Hz |
| Switching Frequency range - External clock with internal PWM (recommended) | $f_{PWM\_EXT}$ | 20  | - | 1000 | Hz |

Notes:

28. Rising and Falling edge slew rates specified for a 20% to 80% voltage variation on a  $10.0\ \Omega$  resistive load (see [Figure 4](#)).
29. Time required to detect and report the fault to the FSB pin.
30. Time required to switch off the channel after detection of overtemperature (OT), overcurrent (OC), SC or UV error (time measured between start of the negative edge on the FSB pin and the falling edge on the output voltage until  $V(\text{HS}[0:1]) = 50\%$  of  $V_{PWR}$ ).
31. Settling time ( $= t_{CSNSVAL\_XX}$ ), SYNC output signal delay ( $= t_{SYNCVAL\_XX}$ ) and Read-out delay ( $= t_{SYNREAD\_XX}$ ) are defined for a stepped load current using a  $10\ \Omega$  resistive load for  $\text{CSNS\_RATIO\_s} = 0$ . (see [Figure 9](#) and [Output Current Monitoring \(CSNS\)](#)).
32. In Direct Input mode, the lower frequency limit is 0 Hz with  $\text{RSTB} = 5.0\text{ V}$  and 4.0 Hz with  $\text{RSTB} = 0\text{ V}$ . Duty-cycle applies to instants at which  $V_{HS} = 50\% V_{PWR}$ . For low duty-cycle values, the effective value also depends on the value of the selected slew rate.

**Table 4. Dynamic Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| Parameter  | Symbol            | Min               | Typ         | Max             | Unit          |
|--|-------------------|-------------------|-------------|-----------------|---------------|
| <b>FREQUENCY &amp; PWM DUTY CYCLE RANGES (CONTINUED)</b> <sup>(33)</sup> (protections fully operational, see <a href="#">Protective Functions</a> )  |                   |                   |             |                 |               |
| Switching Frequency range - Internal clock with internal PWM (recommended)   | $f_{PWM\_INT}$    | 60                | –           | 1000            | Hz            |
| Duty Cycle range   | $R_{CONTROL}$     | 0.0               | –           | 100             | %             |
| <b>AVAILABILITY DIAGNOSTIC FUNCTIONS OVER DUTY-CYCLE AND SWITCHING FREQUENCY</b><br><b>(PROTECTIONS &amp; DIAGNOSTICS BOTH FULLY OPERATIONAL, SEE <a href="#">DIAGNOSTIC FEATURES</a> FOR THE EXACT BOUNDARY VALUES)</b> |                   |                   |             |                 |               |
| Available Duty Cycle Range, $f_{PWM} = 1.0\text{ kHz}$ high slew rate, PWM mode <sup>(34)</sup><br>OL_OFF<br>OL_ON<br>OS   | $R_{PWM\_1K\_H}$  | 0.0<br>35<br>0.0  | –<br>–<br>– | 62<br>100<br>90 | %             |
| Available Duty Cycle Range, $f_{PWM} = 400\text{ Hz}$ , medium slew rate, PWM mode <sup>(34)</sup><br>OL_OFF<br>OL_ON<br>OS  | $R_{PWM\_400\_M}$ | 0.0<br>21<br>0.0  | –<br>–<br>– | 81<br>100<br>88 | %             |
| Available Duty Cycle Range, $f_{PWM} = 400\text{ Hz}$ , high slew rate, PWM mode <sup>(34)</sup><br>OL_OFF<br>OL_ON<br>OS  | $R_{PWM\_400\_H}$ | 0.0<br>14<br>0.0  | –<br>–<br>– | 84<br>100<br>95 | %             |
| Available Duty Cycle Range, $f_{PWM} = 200\text{ Hz}$ , low slew rate mode, PWM mode <sup>(34)</sup><br>OL_OFF<br>OL_ON<br>OS  | $R_{PWM\_200\_L}$ | 0.0<br>15<br>0.0  | –<br>–<br>– | 86<br>100<br>93 | %             |
| Available Duty Cycle Range, $f_{PWM} = 200\text{ Hz}$ , medium slew rate, PWM mode <sup>(34)</sup><br>OL_OFF<br>OL_ON<br>OS  | $R_{PWM\_200\_M}$ | 0.0<br>11<br>0.0  | –<br>–<br>– | 90<br>100<br>94 | %             |
| Available Duty Cycle Range, $f_{PWM} = 100\text{ Hz}$ in low slew rate, PWM mode <sup>(34)</sup><br>OL_OFF<br>OL_ON<br>OS  | $R_{PWM\_100\_L}$ | 0.0<br>8.0<br>0.0 | –<br>–<br>– | 93<br>100<br>96 | %             |
| Deviation of the internal clock PWM frequency after Calibration <sup>(35)</sup>  | $A_{FPWM(CAL)}$   | -10               | –           | +10             | %             |
| Default output frequency when using an uncalibrated oscillator   | $f_{PWM(0)}$      | 280               | 400         | 520             | Hz            |
| Minimal required Low Time during Calibration of the Internal Clock through CSB   | $t_{CSB(MIN)}$    | 1.0               | 1.5         | 2.0             | $\mu\text{s}$ |
| Maximal allowed Low Time during Calibration of the Internal Clock through CSB  | $t_{CSB(MAX)}$    | 70                | 100         | 130             | $\mu\text{s}$ |
| Recommended external Clock Frequency Range (external clock/PWM Module)   | $f_{CLOCK}$       | 15                | –           | 512             | kHz           |
| Upper detection threshold for external clock frequency monitoring  | $f_{CLOCK(MAX)}$  | 512               | 730         | 930             | kHz           |
| Lower detection threshold for external clock frequency monitoring  | $f_{CLOCK(MIN)}$  | 5.0               | 7.0         | 10              | kHz           |

**Notes**

33. In Direct Input mode, the lower frequency limit is 0 Hz with  $\text{RSTB}=5.0\text{ V}$  and 4.0 Hz with  $\text{RSTB}=0\text{V}$ . Duty-cycle applies to instants at which  $V_{HS} = 50\% V_{PWR}$ . For low duty-cycle values, the effective value also depends on the value of the selected slew rate.
34. Actually, the device can be operated outside the specified duty cycle and frequency ranges (basic protective functions OC, SC, UV, OV, OT remain active) but the availability of the diagnostic functions OL\_ON, OL\_OFF, OS is affected.
35. Values guaranteed from 60 Hz to 1.0 kHz (recommended switching frequency range for internal clock operation).

**Table 4. Dynamic Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------|--------|-----|-----|-----|------|
|-----------|--------|-----|-----|-----|------|

**TIMING: SPI PORT, IN[0]/ IN[1] SIGNALS & AUTORETRY**

|   |                |      |      |      |    |
|---|----------------|------|------|------|----|
| Required Low time allowing delatching or triggering sleep mode (direct input mode)      | $t_{IN}$       | 175  | 250  | 325  | ms |
| Watchdog Timeout for entering Fail-safe Mode due to loss of SPI contact <sup>(36)</sup> | $t_{WDTO}$     | 217  | 310  | 400  | ms |
| Auto-Retry Repetition Period (when activated):  |                |      |      |      | ms |
| Auto_period bits = 00   | $t_{AUTO\_00}$ | 105  | 150  | 195  |    |
| Auto_period bits = 01   | $t_{AUTO\_01}$ | 52.5 | 75   | 97.5 |    |
| Auto_period bits = 10   | $t_{AUTO\_10}$ | 26.2 | 37.5 | 47.8 |    |
| Auto_period bits = 11   | $t_{AUTO\_11}$ | 13.1 | 17.7 | 24.4 |    |

**GND PIN TEMPERATURE SENSING FUNCTION**

|  |                        |      |      |      |                        |
|--|------------------------|------|------|------|------------------------|
| Thermal Prewarning Detection Threshold <sup>(37)</sup>   | $T_{OTWAR}$            | 110  | 125  | 140  | $^{\circ}\text{C}$     |
| Temperature Sensing output voltage @ $T_A = 25\text{ }^{\circ}\text{C}$ ( $470\text{ }\Omega < R_{CSNS} < 10\text{ k}\Omega$ )                                   | $T_{FEED}$             | 918  | 1078 | 1238 | mV                     |
| Gain Temperature Sensing output @ $T_A = 25\text{ }^{\circ}\text{C}$ ( $470\text{ }\Omega < R_{CSNS} < 10\text{ k}\Omega$ ) <sup>(37)</sup>                      | $DT_{FEED}$            | 10.7 | 11.1 | 11.5 | mV/ $^{\circ}\text{C}$ |
| Temperature Sensing Error, range $[-40\text{ }^{\circ}\text{C}, 150\text{ }^{\circ}\text{C}]$ , default <sup>(37)</sup>  | $T_{FEED\_ERROR}$      | -15  | –    | +15  | $^{\circ}\text{C}$     |
| Temperature Sensing Error, $[-40\text{ }^{\circ}\text{C}, 150\text{ }^{\circ}\text{C}]$ after 1 point calibration @ $25\text{ }^{\circ}\text{C}$ <sup>(37)</sup> | $T_{FEED\_ERROR\_CAL}$ | -5.0 | –    | +5.0 | $^{\circ}\text{C}$     |

Notes

- 36. Only when the WD\_dis bit set to logic [0] (default). Watchdog timeout defined from the rising edge on RST to rising edge HS[0,1]
- 37. Values were obtained by lab characterization.

**Table 4. Dynamic Electrical Characteristics (continued)**

Unless specified otherwise:  $8.0\text{ V} \leq V_{PWR} \leq 36\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ . Typical values are average values evaluated under nominal conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{PWR} = 28\text{ V}$  &  $V_{DD} = 5.0\text{ V}$ , unless specified otherwise.

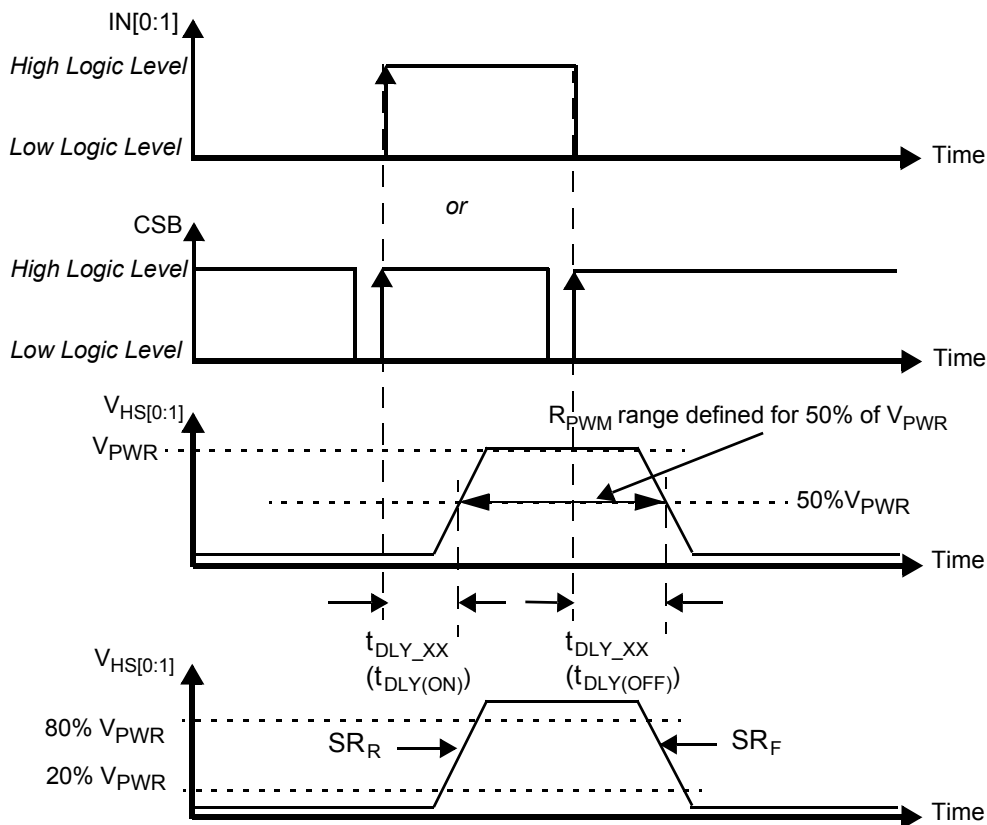
| Parameter   | Symbol              | Min | Typ | Max | Unit          |
|---|---------------------|-----|-----|-----|---------------|
| <b>SPI INTERFACE ELECTRICAL CHARACTERISTICS<sup>(38)</sup></b>  |                     |     |     |     |               |
| Maximum Operating Frequency of the Serial Peripheral Interface (SPI) <sup>(39)</sup>                  | $f_{\text{SPI}}$    | –   | –   | 8.0 | MHz           |
| Required Low-state Duration for reset RSTB <sup>(40)</sup>  | $t_{\text{WRSTB}}$  | 10  | –   | –   | $\mu\text{s}$ |
| Required duration from the Rising to the Falling Edge of CSB (Required Setup Time) <sup>(41)</sup>    | $t_{\text{CSB}}$    | 1.0 | –   | –   | $\mu\text{s}$ |
| Rising Edge of RSTB to Falling Edge of CSB (Required Setup Time) <sup>(41)</sup>                      | $t_{\text{ENBL}}$   | 5.0 | –   | –   | $\mu\text{s}$ |
| Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time) <sup>(41)</sup>                      | $t_{\text{LEAD}}$   | 500 | –   | –   | ns            |
| Falling Edge of SCLK to Rising Edge of CSB (Required Setup lag Time) <sup>(41)</sup>                  | $t_{\text{LAG}}$    | 60  | –   | –   | ns            |
| Required High State Duration of SCLK (Required Setup Time) <sup>(41)</sup>                            | $t_{\text{WSCLKh}}$ | 50  | –   | –   | ns            |
| Required Low State Duration of SCLK (Required Setup Time) <sup>(41)</sup>                             | $t_{\text{WSCLKl}}$ | 50  | –   | –   | ns            |
| SI to Falling Edge of SCLK (Required Setup Time) <sup>(42)</sup>                                      | $t_{\text{SI(SU)}}$ | 15  | –   | –   | ns            |
| Falling Edge of SCLK to SI (Required hold Time of the SI signal) <sup>(42)</sup>                      | $t_{\text{SI(H)}}$  | 30  | –   | –   | ns            |
| SO Rise Time<br>$C_L = 80\text{ pF}$  | $t_{\text{RSO}}$    | –   | –   | 20  | ns            |
| SO Fall Time<br>$C_L = 80\text{ pF}$  | $t_{\text{FSO}}$    | –   | –   | 20  | ns            |
| SI, CSB, SCLK, Max. Rise Time allowing operation at $f_{\text{SPI}} = 8.0\text{ MHz}$ <sup>(42)</sup> | $t_{\text{RSI}}$    | –   | –   | 11  | ns            |
| SI, CSB, SCLK, Max. Fall Time allowing operation at $f_{\text{SPI}} = 8.0\text{ MHz}$ <sup>(42)</sup> | $t_{\text{FSI}}$    | –   | –   | 11  | ns            |
| Time from Rising Edge of SCLK to reach a valid level at the SO pin <sup>(43)</sup>                    | $t_{\text{VALID}}$  | –   | –   | 44  | ns            |
| Time from Falling Edge of CSB to reach low-impedance on SO (access time) <sup>(44)</sup>              | $t_{\text{SOEN}}$   | –   | –   | 30  | ns            |
| Time from Rising Edge of CSB to reach high-impedance on SO pin (turn off time)                        | $t_{\text{SODIS}}$  |     |     | 30  | ns            |

**Notes:**

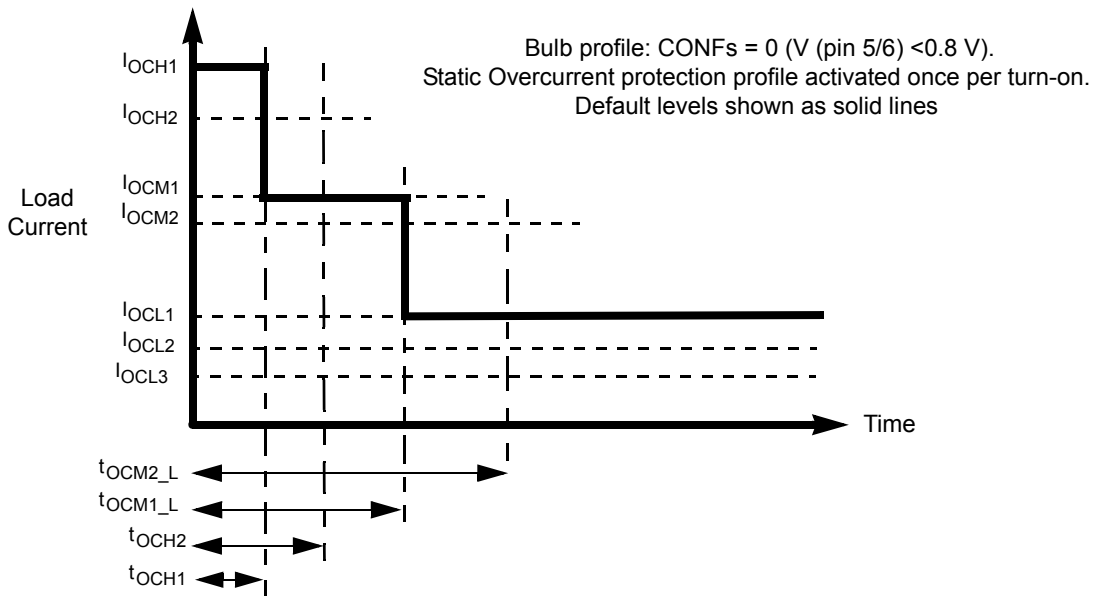
38. Parameters guaranteed by design. It is recommended to tie unused SPI-pins to GND by resistors  $1.0\text{ k} < R < 10\text{ k}$
39. For clock frequencies  $> 4.0\text{ MHz}$ , series resistors on the SPI pins should preferably be removed. Otherwise,  $470\text{ pF}$  ( $V_{\text{MAX}} > 40\text{ V}$ ) ceramic speed-up capacitors in parallel with the  $> 8.0\text{ k}\Omega$  input resistors are required on pins SCLK, SI, SO, CS
40. RSTB low duration is defined as the minimum time required to switch off the channel when previously put ON in SPI mode (direct inputs inactive).
41. Minimum setup time required for the device is the minimum required time that the microcontroller must wait or remain in a given state.
42. Rise and Fall time of incoming SI, CSB, and SCLK signals.
43. Time required for output data to be available for use at SO, measured with a  $80\text{ pF}$  capacitive load.
44. Time required for output data to be terminated at SO measured without a series resistor connected CSB.



**TIMING DIAGRAMS**



**Figure 4. Output Voltage Slew Rate and Delay**



**Figure 5. Overcurrent Protection Profile for Bulb Applications**

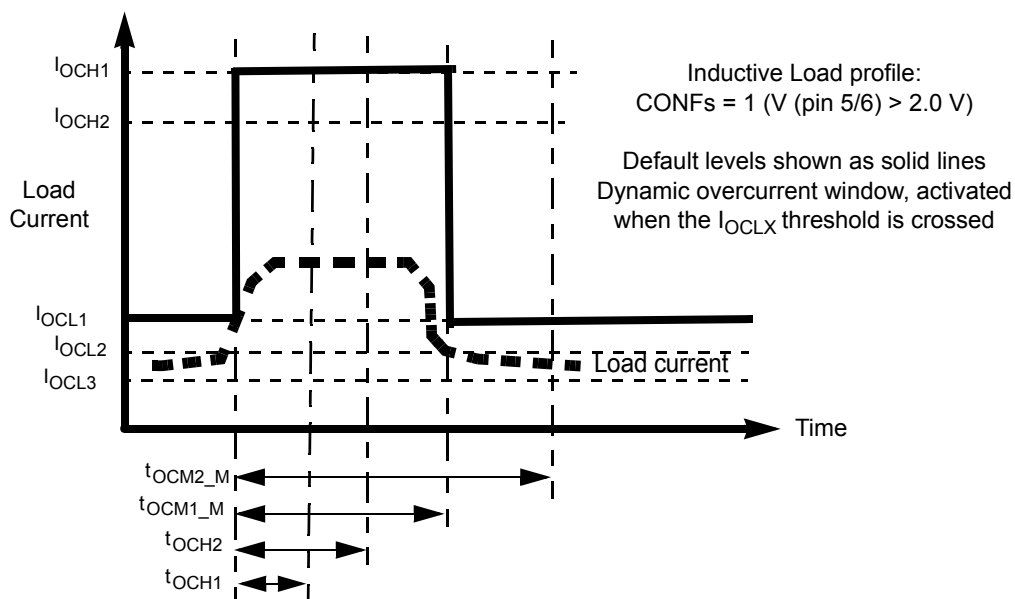


Figure 6. Overcurrent Protection Profile for Applications with Inductive Loads (DC motors, solenoids)

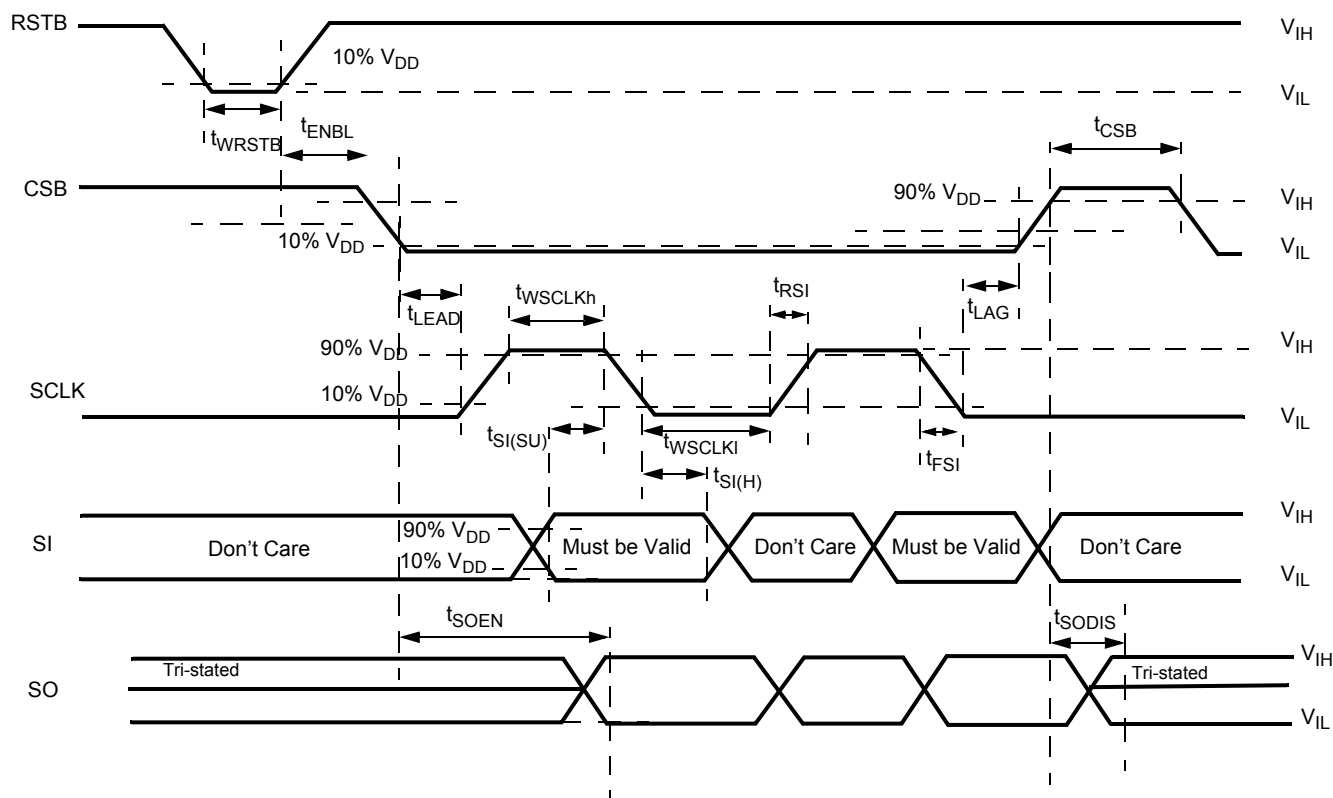


Figure 7. Timing Requirements During SPI Communication

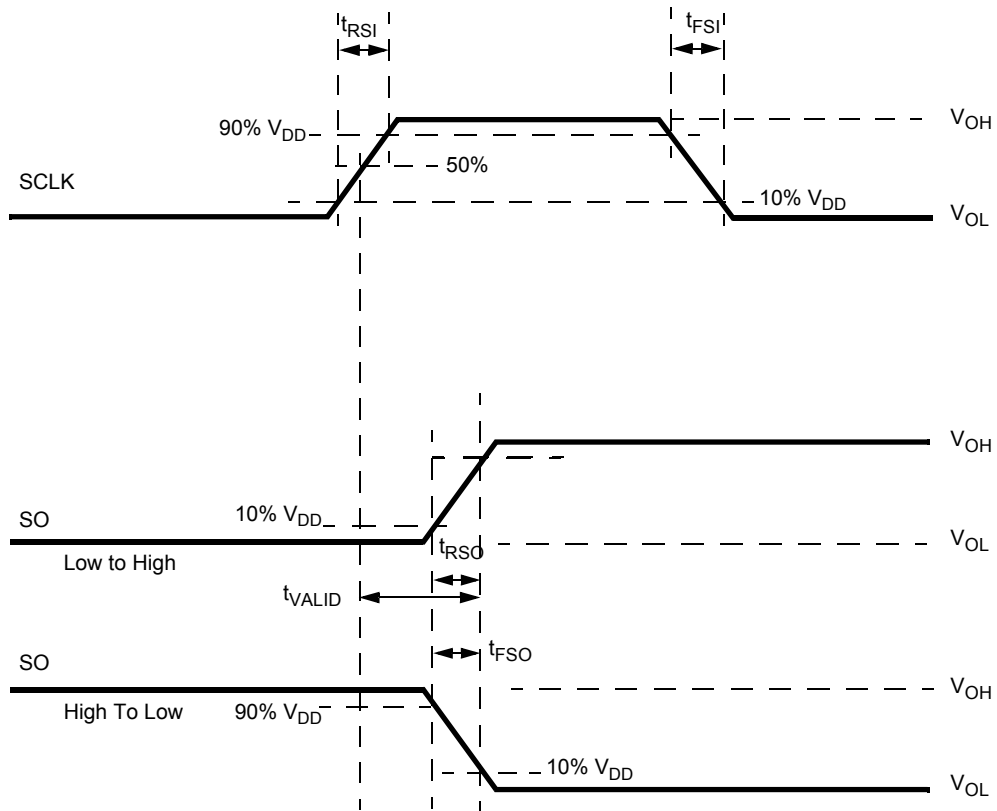


Figure 8. Timing Diagram for Serial Output (SO) Data Communication

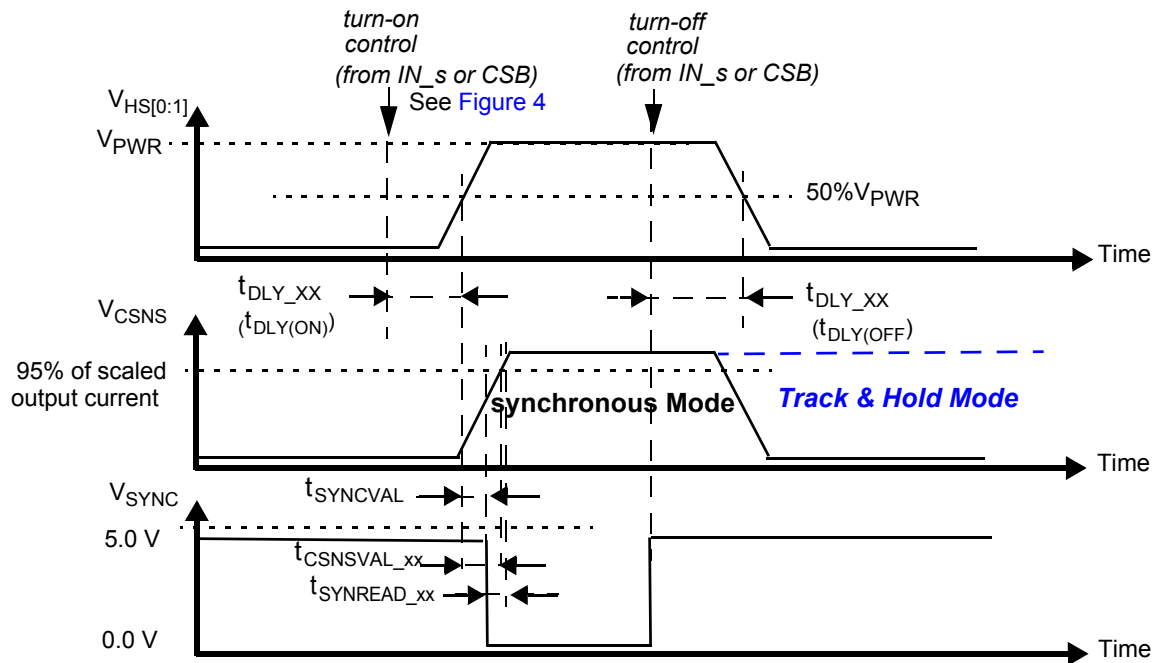


Figure 9. Synchronous & Track-and-Hold Current Sensing Modes: Associated Delay & Settling Times

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 06XSD200 is a two-channel, high side switch that can sustain up to 36 V, with integrated control and diagnostics designed for industrial applications. The device provides a high number of protective functions. Both low  $R_{DS(ON)}$  channels (<6.0 m $\Omega$ ) can independently drive various load types like light bulbs, solenoid actuators, or DC motors. Device control and diagnostics are configured through a 16-bit SPI port with daisy chain capability.

Independently programmable output voltage slew rates allow satisfying electromagnetic compatibility (EMC) requirements.

Both channels can independently be operated in several different switching modes: internal clock, internal PWM mode (fully autonomous operation), external clock, and direct control switching mode.

Current sensing with an adjustable ratio is available on both channels, allowing both high current (bulbs) and low

current (LED) monitoring. By activating the Track & Hold mode, current monitoring can be performed during the switch-Off phase. This allows random access to the current sense functionality. A patented offset compensation technique further enhances current sense accuracy.

To avoid turning off during inrush current, while being able to monitor it, the device features a dynamic overcurrent threshold profile. For bulbs, this profile is a stair function with stages of which the height and width are programmable through the SPI port. DC motors can be protected from overheating by activating a specific window-shaped overcurrent profile that allows stall currents of limited duration.

Whenever communication with the external micro-controller is lost, the device enters Fail-safe Operation mode, but remains operational, controllable and protected.

### PIN ASSIGNMENT AND FUNCTIONS

Functions and register bits that are implemented independently for both channels have extension “\_s”. Max. ratings of the pins are given in [Table 2](#).

#### OUTPUT CURRENT MONITORING (CSNS)

The CSNS pin allows independent current monitoring of channel 0 or channel 1 up to the steady-state overcurrent threshold. It can also be used to sense the device temperature. The different functions are selected by setting bits CSNS1\_en and CSNS0\_en to the appropriate value ([Table 11](#)). When the CSNS pin is sensed during switch-off in the (optional) track & hold mode, it outputs the scaled value of the load current as it was just before turn-Off. When several devices share the same pull-down resistor, the CSNS pins of unused devices must be tri-stated. This is accomplished by setting CSNS0\_en = 0 and CSNS1\_en = 0 in the GCR register. Settling time ( $t_{CSNSVAL\_XX}$ ) is defined as the time between the instant at the middle of the output voltage's rising edge ( $HS[0:1] = 50\%$  of  $V_{PWR}$ ), and the instant at which the voltage on the CSNS-pin has settled to  $\pm 5.0\%$  of its final value. Anytime an overcurrent window is active, the CSNS pin is disabled (see [Overcurrent Detection on Resistive and Inductive Loads](#)). The current and temperature sensing functions are unavailable in Fail-safe mode and in Normal mode when operating without the  $V_{DD}$  supply voltage. In order to generate a voltage output, a pull-down resistor is required ( $R(CSNS) = 1.0$  k $\Omega$  typ. and  $470 < R(CSNS) < 10$  k). When the current sense resistor connected to the CSNS pin is disconnected, the CSNS voltage is clamped to  $V_{CL(CSNS)}$ . The CSNS pin can source currents up to about 5.6 mA.

#### CURRENT SENSE SYNCHRONIZATION (SYNC)

To synchronize current sensing with an external process, the SYNC signal can be connected to a digital input of an external MCU. SYNC is asserted logic low when the current sense signal is accurate and ready to be read. The current sense signal on the CSNS pin has the specified accuracy  $t_{SYNCREAD\_XX}$  seconds after the falling edge on the SYNC pin ([Figure 9](#)) and remains valid until a rising edge is generated. The rising edge that is generated by the SYNC pin at the turn-OFF instant (internal or external) may also be used to implement synchronization with the external MCU. Parameter  $t_{SYNCVAL\_XX}$  is defined as the time between the instant at the middle of the output-voltage rising edge ( $HS[0:1] = 50\%$  of  $V_{PWR}$ ), and the instant at which the voltage on the SYNC-pin drops below 0.4 V ( $V_{SOL}$ ). The SYNC pins of different devices can be connected together to save micro-controller input channels. However, in this configuration, the CSNS function of only one device should be active at a time. Otherwise, the MCU does not determine the origin of the SYNC signal. The SYNC pin is open drain and requires an external pull-up resistor to  $V_{DD}$ .

#### DIRECT CONTROL INPUTS (IN0 AND IN1)

The IN[0:1] pins allow direct control of both channels. A logic [0] level turns off the channel and a logic[1] level turns it on ([Channel Control in Normal Mode](#)). When the device is in Sleep mode, a transition from logic 0 to logic 1 on any of these pins wakes up the device ([Sleep Mode](#)). If it is desired to automatically turn on the channels after a transition to Fail-safe mode, inputs IN[0] and IN[1] must be externally connected to the VPWR pin by a pull-up resistor (e.g. 10 k $\Omega$  typ.). However, this prevents the device from going into Sleep

mode. Both IN pins are internally connected to a pull-down resistor.

### CONFIGURATION INPUTS (CONF0 AND CONF1)

The CONF[0:1] input pins allow configuring both channels for the appropriate load type. CONF = 0 activates the bulb overcurrent protection profile, and CONF = 1 the DC motor profile. These inputs are connected to an internal voltage regulator of 3.3 V by an internal pull-up current source  $I_{UP}$ . Therefore, CONF = 1 is the default value when these pins are disconnected. Details on how to configure the channels are given in the table [Overcurrent Profile Selection](#).

### FAULT STATUS (FSB)

This open-drain output is asserted low when any of the following faults occurs (see [Fault Mode](#)): overcurrent (OC), overtemperature (OT), Output connected to  $V_{PWR}$ , Severe short-circuit (SC), OpenLoad in ON state (OL\_ON), OpenLoad in OFF state (OL\_OFF), External Clock-fail (CLOCK\_fail), overvoltage (OV), and undervoltage (UV). Each fault type has its own assigned bit inside the STATR, FAULTR\_s, or DIAGR\_s register. Fault type identification and fault bit reset are accomplished by reading out these registers. They are part of the SO register ([Table 12](#)) and are accessed through the SPI port.

### PWM CLOCK (CLOCK)

This pin is the input for an external clock signal that controls the internal PWM module. The clock signal is monitored by the device. The PWM module controls ON-time and turn-ON delay of the selected channels. The CLOCK pin should not be confused with the SCLK pin, which is the clock pin of the SPI interface. CLOCK has an internal pull-down current source ( $I_{DWN}$ ) to GND.

### RESET (RSTB)

All SPI register contents are reset when RSTB = 0. When RSTB = 0, the device returns to Sleep mode  $t_{IN}$  sec. after the last falling edge of the last active IN[0:1] signal. As long as the Reset input (RSTB pin) is at logic 0 and both direct input states are low, the device remains in Sleep mode ([Channel configuration through the SPI](#)). A 0-to-1 transition on RSTB wakes up the device and starts a watchdog timer to check the continuous presence of the SPI signals. To do this, the device monitors the contents of the first bit (WDIN bit) of all SPI words following that transition (regardless the register it is contained in). When this contents is not alternated within a duration  $t_{WDTO}$ , SPI communication is considered lost, and Fail-safe mode is entered ([Entering Fail-safe Mode](#)). RSTB is internally pulled-down to GND by resistor  $R_{DWN}$ .

### CHIP SELECT (CSB)

Data communication over the SPI port is enabled when the CSB pin is in the logic [0] state. Data from the Input Shift registers are locked in the addressed SI registers on the rising edge of CSB. The device transfers the contents of one of the 8 internal registers to the SO register on the falling

edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is at logic [0] ([Figure 7](#) and [Figure 8](#)). CSB is internally pulled up to  $V_{DD}$  through  $I_{UP}$ .

### SPI SERIAL CLOCK (SCLK)

The SCLK pin clocks the SPI data communication of the device. The serial input pin (SI) transfers data to the SI shift registers on the falling edge of the SCLK signal while data in the SO registers are transferred to the SO pin on the rising edge of the SCLK signal. The SCLK pin must be in the low state when CSB makes any transition. For this reason, it is recommended to have the SCLK pin in the logic [0] state when the device is not accessed (CSB is at logic [1]). When CSB is set to logic [1], signals at the SCLK and SI pins are ignored and the SO output is tri-stated (high-impedance). The SCLK pin is connected to an internal pull-down current source  $I_{DWN}$ .

### SERIAL INPUT (SI)

Serial input (SI) data bits are shifted in at this pin. SI data is read on the falling edge of SCLK. 16-bit data packages are required on the SI pin (see [Figure 7](#)), starting with bit D15 (MSB) and ending with D0 (LSB). All the internal device registers are addressed and controlled by a 4-bit address (D9-D12) described in [Table 10](#). Register addresses and function attribution are described in [Table 11](#). The SI pin is internally connected to a pull-down current source,  $I_{DWN}$ .

### SUPPLY OF THE DIGITAL CIRCUITRY (VDD)

This pin supplies the SPI circuit (3.3 V or 5.0 V). When lost, all circuitry becomes supplied by a  $V_{PWR}$  derived voltage, except the SPI's SO shift-register that can no longer be read.

### GROUND (GND)

This is the GND pin common for both the SPI and the other circuitry.

### POSITIVE SUPPLY PIN (VPWR)

This pin is the positive supply and the common input pin of both switches. A 100 nF ceramic capacitor must be connected between VPWR and GND, close to the device. In addition, it is recommended to put a ceramic capacitor of at least 1.0  $\mu$ F in parallel with this 100 nF capacitor.

### SERIAL OUTPUT (SO)

The SO pin is a tri-stateable output pin that conveys data from one of the 13 internal SO registers or from the previous SI register to the outside world. The SO pin remains in a high-impedance state (tri-state) until the CSB pin becomes logic [0]. It then transfers the SPI data (device state, configuration, fault information). The SO pin changes state at the rising edge of the SCLK signal. For daisy-chaining, it can be read out on the falling edge of SCLK.  $V_{DD}$  must be present

before the SO registers can be read. The SO register assignment is described in [Table 12](#).

- 20%) is recommended between these pins and GND for optimal EMC performances.

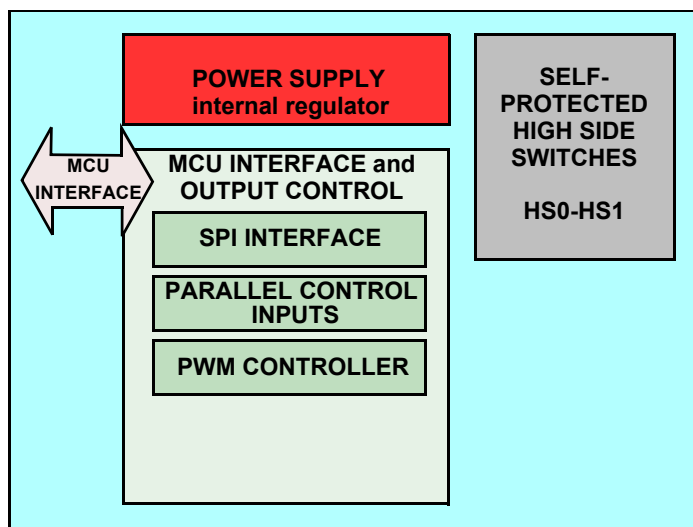
**POWER SWITCH OUTPUT PINS (HS0 AND HS1)**

HS0 and HS1 are the output pins of the power switches, to be connected to the loads. A ceramic capacitor ( $\leq 22$  nF (+/

**FAIL-SAFE OUTPUT (FSOB)**

This pin (active low) is used to indicate loss of SPI communication or loss of SPI supply voltage,  $V_{DD}$ . This open-drain output requires an external pull-up resistor to VPWR.

**FUNCTIONAL INTERNAL BLOCK DESCRIPTION**



**POWER SUPPLY**

The device operates with supply voltages from 6.0 to 58 V ( $V_{PWR}$ ), but is full spec. compliant between 8.0 and 36 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VDD pin (5.0 V typ.) supplies the output register of the Serial Peripheral Interface (SPI). Consequently, the SPI registers cannot be read without presence of  $V_{DD}$ . The employed IC architecture guarantees a low quiescent current in Sleep mode.

**SWITCH OUTPUT PINS HS0 & HS1**

HS0 and HS1 are the output pins of the power switches. Both channels are protected against various kinds of short-circuits and have active clamp circuitry that may be activated when switching off inductive loads. Many protective and diagnostic functions are available. For large inductive loads, it is recommended to use a freewheeling diode. The device can be configured to control the output switches in parallel, which guarantees good switching synchronization.

**COMMUNICATION INTERFACE AND DEVICE CONTROL**

In Normal mode the output channels can either be controlled by the direct inputs or by the internal PWM module, which is configured by the SPI register settings. For bidirectional SPI communication,  $V_{DD}$  has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: OpenLoad, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, undervoltage, and overvoltage. The SPI port can be supplied either by a 5.0 V or by a 3.3 V voltage supply. For direct input control,  $V_{DD}$  is not required.

A Pulse Width Modulation (PWM) circuit allows driving loads at frequencies up to 1.0 kHz from an external or an internal clock. SPI communication is required to set these options.