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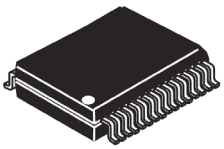
Document Number: MC07XS3200
Rev. 5.0, 8/2018

Dual high-side switch (7.0 mOhm)

07XS3200

HIGH-SIDE SWITCH



EK SUFFIX PB-FREE
98ASA00368D
32-PIN EXPOSED PAD SOIC

The 07XS3200 is one in a family of SMARTMOS devices designed for low-voltage automotive lighting applications. Two low $R_{DS(on)}$ MOSFETs (dual 7.0 mΩ) can control two separate 55 W bulbs, and/or Xenon modules, and/or LEDs.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 07XS3200 allows the user to program via the SPI, the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide fail-safe functionality of the outputs in case of MCU damaged.

The 07XS3200 is packaged in a Pb-free power-enhanced 32 pins SOIC package with exposed pad.

Features

- Dual 7.0 mΩ max high-side switch (at 25 °C)
- Operating voltage range of 6.0 to 20 V with sleep current < 5.0 µA, extended mode from 4.0 V to 28 V
- 8.0 MHz 16-bit 3.3 V and 5.0 V SPI control and status reporting with daisy chain capability
- PWM module using external clock or calibratable internal oscillator with programmable outputs delay management
- Smart overcurrent shutdown compliant to huge inrush current, severe short-circuit, overtemperature protections with time limited autoretry, and Fail-safe mode, in case of MCU damage
- Output off or on openload detection compliant to bulbs or LEDs and short to battery detection. Analog current feedback with selectable ratio and board temperature feedback.

Applications

- Low-voltage automotive lighting
  - Halogen bulbs
  - Incandescent bulbs
  - HID Xenon ballasts
- Low-voltage industrial lighting

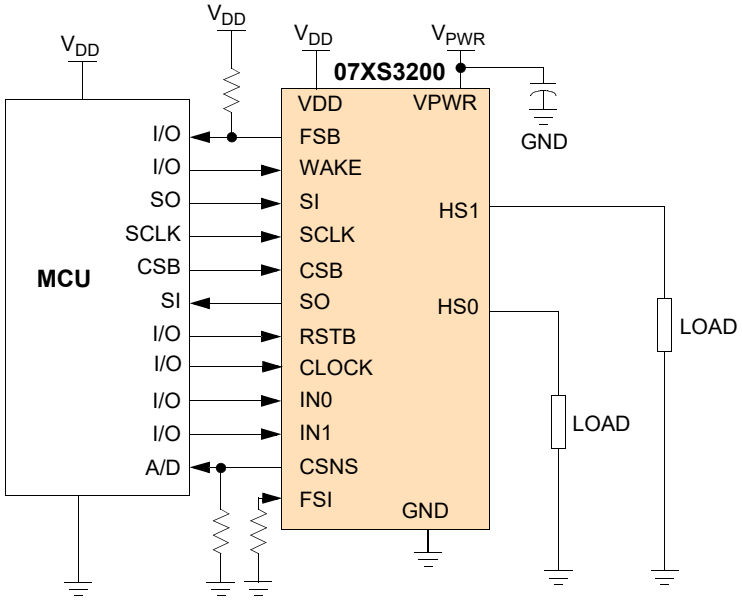


Figure 1. 07XS3200 simplified application diagram

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1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package
MC07XS3200EK (1)	-40 °C to 125 °C	32-pin SOIC

Notes
1. To order parts in tape and reel, add the R2 suffix to the part number.

2 Internal block diagram

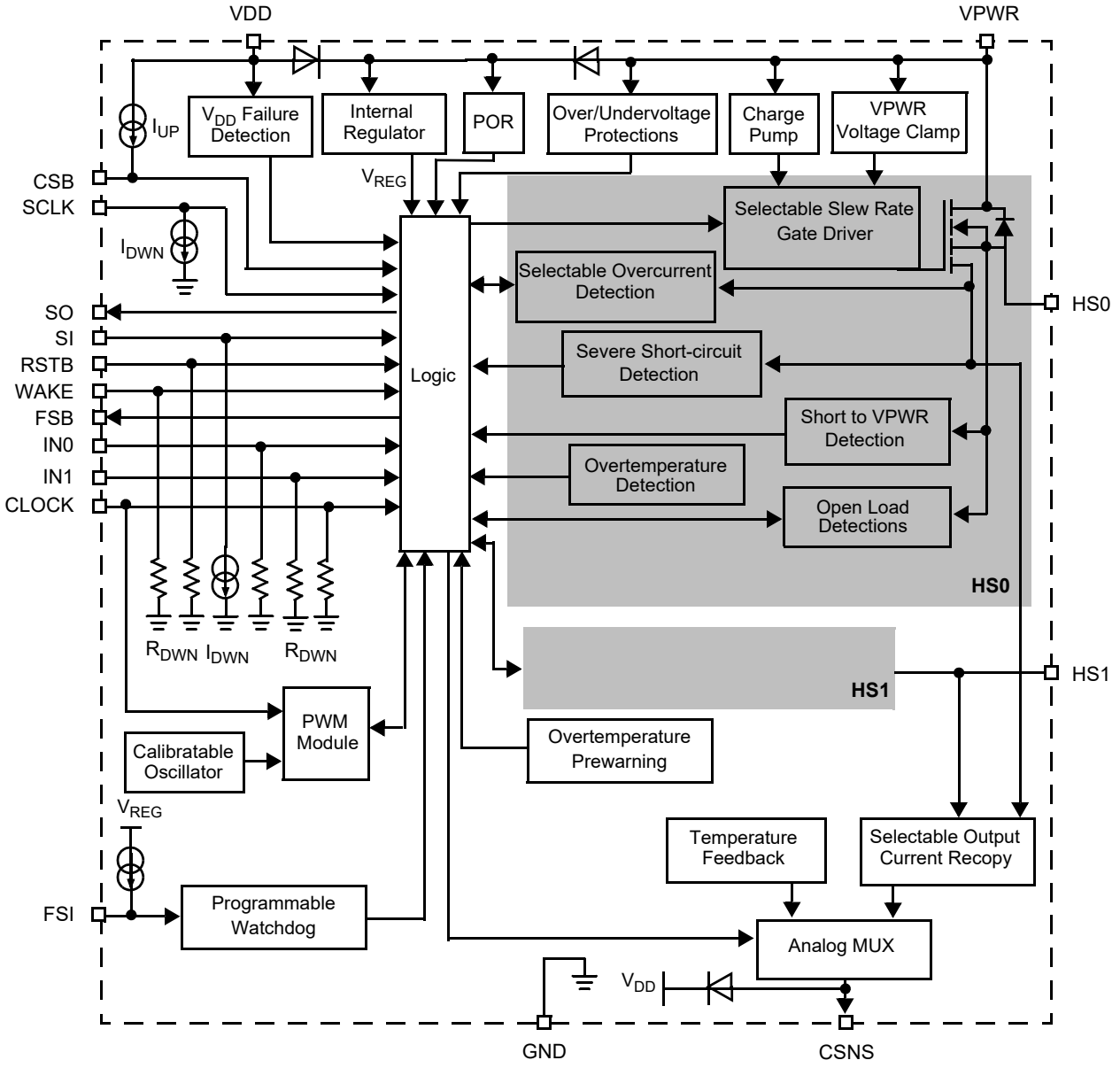


Figure 2. 07XS3200 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

Transparent top view

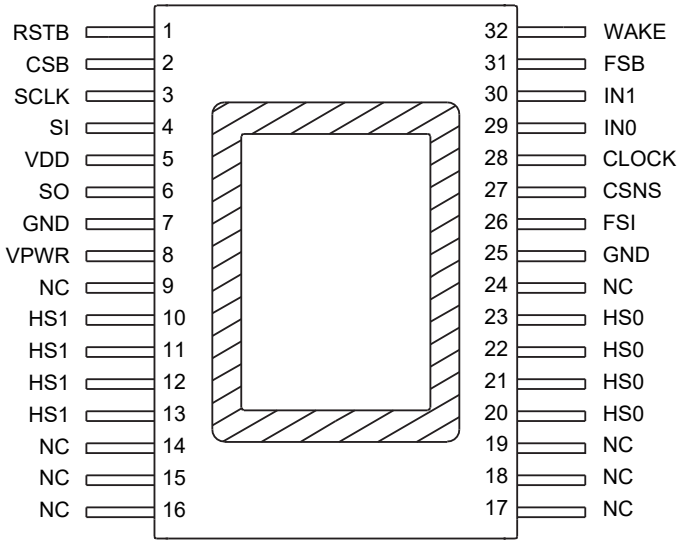


Figure 3. 07XS3200 pin connection

3.2 Pin definitions

A functional description of each pin can be found in the functional pin description section beginning on page 20.

Table 2. 07XS3200 pin definitions

Pin number	Pin name	Pin function	Formal name	Definition
1	RSTB	Input	Reset (active low)	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low current Sleep mode.
2	CSB	Input	Chip select (active low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
3	SCLK	Input	Serial clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.
4	SI	Input	Serial input	This is a command data input pin connected to the SPI Serial Data Output of the MCU or to the SO pin of the previous device of a daisy chain of devices.
5	VDD	Input	Digital drain voltage (power)	This is an external voltage input pin used to supply power to the SPI circuit.
6	SO	Output	Serial output	This output pin is connected to the SPI serial data input pin of the MCU or to the SI pin of the next device of a daisy chain of devices.
7, 25	GND	Ground	Ground	Those pins are the ground for the logic and analog circuitry of the device. These pins must be shorted to board level.
8	VPWR	Power	Positive power supply	Pin 8 is a positive supply for quiet and accurate control. Pin 33 is a power supply for the high current switch. These pins must be shorted at board level. Connecting a heatsink to pin 33 guarantees optimal heat-evacuation properties.
9, 14 to 19, 24	NC	—	No connect	These pins are no connected pins. It is recommended to connect these pins to ground.

Table 2. 07XS3200 pin definitions (continued)

Pin number	Pin name	Pin function	Formal name	Definition
10, 11, 12, 13	HS1	Output	High-side output	Protected 7.0 mΩ high-side power output pin to the load. Those pins must be shorted at board level.
20, 21, 22, 23	HS0	Output	High-side output	Protected 7.0 mΩ high-side power output pin to the load. Those pins must be shorted at board level.
26	FSI	Input	Fail-safe input	The value of the resistance connected between this pin and ground determines the state of the outputs after a watchdog timeout occurs.
27	CSNS	Output	Output current Monitoring	This pin is used to output a current proportional to the designated HS0-1 output.
28	CLOCK	Input	Reference clock	This pin is used to apply a reference clock used to control the outputs in PWM mode through embedded PWM module.
29	IN0	Input	Direct input 0	This input pin is used to directly control the output HS0.
30	IN1	Input	Direct input 1	This input pin is used to directly control the output HS1.
31	FSB	Output	Fault status (active low)	This is an open drain configured output requiring an external pull-up resistor to VDD for fault reporting.
32	WAKE	Input	Wake	This pin is used to input a Logic [1] signal so as to enable the watchdog timer function.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{PWR(SS)}$	V_{PWR} supply voltage range • Load dump at 25 °C (400 ms) • Maximum operating voltage • Reverse battery	 41 28 -18	V	
V_{DD}	V_{DD} supply voltage range	-0.3 to 5.5	V	
	Input/output voltage	-0.3 to V_{DD}+0.3	V	(5)
$I_{CL(WAKE)}$	WAKE input clamp current	2.5	mA	
$I_{CL(CSNS)}$	CSNS input clamp current	2.5	mA	
$V_{HS[0:1]}$	HS [0:1] voltage • Positive • Negative	 41 -24	V	
$I_{HS[0:1]}$	Output current per channel • Nominal continuous current • Short-circuit transient current • Reverse continuous current	 26 116 -26	A	(2)
V_{PWR} - V_{HS}	High-side breakdown voltage	47	V	
$E_{CL[0:1]}$	HS[0,1] output clamp energy using single pulse method	100	mJ	(3)
V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	ESD voltage • Human Body Model (HBM) for HS[0:1], VPWR and GND • Human Body Model (HBM) for other pins • Charge Device Model (CDM) Corner pins (1, 27, 28, 57) All other pins	 ±8000 ±2000 ±750 ±500	V	(4)
Thermal ratings				
T_A T_J	Operating temperature • Ambient • Junction	 -40 to 125 -40 to 150	°C	
T_{STG}	Storage temperature	-55 to 150	°C	

Notes

2. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using board thermal resistance is required.
3. Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14 V, T_J = 150 °C initial).
4. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
5. Input/output pins are: IN[0:1], CLOCK, RSTB, FSI, CSNS, SI, SCLK, CSB, SO, FSB

Table 3. Maximum ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal resistance				
$R_{\theta JC}$ $R_{\theta JA}$	Thermal resistance • Junction to Case • Junction to Ambient	 4.0 35	°C/W	(6)
T_{SOLDER}	Peak Pin Reflow Temperature During Solder Mounting	260	°C	(7)

Notes

6. Device mounted on a 2s2p test board per JEDEC JESD51-2. 20 °C/W of $R_{\theta JA}$ can be reached in a real application case (4 layers board).
7. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power inputs						
V_{PWR}	Battery supply voltage range • Fully operational • Extended mode	 6.0 4.0	 – –	 20 28	V	(8)
$V_{PWR(CLAMP)}$	Battery clamp voltage	41	47	53	V	(9)
$I_{PWR(ON)}$	V_{PWR} operating supply current • Outputs commanded ON, HS[0:1] open, IN[0:1] > V_{IH}	–	6.5	20	mA	
$I_{PWR(SBY)}$	V_{PWR} supply current • Outputs commanded OFF, OFF openload detection disabled, HS[0:1] shorted to the ground with V_{DD} = 5.5 V WAKE > V_{IH} or RSTB > V_{IH} and IN[0:1] < V_{IL}	–	6.5	7.5	mA	
$I_{PWR(SLEEP)}$	Sleep state supply current V_{PWR} = 12 V, RSTB = WAKE = CLOCK = IN[0:1] < V_{IL}, HS[0:1] shorted to ground • T_A = 25 °C • T_A = 85 °C	 – –	 1.0 –	 5.0 30	µA	
$V_{DD(ON)}$	V_{DD} supply voltage	3.0	–	5.5	V	
$I_{DD(ON)}$	V_{DD} supply current at V_{DD} = 5.5 V • No SPI communication • 8.0 MHz SPI communication	 – –	 1.6 5.0	 2.2 –	mA	(10)
$I_{DD(SLEEP)}$	V_{DD} sleep state current at V_{DD} = 5.5 V	–	–	5.0	µA	
$V_{PWR(OV)}$	Overvoltage shutdown threshold	28	32	36	V	
$V_{PWR(OVHYS)}$	Overvoltage shutdown hysteresis	0.2	0.8	1.5	V	
$V_{PWR(UV)}$	Undervoltage shutdown threshold	3.3	3.9	4.3	V	(11)
$V_{SUPPLY(POR)}$	V_{PWR} and V_{DD} power-on reset threshold	0.5	–	0.9	$V_{PWR(UV)}$	
$V_{PWR(UV)\_UP}$	Recovery undervoltage threshold	3.4	4.1	4.5	V	
$V_{DD(FAIL)}$	V_{DD} supply failure threshold (for V_{PWR} > $V_{PWR(UV)}$)	2.2	2.5	2.8	V	

Notes

8. In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 V to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
9. Measured with the outputs open.
10. Typical value guaranteed per design.
11. Output automatically recovers with time limited autoretry to instructed state when V_{PWR} voltage is restored to normal as long as the V_{PWR} degradation level did not go below the undervoltage power-on reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Outputs HS0 TO HS1						
$R_{DS\_01(on)}$	HS[0,1] output Drain-to-Source ON resistance (I_{HS} = 5.0 A, T_A = 25 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	 – – – –	 – – – –	 25.2 11.2 7.0 7.0	mΩ	
$R_{DS\_01(on)}$	HS[0,1] output Drain-to-Source ON resistance (I_{HS} = 5.0 A, T_A = 150 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	 – – – –	 – – – –	 42.8 19.1 11.9 11.9	mΩ	
$R_{SD\_01(on)}$	HS[0,1] output Source-to-Drain ON resistance (I_{HS} = -5.0 A, $V_{PWR=}$ -18 V) • T_A = 25 °C • T_A = 150 °C	 – –	 – –	 10.5 14	mΩ	(12)
R_{SHORT_01}	HS[0,1] maximum severe short-circuit impedance detection	21	47	75	mΩ	(13)
OCHI1 OCHI2 OC1 OC2 OC3 OC4 OCLO4 OCLO3 OCLO2 OCLO1	HS[0,1] output overcurrent detection levels (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V)	89.9 67 48 42 35.2 28.8 21 13.3 11.3 7.4	114.8 83.7 61.2 53.2 44.6 36.4 26.6 18.4 14.2 9.3	139.8 100.4 74.4 64.4 54 44 32.1 23.5 17.1 11.2	A	
C_{SR0} C_{SR1}	HS[0,1] current sense ratio (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V, CSNS ≤ 5.0 V) • CSNS_ratio bit = 0 • CSNS_ratio bit = 1	 – –	 1/10700 1/63600	 – –	–	(14)

Notes

12. Source-Drain ON resistance (reverse Drain-to-Source ON resistance) with negative polarity V_{PWR}.
13. Short-circuit impedance calculated from HS[0:1] to GND pins. Value guaranteed per design.
14. Current sense ratio = I_{CSNS} / $I_{HS[0:1]}$

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Outputs HS0 TO HS1 (continued)						
C_{SR0_ACC}	HS[0,1] current sense ratio (C_{SR0}) accuracy (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) 25 °C and 125 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 5.0 A • $I_{HS[0:1]}$ = 3.0 A • $I_{HS[0:1]}$ = 1.5 A -40 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 5.0 A • $I_{HS[0:1]}$ = 3.0 A • $I_{HS[0:1]}$ = 1.5 A	 -13 -20 -25 -30 -18 -25 -30 -40	 – – – – – – – –	 13 20 26 30 18 25 30 40	%	
C_{SR0_ACC} (CAL)	HS[0,1] current recopy accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) • $I_{HS[0:1]}$ = 5.0 A	 -5.0	 –	 5.0	%	(15)
$\Delta(C_{SR0})/\Delta(T)$	HS[0,1] C_{SR0} current recopy temperature drift (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) • $I_{HS[0:1]}$ = 5.0 A	 –	 –	 0.04	%/°C	(16)
C_{SR1_ACC}	HS[0,1] current sense ratio (C_{SR1}) accuracy (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) 25 °C and 125 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 75 A -40 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 75 A	 -17 -15 -25 -22	 – – – –	 17 15 25 22	%	
C_{SR1_ACC} (CAL)	HS[0,1] current recopy accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) • $I_{HS[0:1]}$ = 12.5 A	 -5.0	 –	 5.0	%	(15)
$V_{CL(CSNS)}$	Current sense clamp voltage • CSNS Open; $I_{HS[0:1]}$ = 5.0 A with C_{SR0} ratio	V_{DD}+0.25	–	V_{DD}+1.0	V	
$I_{OLD(OFF)}$	OFF openload detection source current	30	–	100	µA	(17)
$V_{OLD(THRES)}$	OFF openload fault detection voltage threshold	2.0	3.0	4.0	V	
$I_{OLD(ON)}$	ON openload fault detection current threshold	80	330	660	mA	
$I_{OLD(ON\_LED)}$	ON openload fault detection current threshold with LED • $V_{HS[0:1]}$ = V_{PWR} - 0.75 V	2.5	5.0	10	mA	
$V_{OSD(THRES)}$	Output short to V_{PWR} detection voltage threshold • Output programmed OFF	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V	
V_{CL}	Output negative clamp voltage • 0.5 A ≤ $I_{HS[0:1]}$ ≤ 5.0 A, output programmed OFF	-22	–	-16	V	
T_{SD}	Output overtemperature shutdown for 4.5 V < V_{PWR} < 28 V	155	175	195	°C	

Notes

15. Based on statistical analysis. It is not production tested.
16. Based on statistical data: delta(C_{SR0})/delta(T)={(measured I_{CSNS} at T_1 - measured I_{CSNS} at T_2) / measured I_{CSNS} at room} / {T_1-T_2}. No production tested.
17. Output OFF openload detection current is the current required to flow through the load for the purpose of detecting the existence of an openload condition when the specific output is commanded OFF. Pull-up current is measured for V_{HS} = $V_{OLD(THRES)}$

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Control interface						
V_{IH}	Input logic high voltage	2.0	–	V_{DD}+0.3	V	(18)
V_{IL}	Input logic low voltage	-0.3	–	0.8	V	(18)
I_{DWN}	Input logic pull-down current (SCLK, SI)	5.0	–	20	µA	(21)
I_{UP}	Input logic pull-up current (CSB)	5.0	–	20	µA	(22)
C_{SO}	SO, FSB tri-state capacitance	–	–	20	pF	(19)
R_{DWN}	Input logic pull-down resistor (RSTB, WAKE, CLOCk and IN[0:1])	125	250	500	kΩ	
C_{IN}	Input capacitance	–	4.0	12	pF	(19)
$V_{CL(WAKE)}$	Wake input clamp voltage • $I_{CL(WAKE)}$ < 2.5 mA	18	25	32	V	(20)
$V_{F(WAKE)}$	Wake input forward voltage • $I_{CL(WAKE)}$ = -2.5 mA	-2.0	–	-0.3	V	
V_{SOH}	SO high state output voltage • I_{OH} = 1.0 mA	V_{DD}-0.4	–	–	V	
V_{SOL}	SO and FSB low state output voltage • I_{OL} = -1.0 mA	–	–	0.4	V	
$I_{SO(LEAK)}$	SO, CSNS and FSB tri-state leakage current • CSB = V_{IH} and 0 V ≤ V_{SO} ≤ V_{DD}, or FSB = 5.5 V, or CSNS = 0.0 V	-2.0	0.0	2.0	µA	
RFS	FSI external pull-down resistance • Watchdog disabled • Watchdog enabled	– 10	0.0 Infinite	1.0 –	kΩ	(23)

Notes

18. Upper and lower logic threshold voltage range applies to SI, CSB, SCLK, FSB, IN[0:1], CLOCK and WAKE input signals. The WAKE and RSTB signals may be supplied by a derived voltage referenced to V_{PWR}.
19. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CLOCK and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
20. The current must be limited by a series resistance when using voltages > 7.0 V.
21. Pull-down current is with V_{SI} ≥ 1.0 V and V_{SCLK} ≥ 1.0 V.
22. Pull-up current is with V_{CSB} ≤ 2.0 V. CSB has an active internal pull-up to V_{DD}.
23. In Fail-safe HS[0:1] depends respectively on IN[0:1]. FSI has an active internal pull-up to V_{REG} ~ 3.0 V.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power output timing HS0 TO HS1						
SR_{R_00}	Output rising medium slew rate (medium speed slew rate / SR[1:0] = 00) • V_{PWR} = 14 V	0.15	0.3	0.6	V/µs	(24)
SR_{R_01}	Output rising slow slew rate (low speed slew rate / SR[1:0] = 01) • V_{PWR} = 14 V	0.07	0.15	0.3	V/µs	(24)
SR_{R_10}	Output falling fast slew rate (high speed slew rate / SR[1:0] = 10) • V_{PWR} = 14 V	0.3	0.6	1.2	V/µs	(24)
SR_{F_00}	Output falling medium slew rate (medium speed slew rate / SR[1:0] = 00) • V_{PWR} = 14 V	0.15	0.3	0.6	V/µs	(24)
SR_{F_01}	Output falling slow slew rate (low speed slew rate / SR[1:0] = 01) • V_{PWR} = 14 V	0.07	0.15	0.3	V/µs	(24)
SR_{F_10}	Output rising fast slew rate (high speed slew rate / SR[1:0] = 10) • V_{PWR} = 14 V	0.3	0.6	1.2	V/µs	(24)
t_{DLY_12}	HS[0:1] outputs turn-on and off delay time V_{PWR} = 14 V for medium speed slew rate (SR[1:0] = 00) • $t_{DLY(ON)}$ • $t_{DLY(OFF)}$	 90 40	 135 70	 180 100	µs	(25) (26)
ΔSR	Driver output matching slew rate (SR_R /SR_F) • V_{PWR} = 14 V at 25 °C and for medium speed slew rate (SR[1:0] = 00)	0.8	1.0	1.2		
Δt_{RF_01}	HS[0:1] driver output matching time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) • V_{PWR} = 14 V, f_{PWM} = 240 Hz, PWM duty cycle = 50%, at 25 °C for medium speed slew rate (SR[1:0] = 00)	25	60	95	µs	
t_{FAULT}	Fault detection blanking time	1.0	5.0	20	µs	(27)
t_{DETECT}	Output shutdown delay time	–	7.0	30	µs	(28)
t_{CNSVAL}	CSNS valid time	–	70	100	µs	(29)
t_{WDTO}	Watchdog timeout	217	310	400	ms	(30)
T_{OLLED}	ON openload fault cyclic detection period with LED • Internal clock (PWM_en bit = 1 & CLOCK_Set = 1) • External clock (PWM_en bit = 1 & CLOCK_Set = 0)	6.4 -	8.3 PWM period	12 -	ms	

Notes

24. Rise and fall slew rates measured across a 5.0 Ω resistive load at high-side output = 30% to 70% (see Figure 4, page 17).
25. Turn-on delay time measured from rising edge of any signal (IN[0:1] and CSB) that would turn the output ON to $V_{HS[0:1]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load.
26. Turn-off delay time measured from falling edge of any signal (IN[0:1] and CSB) that would turn the output OFF to $V_{HS[0:1]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load.
27. Time necessary to report the fault to FSB pin.
28. Time necessary to switch-off the output in case of OT or OC or SC or UV fault detection (from negative edge of FSB pin to HS voltage = 50% of V_{PWR}
29. Time necessary for CSNS to be within ±5% of the targeted value (from HS voltage = 50% of V_{PWR} to ±5% of the targeted CSNS value).
30. For FSI open, the watchdog timeout delay measured from the rising edge of RSTB, to HS[0,1] output state depend on the corresponding input command.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power output timing HS0 TO HS1 (continued)						
t_{OC1_00}		4.40	6.30	8.02		
t_{OC2_00}		1.62	2.32	3.00		
t_{OC3_00}	HS[0,1] output overcurrent time step	2.10	3.00	3.90		
t_{OC4_00}	OC[1:0] = 00 (slow by default)	2.88	4.12	5.36		
t_{OC5_00}		4.58	6.56	8.54		
t_{OC6_00}		10.16	14.52	18.88		
t_{OC7_00}		73.2	104.6	134.0		
t_{OC1_01}		1.10	1.57	2.00		
t_{OC2_01}		0.40	0.58	0.75		
t_{OC3_01}		0.52	0.75	0.98		
t_{OC4_01}	OC[1:0]=01 (fast)	0.72	1.03	1.34		
t_{OC5_01}		1.14	1.64	2.13		
t_{OC6_01}		2.54	3.63	4.72		
t_{OC7_01}		18.2	26.1	34.0	ms	
t_{OC1_10}		2.20	3.15	4.01		
t_{OC2_10}		0.81	1.16	1.50		
t_{OC3_10}		1.05	1.50	1.95		
t_{OC4_10}	OC[1:0]=10 (medium)	1.44	2.06	2.68		
t_{OC5_10}		2.29	3.28	4.27		
t_{OC6_10}		5.08	7.26	9.44		
t_{OC7_10}		36.6	52.3	68.0		
t_{OC1_11}		8.8	12.6	16.4		
t_{OC2_11}		3.2	4.6	21.4		
t_{OC3_11}		4.2	6.0	7.8		
t_{OC4_11}	OC[1:0]=11 (very slow)	5.7	8.2	10.7		
t_{OC5_11}		9.1	13.1	17.0		
t_{OC6_11}		20.3	29.0	37.7		
t_{OC7_11}		146.4	209.2	272.0		
t_{BC1_00}	HS[0,1] bulb cooling time step	242	347	452		
t_{BC2_00}	CB[1:0] = 00 or 11 (medium)	126	181	236		
t_{BC3_00}		140	200	260		
t_{BC4_00}		158	226	294		
t_{BC5_00}		181	259	337		
t_{BC6_00}		211	302	393		
t_{BC1_01}	CB[1:0] = 01 (fast)	121	173	226		
t_{BC2_01}		63	90	118		
t_{BC3_01}		70	100	130	ms	
t_{BC4_01}		79	113	147		
t_{BC5_01}		90	129	169		
t_{BC6_01}		105	151	197		
	CB[1:0] = 10 (slow)					
t_{BC1_10}		484	694	1904		
t_{BC2_10}		252	362	472		
t_{BC3_10}		280	400	520		
t_{BC4_10}		316	452	588		
t_{BC5_10}		362	518	674		
t_{BC6_10}		422	604	786		

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
PWM Module timing						
f_{CLOCK}	Input PWM clock range on CLOCK	7.68	–	30.72	kHz	
$f_{CLOCK(LOW)}$	Input PWM clock low frequency detection range on CLOCK	1.0	2.0	4.0	kHz	(32)
$f_{CLOCK(HIGH)}$	Input PWM clock high frequency detection range on CLOCK	100	–	400	kHz	(32)
f_{PWM}	Output PWM frequency range using external clock on CLOCK	31.25	–	781	Hz	(31)
$A_{FPWM(CAL)}$	Output PWM frequency accuracy using calibrated oscillator	-10	–	+10	%	(31)
$f_{PWM(0)}$	Default output PWM frequency using internal oscillator	84	120	156	Hz	
$t_{CSB(MIN)}$	CSB calibration low minimum time detection range	14	20	26	µs	
$t_{CSB(MAX)}$	CSB calibration low maximum time detection range	140	200	260	µs	
R_{PWM}_1k	Output PWM duty cycle range for f_{PWM} = 1.0 kHz for high speed slew rate	10	–	94	%	(32)
R_{PWM}_400	Output PWM duty cycle range for f_{PWM} = 400 Hz	6.0	–	98	%	(32)
R_{PWM}_200	Output PWM duty cycle range for f_{PWM} = 200 Hz	5.0	–	98	%	(32)
Input timing						
t_{IN}	Direct input toggle timeout	175	250	325	ms	
Autoretry timing						
t_{AUTO}	Autoretry period	105	150	195	ms	
Temperature on the GND flag						
T_{OTWAR}	Thermal prewarning detection	110	125	140	°C	(33)
T_{FEED}	Analog temperature feedback at T_A = 25 °C with R_{CSNS} = 2.5 kΩ	1.15	1.20	1.25	V	
DT_{FEED}	Analog temperature feedback derating with R_{CSNS} = 2.5 kΩ	-3.5	-3.7	-3.9	mV/°C	(34)

Notes

31. Clock Fail detector available for PWM_en bit is set to logic [1] and CLOCK_sel is set to logic [0].
32. The PWM ratio is measured at V_{HS} = 50% of V_{PWR} and for the default SR value. It is possible to put the device fully-on (PWM duty cycle 100%) and fully-off (duty cycle 0%). For values outside this range, a calibration is needed between the PWM duty cycle programming and the PWM on the output with R_L = 5.0 Ω resistive load.
33. Typical value guaranteed per design.
34. Value guaranteed per statistical analysis.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SPI interface characteristics[35]						
f_{SPI}	Maximum frequency of SPI operation	–	–	8.0	MHz	
t_{WRSTB}	Required low state duration for RSTB	10	–	–	µs	[36]
$t_{\overline{CSB}}$	Rising edge of CSB to falling edge of CSB (required setup time)	–	–	1.0	µs	[37]
t_{ENBL}	Rising edge of RSTB to falling edge of CSB (required Setup time)	–	–	5.0	µs	[37]
t_{LEAD}	Falling edge of CSB to Rising Edge of SCLK (required setup time)	–	–	500	ns	[37]
t_{WSCLKh}	Required high state duration of SCLK (required setup time)	–	–	50	ns	[37]
t_{WSCLKl}	Required low state duration of SCLK (required setup time)	–	–	50	ns	[37]
t_{LAG}	Falling edge of SCLK to rising edge of CSB (required setup time)	–	–	60	ns	[37]
$t_{SI(SU)}$	SI to falling edge of SCLK (required setup time)	–	–	37	ns	[38]
$t_{SI(HOLD)}$	Falling edge of SCLK to SI (required setup time)	–	–	49	ns	[38]
t_{RSO}	SO rise time • C_L = 80 pF	–	–	13	ns	
t_{FSO}	SO Fall time • C_L = 80 pF	–	–	13	ns	
t_{RSI}	SI, CSB, SCLK, incoming signal rise time	–	–	13	ns	[38]
t_{FSI}	SI, CSB, SCLK, incoming signal fall time	–	–	13	ns	[38]
$t_{SO(EN)}$	Time from falling edge of CSB to SO low-impedance	–	–	60	ns	[39]
$t_{SO(DIS)}$	Time from rising edge of CSB to SO high-impedance	–	–	60	ns	[40]

Notes

35. Parameters guaranteed by design.
36. RSTB low duration measured with outputs enabled and going to OFF or disabled condition.
37. Maximum setup time required for the 07XS3200 is the minimum guaranteed time needed from the microcontroller.
38. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
39. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on CSB.
40. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on CSB.

4.4 Timing diagrams

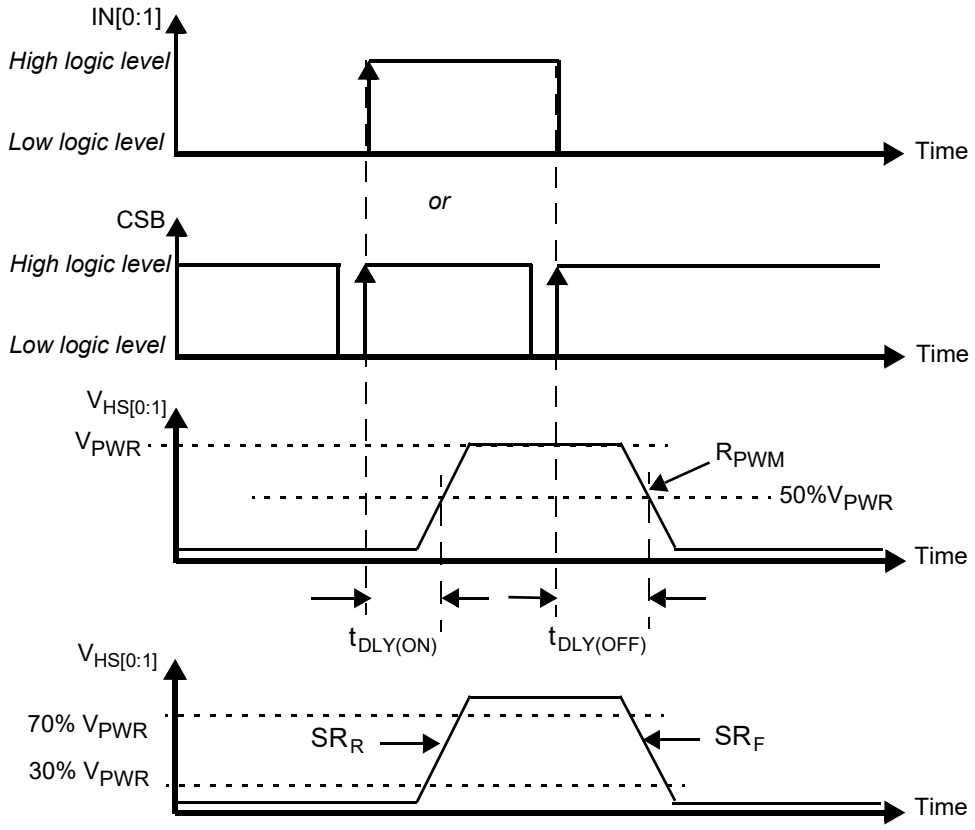


Figure 4. Output slew rate and time delays

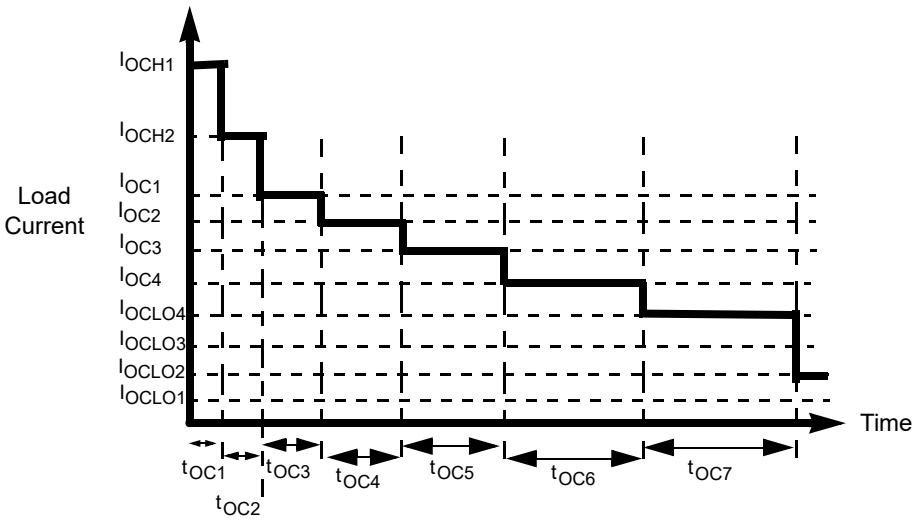


Figure 5. Overcurrent shutdown protection

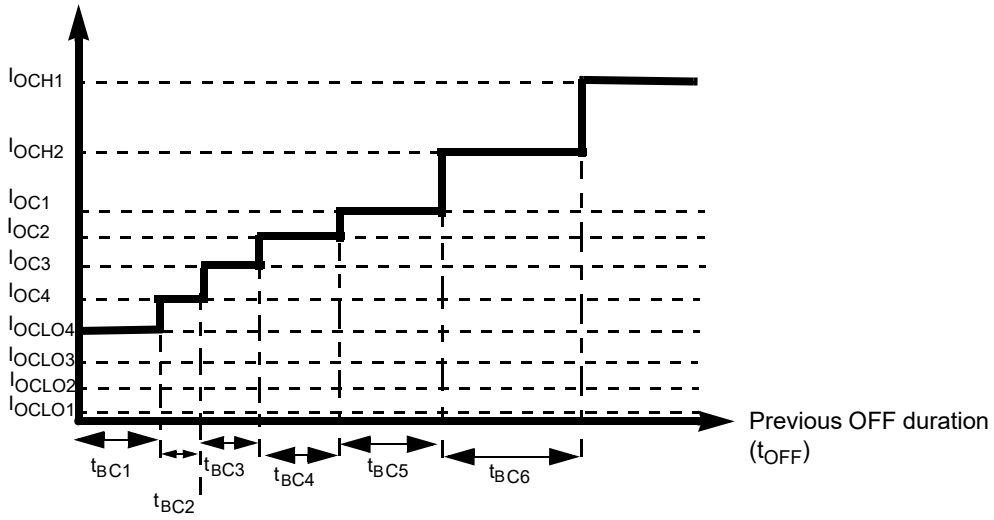


Figure 6. Bulb cooling management

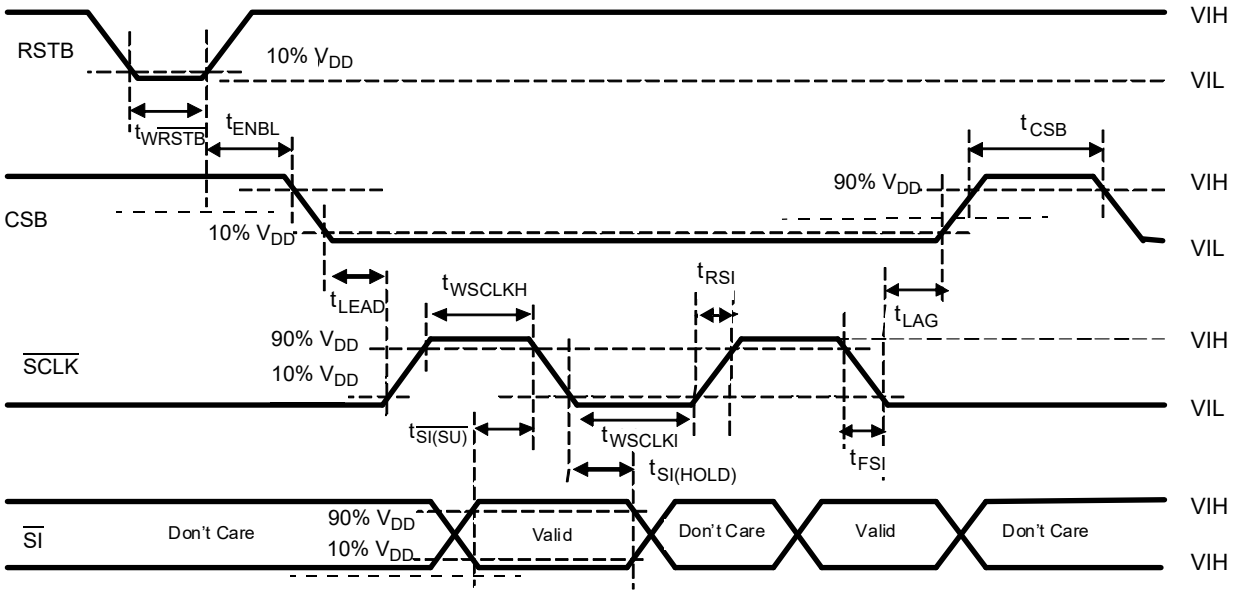


Figure 7. Input timing switching characteristics

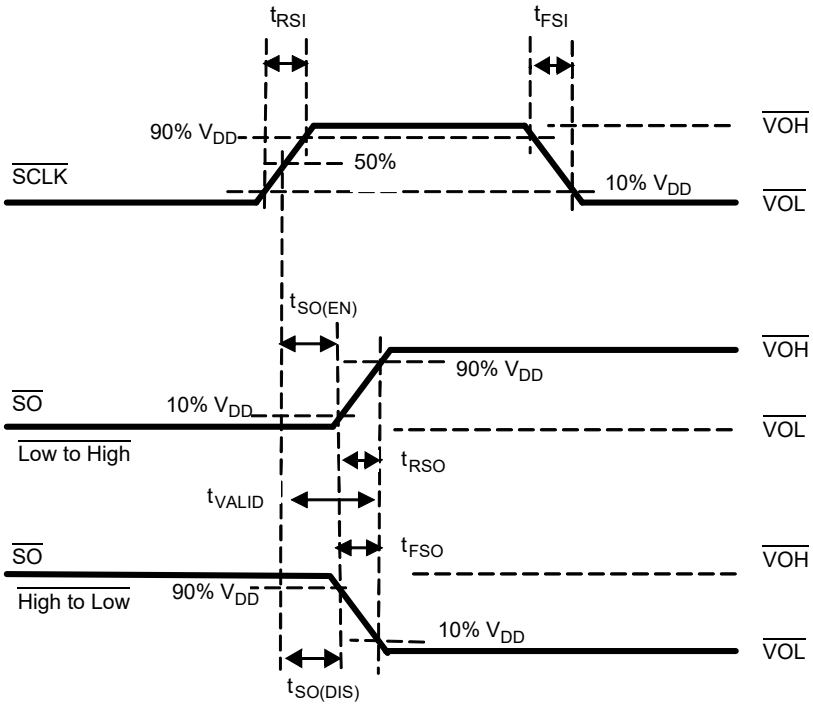


Figure 8. SCLK waveform and valid SO data delay time

5 Functional description

5.1 Introduction

The 07XS3200 is one in a family of devices designed for low-voltage automotive lighting applications. Its two low $R_{DS(on)}$ MOSFETs (dual 7.0 mΩ) can control two separate 55 W bulbs and/or Xenon modules.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 07XS3200 allows the user to program via the SPI, the fault current trip levels and duration of acceptable lamp inrush. The device has fail-safe mode to provide fail-safe functionality of the outputs in case of MCU damaged.

5.2 Functional pin description

5.2.1 Output current monitoring (CSNS)

The Current Sense pin provides a current proportional to the designated HS0:HS1 output or a voltage proportional to the temperature on the GND flag. That current is fed into a ground-referenced resistor (2.5 kΩ typical) and its voltage is monitored by an MCU's A/D. The output type is selected via the SPI. This pin can be tri-stated through the SPI.

5.2.2 Direct inputs (IN0, IN1)

Each IN input wakes the device. The IN0:IN1 high-side input pins are also used to directly control HS0:HS1 high-side output pins. If the outputs are controlled by PWM module, the external PWM clock is applied to IN0 pin. These pins are to be driven with CMOS levels, and they have a passive internal pull-down, R_{DWN}.

5.2.3 Fault status (FSB)

This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. If a device fault condition is detected, this pin is active LOW. Specific device diagnostics and faults are reported via the SPI SO pin.

5.2.4 Wake (WAKE)

The WAKE input wakes the device. An internal clamp protects this pin from high damaging voltages with a series resistor (10 kΩ typ). This input has a passive internal pull-down, R_{DWN}.

5.2.5 PWM Clock (CLOCK)

The clock input wakes the device. The PWM frequency and timing are generated from clock input by the PWM module. The clock input frequency is the selectable factor 2^7 = 128. This input has a passive internal pull-down, R_{DWN}.

5.2.6 Reset (RSTB)

The RESET input wakes the device. This is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin has a passive internal pull-down, R_{DWN}.

5.2.7 Chip select (CSB)

The CSB pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 07XS3200 latches in data from the Input Shift registers to the addressed registers on the rising edge of CSB. The device transfers status information from the power output to the Shift register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. CSB has an active internal pull-up from V_{DD}, I_{UP}.

5.2.8 Serial clock (SCLK)

The SCLK pin clocks the internal shift registers of the 07XS3200 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic low state whenever CSB makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed (CSB logic [1] state). SCLK has an active internal pull-down. When CSB is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 10, page 23). SCLK input has an active internal pull-down, I_{DWN}.

5.2.9 Serial input (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 (MSB) to D0 (LSB). The internal registers of the 07XS3200 are configured and controlled using a 5-bit addressing scheme described in Table 10, page 33. Register addressing and configuration are described in Tables 11, page 33. SI input has an active internal pull-down, I_{DWN}.

5.2.10 Digital drain voltage (VDD)

This pin is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost (V_{DD} Failure), the device goes to Fail-safe mode.

5.2.11 Ground (GND)

These pins are the ground for the device.

5.2.12 Positive power supply (VPWR)

This pin connects to the positive power supply and is the source of operational power for the device. The VPWR contact is the backside surface mount tab of the package.

5.2.13 Serial output (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high impedance state until the CSB pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, the state of the key inputs, etc. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. SO reporting descriptions are provided in Table 23, page 39.

5.2.14 High-side outputs (HS0, HS1)

Protected 7.0 mΩ high-side power outputs to the load.

5.2.15 Fail-safe input (FSI)

This pin incorporates an active internal pull-up current source from internal supply (V_{REG}). This enables the watchdog timeout feature. When the FSI pin is opened, the watchdog circuit is enabled. After a watchdog timeout occurs, the output states depends on IN[0:1]. When the FSI pin is connected to GND, the watchdog circuit is disabled. The output states depends on IN[0:1] in case of V_{DD} failure condition, in case V_{DD} failure detection is activated (VDD_FAIL_en bit sets to logic [1]).

5.3 Functional internal block description

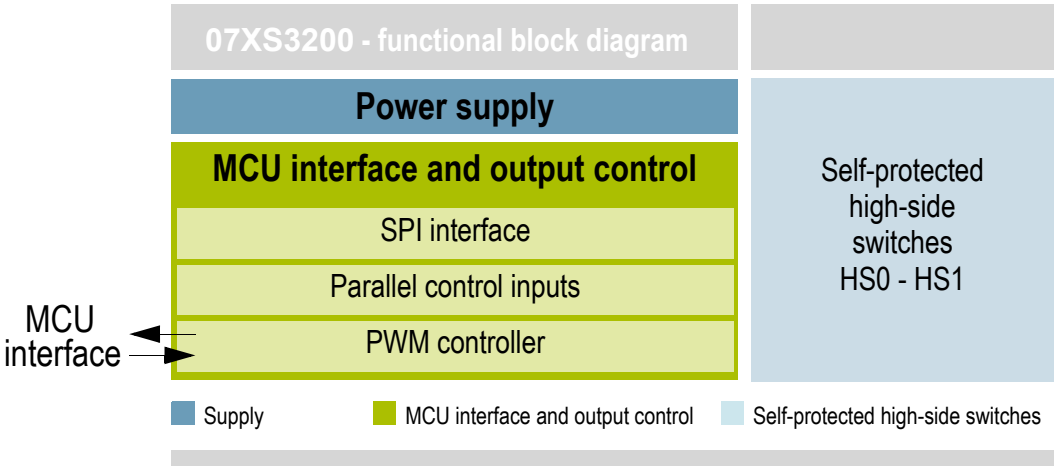


Figure 9. Functional block diagram

5.3.1 Power supply

The 07XS3200 is designed to operate from 4.0 V to 28 V on the VPWR pin. Characteristics are provided from 6.0 V to 20 V for the device. The VPWR pin supplies power to internal regulator, analog, and logic circuit blocks. The V_{DD} supply is used for Serial Peripheral Interface (SPI) communication to configure and diagnose the device. This IC architecture provides a low quiescent current sleep mode. Applying V_{PWR} and V_{DD} to the device places the device in the Normal mode. The device transits to Fail-safe mode in case of failures on the SPI or/and on V_{DD} voltage.

5.3.2 High-side switches: HS0–HS1

These pins are the high-side outputs controlling automotive lamps located for the front of vehicle, such as 65 W/55 W bulbs and Xenon-HID modules. N-channel MOSFETs with 7.0 mΩ $R_{DS(on)}$ are self-protected and present extended diagnostics to detect bulb outage and a short-circuit fault condition. The HS output is actively clamped during turn off of inductive loads and inductive battery line. When driving DC motor or solenoid loads demand multiple switching, an external recirculation device must be used to maintain the device in its Safe Operating Area.

5.3.3 MCU interface and output control

In Normal mode, each bulb is controlled directly from the MCU through the SPI. A pulse width modulation control module allows improvement of lamp lifetime with bulb power regulation (PWM frequency range from 100 Hz to 400 Hz) and addressing the dimming application (day running light). An analog feedback output provides a current proportional to the load current or the temperature of the board. The SPI is used to configure and to read the diagnostic status (faults) of high-side outputs. The reported fault conditions are: openload, short-circuit to battery, short-circuit to ground (overcurrent and severe short-circuit), thermal shutdown, and under/overvoltage. The vehicle is lighter thanks to accurate and configurable overcurrent detection circuitry and wire-harness optimization.

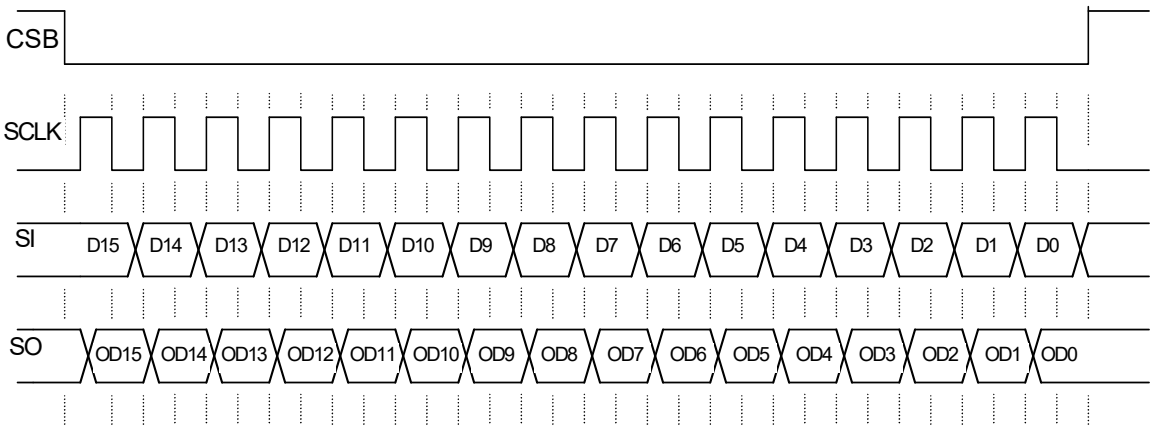
In Fail-safe mode, each lamp is controlled with dedicated parallel input pins. The device is configured in default mode.

6 Functional device operation

6.1 SPI protocol description

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select (CSB).

The SI/SO pins of the 07XS3200 follow a first-in first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V or 3.3 V CMOS logic levels.



Notes 1. RSTB is a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of data into the device.
3. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 10. Single 16-bit word SPI communication

6.2 Operational modes

The 07XS3200 has four operating modes: Sleep, Normal, Fail-safe and Fault. Table 6 and Figure 12 summarize details contained in succeeding paragraphs.

The Figure 11 describes an internal signal called IN_ON[x] depending on IN[x] input.

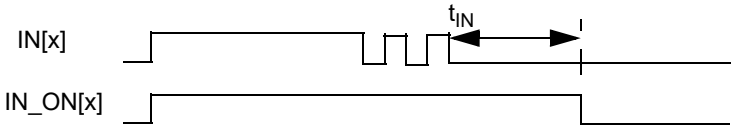


Figure 11. IN_ON[x] internal signal

The 07XS3200 transits to operating modes according to the following signals:

- wake-up = RSTB or WAKE or IN_ON[0] or IN_ON[1] or CLOCK_ON,
- fail = (V_{DD} Failure and VDD_FAIL_en) or (Watchdog timeout and FSI input not shorted to ground),
- fault = OC[0:1] or OT[0:1] or SC[0:1] or UV or (OV and $\overline{\text{OV\_dis}}$).

Table 6. 07XS3200 operating modes

Mode	Wake-up	Fail	Fault	Comments
Sleep	0	x	x	Device is in Sleep mode. All outputs are OFF.
Normal	1	0	0	Device is currently in Normal mode. Watchdog is active if enabled.
Fail-safe	1	1	0	Device is currently in Fail-safe mode due to watchdog timeout or V_{DD} Failure conditions. The output states are defined with the RFS resistor connected to FSI.
Fault	1	X	1	Device is currently in fault mode. The faulted output(s) is (are) OFF. The safe autoretry circuitry is active to turn-on again the output(s).

x = Don't care.

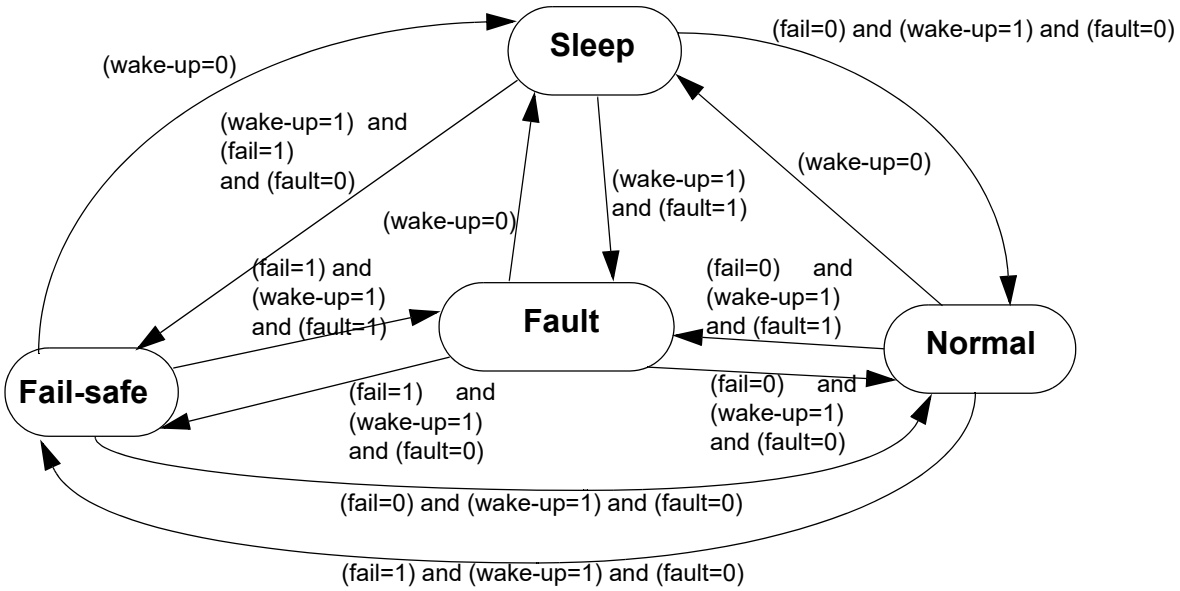


Figure 12. Operating modes

6.2.1 Sleep mode

The 07XS3200 is in Sleep mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 0,
- fail = X,
- fault = X.

This is the Default mode of the device after first applying battery voltage (V_{PWR}) prior to any I/O transitions. This is also the state of the device when the WAKE and RSTB, CLOCK_ON and IN_ON[0:1] are logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal regulator, are off to minimize draw current. In addition, all SPI-configurable features of the device are as if set to logic [0].

In the event of an external V_{PWR} supply disconnect, an unexpected current consumption may sink on the VDD supply pin (In Sleep state). This current leakage is about 70 mA instead of 5.0 µA and it may impact the device reliability. The device recovers its normal operational mode once V_{PWR} is reconnected.

To avoid this unexpected current leakage on the VDD supply pin, maintain the device in Normal mode with RSTB pin set to logic[1]. This allows diagnosis of the battery disconnection event through UV fault reporting in SPI. Then, apply 0 V on the VDD supply pin to switch the device to Sleep state.

6.2.2 Normal mode

The 07XS3200 is in Normal mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 1,
- fail = 0,
- fault = 0.

In this mode, the NM bit is set to lfault_contrologic [1] and the outputs HS[0:1] are under control, as defined by the hson signal:

hson[x] = (((IN[x] and $\overline{\text{DIR\_dis}}$[x]) or On bit[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x] and Duty_cycle[x] and PWM_en).

In this mode and also in Fail-safe, the fault condition reset depends on fault_control signal, as defined below:

fault_control[x] = ((IN_ON[x] and $\overline{\text{DIR\_dis}}$[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x]).

6.2.2.1 Programmable PWM module

The outputs HS[0:1] are controlled by the programmable PWM module if PWM_en and On bits are set to logic [1].

The clock frequency from CLOCK input pin or from the internal clock is the factor 2^7 (128) of the output PWM frequency (CLOCK_sel bit). The outputs HS[0:1] can be controlled in the range of 5.0% to 98% with a resolution of 7 bits of duty cycle (Table 7). The state of other IN pin is ignored.

Table 7. Output PWM resolution

On bit	Duty cycle	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty cycle)
1	0000001	PWM (2/128 duty cycle)
1	0000010	PWM (3/128 duty cycle)
1	n	PWM ((n+1)/128 duty cycle)
1	1111111	fully ON

The timing includes seven programmable PWM switching delay (number of PWM clock rising edges) to improve overall EMC behavior of the light module (Table 8).

Table 8. Output PWM switching delay

Delay bits	Output delay
000	no delay
001	16 PWM clock periods
010	32 PWM clock periods
011	48 PWM clock periods
100	64 PWM clock periods
101	80 PWM clock periods
110	96 PWM clock periods
111	112 PWM clock periods

The clock frequency from CLOCK is permanently monitored in order to report a clock failure in case the frequency is out a specified frequency range (from $f_{CLOCK(LOW)}$ to $f_{CLOCK(HIGH)}$). In case of clock failure, no PWM feature is provided, the On bit defines the outputs state and the CLOCK_fail bit reports [1].