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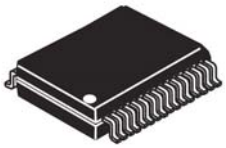
Document Number: MC07XSC200
Rev. 2.0, 9/2013

RoHS

Dual High Side Switch (7.0 mOhm)

07XSC200

HIGH SIDE SWITCH



EK SUFFIX PB-FREE
98ASA00368D
32-PIN EXPOSED PAD SOIC

The 07XSC200 is one in a family of devices designed for low-voltage lighting or factory automation applications. Its two low $R_{DS(ON)}$ MOSFETs (dual 7.0 mΩ) can control two separate 55 W / 28 W bulbs, and/or Xenon modules, and/or LEDs, and/or DC low voltage motors.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 07XSC200 allows the user to program via the SPI, the fault current trip levels and duration of acceptable inrush. The device has Fail-safe mode to provide fail-safe functionality of the outputs in case of MCU damaged.

The 07XSC200 is packaged in a Pb-free power-enhanced 32 pins SOIC package with exposed tab.

This device is powered by SMARTMOS technology.

Features

- Dual 7.0 mΩ max high side switch (at 25 °C)
- Operating voltage range of 6.0 to 20 V with sleep current < 5.0 µA, extended mode from 4.0 to 28 V
- 8.0 MHz 16-bit 3.3 V and 5.0 V SPI control and status reporting with daisy chain capability
- PWM module using external clock or calibratable internal oscillator with programmable outputs delay management
- Smart overcurrent shutdown compliant to huge inrush current, severe short-circuit, overtemperature protections with time limited auto-retry, and Fail-safe mode, in case of MCU damage
- Output OFF or ON OpenLoad detection compliant to bulbs or LEDs and short to battery detection. Analog current feedback with selectable ratio and board temperature feedback.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC07XSC200EK	-40 to 125 °C	32 SOIC

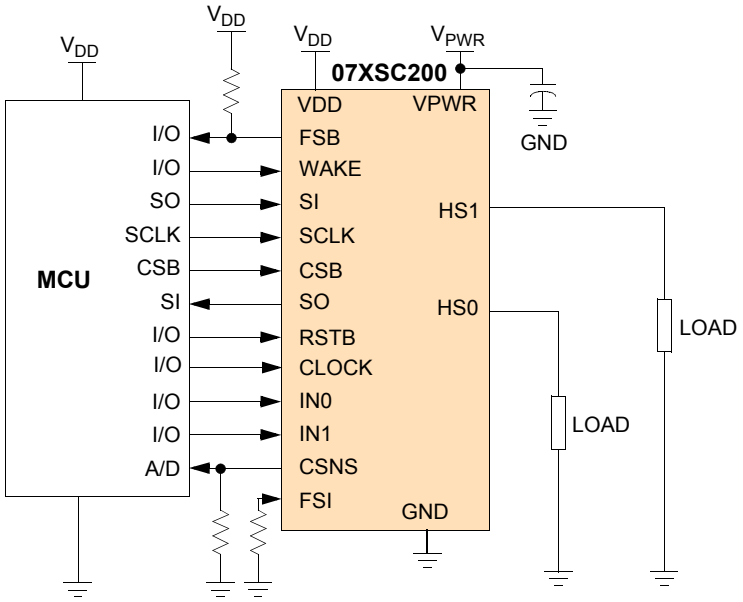


Figure 1. 07XSC200 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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freescale semiconductor

1 Internal Block Diagram

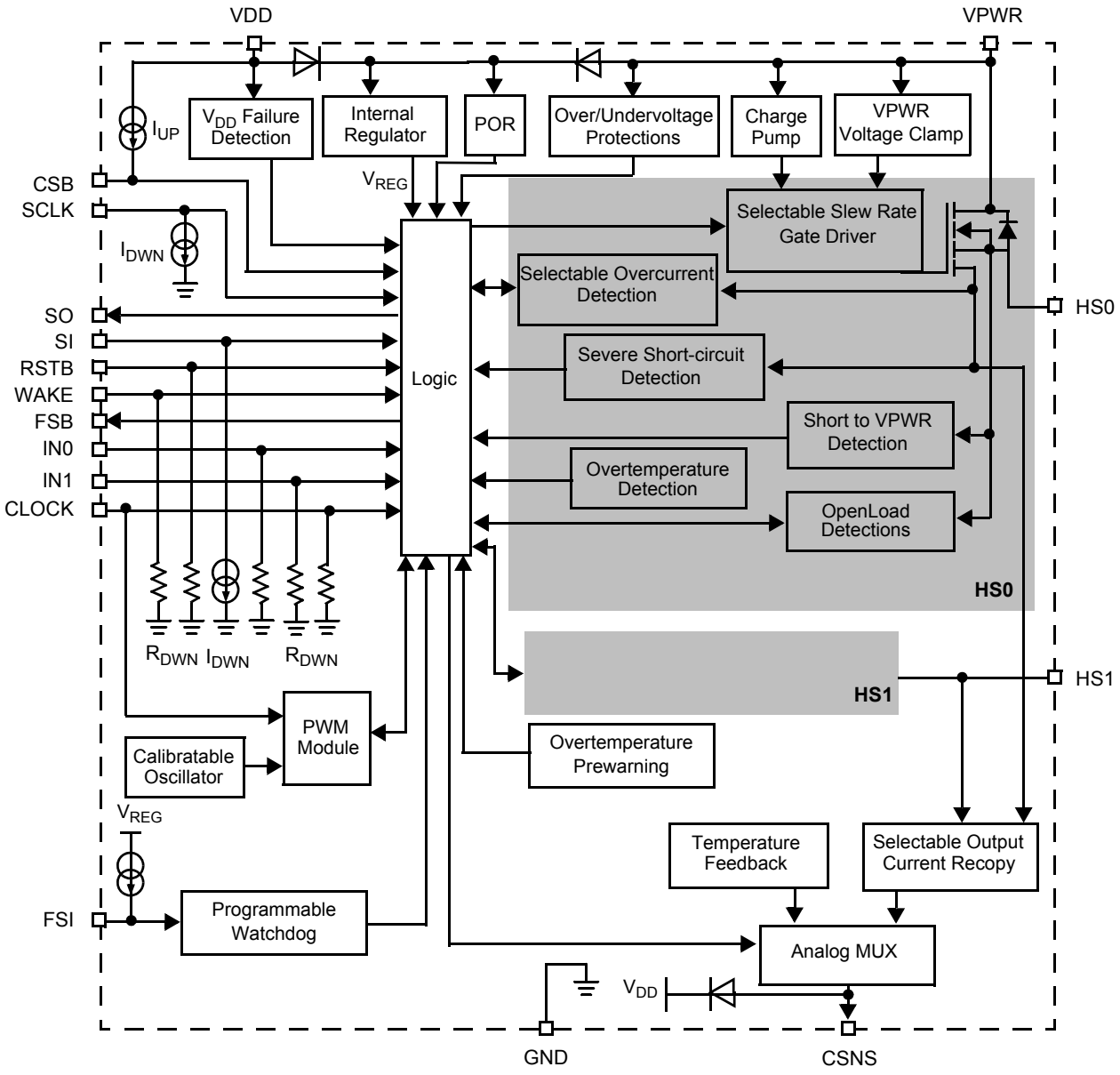

Figure 2. 07XSC200 Simplified Internal Block Diagram

2 Pin Connections

2.1 Pinout Diagram

Transparent top View

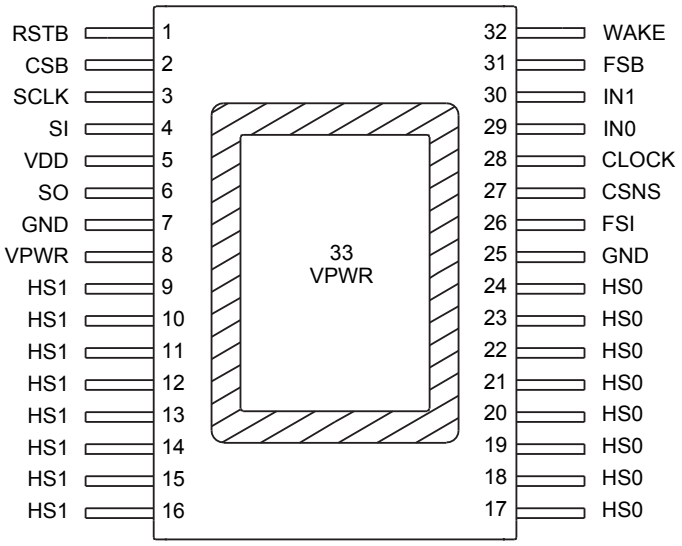

Figure 3. 07XSC200 Pin Connection

2.2 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 22.

Table 1. 07XSC200 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	RSTB	Input	Reset (Active Low)	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low current Sleep mode.
2	CSB	Input	Chip Select (Active Low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
3	SCLK	Input	Serial Clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.
4	SI	Input	Serial Input	This is a command data input pin connected to the SPI Serial Data Output of the MCU or to the SO pin of the previous device of a daisy chain of devices.
5	VDD	Input	Digital Drain Voltage (Power)	This is an external voltage input pin used to supply power to the SPI circuit.
6	SO	Output	Serial Output	This output pin is connected to the SPI serial data input pin of the MCU or to the SI pin of the next device of a daisy chain of devices.
7, 25	GND	Ground	Ground	Those pins are the ground for the logic and analog circuitry of the device. These pins must be shorted to board level.

Table 1. 07XSC200 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
8, 33	VPWR	Power	Positive Power Supply	Pin 8 is a positive supply for quiet and accurate control. Pin 33 is a power supply for the high current switch. These pins must be shorted at board level. Connecting a heatsink to pin 33 guarantees optimal heat-evacuation properties.
9 to 16	HS1	Output	High Side Output	Protected 7.0 mΩ high side power output pin to the load. Those pins must be shorted at board level.
26	FSI	Input	Fail-safe Input	The value of the resistance connected between this pin and ground determines the state of the outputs after a watchdog time-out occurs.
27	CSNS	Output	Output Current Monitoring	This pin is used to output a current proportional to the designated HS0-1 output.
28	CLOCK	Input	Reference Clock	This pin is used to apply a reference clock used to control the outputs in PWM mode through embedded PWM module.
29	IN0	Input	Direct Input 0	This input pin is used to directly control the output HS0.
30	IN1	Input	Direct Input 1	This input pin is used to directly control the output HS1.
31	FSB	Output	Fault Status (Active Low)	This is an open drain configured output requiring an external pull-up resistor to VDD for fault reporting.
32	WAKE	Input	Wake	This pin is used to input a Logic [1] signal so as to enable the watchdog timer function.

3 Electrical Characteristics

3.1 Maximum Ratings

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
V_{PWR} Supply Voltage Range • Load Dump at 25 °C (400 ms) • Maximum Operating Voltage • Reverse Battery	$V_{PWR(SS)}$	 41 28 -18	V
V_{DD} Supply Voltage Range	V_{DD}	-0.3 to 5.5	V
Input/Output Voltage	(4)	-0.3 to V_{DD}+0.3	V
WAKE Input Clamp Current	$I_{CL(WAKE)}$	2.5	mA
CSNS Input Clamp Current	$I_{CL(CSNS)}$	2.5	mA
HS [0:1] Voltage • Positive • Negative	$V_{HS[0:1]}$	 41 -24	V
Output Current per Channel • Nominal Continuous Current(1) • Short-circuit Transient Current • Reverse Continuous Current(1)	$I_{HS[0:1]}$	 26 116 -26	A
High Side Breakdown Voltage	V_{PWR} - V_{HS}	47	V
HS[0,1] Output Clamp Energy using single pulse method(2)	$E_{CL[0:1]}$	100	mJ
ESD Voltage(3) • Human Body Model (HBM) for HS[0:1], VPWR and GND • Human Body Model (HBM) for other pins • Charge Device Model (CDM) Corner Pins (1, 27, 28, 57) All Other Pins	 V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	 ±8000 ±2000 ±750 ±500	V

Notes

1. Continuous high side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using board thermal resistance is required.
2. Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14 V, T_J = 150 °C initial).
3. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
4. Input / Output pins are: IN[0:1], CLOCK, RSTB, FSI, CSNS, SI, SCLK, CSB, SO, FSB

Table 2. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature • Ambient • Junction [5]	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
THERMAL RESISTANCE			
Thermal Resistance • Junction to Case • Junction to Ambient[6]	 $R_{\theta JC}$ $R_{\theta JA}$	 4.0 35	°C/W
Peak Pin Reflow Temperature During Solder Mounting[7]	T_{SOLDER}	260	°C

Notes

5. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
6. Device mounted on a 2s2p test board per JEDEC JESD51-2. 20 °C/W of $R_{\theta JA}$ can be reached in a real application case (4 layers board).
7. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

3.2 Static Electrical Characteristics

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUTS					
Battery Supply Voltage Range	V_{PWR}				V
• Fully Operational		6.0	–	20	
• Extended mode[8]		4.0	–	28	
Battery Clamp Voltage[9]	$V_{PWR(CLAMP)}$	41	47	53	V
V_{PWR} Operating Supply Current	$I_{PWR(ON)}$				mA
• Outputs commanded ON, HS[0:1] open, IN[0:1] > V_{IH}		–	6.5	20	
V_{PWR} Supply Current	$I_{PWR(SBY)}$				mA
• Outputs commanded OFF, OFF Open-load Detection Disabled, HS[0:1] shorted to the ground with V_{DD} = 5.5 V WAKE > V_{IH} or RSTB > V_{IH} and IN[0:1] < V_{IL}		–	6.5	7.5	
Sleep State Supply Current V_{PWR} = 12 V, RSTB = WAKE = CLOCK = IN[0:1] < V_{IL}, HS[0:1] shorted to ground	$I_{PWR(SLEEP)}$				µA
• T_A = 25 °C		–	1.0	5.0	
• T_A = 85 °C		–	–	30	
V_{DD} Supply Voltage	$V_{DD(ON)}$	3.0	–	5.5	V
V_{DD} Supply Current at V_{DD} = 5.5 V	$I_{DD(ON)}$				mA
• No SPI Communication		–	1.6	2.2	
• 8.0 MHz SPI Communication[10]		–	5.0	–	
V_{DD} Sleep State Current at V_{DD} = 5.5 V	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage Shutdown Threshold	$V_{PWR(OV)}$	28	32	36	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Shutdown Threshold[11]	$V_{PWR(UV)}$	3.3	3.9	4.3	V
V_{PWR} and V_{DD} Power on Reset Threshold	$V_{SUPPLY(POR)}$	0.5	–	0.9	$V_{PWR(UV)}$
Recovery Undervoltage Threshold	$V_{PWR(UV)\_UP}$	3.4	4.1	4.5	V
V_{DD} Supply Failure Threshold (for V_{PWR} > $V_{PWR(UV)}$)	$V_{DD(FAIL)}$	2.2	2.5	2.8	V

Notes

8. In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
9. Measured with the outputs open.
10. Typical value guaranteed per design.
11. Output will automatically recover with time limited auto-retry to instructed state when V_{PWR} voltage is restored to normal as long as the V_{PWR} degradation level did not go below the undervoltage power-ON reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS1					
HS[0,1] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 25 °C)	$R_{DS\_01(ON)}$				mΩ
• V_{PWR} = 4.5 V		–	–	25.2	
• V_{PWR} = 6.0 V		–	–	11.2	
• V_{PWR} = 10 V		–	–	7.0	
• V_{PWR} = 13 V		–	–	7.0	
HS[0,1] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 150 °C)	$R_{DS\_01(ON)}$				mΩ
• V_{PWR} = 4.5 V		–	–	42.8	
• V_{PWR} = 6.0 V		–	–	19.1	
• V_{PWR} = 10 V		–	–	11.9	
• V_{PWR} = 13 V		–	–	11.9	
HS[0,1] Output Source-to-Drain ON Resistance (I_{HS} = -5.0 A, $V_{PWR=}$ -18 V)(12)	$R_{SD\_01(ON)}$				mΩ
• T_A = 25 °C		–	–	10.5	
• T_A = 150 °C		–	–	14	
HS[0,1] Maximum Severe Short-circuit Impedance Detection(13)	R_{SHORT_01}	21	47	75	mΩ
HS[0,1] Output Overcurrent Detection Levels (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V)					A
• 28W bit = 0	OCHI1_0	89.9	114.8	139.8	
	OCHI2_0	67	83.7	100.4	
	OC1_0	48	61.2	74.4	
	OC2_0	42	53.2	64.4	
	OC3_0	35.2	44.6	54	
	OC4_0	28.8	36.4	44	
	OCLO4_0	21	26.6	32.1	
	OCLO3_0	13.3	18.4	23.5	
	OCLO2_0	11.3	14.2	17.1	
	OCLO1_0	7.4	9.3	11.2	
• 28W bit = 1	OCHI1_1	44.9	57.4	69.9	
	OCHI2_1	33.5	41.9	50.2	
	OC1_1	24	30.6	37.2	
	OC2_1	20.8	26.5	32.1	
	OC3_1	17.6	22.3	27	
	OC4_1	14.4	18.2	22	
	OCLO4_1	6.1	7.6	9.0	
	OCLO3_1	6.1	7.6	9.0	
	OCLO2_1	6.1	7.6	9.0	
	OCLO1_1	2.7	4.9	7.0	

Notes

12. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.
13. Short-circuit impedance calculated from HS[0:1] to GND pins. Value guaranteed per design.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS1 (CONTINUED)					
HS[0,1] Current Sense Ratio (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V, CSNS ≤ 5.0 V)[14]					–
• 28W bit = 0					
• CSNS_ratio bit = 0	C_{SR0_0}	–	1/10700	–	
• CSNS_ratio bit = 1	C_{SR1_0}	–	1/63600	–	
• 28W bit = 1					
• CSNS_ratio bit = 0	C_{SR0_1}	–	1/5350	–	
• CSNS_ratio bit = 1	C_{SR1_1}	–	1/31800	–	
HS[0,1] Current Sense Ratio (C_{SR0}) Accuracy (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 0	$C_{SR0\_0\_ACC}$				%
25 and 125 °C					
• $I_{HS[0:1]}$ = 12.5 A		-15	–	15	
• $I_{HS[0:1]}$ = 5.0 A		-22	–	22	
• $I_{HS[0:1]}$ = 3.0 A		-27	–	27	
• $I_{HS[0:1]}$ = 1.5 A		-30	–	30	
-40 °C					
• $I_{HS[0:1]}$ = 12.5 A		-20	–	20	
• $I_{HS[0:1]}$ = 5.0 A		-27	–	27	
• $I_{HS[0:1]}$ = 3.0 A		-30	–	30	
• $I_{HS[0:1]}$ = 1.5 A		-40	–	40	
HS[0,1] Current Recopy Accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 0[15]	$C_{SR0\_0\_ACC}$ (CAL)				%
• $I_{HS[0:1]}$ = 5.0 A		-5.0	–	5.0	
HS[0,1] Current Sense Ratio (C_{SR0}) Accuracy (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 1	$C_{SR0\_1\_ACC}$				%
25 and 125 °C					
• $I_{HS[0:1]}$ = 3.0 A		-25	–	25	
• $I_{HS[0:1]}$ = 1.5 A		-30	–	30	
-40 °C					
• $I_{HS[0:1]}$ = 3.0 A		-30	–	30	
• $I_{HS[0:1]}$ = 1.5 A		-40	–	40	
HS[0,1] Current Recopy Accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 1[15]	$C_{SR0\_1\_ACC}$ (CAL)				%
• $I_{HS[0:1]}$ = 3.0 A		-5.0	–	5.0	
HS[0,1] C_{SR0} Current Recopy Temperature Drift (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 0[16]	$\Delta(C_{SR0\_0})/\Delta(T)$				%/°C
• $I_{HS[0:1]}$ = 5.0 A		–	–	0.04	

Notes

14. Current sense ratio = I_{CSNS} / $I_{HS[0:1]}$
15. Based on statistical analysis. It is not production tested.
16. Based on statistical data: delta(C_{SR0})/delta(T)={(measured I_{CSNS} at T_1 - measured I_{CSNS} at T_2) / measured I_{CSNS} at room} / {T_1-T_2}. No production tested.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS1 (CONTINUED)					
HS[0,1] Current Sense Ratio (C_{SR1}) Accuracy (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 0	$C_{SR1\_0\_ACC}$				%
25 and 125 °C					
• $I_{HS[0:1]}$ = 12.5 A		-20	–	20	
• $I_{HS[0:1]}$ = 75 A		-17	–	17	
-40 °C					
• $I_{HS[0:1]}$ = 12.5 A		-28	–	28	
• $I_{HS[0:1]}$ = 75 A		-25	–	25	
HS[0,1] Current Recopy Accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 0[17]	$C_{SR1\_0\_ACC}$ (CAL)				%
• $I_{HS[0:1]}$ = 12.5 A		-5.0	–	5.0	
HS[0,1] Current Sense Ratio (C_{SR1}) Accuracy (6.0V ≤ $V_{HS[0:1]}$ ≤ 20V) with 28W bit = 1	$C_{SR1\_1\_ACC}$				%
25 and 125 °C					
• $I_{HS[0:1]}$ = 12.5 A		-20	–	20	
• $I_{HS[0:1]}$ = 37.5 A		-17	–	17	
-40 °C					
• $I_{HS[0:1]}$ = 12.5 A		-28	–	28	
• $I_{HS[0:1]}$ = 75 A		-25	–	25	
HS[0,1] Current Recopy Accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) with 28W bit = 1[17]	$C_{SR1\_1\_ACC}$ (CAL)				%
• $I_{HS[0:1]}$ = 12.5 A		-5.0	–	5.0	
Current Sense Clamp Voltage	$V_{CL(CSNS)}$				V
• CSNS Open; $I_{HS[0:1]}$ = 5.0 A with C_{SR0} ratio		V_{DD}+0.25	–	V_{DD}+1.0	
OFF OpenLoad Detection Source Current[18]	$I_{OLD(OFF)}$	30	–	100	µA
OFF OpenLoad Fault Detection Voltage Threshold	$V_{OLD(THRES)}$	2.0	3.0	4.0	V
ON OpenLoad Fault Detection Current Threshold	$I_{OLD(ON)}$	80	330	660	mA
ON OpenLoad Fault Detection Current Threshold with LED	$I_{OLD(ON\_LED)}$				mA
• $V_{HS[0:1]}$ = V_{PWR} - 0.75 V		2.5	5.0	10	
Output Short to V_{PWR} Detection Voltage Threshold	$V_{OSD(THRES)}$				V
• Output programmed OFF		V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	
Output Negative Clamp Voltage	V_{CL}				V
• 0.5 A ≤ $I_{HS[0:1]}$ ≤ 5.0 A, Output programmed OFF		-22	–	-16	
Output Overtemperature Shutdown for 4.5 V < V_{PWR} < 28 V	T_{SD}	155	175	195	°C

Notes

17. Based on statistical analysis. It is not production tested.
18. Output OFF OpenLoad Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open-load condition when the specific output is commanded OFF. Pull-up current is measured for V_{HS} = $V_{OLD(THRES)}$

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Logic High Voltage[19]	V_{IH}	2.0	–	V_{DD}+0.3	V
Input Logic Low Voltage[19]	V_{IL}	-0.3	–	0.8	V
Input Logic Pull-down Current (SCLK, SI)[22]	I_{DWN}	5.0	–	20	µA
Input Logic Pull-up Current (CSB) [23]	I_{UP}	5.0	–	20	µA
SO, FSB Tri-state Capacitance[20]	C_{SO}	–	–	20	pF
Input Logic Pull-down Resistor (RSTB, WAKE, CLOCk and IN[0:1])	R_{DWN}	125	250	500	kΩ
Input Capacitance[20]	CIN	–	4.0	12	pF
Wake Input Clamp Voltage[21] • $I_{CL(WAKE)}$ < 2.5 mA	$V_{CL(WAKE)}$	18	25	32	V
Wake Input Forward Voltage • $I_{CL(WAKE)}$ = -2.5 mA	$V_{F(WAKE)}$	-2.0	–	-0.3	V
SO High-state Output Voltage • I_{OH} = 1.0 mA	V_{SOH}	V_{DD}-0.4	–	–	V
SO and FSB Low-state Output Voltage • I_{OL} = -1.0 mA	V_{SOL}	–	–	0.4	V
SO, CSNS and FSB Tri-state Leakage Current • CSB = V_{IH} and 0 V ≤ V_{SO} ≤ V_{DD}, or FSB = 5.5 V, or CSNS = 0.0 V	$I_{SO(LEAK)}$	-2.0	0.0	2.0	µA
FSI External Pull-down Resistance[24] • Watchdog Disabled • Watchdog Enabled	RFS	– 10	0.0 Infinite	1.0 –	kΩ

Notes

19. Upper and lower logic threshold voltage range applies to SI, CSB, SCLK, FSB, IN[0:1], CLOCK and WAKE input signals. The WAKE and RSTB signals may be supplied by a derived voltage referenced to V_{PWR}.
20. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CLOCK and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
21. The current must be limited by a series resistance when using voltages > 7.0 V.
22. Pull-down current is with V_{SI} ≥ 1.0 V and V_{SCLK} ≥ 1.0 V.
23. Pull-up current is with V_{CSB} ≤ 2.0 V. CSB has an active internal pull-up to V_{DD}.
24. In Fail-safe HS[0:1] depends respectively on IN[0:1]. FSI has an active internal pull-up to V_{REG} ~ 3.0 V.

3.3 Dynamic Electrical Characteristics

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS1					
Output Rising Medium Slew Rate (medium speed slew rate / SR[1:0] = 00)(25) • V_{PWR} = 14 V	SR_{R_00}	0.15	0.3	0.6	V/µs
Output Rising Slow Slew Rate (low speed slew rate / SR[1:0] = 01)(25) • V_{PWR} = 14 V	SR_{R_01}	0.07	0.15	0.3	V/µs
Output Falling Fast Slew Rate (high speed slew rate / SR[1:0] = 10)(25) • V_{PWR} = 14 V	SR_{R_10}	0.3	0.6	1.2	V/µs
Output Falling Medium Slew Rate (medium speed slew rate / SR[1:0] = 00)(25) • V_{PWR} = 14 V	SR_{F_00}	0.15	0.3	0.6	V/µs
Output Falling Slow Slew Rate (low speed slew rate / SR[1:0] = 01)(25) • V_{PWR} = 14 V	SR_{F_01}	0.07	0.15	0.3	V/µs
Output Rising Fast Slew Rate (high speed slew rate / SR[1:0] = 10)(25) • V_{PWR} = 14 V	SR_{F_10}	0.3	0.6	1.2	V/µs
HS[0:1] Outputs Turn-ON and OFF Delay Times(26)(27) V_{PWR} = 14 V for medium speed slew rate (SR[1:0] = 00) • $t_{DLY(ON)}$ • $t_{DLY(OFF)}$	t_{DLY_12}	 80 40	 130 90	 180 140	µs
Driver Output Matching Slew Rate (SR_R /SR_F) • V_{PWR} = 14 V @ 25 °C and for medium speed slew rate (SR[1:0] = 00)	ΔSR	0.8	1.0	1.2	
HS[0:1] Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) • V_{PWR} = 14 V, f_{PWM} = 240 Hz, PWM duty cycle = 50%, @ 25 °C for medium speed slew rate (SR[1:0] = 00)	Δt_{RF_01}	0	50	100	µs

Notes

25. Rise and Fall Slew Rates measured across a 5.0 Ω resistive load at high side output = 30% to 70% (see Figure 4, page 19).
26. Turn-ON delay time measured from rising edge of any signal (IN[0:1] and CSB) that would turn the output ON to $V_{HS[0:1]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load.
27. Turn-OFF delay time measured from falling edge of any signal (IN[0:1] and CSB) that would turn the output OFF to $V_{HS[0:1]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS1 (continued)					
Fault Detection Blanking Time[28]	t_{FAULT}	1.0	5.0	20	µs
Output Shutdown Delay Time[29]	t_{DETECT}	–	7.0	30	µs
CSNS Valid Time[30]	t_{CNSVAL}	–	70	100	µs
Watchdog Time-out[31]	t_{WDTO}	217	310	400	ms
ON OpenLoad Fault Cyclic Detection Time with LED	$T_{OLD(LED)}$	105	150	195	ms

Notes

28. Time necessary to report the fault to FSB pin.
29. Time necessary to switch-off the output in case of OT or OC or SC or UV fault detection (from negative edge of FSB pin to HS voltage = 50% of V_{PWR}
30. Time necessary for CSNS to be within ±5% of the targeted value (from HS voltage = 50% of V_{PWR} to ±5% of the targeted CSNS value).
31. For FSI open, the Watchdog time-out delay measured from the rising edge of RSTB, to HS[0,1] output state depend on the corresponding input command.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS1 (continued)					
HS[0,1] Output Overcurrent Time Step for 28W bit = 0					ms
OC[1:0] = 00 (slow by default)	t_{OC1_00}	4.40	6.30	8.02	
	t_{OC2_00}	1.62	2.32	3.00	
	t_{OC3_00}	2.10	3.00	3.90	
	t_{OC4_00}	2.88	4.12	5.36	
	t_{OC5_00}	4.58	6.56	8.54	
	t_{OC6_00}	10.16	14.52	18.88	
	t_{OC7_00}	73.2	104.6	134.0	
OC[1:0]=01 (fast)	t_{OC1_01}	1.10	1.57	2.00	
	t_{OC2_01}	0.40	0.58	0.75	
	t_{OC3_01}	0.52	0.75	0.98	
	t_{OC4_01}	0.72	1.03	1.34	
	t_{OC5_01}	1.14	1.64	2.13	
	t_{OC6_01}	2.54	3.63	4.72	
	t_{OC7_01}	18.2	26.1	34.0	
OC[1:0]=10 (medium)	t_{OC1_10}	2.20	3.15	4.01	
	t_{OC2_10}	0.81	1.16	1.50	
	t_{OC3_10}	1.05	1.50	1.95	
	t_{OC4_10}	1.44	2.06	2.68	
	t_{OC5_10}	2.29	3.28	4.27	
	t_{OC6_10}	5.08	7.26	9.44	
	t_{OC7_10}	36.6	52.3	68.0	
OC[1:0]=11 (very slow)	t_{OC1_11}	8.8	12.6	16.4	
	t_{OC2_11}	3.2	4.6	21.4	
	t_{OC3_11}	4.2	6.0	7.8	
	t_{OC4_11}	5.7	8.2	10.7	
	t_{OC5_11}	9.1	13.1	17.0	
	t_{OC6_11}	20.3	29.0	37.7	
	t_{OC7_11}	146.4	209.2	272.0	

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS1 (continued)					
HS[0,1] Output Overcurrent Time Step for 28W bit = 1					ms
OC[1:0] = 00 (slow by default)	t_{OC1_00}	3.4	4.9	6.4	
	t_{OC2_00}	1.1	1.6	2.1	
	t_{OC3_00}	1.4	2.1	2.8	
	t_{OC4_00}	2.0	2.9	3.8	
	t_{OC5_00}	3.4	4.9	6.4	
	t_{OC6_00}	8.5	12.2	15.9	
	t_{OC7_00}	62.4	89.2	116.0	
OC[1:0] = 01 (fast)	t_{OC1_01}	0.86	1.24	1.61	
	t_{OC2_01}	0.28	0.40	0.52	
	t_{OC3_01}	0.36	0.52	0.68	
	t_{OC4_01}	0.51	0.74	0.96	
	t_{OC5_01}	0.78	1.12	1.46	
	t_{OC6_01}	2.14	3.06	3.98	
	t_{OC7_01}	20.2	22.2	28.9	
OC[1:0] = 10 (medium)	t_{OC1_10}	1.7	2.5	3.3	
	t_{OC2_10}	0.5	0.8	1.0	
	t_{OC3_10}	0.7	1.0	1.3	
	t_{OC4_10}	1.0	1.5	2.0	
	t_{OC5_10}	1.7	2.5	3.3	
	t_{OC6_10}	4.2	6.1	6.0	
	t_{OC7_10}	31.2	44.6	58.0	
OC[1:0] = 11 (very slow)	t_{OC1_11}	6.8	9.8	12.8	
	t_{OC2_11}	2.2	3.2	16.7	
	t_{OC3_11}	2.9	4.2	5.5	
	t_{OC4_11}	4.0	5.8	7.6	
	t_{OC5_11}	6.8	9.8	12.8	
	t_{OC6_11}	17.0	24.4	31.8	
	t_{OC7_11}	124.8	178.4	232.0	

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS1 (continued)					
HS[0,1] Bulb Cooling Time Step for 28W bit = 0					ms
CB[1:0] = 00 or 11 (medium)	t_{BC1_00}	242	347	452	
	t_{BC2_00}	126	181	236	
	t_{BC3_00}	140	200	260	
	t_{BC4_00}	158	226	294	
	t_{BC5_00}	181	259	337	
	t_{BC6_00}	211	302	393	
CB[1:0] = 01 (fast)	t_{BC1_01}	121	173	226	
	t_{BC2_01}	63	90	118	
	t_{BC3_01}	70	100	130	
	t_{BC4_01}	79	113	147	
	t_{BC5_01}	90	129	169	
	t_{BC6_01}	105	151	197	
CB[1:0] = 10 (slow)					
	t_{BC1_10}	484	694	1904	
	t_{BC2_10}	252	362	472	
	t_{BC3_10}	280	400	520	
	t_{BC4_10}	316	452	588	
	t_{BC5_10}	362	518	674	
	t_{BC6_10}	422	604	786	
HS[0,1] for 28W bit = 1					
CB[1:0] = 00 or 11 (medium)					
	t_{BC1_00}	291	417	542	
	t_{BC2_00}	156	224	292	
	t_{BC3_00}	178	255	332	
	t_{BC4_00}	208	298	388	
	t_{BC5_00}	251	359	467	
	t_{BC6_00}	314	449	584	
CB[1:0] = 01 (fast)					
	t_{BC1_01}	146	209	272	
	t_{BC2_01}	78	112	146	
	t_{BC3_01}	88	127	166	
	t_{BC4_01}	101	145	189	
	t_{BC5_01}	126	180	234	
	t_{BC6_01}	226	324	422	
CB[1:0] = 10 (slow)					
	t_{BC1_10}	583	834	1085	
	t_{BC2_10}	312	448	582	
	t_{BC3_10}	357	510	665	
	t_{BC4_10}	417	596	775	
	t_{BC5_10}	501	717	933	
	t_{BC6_10}	628	898	1170	

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PWM MODULE TIMING					
Input PWM Clock Range on CLOCK	f_{CLOCK}	7.68	–	30.72	kHz
Input PWM Clock Low Frequency Detection Range on CLOCK(33)	$f_{CLOCK(LOW)}$	1.0	2.0	4.0	kHz
Input PWM Clock High Frequency Detection Range on CLOCK(33)	$f_{CLOCK(HIGH)}$	100	–	400	kHz
Output PWM Frequency Range using external clock on CLOCK(32)	f_{PWM}	31.25	–	781	Hz
Output PWM Frequency Accuracy using Calibrated Oscillator(32)	$A_{FPWM(CAL)}$	-10	–	+10	%
Default Output PWM Frequency using Internal Oscillator	$f_{PWM(0)}$	84	120	156	Hz
CSB Calibration Low Minimum Time Detection Range	$t_{CSB(MIN)}$	14	20	26	µs
CSB Calibration Low Maximum Tine Detection Range	$t_{CSB(MAX)}$	140	200	260	µs
Output PWM Duty Cycle Range for f_{PWM} = 1.0 kHz for high speed slew rate(33)	R_{PWM_1k}	10	–	94	%
Output PWM Duty Cycle Range for f_{PWM} = 400 Hz(33)	R_{PWM_400}	6.0	–	98	%
Output PWM Duty Cycle Range for f_{PWM} = 200 Hz(33)	R_{PWM_200}	5.0	–	98	%
INPUT TIMING					
Direct Input Toggle Time-out	t_{IN}	175	250	325	ms
AUTO-RETRY TIMING					
Auto-retry Period	t_{AUTO}	105	150	195	ms
TEMPERATURE ON THE GND FLAG					
Thermal Prewarning Detection(34)	T_{OTWAR}	110	125	140	°C
Analog Temperature Feedback at T_A = 25 °C with R_{CSNS} = 2.5 kΩ	T_{FEED}	1.15	1.20	1.25	V
Analog Temperature Feedback Derating with R_{CSNS} = 2.5 kΩ(35)	DT_{FEED}	-3.5	-3.7	-3.9	mV/°C

Notes

32. Clock Fail detector available for PWM_en bit is set to logic [1] and CLOCK_sel is set to logic [0].
33. The PWM ratio is measured at V_{HS} = 50% of V_{PWR} and for the default SR value. It is possible to put the device fully-on (PWM duty cycle 100%) and fully-off (duty cycle 0%). For values outside this range, a calibration is needed between the PWM duty cycle programming and the PWM on the output with R_L = 5.0 Ω resistive load.
34. Typical value guaranteed per design.
35. Value guaranteed per statistical analysis.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS[36]					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	8.0	MHz
Required Low State Duration for RSTB[37]	t_{WRSTB}	10	–	–	µs
Rising Edge of CSB to Falling Edge of CSB (Required Setup Time)[38]	$t_{\overline{CSB}}$	–	–	1.0	µs
Rising Edge of RSTB to Falling Edge of CSB (Required Setup Time)[38]	t_{ENBL}	–	–	5.0	µs
Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)[38]	t_{LEAD}	–	–	500	ns
Required High State Duration of SCLK (Required Setup Time)[38]	t_{WSCLKh}	–	–	50	ns
Required Low State Duration of SCLK (Required Setup Time)[38]	t_{WSCLKl}	–	–	50	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)[38]	t_{LAG}	–	–	60	ns
SI to Falling Edge of SCLK (Required Setup Time)[39]	$t_{SI(SU)}$	–	–	37	ns
Falling Edge of SCLK to SI (Required Setup Time)[39]	$t_{SI(HOLD)}$	–	–	49	ns
SO Rise Time • C_L = 80 pF	t_{RSO}	–	–	13	ns
SO Fall Time • C_L = 80 pF	t_{FSO}	–	–	13	ns
SI, CSB, SCLK, Incoming Signal Rise Time[39]	t_{RSI}	–	–	13	ns
SI, CSB, SCLK, Incoming Signal Fall Time[39]	t_{FSI}	–	–	13	ns
Time from Falling Edge of CSB to SO Low-impedance[40]	$t_{SO(EN)}$	–	–	60	ns
Time from Rising Edge of CSB to SO High-impedance[41]	$t_{SO(DIS)}$	–	–	60	ns

Notes

36. Parameters guaranteed by design.
37. RSTB low duration measured with outputs enabled and going to OFF or disabled condition.
38. Maximum setup time required for the 07XSC200 is the minimum guaranteed time needed from the microcontroller.
39. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
40. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on CSB.
41. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on CSB.

3.4 Timing Diagrams

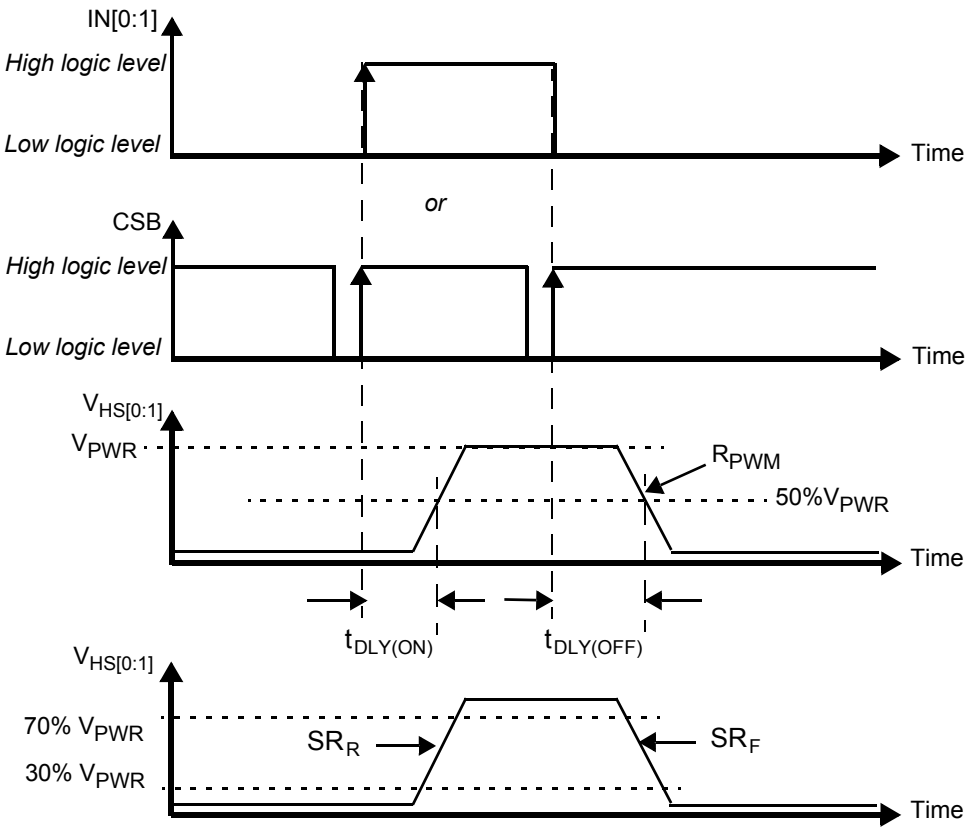

Figure 4. Output Slew Rate and Time Delays

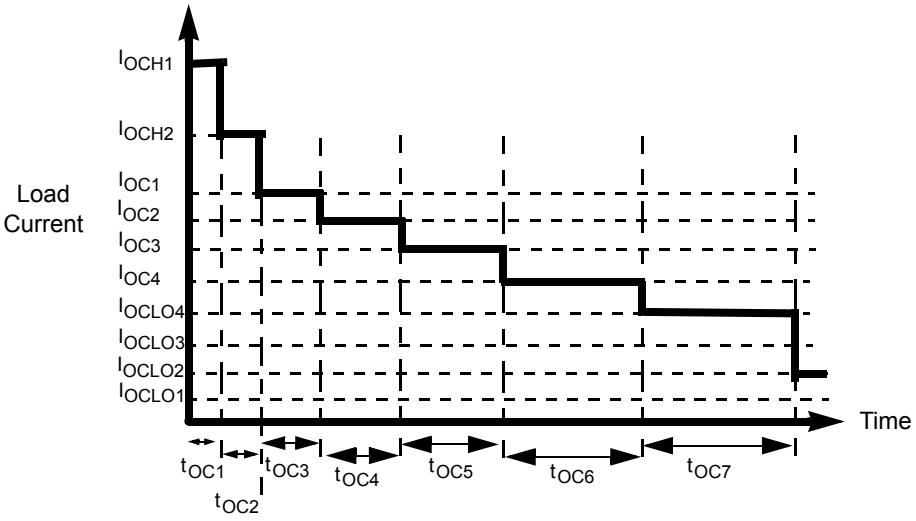

Figure 5. Overcurrent Shutdown Protection

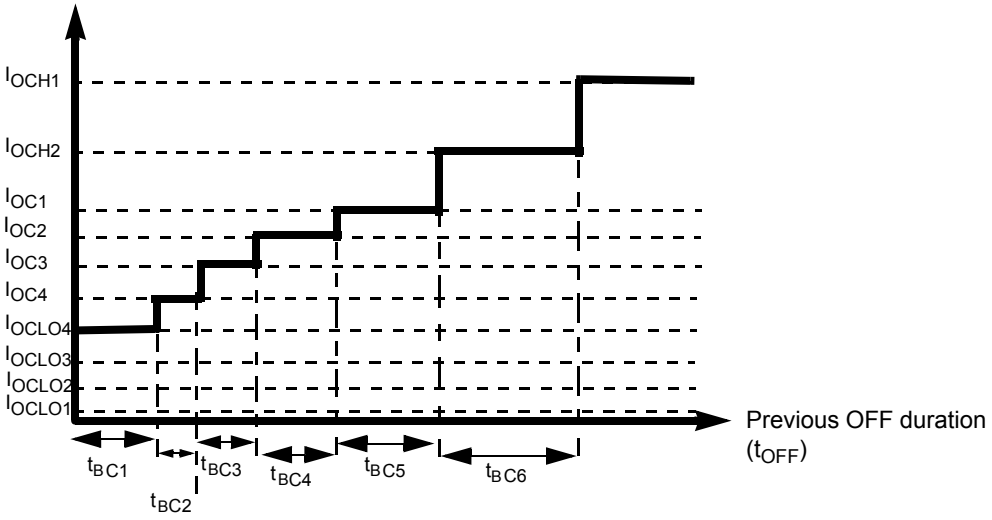

Figure 6. Bulb Cooling Management

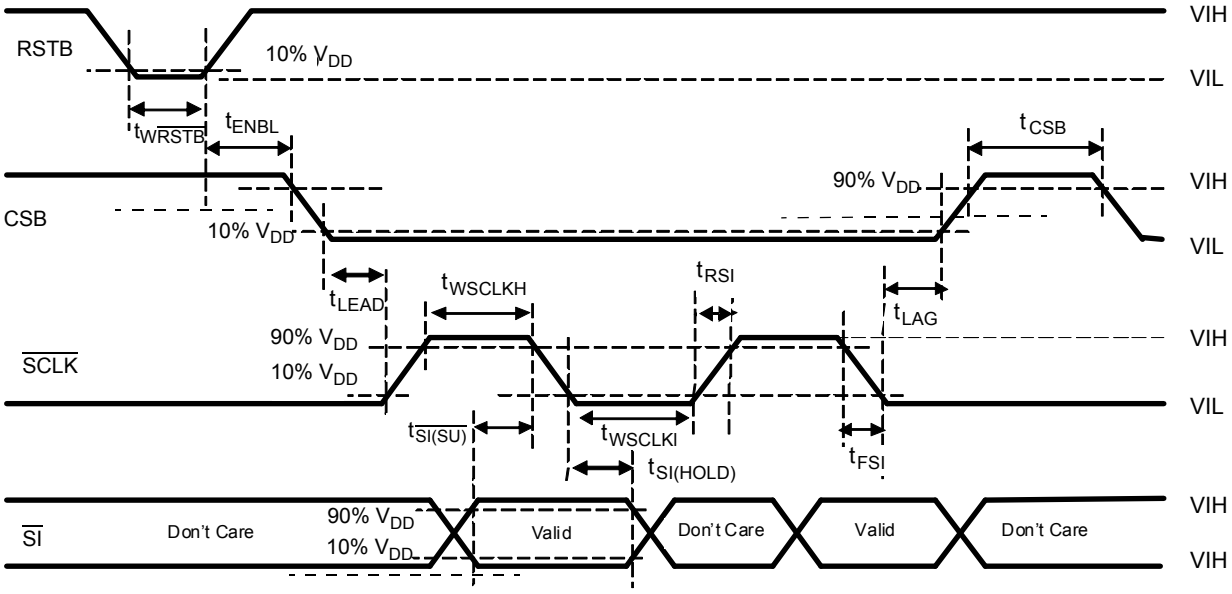

Figure 7. Input Timing Switching Characteristics

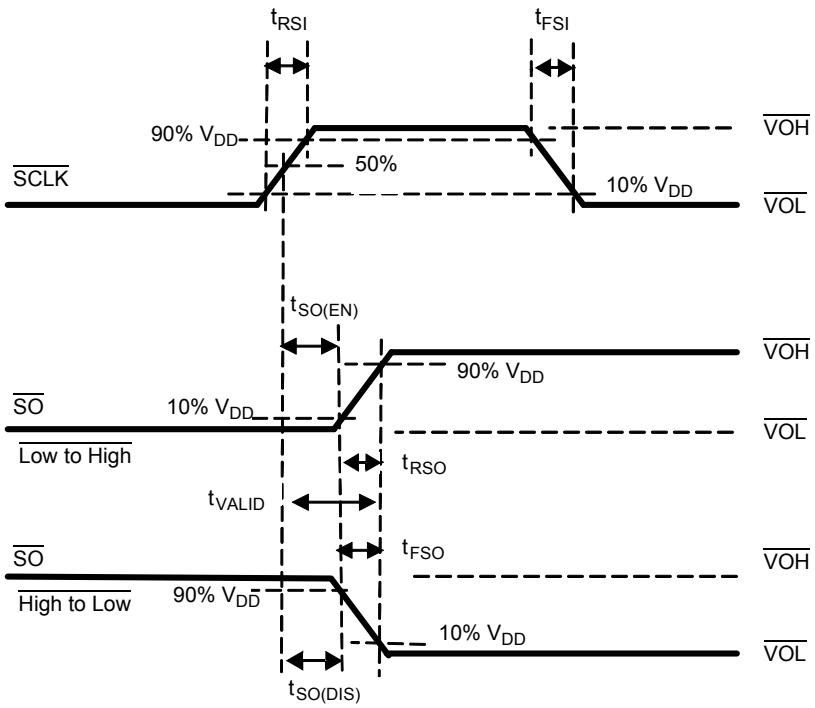

Figure 8. SCLK Waveform and Valid SO Data Delay Time

4 Functional Description

4.1 Introduction

The 07XSC200 is one in a family of devices designed for low-voltage lighting applications. Its two low $R_{DS(ON)}$ MOSFETs (dual 7.0 mΩ) can control two separate 55 W / 28 W bulbs and/or Xenon modules.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 07XSC200 allows the user to program via the SPI, the fault current trip levels and duration of acceptable lamp inrush. The device has fail-safe mode to provide fail-safe functionality of the outputs in case of MCU damaged.

4.2 Functional Pin Description

4.2.1 Output Current Monitoring (CSNS)

The Current Sense pin provides a current proportional to the designated HS0:HS1 output or a voltage proportional to the temperature on the GND flag. That current is fed into a ground-referenced resistor (2.5 kΩ typical) and its voltage is monitored by an MCU's A/D. The output type is selected via the SPI. This pin can be tri-stated through the SPI.

4.2.2 Direct Inputs (IN0, IN1)

Each IN input wakes the device. The IN0:IN1 high side input pins are also used to directly control HS0:HS1 high side output pins. If the outputs are controlled by PWM module, the external PWM clock is applied to IN0 pin. These pins are to be driven with CMOS levels, and they have a passive internal pull-down, R_{DWN}.

4.2.3 Fault Status (FSB)

This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. If a device fault condition is detected, this pin is active LOW. Specific device diagnostics and faults are reported via the SPI SO pin.

4.2.4 WAKE (WAKE)

The WAKE input wakes the device. An internal clamp protects this pin from high damaging voltages with a series resistor (10 kΩ typ). This input has a passive internal pull-down, R_{DWN}.

4.2.5 PWM Clock (CLOCK)

The clock input wakes the device. The PWM frequency and timing are generated from clock input by the PWM module. The clock input frequency is the selectable factor 2^7 = 128. This input has a passive internal pull-down, R_{DWN}.

4.2.6 RESET (RSTB)

The RESET input wakes the device. This is used to initialize the device configuration and fault registers, as well as place the device in a low-current sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin has a passive internal pull-down, R_{DWN}.

4.2.7 Chip Select (CSB)

The CSB pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 07XSC200 latches in data from the Input Shift registers to the addressed registers on the rising edge of CSB. The device transfers status information from the power output to the Shift register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. CSB has an active internal pull-up from V_{DD}, I_{UP}.

4.2.8 Serial Clock (SCLK)

The SCLK pin clocks the internal shift registers of the 07XSC200 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic low state whenever CSB makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed (CSB logic [1] state). SCLK has an active internal pull-down. When CSB is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 10, page 26). SCLK input has an active internal pull-down, I_{DWN}.

4.2.9 Serial Input (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 (MSB) to D0 (LSB). The internal registers of the 07XSC200 are configured and controlled using a 5-bit addressing scheme described in Table 9, page 36. Register addressing and configuration are described in Tables 10, page 36. SI input has an active internal pull-down, I_{DWN}.

4.2.10 Digital Drain Voltage (VDD)

This pin is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost (V_{DD} Failure), the device goes to Fail-safe mode.

4.2.11 Ground (GND)

These pins are the ground for the device.

4.2.12 Positive Power Supply (VPWR)

This pin connects to the positive power supply and is the source of operational power for the device. The VPWR contact is the backside surface mount tab of the package.

4.2.13 Serial Output (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high impedance state until the CSB pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, the state of the key inputs, etc. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. SO reporting descriptions are provided in Table 22, page 42.

4.2.14 High Side Outputs (HS0, HS1)

Protected 7.0 mΩ high side power outputs to the load.

4.2.15 Fail-safe Input (FSI)

This pin incorporates an active internal pull-up current source from internal supply (V_{REG}). This enables the watchdog time-out feature.

When the FSI pin is opened, the watchdog circuit is enabled. After a watchdog time-out occurs, the output states depends on IN[0:1].

When the FSI pin is connected to GND, the watchdog circuit is disabled. The output states depends on IN[0:1] in case of V_{DD} Failure condition, in case V_{DD} failure detection is activated (VDD_FAIL_en bit sets to logic [1]).

4.3 Functional Internal Block Description

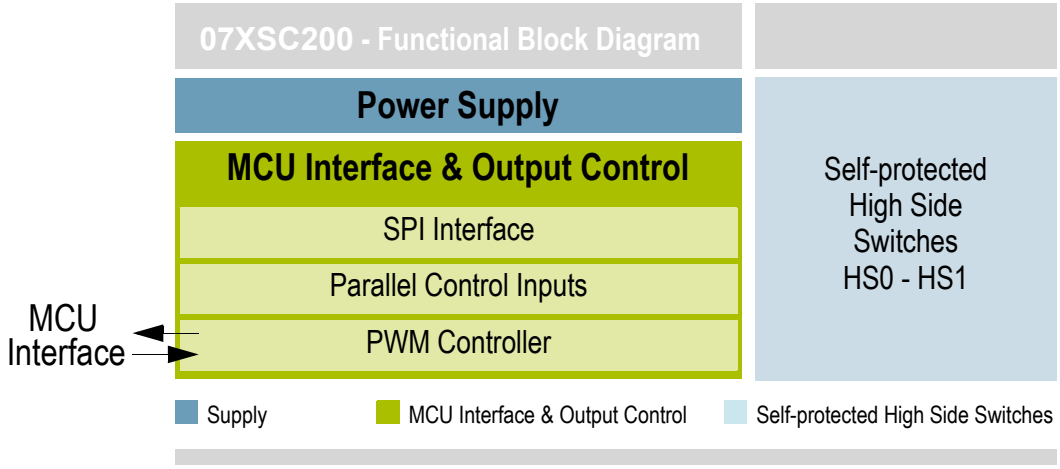

Figure 9. Functional Block Diagram

4.3.1 Power Supply

The 07XSC200 is designed to operate from 4.0 to 28 V on the VPWR pin. Characteristics are provided from 6.0 to 20 V for the device. The VPWR pin supplies power to internal regulator, analog, and logic circuit blocks. The V_{DD} supply is used for Serial Peripheral Interface (SPI) communication to configure and diagnose the device. This IC architecture provides a low quiescent current sleep mode. Applying V_{PWR} and V_{DD} to the device will place the device in the Normal mode. The device will transit to Fail-safe mode in case of failures on the SPI or/and on V_{DD} voltage.

4.3.2 High Side Switches: HS0–HS1

These pins are the high side outputs controlling lamps located for the front of vehicle, such as 65 W/55 W bulbs and Xenon-HID modules. N-channel MOSFETs with 7.0 mΩ $R_{DS(ON)}$ are self-protected and present extended diagnostics to detect bulb outage and a short-circuit fault condition. The HS output is actively clamped during turn off of inductive loads and inductive battery line. When driving DC motor or solenoid loads demand multiple switching, an external recirculation device must be used to maintain the device in its Safe Operating Area.

4.3.3 MCU Interface and Output Control

In Normal mode, each bulb is controlled directly from the MCU through the SPI. A pulse width modulation control module allows improvement of lamp lifetime with bulb power regulation (PWM frequency range from 100 to 400 Hz) and addressing the dimming application (day running light). An analog feedback output provides a current proportional to the load current or the temperature of the board. The SPI is used to configure and to read the diagnostic status (faults) of high side outputs. The reported fault conditions are: OpenLoad, short-circuit to battery, short-circuit to ground (overcurrent and severe short-circuit), thermal shutdown, and under/overvoltage.

In Fail-safe mode, each lamp is controlled with dedicated parallel input pins. The device is configured in default mode.