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Document order number: MC07XSF517
Rev. 2.0, 9/2013

Triple 7.0 mOhm and Dual 17 mOhm High Side Switch

07XSF517

ENHANCED PENTA HIGH SIDE SWITCH

EK SUFFIX (PB-FREE)
98ASA00367D
54-PIN SOICEP

The 07XSF517 is the latest achievement in DC motors and lighting drivers. It belongs to an expanding family to control and diagnose various types of loads, such as incandescent lamps or light-emitting diodes (LEDs) with enhanced precision. It combines flexibility through daisy chainable SPI 5.0 MHz, extended digital and analog feedbacks, safety, and robustness.

Output edge shaping helps to improve electromagnetic performance. To avoid shutting off the device upon inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a Fail operation mode, but remains operational, controllable, and protected.

This new generation of high side switch products family facilitates ECU design due to compatible MCU software and PCB foot prints for each device variant.

This family is packaged in a Pb-free power-enhanced SOIC package with an exposed pad, which is End of Life Vehicles directive compliant.

This device is powered by SMARTMOS technology.

Features

- Triple 7.0 mΩ and dual 17 mΩ high side switches with high transient current capability
- 16-bit 5.0 MHz SPI control of overcurrent profiles, channel control including PWM duty-cycles, output-ON and -OFF OpenLoad detections, thermal shut-down and prewarning, and fault reporting
- Output current monitoring with programmable synchronization signal and supply voltage feedback
- Limp Home mode
- External smart power switch control
- Operating voltage is 7.0 to 18 V with sleep current < 5.0 µA, extended mode from 6.0 to 28 V
- -16 V reverse polarity and ground disconnect protections
- Compatible PCB foot print and SPI software driver among the family

Applications

- Low voltage exterior lighting
- Low voltage industrial lighting
- Low voltage automation systems
- Halogen lamps
- Incandescent bulbs
- Light-emitting diodes (LEDs)
- HID Xenon ballasts
- DC motors

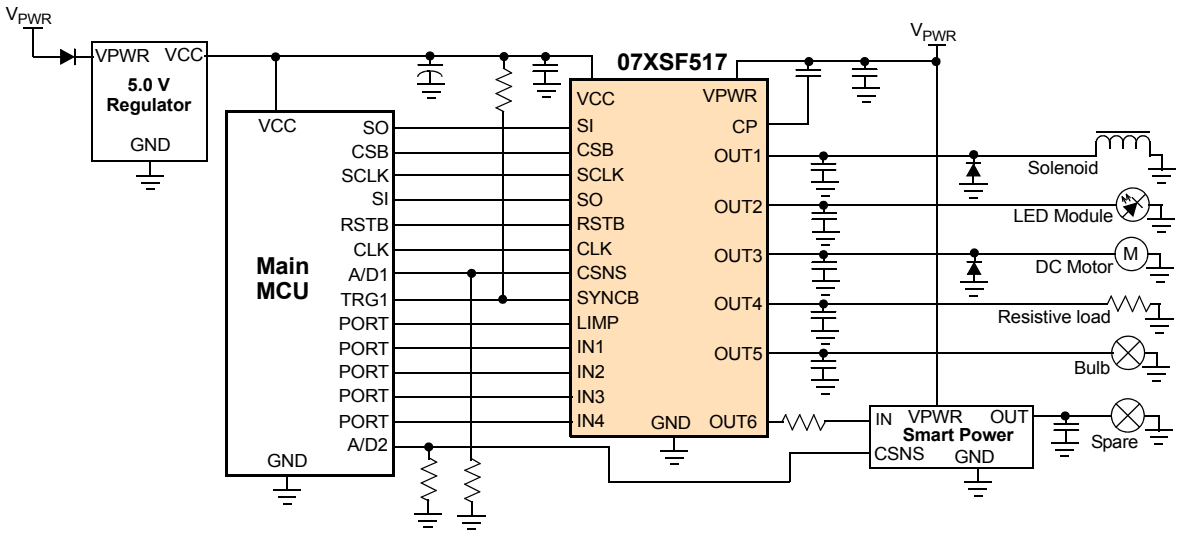

Figure 1. Triple 7.0 mOhm and Dual 17 mOhm Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

1 Orderable Parts

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable Part Variations

Part Number	Notes	Temperature (T_A)	Package	OUT1 Rds(on)	OUT2 Rds(on)	OUT3 Rds(on)	OUT4 Rds(on)	OUT5 Rds(on)	OUT6
MC07XSF517EK	(1)	-40 to 125 °C	SOIC 54 pins exposed pad	17 mΩ	17 mΩ	7.0 mΩ	7.0 mΩ	7.0 mΩ	Yes

Notes

1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers: 07XSF517.

Table of Contents

2 Internal Block Diagram

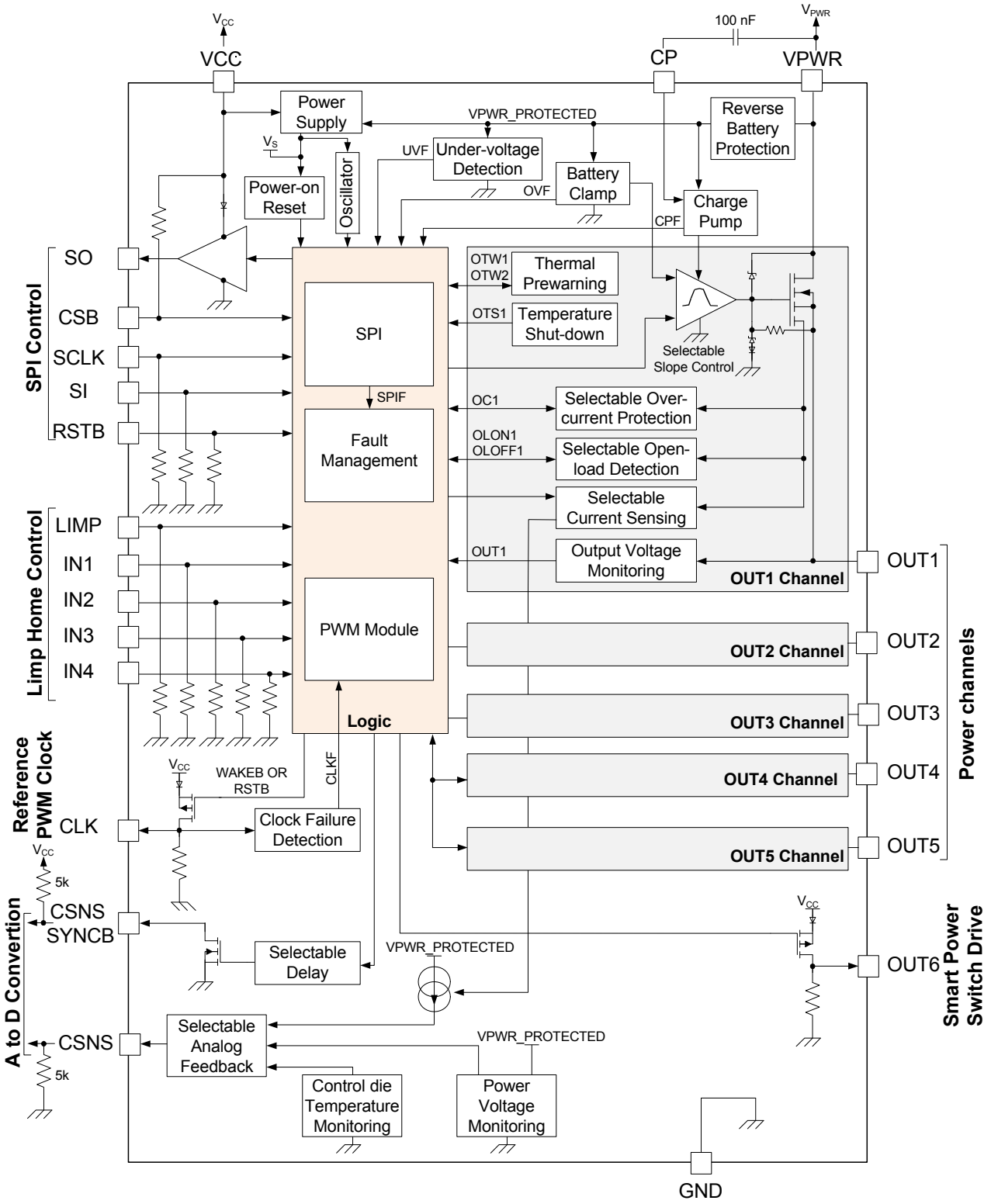

Figure 2. Simplified Internal Block Diagram (Penta version)

3 Pin Connections

3.1 Pinout Diagram

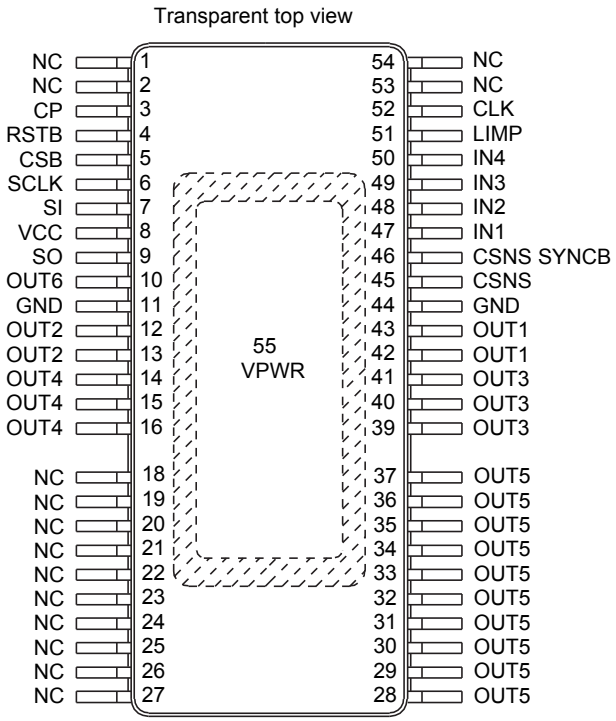

Figure 3. Pinout Diagram

3.2 Pin Definitions

Table 2. 07XSF517 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
3	CP	Internal supply	Charge-pump	This pin is the connection for an external capacitor for charge pump use only.
4	RSTB	SPI	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current sleep mode. This pin has a passive internal pull-down.
5	CSB	SPI	Chip select	This input pin is connected to a chip select output of a master microcontroller (MCU). When this digital signal is high, SPI signals are ignored. Asserting this pin low starts an SPI transaction. The transaction is indicated as completed when this signal returns to high level. This pin has a passive internal pull-up to V_{CC} through a diode.
6	SCLK	SPI	Serial clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication. This pin has an passive internal pull-down.
7	SI	SPI	Serial input	This pin is the data input of the SPI communication interface. The data at the input are sampled on the positive edge of the SCLK. This pin has a passive internal pull-down.

Table 2. 07XSF517 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
8	VCC	Power supply	MCU power supply	This pin is a power supply pin for internal logic, the SPI I/Os and the OUT6 driver.
9	SO	SPI	Serial Output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device of a daisychain of devices. The SPI changes on the negative edge of SCLK. When CSB is high, this pin is high-impedance.
10	OUT6	Output	External Solid State	This output pin controls an external Smart Power Switch by logic level. This pin has a passive internal pull-down.
11, 44	GND	Ground	Ground	These pins are the ground for the logic and analog circuitries of the device. For ESD and electrical parameter accuracy purpose, the ground pins must be shorted on the board.
12, 13	OUT2	Output	Channel #2	Protected high side power output pins to the load.
14, 15, 16	OUT4	Output	Channel #4	Protected high side power output pins to the load.
1, 2, 18… 27, 53, 54	NC	N/A	Not connected	These pins are not connected.
28… 37	OUT5	Output	Channel #5	Protected high side power output pins to the load.
39, 40, 41	OUT3	Output	Channel #3	Protected high side power output pins to the load.
42, 43	OUT1	Output	Channel #1	Protected high side power output pins to the load.
45	CSNS	Feedback	Current sense	This pin reports an analog value proportional to the designated OUT[1:5] output current or the temperature of the exposed pad or the supply voltage. It is used externally to generate a ground-referenced voltage for the microcontroller (MCU). Current recopy and analog voltage feedbacks are SPI programmable.
46	CSNS SYNCB	Feedback	Current sense synchronization	This open drain output pin allows synchronizing the MCU A/D conversion. This pin requires an external pull-up resistor to VCC.
47	IN1	Input	Direct input #1	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down.
48	IN2	Input	Direct input #2	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down
49	IN3	Input	Direct input #3	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down
50	IN4	Input	Direct input #4	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down
51	LIMP	Input	Limp Home	The Fail mode can be activated by this digital input. This pin has a passive internal pull-down.

Table 2. 07XSF517 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
52	CLK	Input/Output	Device mode feedback Reference PWM clock	This pin is an input/output pin. It is used to report the device sleep-state information. It is also used to apply reference PWM clock which will be divided by 2^8 in Normal operating mode. This pin has a passive internal pull-down.
55	VPWR	Power Supply	Supply power supply	This exposed pad connects to the positive power supply and is the source of operational power for the device.

Pins 17 and 38 are omitted.

4 General Product Characteristics

4.1 Relationship Between Ratings and Operating Requirements

The analog portion of device is supplied by the voltage applied to the VPWR exposed pad. Thereby the supply of internal circuitry (logic in case of a V_{CC} disconnect, charge pump, gate drive,...) is derived from the VPWR pin.

In case of a reverse supply:

- the internal supply rail is protected (max. -16 V)
- the output drivers (OUT1… OUT5) are switched on, to reduce the power consumption in the drivers when using incandescent bulbs

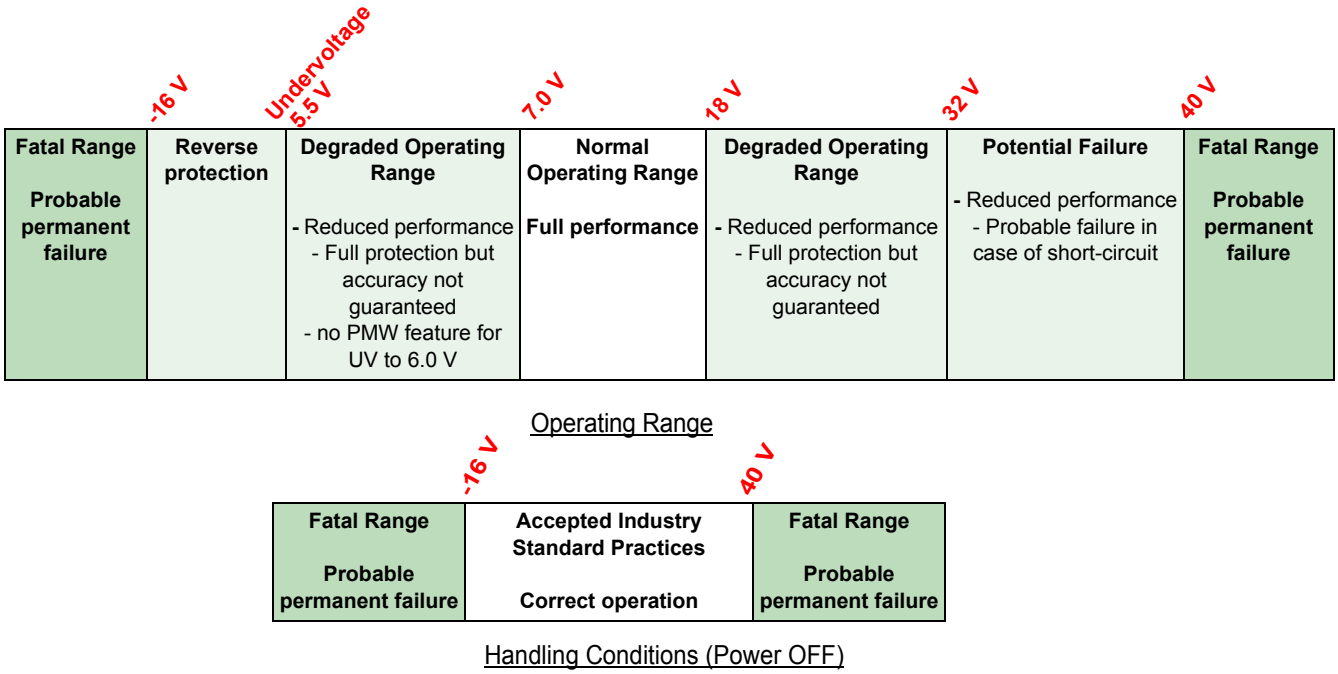

Figure 4. Ratings vs. Operating Requirements (VPWR pin)

The device's digital circuitry is powered by the voltage applied to the VCC pin. If VCC is disconnected, the logic part is supplied by the VPWR pin.

The output driver for SPI signals, CLK pin (wake feedback), and OUT6 are supplied by the VCC pin only. This pin shall be protected externally in case of a reverse polarity, and in case of a high-voltage disturbance.

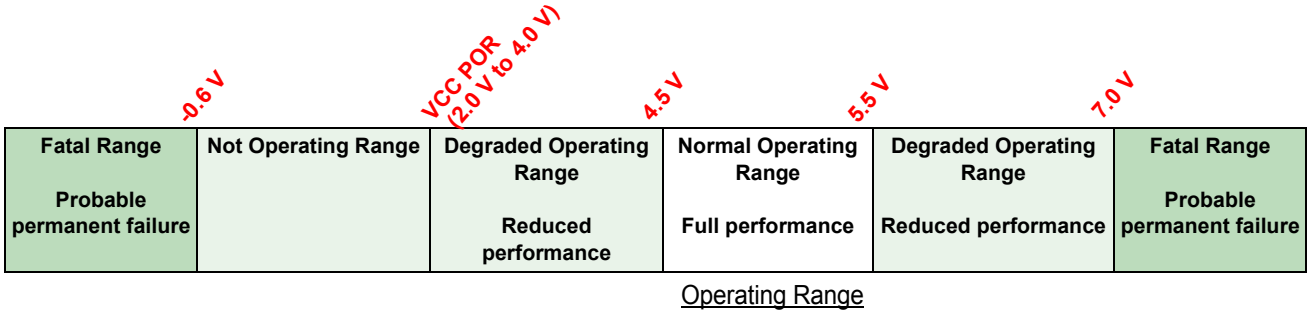

Figure 5. Ratings vs. Operating Requirements (VCC pin)

4.2 Maximum Ratings

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
ELECTRICAL RATINGS					
V_{PWR}	V_{PWR} Voltage Range	-16	40	V	
V_{CC}	VCC Logic Supply Voltage	-0.3	7.0	V	
V_{IN}	Digital Input Voltage			V	(2)
	• IN1… IN4 and LIMP	-0.3	40		
	• CLK, SI, SCLK, CSB, and RSTB	-0.3	20		
V_{OUT}	Digital Output Voltage			V	(2)
	• SO, CSNS, SYNC, OUT6, CLK	-0.3	20		
I_{CL}	Negative Digital Input Clamp Current	–	5.0	mA	(3)
I_{OUT}	Power Channel Current			A	(4)
	• 7.0 mΩ channel	–	11		
	• 17 mΩ channel	–	5.5		
E_{CL}	Power Channel Clamp Energy Capability			mJ	(5)
	• 7.0 mΩ channel - Initial T_J = 25 °C	–	200		
	• 7.0 mΩ channel - Initial T_J = 150 °C	–	100		
	• 17 mΩ channel - Initial T_J = 25 °C	–	100		
	• 17 mΩ channel - Initial T_J = 150 °C	–	50		
V_{ESD}	ESD Voltage			V	(6)
	• Human Body Model (HBM) - VPWR, Power Channel, and GND pins	-8000	+8000		
	• Human Body Model (HBM) - All other pins	-2000	+2000		
	• Charge Device Model (CDM) - Corner pins	-750	+750		
	• Charge Device Model (CDM) - All other pins	-500	+500		

Notes

2. Exceeding voltage limits on those pins may cause a malfunction or permanent damage to the device.
3. Maximum current in negative clamping for IN1… IN4, LIMP, RSTB, CLK, SI, SO, SCLK, and CSB pins
4. Continuous high side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
5. Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14 V). Please refer to Output Clamps section.
6. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model.

4.3 Thermal Characteristics

Table 4. Thermal Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
THERMAL RATINGS					
	Operating Temperature			°C	(7)
T_A	• Ambient	-40	+125		
T_J	• Junction	-40	+150		
T_{STG}	Storage Temperature	-55	+ 150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	–	260	°C	(8) (9)
THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\Theta JB}$	Junction-to-Board (1]Soldered to Board)	–	2.5	°/W	(10)
$R_{\Theta JA}$	Junction-to-Ambient, Natural Convection, Four-Layer Board (2s2p)	–	17.4	°/W	(11) (12)
$R_{\Theta JC}$	Junction-to-Case (Case top surface)	–	10.6	°/W	(13)

Notes

7. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
10. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
11. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
12. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
13. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

4.4 Operating Conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

Table 5. Operating Conditions

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min	Max	Unit	Notes
V_{PWR}	Functional operating supply voltage - Device is fully functional. All features are operating.	7.0	18	V	
	Overvoltage range			V	
	• Jump Start	–	28		
	• Load dump	–	40		
	Reverse Supply	-16	–	V	
V_{CC}	Functional operating supply voltage - Device is fully functional. All features are operating.	4.5	5.5	V	

4.5 Supply Currents

This section describes the current consumption characteristics of the device.

Table 6. Supply Currents

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Ratings	Min	Typ.	Max	Unit	Notes
VPWR CURRENT CONSUMPTIONS						
I_{QVPWR}	Sleep mode measured at V_{PWR} = 12 V • T_A = 25 °C • T_A = 125 °C	 – –	 1.2 10	 5.0 30	µA	(14) (15)
I_{VPWR}	Operating mode measured at V_{PWR} = 18 V	–	7.0	8.0	mA	(15)
VCC CURRENT CONSUMPTIONS						
I_{QVCC}	Sleep mode measured at V_{CC} = 5.5 V	–	0.05	5.0	µA	
I_{VCC}	Operating mode measured at V_{PWR} = 5.5 V (SPI frequency 5.0 MHz)	–	2.8	4.0	mA	

Notes

14. With the OUT1… OUT5 power channels grounded.
15. With the OUT1… OUT5 power channels opened.

5 General IC Functional Description and Application Information

5.1 Introduction

The 07XSF517 is an evolution of the successful Gen3 by providing improved features of a complete family of devices using Freescale's latest and unique technologies for the controller and the power stages.

It consists of a scalable family of devices compatible in terms of software driver and package footprint. It allows diagnosing the light-emitting diodes (LEDs) with an enhanced current sense precision with synchronization pin, as well as driving high power motors with a perfect control of its current consumption. It combines flexibility through daisy chainable SPI 5.0 MHz, extended digital and analog feedbacks, safety, and robustness. It integrates an enhanced PWM module with 8-bit duty cycle capability and PWM frequency prescaler per power channel.

5.2 Features

The main attributes of 07XSF517 are:

- Penta high side switches with overload, overtemperature and undervoltage protection
- control output for 1 external smart power switch
- 16 Bit SPI communication interface with daisy chain capability
- integrated Fail mode (ASIL B compliant functional safety behavior)
- dedicated control inputs for use in Fail mode
- analog feedback pin with SPI programmable multiplexer and sync signal
- channel diagnosis by SPI communication
- advanced current sense mode for LED usage
- synchronous PWM module with external clock, prescaler and multiphase feature
- excellent EMC behavior
- power net and reverse polarity protection
- ultra low power mode
- scalable and flexible family concept
- board layout compatible SOIC54 package with exposed pad

5.3 Block Diagram

The choice of multi-die technology in SOIC exposed pad package including low cost vertical trench FET power die associated with Smart Power control die lead to an optimized solution.

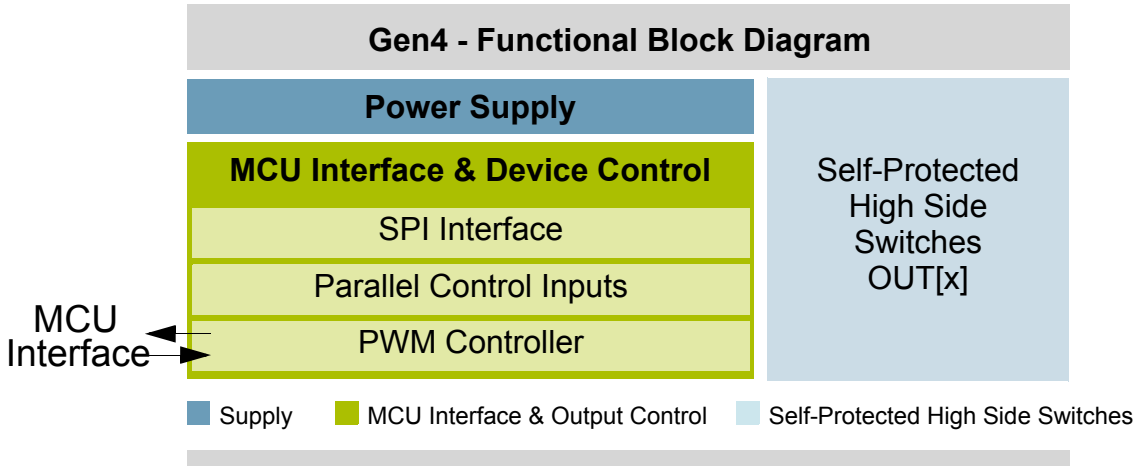

Figure 6. Functional Block Diagram

5.3.1 Self-protected High Side Switches

OUT1… OUT5 are the output pins of the power switches. The power channels are protected against various kinds of short-circuits and have active clamp circuitry that may be activated when switching off inductive loads. Many protective and diagnostic functions are available.

5.3.2 Power Supply

The device operates with supply voltages from 5.5 to 40 V (V_{PWR}), but is full spec. compliant only between 7.0 and 18 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VCC pin (5.0 V typ.) supplies the output register of the serial peripheral interface (SPI). Consequently, the SPI registers cannot be read without presence of V_{CC}. The employed IC architecture guarantees a low quiescent current in Sleep mode.

5.3.3 MCU Interface and Device Control

In Normal mode the power output channels are controlled by the embedded PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, V_{CC} has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: open-load, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, and under and overvoltage.

The device allows driving loads at different frequencies up to 400 Hz.

5.4 Functional Description

The device has four fundamental operating modes: Sleep, Normal, Fail, and Power off. It possesses multiple high side switches (power channels) each of which can be controlled independently:

- in Normal mode by SPI interface. For bidirectional SPI communication, a second supply voltage (V_{CC}) is required.
- in Fail mode by the corresponding the direct inputs IN1… IN4. The OUT5 for the Penta version and the OUT6 are off in this mode.

5.5 Modes of Operation

The operating modes are based on the signals:

- wake = (IN1_ON) OR (IN2_ON) OR (IN3_ON) OR (IN4_ON) OR (RST\). More details in Logic I/O Plausibility Check section.
- fail = (SPI_fail) OR (LIMP). More details in Loss of Communication Interface section.

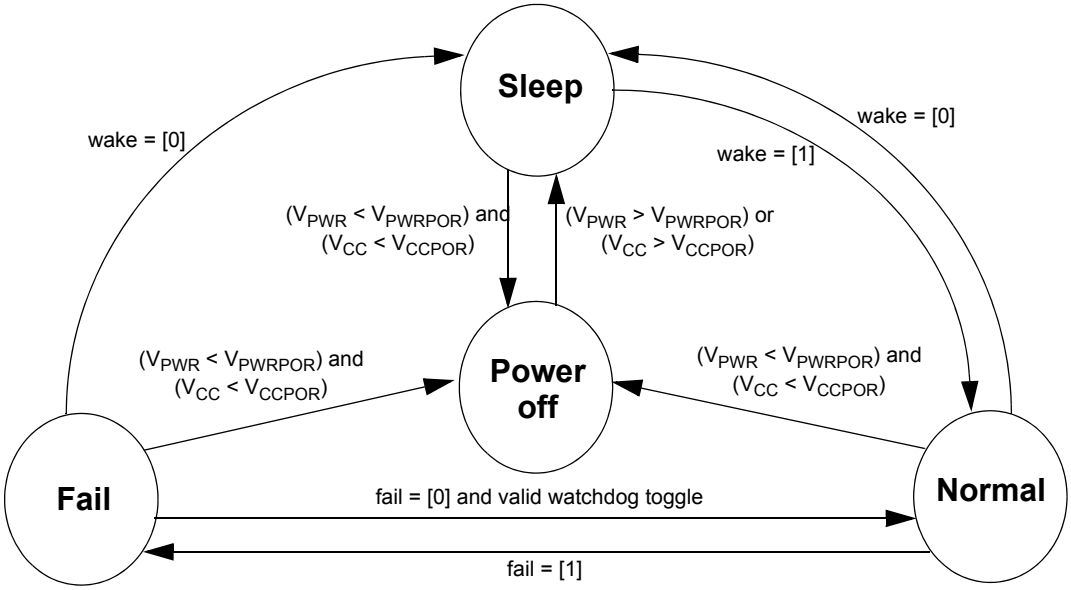

Figure 7. General IC Operating Modes

5.5.1 Power Off Mode

The power off mode is applied when V_{PWR} and V_{CC} are below the power on reset threshold ($V_{PWR\ POR}$, $V_{CC\ POR}$).

In power off, no functionality is available but the device is protected by the clamping circuits. Refer to Supply Voltages Disconnection section.

5.5.2 Sleep Mode

The Sleep mode is used to provide ultra low current consumption. During Sleep mode:

- the component is inactive and all outputs are disabled
- the outputs are protected by the clamping circuits
- the pull-up / pull-down resistors are present

The Sleep mode is the default mode of the device after applying the supply voltages (V_{PWR} or V_{CC}) prior to any wake-up condition (wake = [0]).

The wake-up from Sleep mode is provided by the wake signal.

5.5.3 Normal Mode

The Normal mode is the regular operating mode of the device. The device is in Normal mode, when the device is in the wake state (wake = [1]) and no fail condition (fail = [0]) is detected.

During Normal mode:

- the power outputs are under control of the SPI
- the power outputs are controlled by the programmable PWM module

- the power outputs are protected by the overload protection circuit
- the control of the power outputs by SPI programming
- the digital diagnostic feature transfers status of the smart switch via the SPI
- the analog feedback output (CSNS and CSNS SYNC) can be controlled by SPI

The channel control (CHx) can be summarized:

- CH1… 4 controlled by ONx or iINx (if ir is programmed by SPI)
- CH5… 6 controlled by ONx
- Rising CHx by definition means starting over current window for OUT1… 5.

5.5.4 Fail Mode

The device enters the Fail mode, when

- the LIMP input pin is high (logic [1])
- or a SPI failure is detected

During Fail mode (wake = [1] & fail = [1]):

- the OUT1… OUT4 outputs are directly controlled by the corresponding control inputs (IN1… IN4)
- the OUT5… OUT6 are turned off
- the PWM module is not available
- while no SPI control is feasible, the SPI diagnosis is functional (depending on the fail mode condition):
  - the SO shall report the content of SO register defined by SOA0 to 3 bits
- the outputs are fully protected in case of an overload, overtemperature, and undervoltage
- no analog feedback is available
- the max. output overcurrent profile is activated (OCLO and window times)
- in case of an overload condition or undervoltage, the autorestart feature controls the OUT1… OUT4 outputs
- in case of an overtemperature condition, OCHI1 detection, or severe short-circuit detection, the corresponding output is latched OFF until a new wake-up event.

The channel control (CHx) can be summarized:

- CH1… 4 controlled by iINx, while the overcurrent windows are controlled by IN_ONx
- CH5… 6 are off

5.5.5 Mode Transitions

After a wake-up:

- a power on reset is applied and all SPI SI and SO registers are cleared (logic[0])
- the faults are blanked during $t_{BLANKING}$

The device enters in Normal mode after start-up if following sequence is provided:

- V_{PWR} and V_{CC} power supplies must be above their undervoltage thresholds (Sleep mode)
- generate wake-up event (wake =1) setting RSTB from 0 to 1

The device initialization will be completed after 50 µsec (typ). During this time, the device is robust in case of V_{PWR} interrupts higher than 150nsec.

The transition from “Normal mode” to “Fail mode” is executed immediately when a fail condition is detected.

During the transition, the SPI SI settings are cleared and the SPI SO registers are not cleared.

When the Fail mode condition was a:

- LIMP input, WD toggle timeout, WD toggle sequence, or a SPI modulo 16 error, the SPI diagnosis is available during Fail mode
- SI / SO stuck to static level, the SPI diagnosis is not available during Fail mode

The transition from “Fail mode” to “Normal mode” is enabled, when

- the fail condition is removed and
- two SPI commands are sent within a valid watchdog cycle (first WD=[0] and then WD=[1])

During this transition:

- all SPI SI and SO registers are cleared (logic[0])
- the DSF (device status flag) in the registers #1… #7 and the RCF (Register Clearer flag) in the device status register #1 are set (logic[1])

To delatch the RCF diagnosis, a read command of the quick status register #1 must be performed.

5.6 SPI Interface and Configurations

5.6.1 Introduction

The SPI is used to

- control the device in case of Normal mode
- provide diagnostics in case of Normal and Fail mode

The SPI is a 16 Bit full-duplex synchronous data transfer interface with daisy chain capability.

The interface consists of four I/O lines with 5.0 V CMOS logic levels and termination resistors:

- The SCLK pin clocks the internal shift registers of the device
- The SI pin accepts data into the input shift register on the rising edge of the SCLK signal
- The SO pin changes its state on the rising edge of SCLK and reads out on the falling edge
- The CSB enables the SPI interface
- with the leading edge of CS\ the registers are loaded
- while CSB is logic [0] SI/SO data are shifted
- with the trailing edge of the CSB signal, SPI data is latched into the internal registers
- when CSB is logic [1], the signals at the SCLK and SI pins are ignored and SO is high-impedance

When the RSTB input is

- low (logic [0]), the SPI and the fault registers are reset. The Wake state then depends on the status of the input pins (IN_ON1… IN_ON4)
- high (logic[1]), the device is in Wake status and the SPI is enabled

The functionality of the SPI is checked by a plausibility check. In case of a SPI failure the device enters the Fail mode.

5.6.2 SPI Input Register and Bit Descriptions

The first nibble of the 16 bit data word (D15… D12) serves as address bits.

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
name		4 Bit adress				WD	11 Bit data										

11 bits (D10… D1) are used as data bits.

The D11 bit is the WD toggle bit. This bit has to be toggled with each write command.

When the toggling of the bit is not executed within the WD timeout, a SPI fail is detected.

All register values are logic [0] after a reset. The predefined value is off / inactive unless otherwise noted.

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Initialisation 1	0	0	0	0	0	WD	WD SEL	SYNC EN1	SYNC EN0	MUX2	MUX1	MUX0	SOA MODE	SOA3	SOA2	SOA1	SOA0
initialisation 2	1	0	0	0	1	WD	OCHI THERMAL	OCHI TRANSIENT	NO HID1	NO HID0	OCHI OD5	OCHI OD4	OCHI OD3	OCHI OD2	OCHI OD1	PWM sync	OTW SEL
CH1 control	2	0	0	1	0	WD	PH11	PH01	ON1	PWM71	PWM61	PWM51	PWM41	PWM31	PWM21	PWM11	PWM01
CH2 control	3	0	0	1	1	WD	PH12	PH02	ON2	PWM72	PWM62	PWM52	PWM42	PWM32	PWM22	PWM12	PWM02
CH3 control	4	0	1	0	0	WD	PH13	PH03	ON3	PWM73	PWM63	PWM53	PWM43	PWM33	PWM23	PWM13	PWM03
CH4 control	5	0	1	0	1	WD	PH14	PH04	ON4	PWM74	PWM64	PWM54	PWM44	PWM34	PWM24	PWM14	PWM04
CH5 control	6	0	1	1	0	WD	PH15	PH05	ON5	PWM75	PWM65	PWM55	PWM45	PWM35	PWM25	PWM15	PWM05
CH6 control	7	0	1	1	1	WD	PH16	PH06	ON6	PWM76	PWM66	PWM56	PWM46	PWM36	PWM26	PWM16	PWM06
output control	8	1	0	0	0	WD	PSF5	PSF4	PSF3	PSF2	PSF1	ON6	ON5	ON4	ON3	ON2	ON1
Global PWM control	9-1	1	0	0	1	WD	0	X	X	X	X	GPWM EN6	GPWM EN5	GPWM EN4	GPWM EN3	GPWM EN2	GPWM EN1
	9-2	1	0	0	1	WD	1	X	X	GPWM7	GPWM6	GPWM5	GPWM4	GPWM3	GPWM2	GPWM1	GPWM0
over current control	10-1	1	0	1	0	WD	0	OCLO5	OCLO4	OCLO3	OCLO2	OCLO1	ACM EN5	ACM EN4	ACM EN3	ACM EN2	ACM EN1
	10-2	1	0	1	0	WD	1	NO OCHI5	NO OCHI4	NO OCHI3	NO OCHI2	NO OCHI1	SHORT OCHI5	SHORT OCHI4	SHORT OCHI3	SHORT OCHI2	SHORT OCHI1
input enable	11	1	0	1	1	WD	0	X	X	INEN14	INEN04	INEN13	INEN03	INEN12	INEN02	INEN11	INEN01
prescaler settings	12-1	1	1	0	0	WD	0	PRS15	PRS05	PRS14	PRS04	PRS13	PRS03	PRS12	PRS02	PRS11	PRS01
	12-2	1	1	0	0	WD	1	X	X	X	X	X	X	X	X	PRS16	PRS06
OL control	13-1	1	1	0	1	WD	0	OLON DGL5	OLON DGL4	OLON DGL3	OLON DGL2	OLON DGL1	OLOFF EN5	OLOFF EN4	OLOFF EN3	OLOFF EN2	OLOFF EN1
OLLED control	13-2	1	1	0	1	WD	1	res	res	res	res	OLLED TRIG	OLLED EN5	OLLED EN4	OLLED EN3	OLLED EN2	OLLED EN1
increment / dercrement	14	1	1	1	0	WD	INCR SGN	INCR15	INCR05	INCR14	INCR04	INCR13	INCR03	INCR12	INCR02	INCR11	INCR01
testmode	15	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

WD	#0~#14	= watchdog toggle bit
SOA0 ~ SOA3	#0	= address of next SO data word
SOA MODE	#0	= single read address of next SO data word
MUX0 ~ MUX2	#0	= CSNS multiplexer setting
SYNC EN0~ SYNC EN1	#0	= SYNC delay setting
WD SEL	#0	= watchdog timeout select
OTW SEL	#1	= over temperature warning threshold selection
PWM SYNC	#1	= reset clock module
OCHI ODx	#1	= OCHI window on load demand
NO HIDx	#1	= HID outputs selection
OCHI THERMAL	#1	= OCHI1 level depending on control die temperature
OCHI TRANSIENT	#1	= OCHI1 level adjusted during OFF to ON transition
PWM0x ~ PWM7x	#2~#7	= PWM value (8Bit)
PH0x ~ PH1x	#2~#7	= phase control
ONx	#2~#8	= channel on/off incl. OCHI control
PSFx	#8	= pulse skipping feature for power output channels
GPWM ENx	#9-1	= global PWM enable
GPWM1 ~ GPWM7	#9-2	= global PWM value (8Bit)
ACM ENx	#10-1	= advanced current sense mode enable
OCLOx	#10-1	= OCLO level control
SHORT OCHIx	#10-2	= use short OCHI window time
NO OCHIx	#10-2	= start with OCLO threshold
INEN0x ~ INEN1x	#11	= input enable control
PRS0x ~ PRS1x	#12	= pre scaler setting
OLOFF ENx	#13-1	= OL load in off state enable
OLON DGLx	#13-1	= OL ON deglitch time
OLLED ENx	#13-2	= OL LED mode enable
OLLED TRIG	#13-2	= trigger for OLLED detetcion in 100% d.c.
INCR SGN	#14	= PWM increment / decrement sign
INCR0x ~ INCR1x	#14	= PWM increment / decrement setting

#0

MUX2	MUX1	MUX0	CSNS
0	0	0	off
0	0	1	OUT1 current
0	1	0	OUT2 current
0	1	1	OUT3 current
1	0	0	OUT4 current
1	0	1	OUT5 current
1	1	0	**VPWR monitor**
1	1	1	control die temperature

#0

SYNC EN1	SYNC EN0	Sync status
0	0	sync off
0	1	valid
1	0	trig0
1	1	trig1/2

#1

NO HID1	NO HID0	D Selection
0	0	available for all channels
0	1	available for channel 3 only
1	0	available for channels 3 and 4 only
1	1	unavailable for all channels

#2~#7

PH 1x	PH 0x	Phase
0	0	0°
0	1	90°
1	0	180°
1	1	270°

#11

ONx	INEN1x	INEN0x	GPWM ENx	INx=0 OUTx	INx=0 PWMx	INx=1 OUTx	INx=1 PWMx
0	x	x	x	OFF	x	OFF	x
1	0	0	0	ON	individual	ON	individual
			1	ON	global	ON	global
		1	0	OFF	individual	ON	individual
			1	OFF	global	ON	global
	1	0	0	OFF	individual	ON	individual
			1	OFF	global	ON	global
		1	0	ON	individual	ON	global
			1	ON	global	ON	individual

#12

PRS 1x	PRS 0x	PRS divider	
0	0	/4	25Hz 100Hz
0	1	/2	50Hz 200Hz
1	x	/1	100Hz.... 400Hz

#14

INCR SGN	increment/decrement
0	decrement
1	increment

#14

INCR 1x	INCR 0x	increment/decrement
0	0	no increment/decrement
0	1	4 LSB
1	0	8 LSB
1	1	16 LSB

5.6.3 SPI Output Register and Bit Descriptions

The first nibble of the 16 Bit data word (D12… D15) serves as address bits.

All register values are logic [0] after a reset, except DSF and RCF bits. The predefined value is off / inactive unless otherwise noted.

Register	SO address					SO data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
not used	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
quick status	1	0	0	0	1	FM	DSF	OVLF	OLF	CPF	RCF	CLKF	QSF5	QSF4	QSF3	QSF2	QSF1
CH1 status	2	0	0	1	0	FM	DSF	OVLF	OLF	res	OTS1	OTW1	OC21	OC11	OC01	OLON1	OLOFF1
CH2 status	3	0	0	1	1	FM	DSF	OVLF	OLF	res	OTS2	OTW2	OC22	OC12	OC02	OLON2	OLOFF2
CH3 status	4	0	1	0	0	FM	DSF	OVLF	OLF	res	OTS3	OTW3	OC23	OC13	OC03	OLON3	OLOFF3
CH4 status	5	0	1	0	1	FM	DSF	OVLF	OLF	res	OTS4	OTW4	OC24	OC14	OC04	OLON4	OLOFF4
CH5 status	6	0	1	1	0	FM	DSF	OVLF	OLF	res	OTS5	OTW5	OC25	OC15	OC05	OLON5	OLOFF5
device status	7	0	1	1	1	FM	DSF	OVLF	OLF	res	res	res	TMF	OVF	UVF	SPIF	iLIMP
I/O status	8	1	0	0	0	FM	res	TOGGLE	iIN4	iIN3	iIN2	iIN1	OUT5	OUT4	OUT3	OUT2	OUT1
device ID	9	1	0	0	1	FM	UVF	res	res	DEVID 7	DEVID 6	DEVID 5	DEVID 4	DEVID 3	DEVID 2	DEVID 1	DEVID 0
not used	10	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
not used	11	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
not used	12	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
not used	13	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
not used	14	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
testmode	15	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

QSFx	*#1*	*= quick status (OC or OTW or OTS or OLON or OLOFF)*
CLKF	*#1*	*= PWM clock fail flag*
RCF	*#1*	*= register clear flag*
CPF	*#1*	*= charge pump flag*
OLF	*#1~#7*	*= open load flag (wired or of all OL signals)*
OVLF	*#1~#7*	*= over load flag (wired or of all OC and OTS signals)*
DSF	*#1~#7*	*= device status flag (UVF or OVF or CPF or RCF or CLKF or TMF)*
FM	*#1~#8*	*= fail mode flag*
OLOFFx	*#2~#6*	*= open load in off state status bit*
OLONx	*#2~#6*	*= open load in on state status bit*
OTWx	*#2~#6*	*= over temperature warning bit*
OTSx	*#2~#6*	*= over temperature shutdown bit*
iLIMP	*#7*	*= status of LIMP input after deglitcher (reported in real time)*
SPIF	*#7*	*= SPI fail flag*
UVF	*#7*	*= under voltage flag*
OVF	*#7*	*= over voltage flag*
TMF	*#7*	*= testmode activation flag*
OUTx	*#8*	**= status of VPWR/2 comparator (reported in real time)**
iINx	*#8*	*= status of INx pin after deglitcher (reported in real time)*
TOGGLE	*#8*	*= status of INx_ON signals (IN1_ON or IN2_ON or IN3_ON or IN4_ON)*
DEVID0 ~ DEVID2	*#9*	*= device type*
DEVID3 ~ DEVID4	*#9*	*= device family*
DEVID5 ~ DEVID7	*#9*	*= design status (incremented number)*

#2~#6	*OC2x*	*OC1x*	*OC0x*	*over current status*
	0	*0*	*0*	*no overcurrent*
	0	*0*	*1*	*OCHI1*
	0	*1*	*0*	*OCHI2*
	0	*1*	*1*	*OCHI3*
	1	*0*	*0*	*OCLO*
	1	*0*	*1*	*OCHIOD*
	1	*1*	*0*	*SSC*
	1	*1*	*1*	*not used*

#9	*DEVID2*	*DEVID1*	*DEVID0*	*device type*
	0	*0*	*0*	*Penta3/2*
	0	*0*	*1*	*Penta0/5*
	0	*1*	*0*	*Quad2/2*
	0	*1*	*1*	*Quad0/4*
	1	*0*	*0*	*Triple1/2*
	1	*0*	*1*	*Triple0/3*
	1	*1*	*0*	*res*
	1	*1*	*1*	*res*

5.6.4 Timing Diagrams

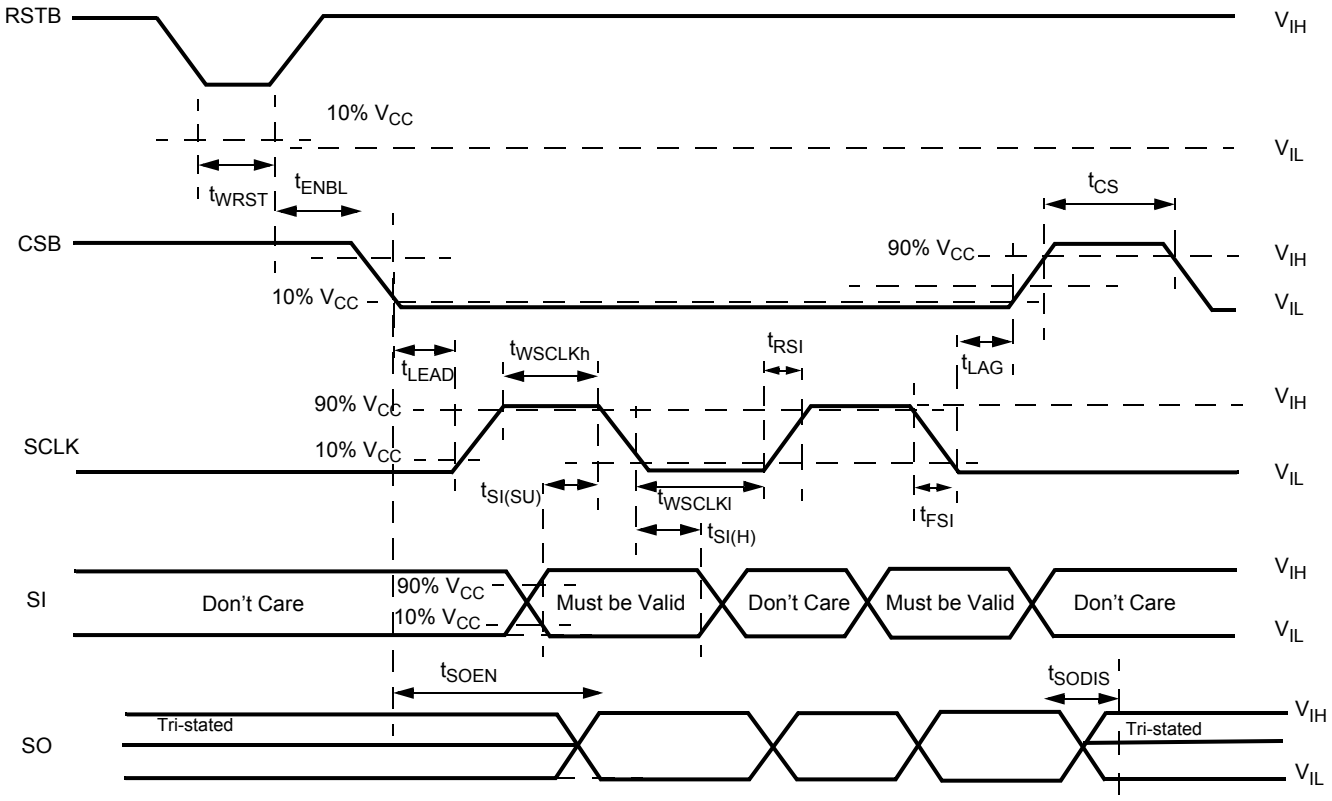

Figure 8. Timing Requirements During SPI Communication

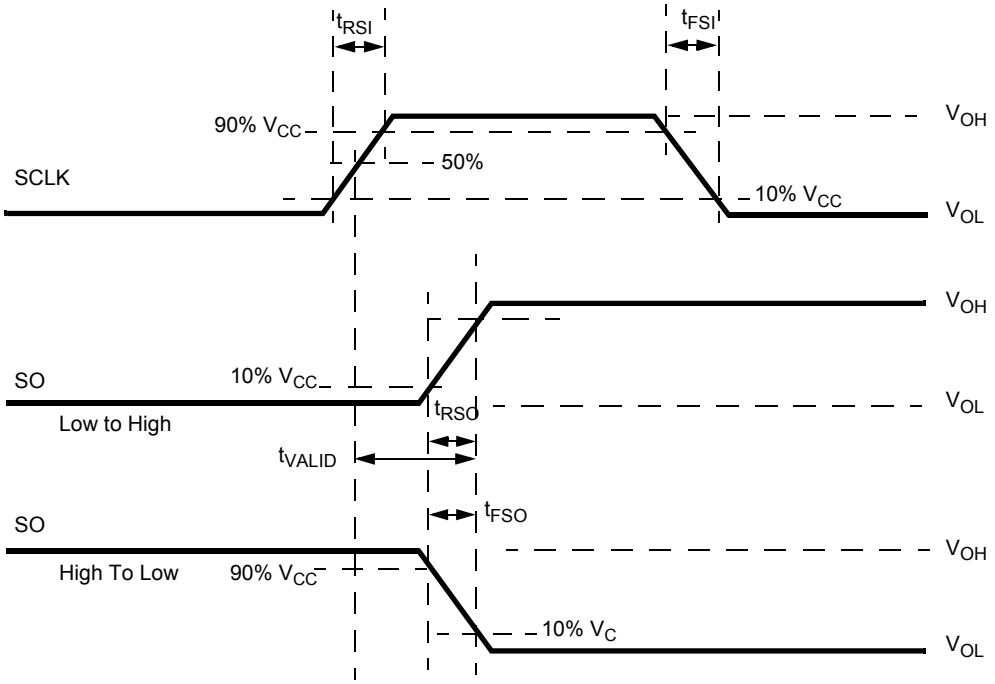

Figure 9. Timing Diagram for Serial Output (SO) Data Communication

5.6.5 Electrical Characterization

Table 7. Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SPI SIGNALS CSB, SI, SO, SCLK, SO						
f_{SPI}	SPI Clock Frequency	0.5	–	5.0	MHz	
V_{IH}	Logic Input High State Level (SI, SCLK, CSB, RSTB)	3.5	–	–	V	
$V_{IH(WAKE)}$	Logic Input High State Level for wake-up (RSTB)	3.75	–	–	V	
V_{IL}	Logic Input Low State Level (SI, SCLK, CSB, RSTB)	–	–	0.85	V	
V_{OH}	Logic Output High State Level (SO)	VCC - 0.4	–	–	V	
V_{OL}	Logic Output Low State Level (SO)	–	–	0.4	V	
I_{IN}	Logic Input Leakage Current in Inactive State (SI = SCLK = RSTB = [0] and CSB = [1])	-0.5	–	+0.5	µA	
I_{OUT}	Logic Output Tri-state Leakage Current (SO from 0 V to V_{CC})	-10	–	+1.0	µA	
R_{PULL}	Logic Input Pull-up / Pull-down Resistor	25	–	100	kΩ	
C_{IN}	Logic Input Capacitance	–	–	20	pF	(16)
t_{RST_DGL}	RSTB deglitch Time	7.5	10	12.5	µs	
t_{SO}	SO Rising and Falling Edges with 80 pF	–	–	20	ns	
t_{WCLKh}	Required High State Duration of SCLK (Required Setup Time)	80	–	–	ns	
t_{WCLKl}	Required Low State Duration of SCLK (Required Setup Time)	80	–	–	ns	
t_{CS}	Required duration from the Rising to the Falling Edge of CSB (Required Setup Time)	1.0	–	–	µs	
t_{RST}	Required Low State Duration for reset RST\	1.0	–	–	µs	
t_{LEAD}	Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	320	–	–	ns	
t_{LAG}	Falling Edge of SCLK to Rising Edge of CSB (Required Setup lag Time)	100	–	–	ns	
$t_{SI(SU)}$	SI to Falling Edge of SCLK (Required Setup Time)	20	–	–	ns	
$t_{SI(H)}$	Falling Edge of SCLK to SI (Required hold Time of the SI signal)	20	–	–	ns	
t_{RSI}	SI, CSB, SCLK, Max. Rise Time Allowing Operation at Maximum f_{SPI}	–	20	50	ns	
t_{FSI}	SI, CSB, SCLK, Max. Fall Time Allowing Operation at Maximum f_{SPI}	–	20	50	ns	
$t_{SO(EN)}$	Time from Falling Edge of CS\ to Reach Low-impedance on SO (access time)	–	–	60	ns	
$t_{SO(DIS)}$	Time from Rising Edge of CSB to Reach Tri-state on SO	–	–	60	ns	

Notes

16. Parameter is derived from simulations.

6 Functional Block Requirements and Behaviors

6.1 Self-protected High Side Switches Description and Application Information

6.1.1 Features

Up to five power outputs are foreseen to drive light as well as DC motor applications. The outputs are optimized for driving bulbs, but also HID ballasts, LEDs, and other resistive or low inductive loads.

The smart switches are controlled by use of high sophisticated gate drivers. The gate drivers provide:

- output pulse shaping
- output protections
- active clamps
- output diagnostics

6.1.2 Output Pulse Shaping

The outputs are controlled with a closed loop active pulse shaping to provide the best compromise between:

- low switching losses
- low EMC emission performance
- minimum propagation delay time

Depending on the programming of the prescaler setting register #12-1, #12-2, the switching speeds of the outputs are adjusted to the output frequency range of each channel.

The edge shaping shall be designed according the following table:

divider factor	PWM freq [Hz] min	PWM freq [Hz] max	PWM period [ms] min	PWM period [ms] max	d.c. range [hex] min	d.c. range [hex] max	d.c. range [LSB] min	d.c. range [LSB] max	min. on/off duty cycle time [µs]
4	*25*	*100*	*10*	*40*	**03**	**FB**	4	252	**156**
2	*50*	*200*	*5*	*20*	**07**	**F7**	8	248	**156**
1	*100*	*400*	*2,5*	*10*	**07**	**F7**	8	248	**78**

The edge shaping provides full symmetry for rising and falling transition:

- the slopes for the rising and falling edge are matched to provide the best EMC emission performance
- the shaping of the upper edges and the lower edges are matched to provide the best EMC emission performance
- the propagation delay time for the rising edge and the falling edge is matched to provide true duty cycle control of the output duty cycle error, $\leq$ 1 LSB at max. frequency
- a digital regulation loop is used to minimize the duty cycle error of the output signal

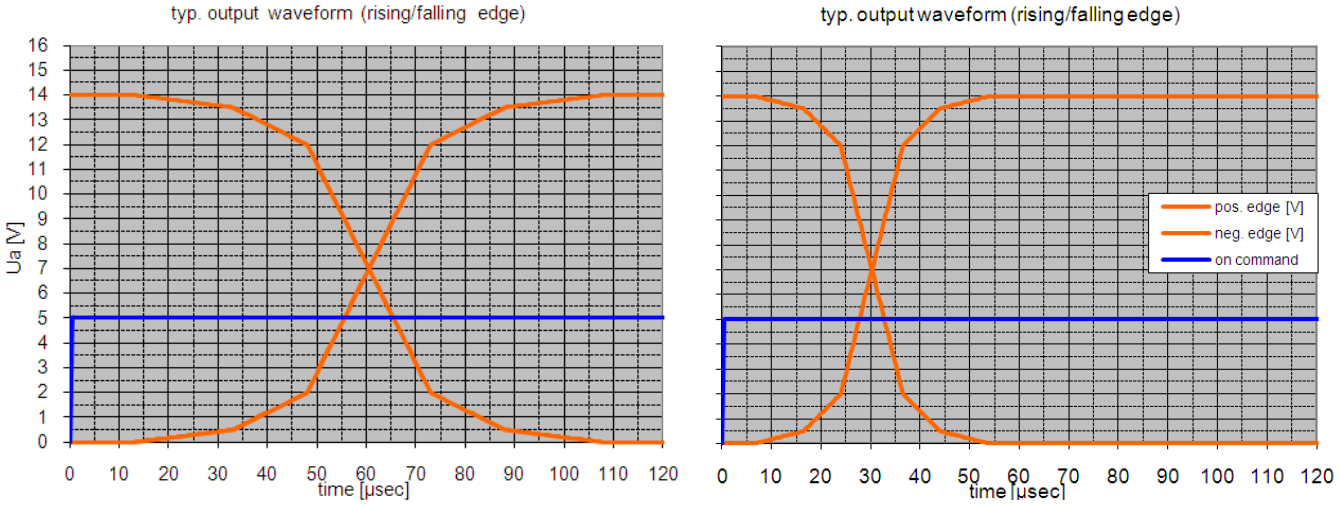

Figure 10. Typical Power Output Switching (slow & fast slew rate)

6.1.2.1 SPI Control and Configuration

For optimized control of the outputs, a synchronous clock module is integrated. The PWM frequency and output timing during Normal mode are generated from the clock input (CLK) by the integrated PWM module. In case of clock fail (very low frequency, very high frequency), the output duty cycle is 100%.

Each output (OUT1… OUT6) can be controlled by an individual channel control register:

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHx control	2~7	channel address				WD	PH1x	PH0x	Onx	PWM7x	PWM6x	PWM5x	PWM4x	PWM3x	PWM2x	PWM1x	PWM0x

where:

- PH0x… PH1x: phase assignment of the output channel x
- ONx: on/off control including overcurrent window control of the output channel x
- PWM0x… PWM7x: 8-bit PWM value individually for each output channel x

The ONx bits are duplicated in the output control register #8 to control the outputs with either the CHx control register or the output control register.

The PRS1x… PRS0x prescaler settings can be set in the prescaler settings register #12-1 and #12-2.

The following changes of the duty cycle are performed asynchronous (with pos. edge of CSB signal)

- turn on with 100% duty cycle (CHx = ON)
- change of duty cycle value to 100%
- turn off (CHx = OFF)
- phase setting (PH0x… PH1x)
- prescaler setting (PRS1x… PRS0x)

A change in phase setting or prescaler setting during CHx = ON may cause an unwanted long ON-time. Therefore it is recommended to turn off the output(s) before execution of this change.

INCR SGN	*increment/decrement*
0	*decrement*
1	*increment*

The following changes of the duty cycle are performed synchronous (with the next PWM cycle)

- turn on with less than 100% duty cycle (OUTx = ONx)
- change of duty cycle value to less than 100%

A change of the duty cycle value can be achieved by a change of the

- PWM0x… PWM7x bits in individual channel control register #2… #7
- GPWM EN1… GPWM EN6 bits (change between individual PWM and global PWM settings) in global PWM control register #9-1
- incremental/decremental register #14

The synchronization of the switching phases between different devices is provided by the PWM SYNC bit in the initialization 2 register #1.

On a SPI write into initialization 2 register (#1):

- initialization when the bit D1 (PWM SYNC) is logic[1], all counters of the PWM module are reset with the positive edge of the CSB, i.e. the phase synchronization is performed immediately within one SPI frame. It could help to synchronize different Gen4 devices in the board.
- when the bit D1 is logic[0], no action is executed

The switching frequency can be adjusted for the corresponding channel as described in the following table:

CLK freq. [kHz]		prescaler setting		divider	PWM freq [Hz]		slew	PWM resolution	
min.	max.	PRS1x	PRS0x	factor	min	max	rate	[Bit]	[steps]
25,6	102,4	0	0	**4**	25	100	**slow**	**8**	**256**
		0	1	**2**	50	200	**slow**		
		1	X	**1**	100	400	**fast**		

PWM duty cycle			pulse skipping frame							
hex	dec	[%]	S0	S1	S2	S3	S4	S5	S6	S7
FF	256	***100,00%***	FF	FF	FF	FF	FF	FF	FF	FF
FE	255	***99,61%***	F7	FF	FF	FF	FF	FF	FF	FF
FD	254	***99,22%***	F7	FF	FF	FF	F7	FF	FF	FF
FC	253	***98,83%***	F7	FF	F7	FF	F7	FF	FF	FF
FB	252	***98,44%***	F7	FF	F7	FF	F7	FF	F7	FF
FA	251	***98,05%***	F7	F7	F7	FF	F7	FF	F7	FF
F9	250	***97,66%***	F7	F7	F7	FF	F7	F7	F7	FF
F8	249	***97,27%***	F7	F7	F7	F7	F7	F7	F7	FF
F7	248	***96,88%***								
F6	247	***96,48%***								
F5	246	***96,09%***								
F4	245	***95,70%***								
.	.	.								
.	.	.								
.	.	.								
.	.	.								
03	4	***1,56%***								
02	3	***1,17%***								
01	2	***0,78%***								
00	1	***0,39%***								

No PWM feature is provided in case of:

- Fail mode
- clock input signal failure

6.1.2.2 Global PWM Control

In addition to the individual PWM register, each channel can be assigned independently to a global PWM register.

The setting is controlled by the GPWM EN bits inside the global PWM control register #9-1. When no control by direct input pin is enabled and the GPWM EN bit is

- low (logic[0]), the output is assigned to individual PWM (default status)
- high (logic[1]), the output is assigned to global PWM

The PWM value of the global PWM channel is controlled by the global PWM control register #9-2.

ONx	INEN1x	INEN0x	GPWM ENx	iINx=0		iINx=1	
				CHx	PWMx	CHx	PWMx
0	x	x	x	OFF	x	OFF	x
1	0	0	0	ON	individual	ON	individual
			1	ON	global	ON	global
	0	1	0	OFF	individual	ON	individual
	1	0	1	OFF	global	ON	global
	1	1	0	ON	individual	ON	global
			1	ON	global	ON	individual

When a channel is assigned to global PWM, the switching phase the prescaler and the pulse skipping are according the corresponding output channel setting.

6.1.2.3 Incremental PWM Control

To reduce the control overhead during soft start/stop of bulbs or DC motors (e.g. theatre dimming), an incremental PWM control feature is implemented.

With the incremental PWM control feature the PWM values of all internal channels OUT1… OUT5 can be incremented or decremented with one SPI frame.

The incremental PWM feature is not available for

- the global PWM channel
- the external channel OUT6

The control is according the increment/decrement register #14:

- INCR SGN: sign of incremental dimming (valid for all channels)
- INCR 1x, INCR 0x increment/decrement

INCR 1x	INCR 0x	increment/decrement
0	0	no increment/decrement
0	1	4
1	0	8
1	1	16

This feature limits the duty cycle to the rails (00 resp. FF) to avoid any overflow.

6.1.2.4 Pulse Skipping

Due to the output pulse shaping feature and the resulting switching delay time of the smart switches, duty cycles close to 0% resp. 100% can not be generated by the device. Therefore the pulse skipping feature (PSF) is integrated to interpolate this output duty cycle range in Normal mode.

The pulse skipping provides a fixed duty cycle pattern with eight states to interpolate the duty cycle values between F7 (Hex) and FF (Hex). The range between 00 (Hex) and 07 (Hex) is not considered to be provided.

The pulse skipping feature

- is available individually for the power output channels (OUT1… OUT5)
- is not available for the external channel (OUT6).

The feature is enabled with the PSF bits in the output control register #8.

When the corresponding PSF bit is

- low (logic[0]), the pulse skipping feature is disabled on this channel (default status)
- high (logic[1]), the pulse skipping feature is enabled on this channel