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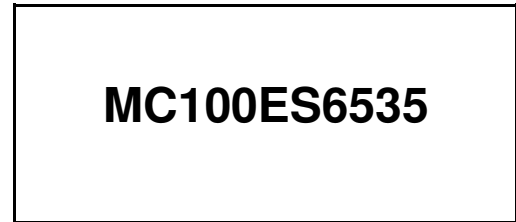


# 3.3V LVCMOS to LVPECL 1:4 Fanout Buffer

The MC100ES6535 is a low skew, high performance 3.3 V 1-to-4 LVCMOS to LVPECL fanout buffer. The ES6535 has two selectable inputs that allow LVCMOS or LVTTTL input levels which translate to LVPECL outputs. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. The ES6535 is ideal for high performance clock distribution applications.

### Features

- 4 differential LVPECL outputs
- 2 selectable LVCMOS/LVTTTL inputs
- 1 GHz maximum output frequency
- Translates LVCMOS/LVTTTL levels to LVPECL levels
- 30 ps maximum output skew
- 190 ps part-to-part skew
- 3.3 V operating range
- 20-lead TSSOP package
- Ambient temperature range -40°C to +85°C



### ORDERING INFORMATION

Device	Package
MC100ES6535DT	TSSOP-20
MC100ES6535DTR2	TSSOP-20

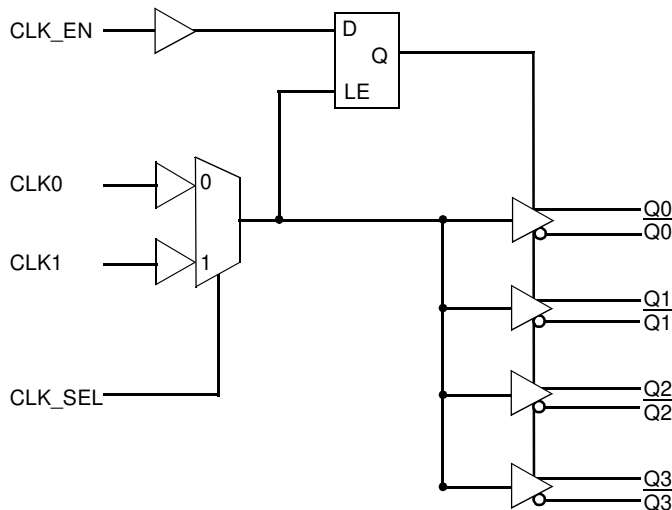


Figure 1. Logic Diagram

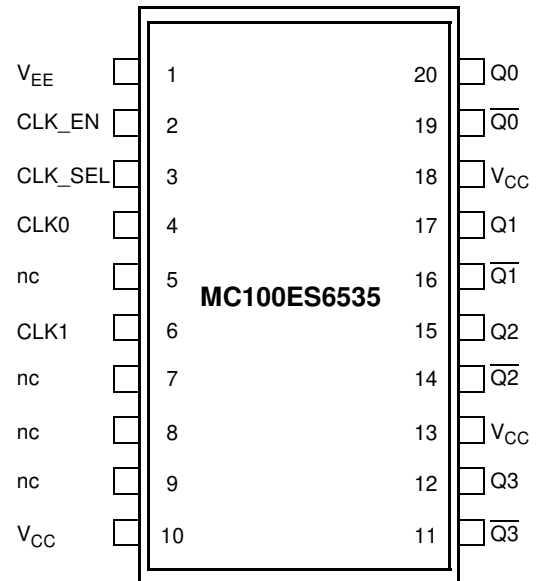


Figure 2. 20-Lead Pinout (Top View)

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**Table 1. PIN DESCRIPTION**

Number	Name	Type		Description
1	V <sub>EE</sub>	Power		Negative supply pin
2	CLK_EN	Input	Pullup <sup>a</sup>	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, $\overline{Q}$ outputs are forced high. LVCMOS/LVTTL interface levels
3	CLK_SEL	Input	Pulldown <sup>a</sup>	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels
4	CLK0	Input	Pulldown <sup>a</sup>	LVCMOS/LVTTL clock input
6	CLK1	Input	Pulldown <sup>a</sup>	LVCMOS/LVTTL clock input
5, 7, 8, 9	nc	Unused		No connect
10, 13, 18	V <sub>CC</sub>	Power		Positive supply pin
11, 12	Q3, $\overline{Q3}$	Output		LVPECL differential output pair
14, 15	Q2, $\overline{Q2}$	Output		LVPECL differential output pair
16, 17	Q1, $\overline{Q1}$	Output		LVPECL differential output pair
19, 20	Q0, $\overline{Q0}$	Output		LVPECL differential output pair

<sup>a</sup> Pullup and Pulldown refer to internal input resistors.

**Table 2. CONTROL INPUT FUNCTION TABLE<sup>a</sup>**

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	$\overline{Q0}:\overline{Q3}$
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

<sup>a</sup> After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 3.

**Table 3. CLOCK INPUT FUNCTION TABLE**

Inputs	Outputs	
CLK0 or CLK1	Q0:Q3	$\overline{Q0}:\overline{Q3}$
0	LOW	HIGH
1	HIGH	LOW

**Table 4. GENERAL SPECIFICATIONS**

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model	4000 V
	Machine Model	200 V
θ <sub>JA</sub> Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP	140°C/W
	500 LFPM, 20 TSSOP	100°C/W
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

**Table 5. ABSOLUTE MAXIMUM RATINGS<sup>a</sup>**

Symbol	Rating	Conditions	Rating	Units
V <sub>SUPPLY</sub>	Power Supply Voltage	Difference between V <sub>CC</sub> & V <sub>EE</sub>	3.9	V
V <sub>IN</sub>	Input Voltage	V <sub>CC</sub> - V <sub>EE</sub> ≤ 3.6 V	V <sub>CC</sub> + 0.3 V <sub>EE</sub> - 0.3	V V
I <sub>out</sub>	Output Current	Continuous Surge	50 100	mA mA
T <sub>A</sub>	Operating Temperature Range		-40 to +85	°C
T <sub>store</sub>	Storage Temperature Range		-65 to +150	°C

<sup>a</sup> Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 6. DC CHARACTERISTICS** (V<sub>CC</sub> = 3.135 V to 3.8 V; V<sub>EE</sub> = 0 V)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current			35			45	mA
V <sub>OH</sub> <sup>a</sup>	Output HIGH Voltage	V <sub>CC</sub> -1150	V <sub>CC</sub> -1020	V <sub>CC</sub> -800	V <sub>CC</sub> -1200	V <sub>CC</sub> -970	V <sub>CC</sub> -750	mV
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> -1950	V <sub>CC</sub> -1620	V <sub>CC</sub> -1250	V <sub>CC</sub> -2000	V <sub>CC</sub> -1680	V <sub>CC</sub> -1300	mV

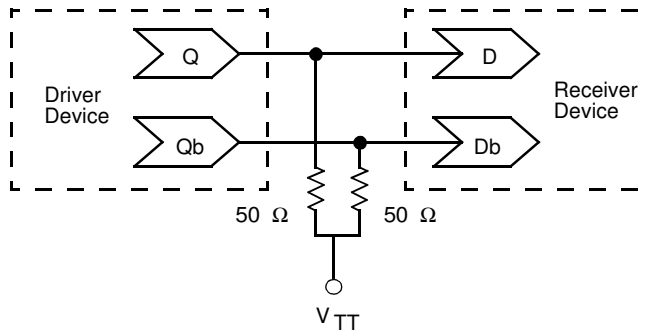
<sup>a</sup> Outputs are terminated through a 50Ω resistor to V<sub>CC</sub>-2 volts.

**Table 7. LVTTTL / LVCMOS INPUT DC CHARACTERISTICS** (V<sub>CC</sub> = 3.135 V to 3.8 V)

Symbol	Characteristic	Condition	-40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = V <sub>CC</sub>			±150			±150	μA
V <sub>IK</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA			-1.2			-1.2	V
V <sub>IH</sub>	Input HIGH Voltage		2.0		V <sub>CC</sub> +0.3	2.0		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage				0.8			0.8	V

**Table 8. AC CHARACTERISTICS** ( $V_{CC} = 3.135\text{ V to }3.8\text{ V}$ ,  $V_{EE} = 0\text{ V}$ )

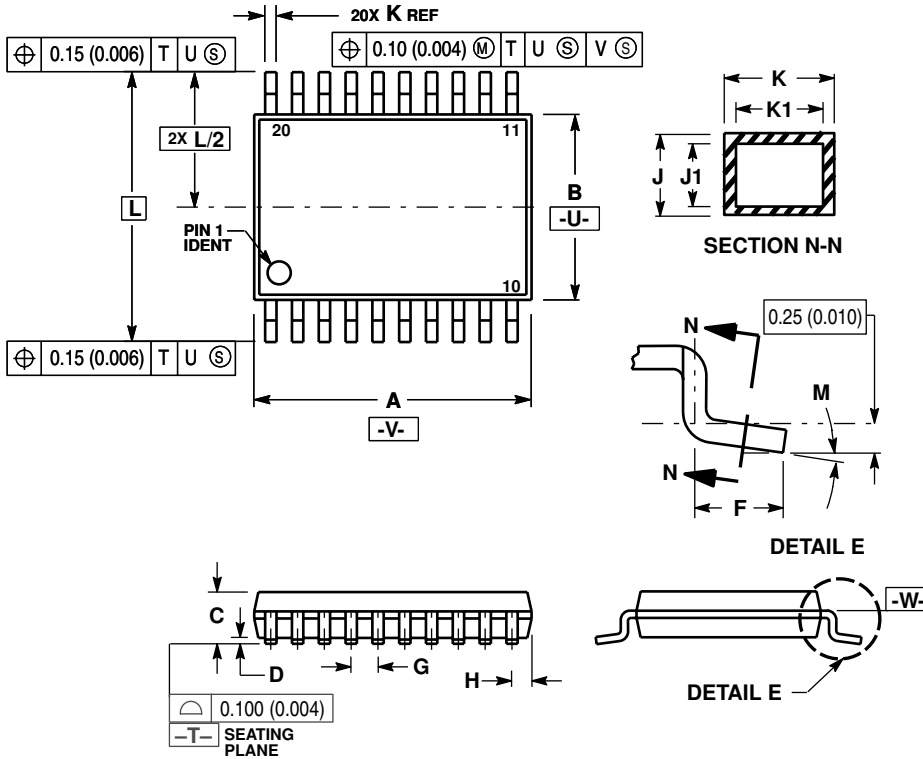
Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency			1			1			1	GHz
$t_{PD}$	Propagation Delay to Output Differential	150	350	500	175	360	550	200	380	600	ps
$t_{SKEW}$	Skew Output-to-Output Part-to-Part		20	30		20	30		20	30	ps
				190			190			190	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter RMS ( $1\sigma$ )			1			1			1	ps
$V_{outPP}$	Output Peak-to-Peak Voltage	350	750		350	750		350	750		mV
$t_r/t_f$	Output Rise/Fall Time (20%–80% @ 50 MHz)	50		400	50		400	50		400	ps



**Figure 3. Typical Termination for Output Driver and Device Evaluation**

OUTLINE DIMENSIONS

TSSOP-20  
DT SUFFIX  
20-LEAD TSSOP PACKAGE  
CASE 948E-02  
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**NOTES**

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MC100ES6535