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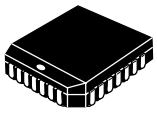
MC10H646, MC100H646

PECL/TTL-TTL 1:8 Clock Distribution Chip

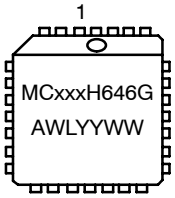
ON Semiconductor®

http://onsemi.com



PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Description

The MC10H/100H646 is a single supply, low skew translating 1:8 clock driver. Devices in the ON Semiconductor H646 translator series utilize the 28−lead PLCC for optimal power pinning, signal flow through and electrical performance. The single supply H646 is similar to the H643, which is a dual supply 1:8 version of the same function.

The H646 was designed specifically to drive series terminated transmission lines. Special techniques were used to match the HIGH and LOW output impedances to about 7.0 Ω. This simplifies the choice of the termination resistor for series terminated applications. To match the HIGH and LOW output impedances, it was necessary to remove the standard I_{OS} limiting resistor. As a result, the user should take care in preventing an output short to ground as the part will be permanently damaged.

The H646 device meets all of the requirements for driving the 60 MHz and 66 MHz Intel Pentium® Microprocessor. The device has no PLL components, which greatly simplifies its implementation into a digital design. The eight copies of the clock allows for point−to−point clock distribution to simplify board layout and optimize signal integrity.

The H646 provides differential PECL inputs for picking up LOW skew PECL clocks from the backplane and distributing it to TTL loads on a daughter board. When used in conjunction with the MC10/100E111, very low skew, very wide clock trees can be designed. In addition, a TTL level clock input is provided for flexibility. Note that only one of the inputs can be used on a single chip. For correct operation, the unused input pins should be left open.

The Output Enable pin forces the outputs into a high impedance state when a logic 0 is applied.

The output buffers of the H646 can drive two series terminated, 50 Ω transmission lines each. This capability allows the H646 to drive up to 16 different point−to−point clock loads. Refer to the Applications section for a more detailed discussion in this area.

The 10H version is compatible with MECL™ 10H ECL logic levels. The 100H version is compatible with 100K levels.

Features

- PECL/TTL−TTL Version of Popular ECLinPS™ E111
- Low Skew
- Guaranteed Skew Spec
- Tri−State Enable
- Differential Internal Design
- V_{BB} Output
- Single Supply
- Extra TTL and ECL Power/Ground Pins
- Matched High and Low Output Impedance
- Meets Specifications Required to Drive Intel® Pentium® Microprocessors
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

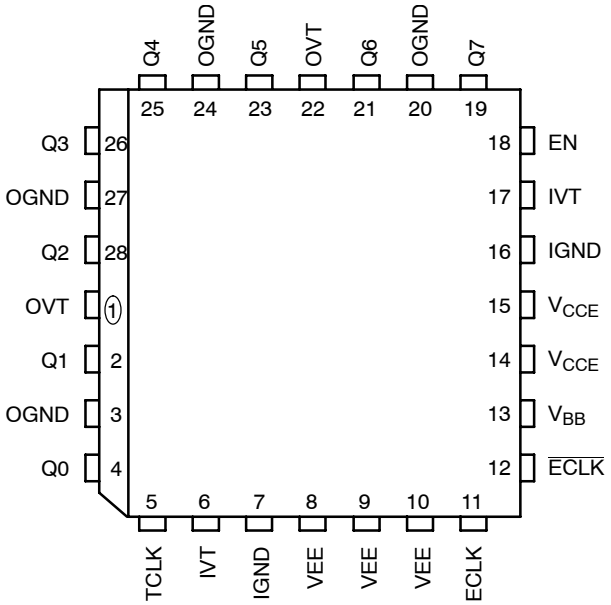


Figure 1. Pinout: PLCC−28
(Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
OGND	TTL Output Ground (0 V)
OVT	TTL Output V_{CC} (+5.0 V)
IGND	Internal TTL GND (0 V)
IVT	Internal TTL V_{CC} (+5.0 V)
V_{EE}	ECL V_{EE} (0 V)
V_{CCE}	ECL Ground (5.0 V)
ECLK, $\overline{ECLK}$	Differential Signal Input (PECL)
V_{BB}	V_{BB} Reference Output
Q0−Q7	Signal Outputs (TTL)
EN	Tri−State Enable Input (TTL)

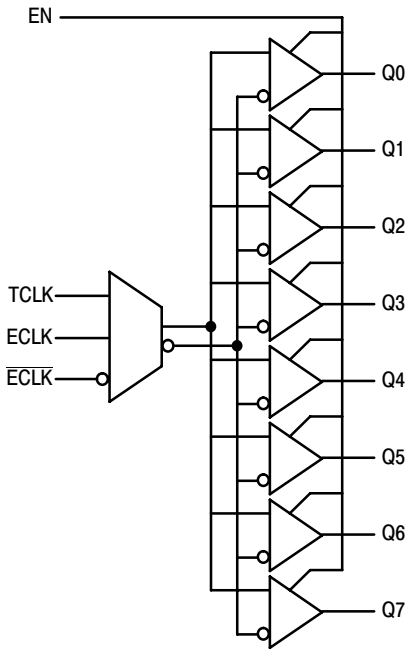


Figure 2. Logic Diagram

Table 2. TRUTH TABLE

TCLK	ECLK	$\overline{ECLK}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

L = Low Voltage Level; H = High Voltage Level; Z = Tristate

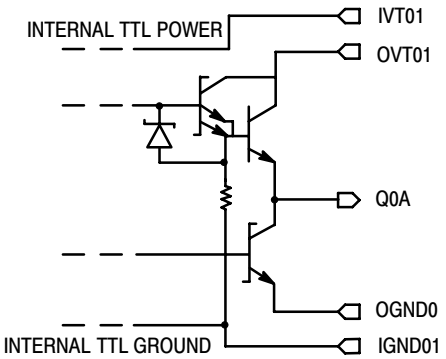


Figure 3. Output Structure

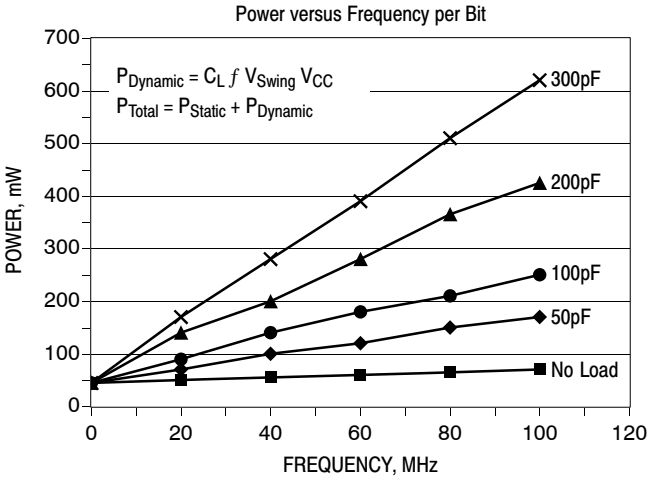


Figure 4. Power versus Frequency (Typical)

Table 3. 10H PECL DC CHARACTERISTICS (IVT = OVT = V_{CCE} = 5.0 V ±5%)

			0°C			25°C			85°C			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{INH}	Input HIGH Current				255			175			175	μA
I_{IL}	Input LOW Current		0.5			0.5			0.5			μA
V_{IH}	Input HIGH Voltage	IVT = IVO = V_{CCE} = 5.0 V (Note 1)	3.83		4.16	3.87		4.19	3.94		4.28	V
V_{IL}	Input LOW Voltage	IVT = IVO = V_{CCE} = 5.0 V (Note 1)	3.05		3.52	3.05		3.52	3.05		3.555	V
V_{BB}	Output Reference Voltage	IVT = IVO = V_{CCE} = 5.0 V (Note 1)	3.62		3.73	3.65		3.75	3.69		3.81	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = 5.0 V

Table 4. 100H PECL DC CHARACTERISTICS (IVT = OVT = V_{CCE} = 5.0 V ±5%)

			0°C			25°C			85°C			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{INH}	Input HIGH Current				255			175			175	μA
I_{IL}	Input LOW Current		0.5			0.5			0.5			μA
V_{IH}	Input HIGH Voltage	IVT = IVO = V_{CCE} = 5.0 V (Note 2)	3.835		4.12	3.835		4.12	3.835		3.835	V
V_{IL}	Input LOW Voltage	IVT = IVO = V_{CCE} = 5.0 V (Note 2)	3.19		3.525	3.19		3.525	3.19		3.525	V
V_{BB}	Output Reference Voltage	IVT = IVO = V_{CCE} = 5.0 V (Note 2)	3.62		3.74	3.62		3.74	3.62		3.74	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = 5.0 V

Table 5. DC CHARACTERISTICS (IVT = OVT = V_{CCE} = 5.0 V ±5%)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = 24 mA	2.6	– –	2.6	– –	2.6	– –	V
V_{OL}	Output LOW Voltage	I_{OL} = 48 mA	–	0.5	–	0.5	–	0.5	V
IOS	Output Short Circuit Current	(Note 3)	–	–	–	–	–	–	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

Table 6. TTL DC CHARACTERISTICS (V_T = V_E = 5.0 V ±5%)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		2.0	 0.8	2.0	 0.8	2.0	 0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V V_{IN} = 7.0 V		20 100		20 100		20 100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V		–0.6		–0.6		–0.6	mA
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA I_{OH} = –24 mA	2.5 2.0		2.5 2.0		2.5 2.0		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA		0.5		0.5		0.5	V
V_{IK}	Input Clamp Voltage	I_{IN} = –18 mA		–1.2		–1.2		–1.2	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. DC CHARACTERISTICS (IVT = OVT = V_{CCE} = 5.0 V ±5%)

Symbol	Characteristic	Condition	0°C		25°C			85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
I_{CCL}	Power Supply Current	Total all OVT, IVT, and V_{CCE} pins		185		166	185		185	mA
I_{CCH}				175		154	175		175	mA
I_{CCZ}				210			210		210	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 8. AC CHARACTERISTICS (IVT = OVT = V_{CCE} = 5.0 V ±5%)

Symbol	Characteristic		Condition	0°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	ECLK to Q TCLK to Q		4.8 5.1	5.8 6.4	5.0 5.3	6.0 6.4	5.6 5.7	6.6 7.0	ns
t_{PHL}	Propagation Delay	ECLK to Q TCLK to Q		4.4 4.7	5.4 6.0	4.4 4.8	5.4 5.9	4.8 5.2	5.8 6.5	ns
$t_{SK(O)}$	Output Skew	Q0, Q3, Q4, Q7 Q1, Q2, Q5 Q0−Q7	(Notes 4, 9)		350 350 500		350 350 500		350 350 500	ps
$t_{SK(PR)}$	Process Skew	ECLK to Q TCLK to Q	(Notes 5, 9)		1.0 1.3		1.0 1.1		1.0 1.3	ns
$t_{SK(P)}$	Pulse Skew	$\Delta t_{PLH} - t_{PHL}$			1.0		1.0		1.0	ns
t_r, t_f	Rise/Fall Time			0.3	1.5	0.3	1.5	0.3	1.5	ns
t_{PW}	Output Pulse Width	66 MHz @ 2.0 V 66 MHz @ 0.8 V 60 MHz @ 2.0 V 60 MHz @ 0.8 V	(Notes 6, 9)	5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		ns
$t_{Stability}$	Clock Stability		(Notes 7, 9)		±75		±75		±75	ps
F_{MAX}	Maximum Input Frequency		(Notes 8, 9)		80		80		80	MHz

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Output skew defined for identical output transitions.
5. Process skew is valid for V_{CC} = 5.0 V ±5%.
6. Parameters guaranteed by $t_{SK(P)}$ and t_r, t_f specification limits.
7. Clock stability is the period variation between two successive rising edges.
8. For series terminated lines. See Applications section for F_{MAX} enhancement techniques.
9. All AC specifications tested driving 50 Ω series terminated transmission lines at 80 MHz.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H646FN	PLCC−28	37 Units / Rail
MC10H646FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H646FNR2	PLCC−28	500 / Tape & Reel
MC10H646FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H646FN	PLCC−28	37 Units / Rail
MC100H646FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100H646FNR2	PLCC−28	500 / Tape & Reel
MC100H646FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

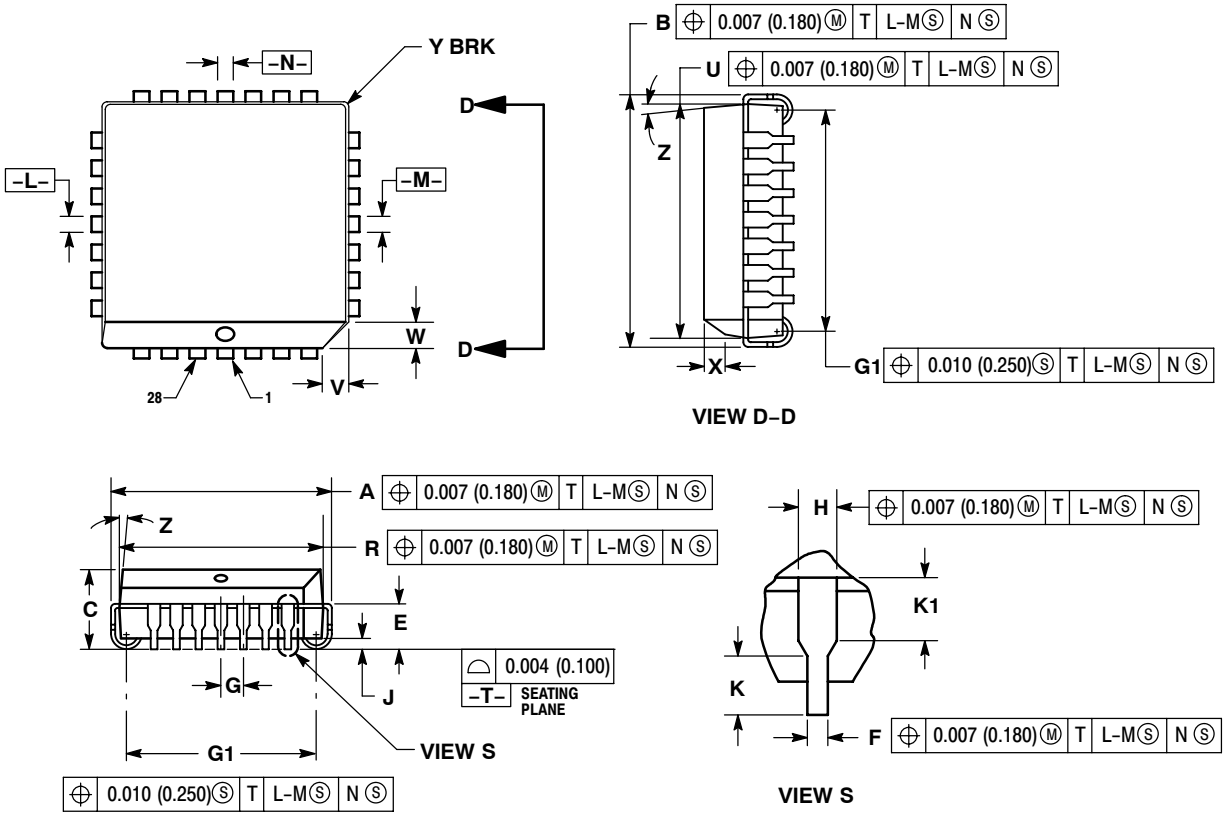
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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MECL 10H is a trademark of Motorola, Inc.
Pentium is a registered trademark of Intel Corporation.

PUBLICATION ORDERING INFORMATION

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For additional information, please contact your local Sales Representative

MC10H646/D