Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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MC10H601, MC100H601

9-Bit ECL to TTL Translator

Description

The MC10H/100H601 is a 9−bit, dual supply ECL to TTL translator. Devices in the ON Semiconductor 9−bit translator series utilize the 28−lead PLCC for optimal power pinning, signal flow−through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. For the 3−state output disable, both ECL and TTL control inputs are provided, allowing maximum design flexibility.

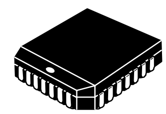
The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

Features

- 9−Bit Ideal for Byte−Parity Applications
- 3−State TTL Outputs
- Flow−Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- ECL and TTL 3−State Control Inputs
- Dual Supply
- 4.8 ns Max Delay into 50 pF, 9.6 ns into 200 pF (all Outputs Switching)
- PNP TTL Inputs for Low Loading
- Pb−Free Packages are Available*

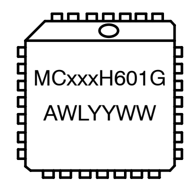
ON Semiconductor®

http://onsemi.com



PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

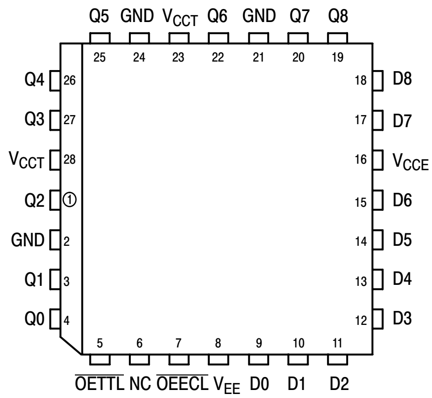


Figure 1. PLCC−28 Pinout (Top View)

Table 1. PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}	Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2 / −4.5 V)
D0 − D8	Data Inputs (ECL)
Q0 − Q8	Data Outputs (TTL)
$\overline{\text{OEECL}}$	3−State Control (ECL)
$\overline{\text{OETTL}}$	3−State Control (TTL)

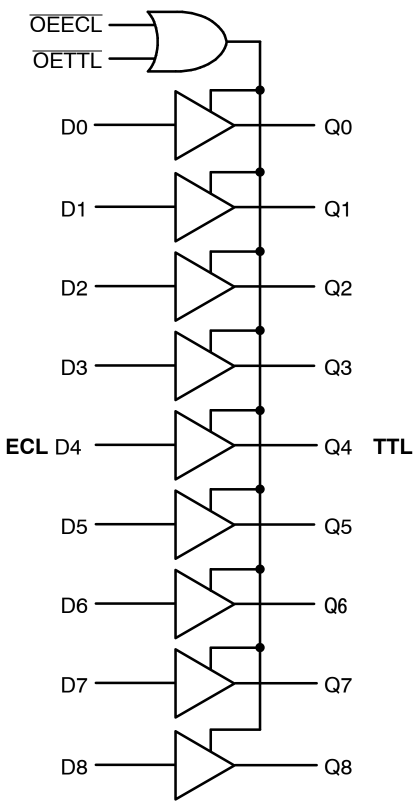


Figure 2. Logic Diagram

Table 2. TRUTH TABLE

$\overline{\text{OEECL}}$	$\overline{\text{OETTL}}$	D	Q
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Table 3. 10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

Symbol	Parameter	0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
I_{EE}	Power Supply Current		−51		−51		−51	mA
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	255	 0.5	175	 0.5	175	μA μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1170 −1950	−840 −1480	−1130 −1950	−810 −1480	−1060 −1950	−720 −1445	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 4. 100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

Symbol	Parameter	0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
I_{EE}	Power Supply Current		−51		−51		−53	mA
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	255	 0.5	175	 0.5	175	μA μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{CCH}	Power Supply Current			110		110		110	mA
I_{CCL}				110		110		110	
I_{CCZ}	Power Supply Current			105		105		105	
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V V_{IN} = 7.0 V		20 100		20 100		20 100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V		−0.6		−0.6		−0.6	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	−100	−225	−100	−225	−100	−225	mA
I_{OZH} I_{OZL}	Output Disable Current HIGH Output Disable Current LOW	V_{OUT} = 2.7 V V_{OUT} = 0.5 V	 −50	50	 −50	50	 −50	50	μA
V_{IHT} V_{ILT}	Input HIGH Voltage Input LOW Voltage		2.0	 0.8	2.0	 0.8	2.0	 0.8	V
V_{OHT}	Output HIGH Voltage	I_{OH} = −3.0 mA I_{OH} = −15 mA	2.5 2.0		2.5 2.0		2.5 2.0		V
V_{OLT}	Output LOW Voltage	I_{OL} = 48 mA		0.55		0.55		0.55	V
V_{IK}	Input Clamp Voltage	I_{IN} = −18 mA		−1.2		−1.2		−1.2	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		Condition	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output		C_L = 50 pF C_L = 200 pF	1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	1.7 3.4	4.8 9.6	ns ns
t_{PLZ} t_{PHZ}	Output Disable Time	$\overline{OEECL}$	C_L = 50 pF C_L = 200 pF	3.7 5.4	6.5 13	3.7 5.4	6.5 13	3.7 5.4	6.5 13	ns ns
t_{PLZ} t_{PHZ}		$\overline{OETTL}$	C_L = 50 pF C_L = 200 pF	4.3 7.0	7.5 15	4.3 7.0	7.5 15	4.3 7.0	7.5 15	ns ns
t_{PZL} t_{PZH}	Output Enable Time	$\overline{OEECL}$	C_L = 50 pF C_L = 200 pF	3.5 5.0	6.0 12	3.5 5.0	6.0 12	3.5 5.0	6.0 12	ns ns
t_{PZL} t_{PZH}		$\overline{OETTL}$	C_L = 50 pF C_L = 200 pF	4.2 6.0	7.0 14	4.2 6.0	7.0 14	4.2 6.0	7.0 14	ns ns
t_R t_F	Output Rise/Fall Time 1.0 V−2.0 V		C_L = 50 pF C_L = 200 pF		1.2 3.0		1.2 3.0		1.2 3.0	ns ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H601FN	PLCC−28	37 Units / Rail
MC10H601FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H601FNR2	PLCC−28	500 / Tape & Reel
MC10H601FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H601FN	PLCC−28	37 Units / Rail
MC100H601FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100H601FNR2	PLCC−28	500 / Tape & Reel
MC100H601FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

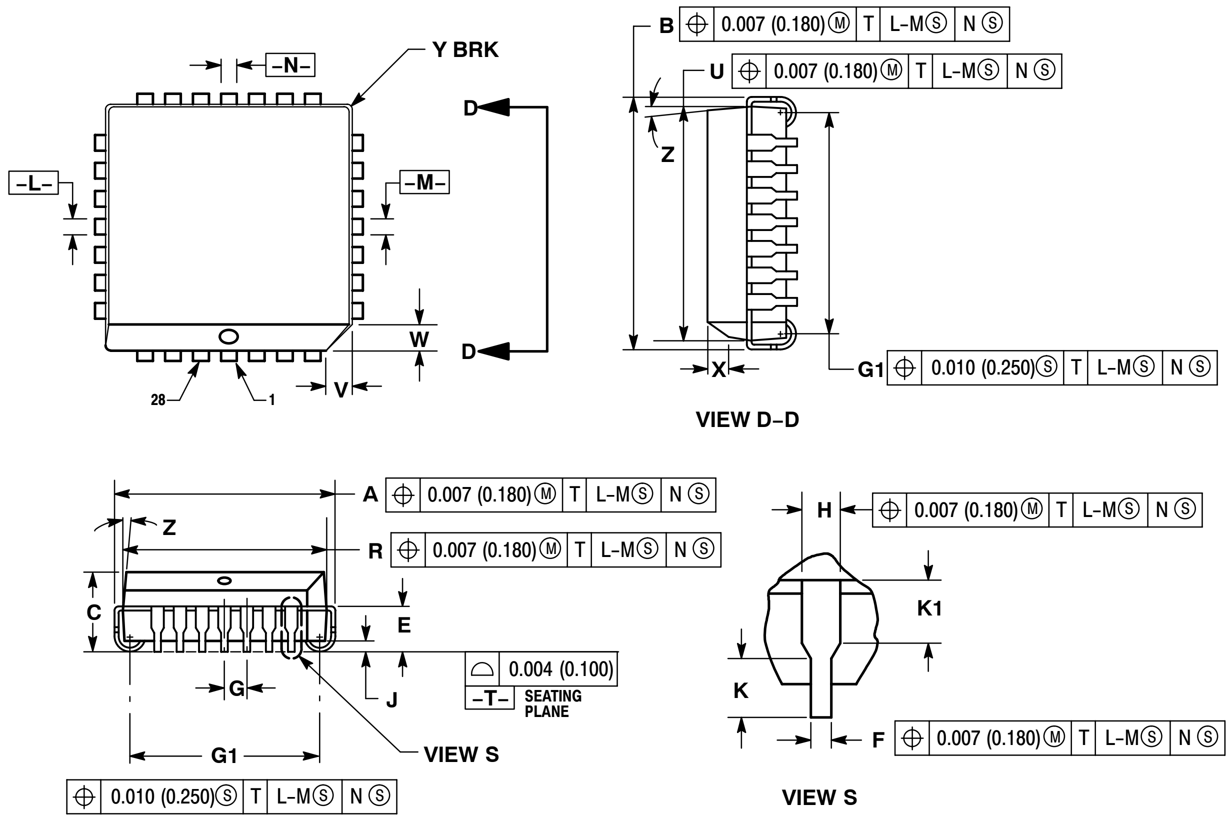
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques
AN1406/D – Designing with PECL (ECL at +5.0 V)
AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D – Metastability and the ECLinPS Family
AN1568/D – Interfacing Between LVDS and ECL
AN1672/D – The ECL Translator Guide
AND8001/D – Odd Number Counters Design
AND8002/D – Marking and Date Codes
AND8020/D – Termination of ECL Logic Devices
AND8066/D – Interfacing with ECLinPS
AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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MECL 10H is a trademark of Motorola, Inc.

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