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MC10SX1189

Fibre Channel Coaxial Cable Driver and Loop Resiliency Circuit

ON Semiconductor®

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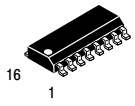
FIBRE CHANNEL COAXIAL CABLE DRIVER AND LOOP RESILIENCY CIRCUIT



SOIC−16
CASE 751B−05

Description

The MC10SX1189 is a differential receiver, differential transmitter specifically designed to drive coaxial cables. It incorporates the output cable drive capability of the MC10EL89 Coaxial Cable Driver with additional circuitry to multiplex the output cable drive source between the cable receiver or the local transmitter inputs. The multiplexer control circuitry is TTL compatible for ease of operation.

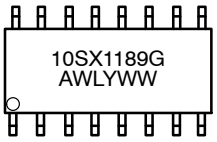
The MC10SX1189 is useful as a bypass element for Fibre Channel-Arbitrated Loop (FC-AL) or Serial Storage Architecture (SSA) applications, to create loop style interconnects with fault tolerant, active switches at each device node. This device is particularly useful for back panel applications where small size is desirable.

The EL89 style drive circuitry produces swings twice as large as a standard PECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize reflections. The 1.6 V output swings allow for proper termination at both ends of the cable, while maintaining the required swing at the receiving end of the cable. Because of the larger output swings, the QT, $\overline{QT}$ outputs are terminated into the thevenin equivalent of 50 Ω to V_{CC} − 3.0 V instead of 50 Ω to V_{CC} − 2.0 V.

Features

- 425 ps Propagation Delay
- 1.6 V Output Swing on the Cable Driving Output
- Operation Range:
  - V_{CC} = 4.5 V to 5.5 V
- 75 kΩ Internal Input Pull Down Resistors
- >1000 V ESD Protection
- Transistor Count = 102
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM*



10SX1189 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping
MC10SX1189DG	SOIC−16 (Pb-Free)	48 Units/Tube

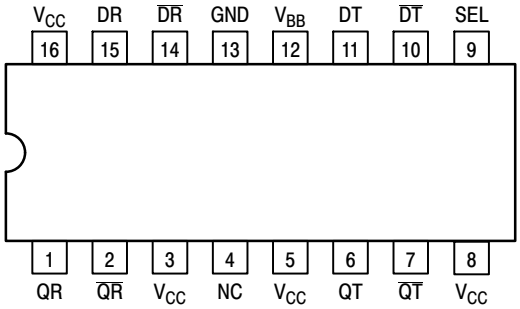


Figure 1. Pinout: SOIC−16 (Top View)

TRUTH TABLE

SEL	Function
L	DR → QT
H	DT → QT

PIN NAMES

Pins	Function
DR/$\overline{DR}$	Differential Input from Receive Cable
QR/$\overline{QR}$	Buffered Differential Output from Receive Cable
DT/$\overline{DT}$	Differential Input to Transmit Cable
QT/$\overline{QT}$	Buffered Differential Output to Transmit Cable
SEL	Multiplexer Control Signal (TTL)
V_{CC}	Positive Power Supply
GND	Ground
V_{BB}	Reference Voltage Output

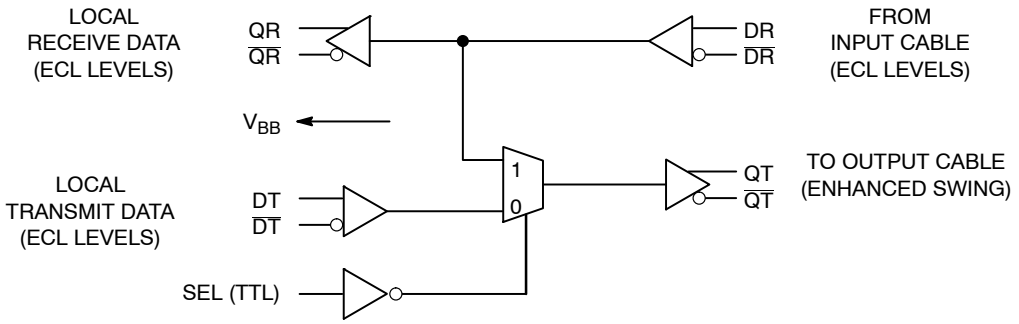


Figure 2. LOGIC DIAGRAM

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage (Referenced to GND)	0 to +7.0	Vdc
V_{IN}	Input Voltage (Referenced to GND)	0 to +6.0	Vdc
I_{OUT}	Output Current Continuous Surge	 50 100	mA
T_A	Operating Temperature Range	−40 to +85	°C
T_{STG}	Storage Temperature Range	−50 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. DC CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output Voltage High (QR,$\overline{QR}$) V_{CC} = 5.0 V, GND = 0 V (Notes 1, 2)	3.92	4.05	4.22	3.97	4.11	4.27	4.00	4.16	4.30	V
V_{OL}	Output Voltage Low (QR,$\overline{QR}$) V_{CC} = 5.0 V, GND = 0 V (Notes 1, 2)	3.05	3.23	3.35	3.07	3.24	3.37	3.10	3.25	3.41	V
V_{OH}	Output Voltage High (QT,$\overline{QT}$) V_{CC} = 5.0 V, GND = 0 V (Notes 1, 3)	3.83	3.95	4.10	3.88	4.02	4.15	3.90	4.09	4.17	V
V_{OL}	Output Voltage Low (QT,$\overline{QT}$) V_{CC} = 5.0 V, GND = 0 V (Notes 1, 3)	1.90	2.33	2.50	1.85	2.26	2.45	1.85	2.23	2.45	V
I_{CC}	Quiescent Supply Current (Note 4)	20	25	42	23	27	47	25	28	47	mA
V_{IH}	Input Voltage High (DR,$\overline{DR}$ & DT,$\overline{DT}$) V_{CC} = 5.0 V, GND = 0 V (Note 1)	3.77		4.11	3.87		4.19	3.94		4.28	V
V_{IL}	Input Voltage Low (DR,$\overline{DR}$ & DT,$\overline{DT}$) V_{CC} = 5.0 V, GND = 0 V (Note 1)	3.05		3.50	3.05		3.52	3.05		3.56	V
V_{IH}	Input Voltage High SEL	2.0			2.0			2.0			V
V_{IL}	Input Voltage Low SEL			0.8			0.8			0.8	V
V_{BB}	Output Reference Voltage V_{CC} = 5.0 V, GND = 0 V (Note 1)	3.57	3.63	3.70	3.65	3.70	3.75	3.69	3.75	3.81	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Values will track 1:1 with the V_{CC} supply. V_{EE} can vary +0.5 V to −0.5 V.
2. Outputs loaded with 50 Ω to V_{CC} − 2.0 V.
3. Outputs loaded with 50 Ω to V_{CC} − 3.0 V.
4. Outputs open circuited.

Table 3. AC CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V) (Note 1)

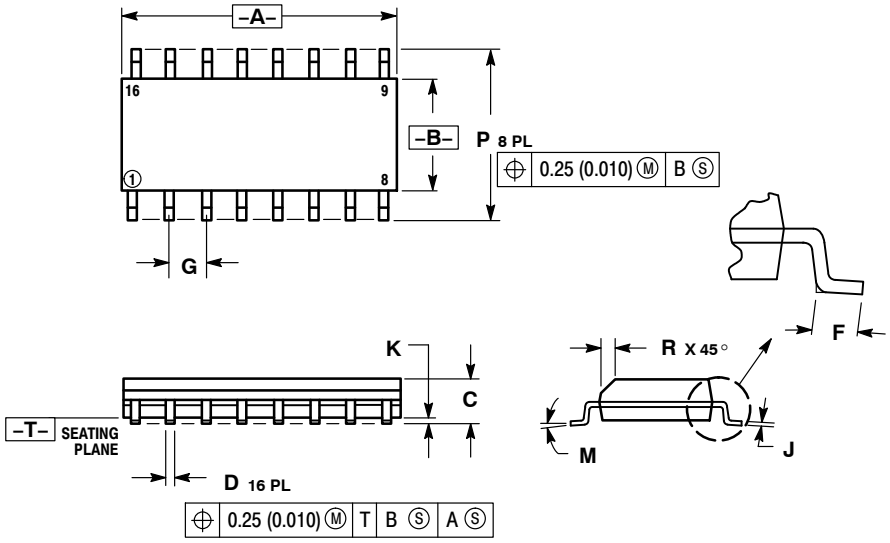
Symbol	Characteristic	–40°C			0 to 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
t_{PLH}, t_{PHL}	Propagation Delay to Output							ps	Note 2
	DR → QR (Diff)	175	300	450	225	325	500		Note 3
	(SE)	150	300	500	175	325	550		
	DR → QT (Diff)	250	425	650	300	450	650		
	(SE)	225	425	700	250	450	700		
	DT → QT (Diff)	225	400	650	275	425	650		
	(SE)	200	400	725	225	425	725		
	Propagation Delay SEL → QT,$\overline{QT}$	450	600	850	500	650	800		1.5V to 50% Pt
t_r, t_f	Rise TimeQR,$\overline{QR}$	100	275	400	125	275	400	ps	20% to 80%
	Fall Time	100	275	400	125	275	400		80% to 20%
t_r, t_f	Rise TimeQT,$\overline{QT}$	150	300	550	150	300	550	ps	20% to 80%
	Fall Time	150	300	550	150	300	550		80% to 20%
t_{skew}	Within Device Skew		15			15		ps	Note 4
V_{PP}	Minimum Input Swing	200		1000	200		1000	mV	Note 5
V_{CMR}	Common Mode Range	3.00		4.35	3.00		4.35	V	Note 6

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. V_{EE} can vary +0.5 V to −0.5 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. Duty cycle skew is the difference between t_{PLH} and t_{PHL} propagation delay through a device.
5. Minimum input swing for which AC parameters are guaranteed.
6. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\ Min}$ and 1.0 V.

PACKAGE DIMENSIONS

SOIC−16
CASE 751B−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:
PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:
PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

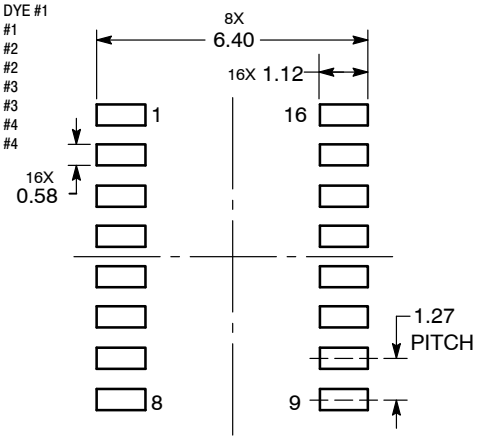
STYLE 4:
PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:
PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:
PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:
PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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