Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

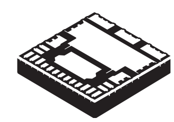
Document Number: MC10XS3412
Rev. 12.0, 2/2013

RoHS

Quad High Side Switch (Dual 10 mOhm, Dual 12 mOhm)

10XS3412

HIGH SIDE SWITCH



FK SUFFIX (PB-FREE) 98ARL10596D 24-PIN PQFN	FK SUFFIX (PB-FREE) 98ASA00426D 24-PIN PQFN

ORDERING INFORMATION		
Device (for Tape and Reel, add an R2 suffix)	**Temperature Range (T_A)**	**Package**
MC10XS3412CHFK	-40 to 125°C	24 PQFN
MC10XS3412JHFK		

The 10XS3412 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(ON)}$ MOSFETs (dual 10 mOhm/dual 12 mOhm) can control four separate 55/28 W bulbs, and/or Xenon modules, and/or LEDs.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control. The 10XS3412 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide functionality of the outputs in case of MCU damage.

Features

- Four protected 10 mΩ and 12 mΩ high side switches (at 25 °C)
- Operating voltage range of 6.0 to 20 V with sleep current < 5.0 µA, extended mode from 4.0 to 28 V
- 8.0 MHz 16-bit 3.3 V and 5.0 V SPI control and status reporting with daisy chain capability
- PWM module using external clock or calibratable internal oscillator with programmable outputs delay management
- Smart overcurrent shutdown, severe short-circuit, overtemperature protection with time limited autoretry, and Fail-safe mode in case of MCU damage
- Output OFF or ON open-load detection compliant to bulbs or LEDs and short to battery detection
- Analog current feedback with selectable ratio and board temperature feedback

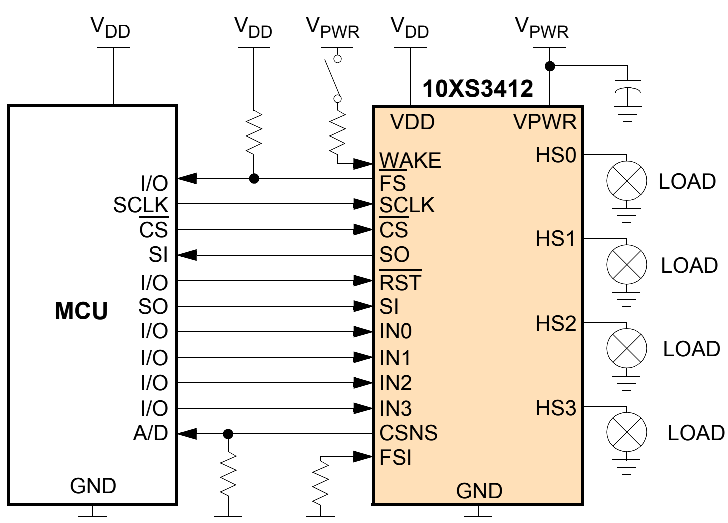


Figure 1. 10XS3412 Simplified Application Diagram

DEVICE VARIATIONS

Table 1. Device Variations

Characteristic	Symbol	Min	Typ	Max	Unit
Wake Input Clamp Voltage, $I_{CL(WAKE)} < 2.5$ mA	$V_{CL(WAKE)}$				V
10XS3412CHFK		19	25	32	
10XS3412JHFK		20	27	35	
Fault Detection Blanking Time	t_{FAULT}				μs
10XS3412CHFK		-	5.0	20	
10XS3412JHFK		-	5.0	10	
Output Shutdown Delay Time	t_{DETECT}				μs
10XS3412CHFK		-	7.0	30	
10XS3412JHFK		-	7.0	20	
Peak Package Reflow Temperature During Reflow, [(1)], [(2)]	T_{PPRT}				°C
10XS3412CHFK				Note 2	
10XS3412JHFK					

Notes

1. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
2. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

INTERNAL BLOCK DIAGRAM

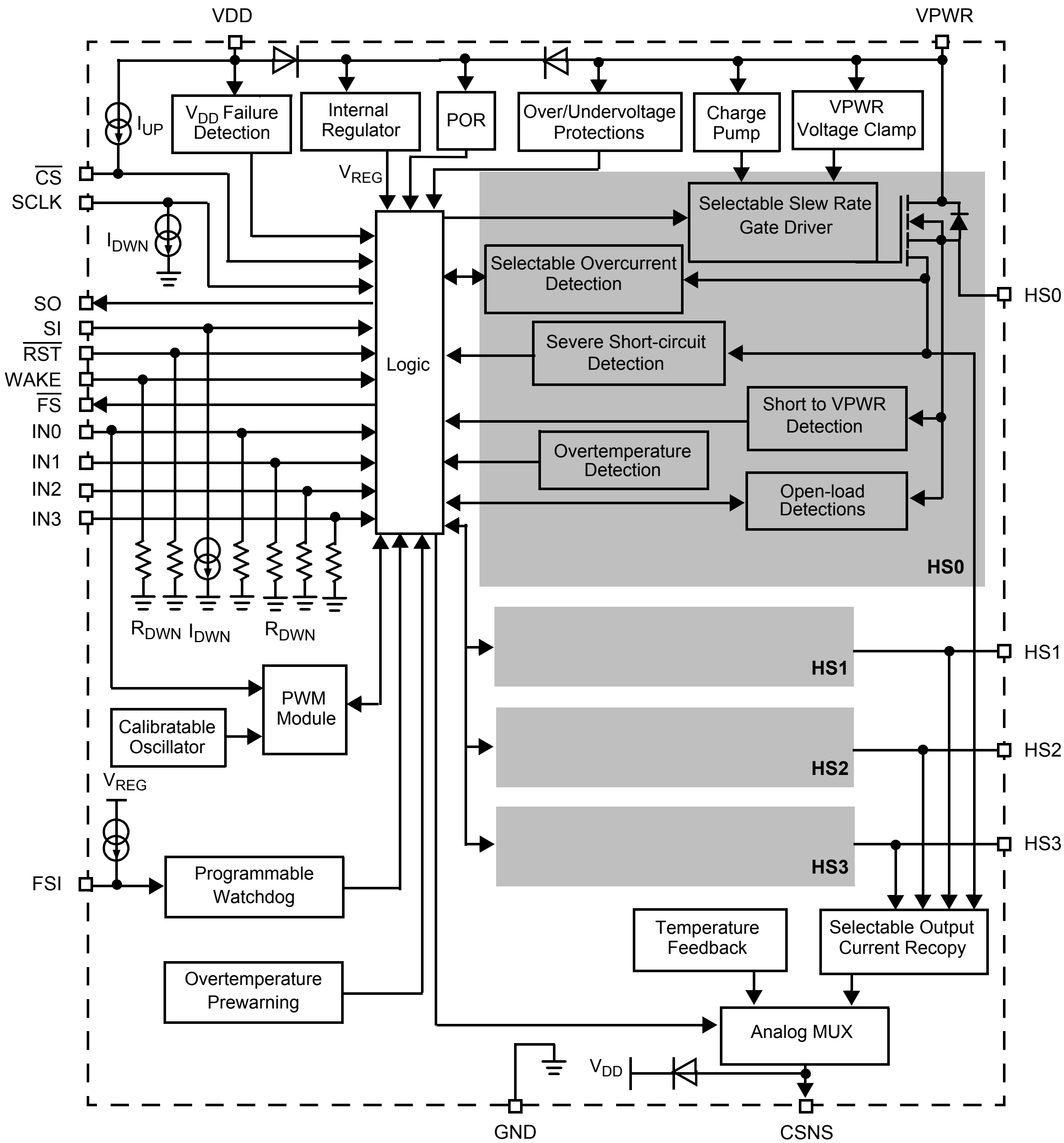


Figure 2. 10XS3412 Simplified Internal Block Diagram

PIN CONNECTIONS

Transparent Top View of Package

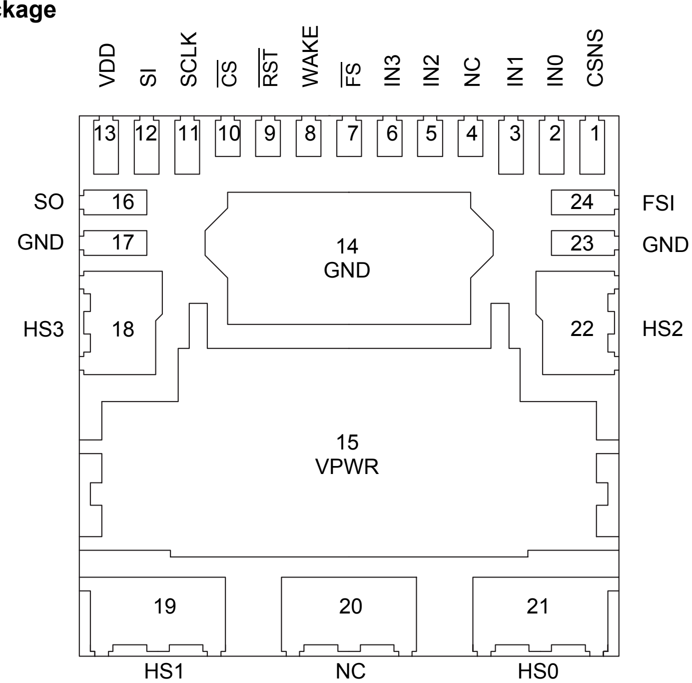


Figure 3. 10XS3412 Pin Connections

Table 2. 10XS3412 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 23.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	CSNS	Output	Output Current Monitoring	This pin reports an analog value proportional to the designated HS[0:3] output current or the temperature of the GND flag (pin 14). It is used externally to generate a ground-referenced voltage for the microcontroller (MCU) . Current recopy and temperature feedback is SPI programmable.
2 3 5 6	IN0 IN1 IN2 IN3	Input	Direct Inputs	Each direct input controls the device mode. The IN[0:3] high side input pins are used to directly control HS0:HS3 high side output pins. The PWM frequency can be generated from IN0 pin to PWM module in case of external clock is set.
7	$\overline{FS}$	Output	Fault Status (Active Low)	This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting.
8	WAKE	Input	Wake	This input pin controls the device mode.
9	$\overline{RST}$	Input	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode.
10	$\overline{CS}$	Input	Chip Select (Active Low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
11	SCLK	Input	Serial Clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.
12	SI	Input	Serial Input	This pin is a command data input pin connected to the SPI serial data output of the MCU or to the SO pin of the previous device of a daisy-chain of devices.
13	VDD	Power	Digital Drain Voltage	This pin is an external voltage input pin used to supply power interfaces to the SPI bus.

Table 2. 10XS3412 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 23.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
14, 17, 23	GND	Ground	Ground	These pins, internally shorted, are the ground for the logic and analog circuitry of the device. These ground pins must be also shorted in the board.
15	VPWR	Power	Positive Power Supply	This pin connects to the positive power supply and is the source of operational power for the device.
16	SO	Output	Serial Output	This output pin is connected to the SPI serial data input pin of the MCU or to the SI pin of the next device of a daisy-chain of devices.
18 19 21 22	HS3 HS1 HS0 HS2	Output	High Side Outputs	Protected 10 mΩ (HS0 and HS1) 12 mΩ (HS2 and HS3) high side power output pins to the load.
4, 20	NC	N/A	No Connect	These pins may not be connected.
24	FSI	Input	Fail Safe Input	This input enables the watchdog timeout feature.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
V_{PWR} Supply Voltage Range Load Dump at 25 °C (400 ms) Maximum Operating Voltage Reverse Battery at 25 °C (2.0 min.)	$V_{PWR(SS)}$	 41 28 -18	V
V_{DD} Supply Voltage Range	V_{DD}	-0.3 to 5.5	V
Input/Output Voltage	[6]	-0.3 to V_{DD}+0.3	V
WAKE Input Clamp Current	$I_{CL(WAKE)}$	2.5	mA
CSNS Input Clamp Current	$I_{CL(CSNS)}$	2.5	mA
HS [0:3] Voltage Positive Negative	$V_{HS[0:3]}$	 41 -16	V
Output Current[3]	$I_{HS[0:3]}$	6	A
Output Clamp Energy Using Single-pulse Method[4]	$E_{CL[0:3]}$	100	mJ
ESD Voltage[5] Human Body Model (HBM) for HS[0:3], VPWR and GND Human Body Model (HBM) for other pins Charge Device Model (CDM) Corner Pins (1, 13, 19, 21) All Other Pins (2-12, 14-18, 20, 22-24)	 V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	 ±8000 ±2000 ±750 ±500	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C

Notes
3. Continuous high side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
4. Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14 V, T_J = 150°C initial).
5. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
6. Input / Output pins are: IN[0:3], RSTB, FSI, CSNS, SI, SCLK, CSB, SO, FSB

Table 3. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RESISTANCE			
Thermal Resistance[7] Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 <1.0 30	°C/W
Peak Package Reflow Temperature During Reflow[8], [9] 10XS3412CHFK 10XS3412JHFK	T_{PPRT}	Note 9	°C

Notes

7. Device mounted on a 2s2p test board per JEDEC JESD51-2. 15 °C/W of $R_{\theta JA}$ can be reached in a real application case (4 layers board).
8. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUTS					
Battery Supply Voltage Range Fully Operational Extended mode[10]	V_{PWR}	 6.0 4.0	 – –	 20 28	V
Battery Clamp Voltage[11]	$V_{PWR(CLAMP)}$	41	47	53	V
V_{PWR} Operating Supply Current Outputs commanded ON, HS[0:3] open, IN[0:3] > V_{IH}	$I_{PWR(ON)}$	–	6.5	20	mA
V_{PWR} Supply Current Outputs commanded OFF, OFF Open-load Detection Disabled, HS[0:3] shorted to the ground with V_{DD}= 5.5 V WAKE > V_{IH} or $\overline{RST}$ > V_{IH} and IN[0:3] < V_{IL}	$I_{PWR(SBY)}$	–	6.5	8.0	mA
Sleep State Supply Current V_{PWR} = 12 V, $\overline{RST}$ = WAKE = IN[0:3] < V_{IL}, HS[0:3] shorted to the ground T_A = 25 °C T_A = 85 °C	$I_{PWR(SLEEP)}$	 – –	 1.0 –	 5.0 30	µA
V_{DD} Supply Voltage	$V_{DD(ON)}$	3.0	–	5.5	V
V_{DD} Supply Current at V_{DD} = 5.5 V No SPI Communication 8.0 MHz SPI Communication[12]	$I_{DD(ON)}$	 – –	 1.6 5.0	 2.2 –	mA
V_{DD} Sleep State Current at V_{DD} = 5.5 V	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage Shutdown Threshold	$V_{PWR(OV)}$	28	32	36	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Shutdown Threshold[13]	$V_{PWR(UV)}$	3.3	3.9	4.3	V
V_{PWR} and V_{DD} Power on Reset Threshold	$V_{SUPPLY(POR)}$	0.5	-	0.9	$V_{PWR(UV)}$
Recovery Undervoltage Threshold	Vpwr(UV)_UP	3.4	4.1	4.5	V
V_{DD} Supply Failure Threshold (for V_{PWR} > $V_{PWR(UV)}$)	$V_{DD(FAIL)}$	2.2	2.5	2.8	V

Notes

10. In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 V to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
11. Measured with the outputs open.
12. Typical value guaranteed per design.
13. Output will automatically recover with time limited autoretry to instructed state when V_{PWR} voltage is restored to normal as long as the V_{PWR} degradation level did not go below the undervoltage power-ON reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS3					
HS[0,1] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 25 °C)	$R_{DS\_01(ON)}$				mΩ
V_{PWR} = 4.5 V		–	–	36	
V_{PWR} = 6.0 V		–	–	16	
V_{PWR} = 10 V		–	–	10	
V_{PWR} = 13 V		–	–	10	
HS[0,1] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 150 °C)	$R_{DS\_01(ON)}$				mΩ
V_{PWR} = 4.5 V		–	–	62	
V_{PWR} = 6.0 V		–	–	27	
V_{PWR} = 10 V		–	–	17	
V_{PWR} = 13 V		–	–	17	
HS[0,1] Output Source-to-Drain ON Resistance (I_{HS} = -5.0 A, V_{PWR} = 18 V)(14)	$R_{SD\_01(ON)}$				mΩ
T_A = 25 °C		–	–	15	
T_A = 150 °C		–	–	20	
HS[2,3] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 25 °C)	$R_{DS\_23(ON)}$				mΩ
V_{PWR} = 4.5 V		–	–	44	
V_{PWR} = 6.0 V		–	–	19	
V_{PWR} = 10 V		–	–	12	
V_{PWR} = 13 V		–	–	12	
HS[2,3] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 150 °C)	$R_{DS\_23(ON)}$				mΩ
V_{PWR} = 4.5 V		–	–	75	
V_{PWR} = 6.0 V		–	–	33	
V_{PWR} = 10 V		–	–	21	
V_{PWR} = 13 V		–	–	21	
HS[2,3] Output Source-to-Drain ON Resistance (I_{HS} = -5.0 A, V_{PWR} = -18 V)(14)	$R_{SD\_23(ON)}$				mΩ
T_A = 25 °C		–	–	18	
T_A = 150 °C		–	–	24	
Maximum Severe Short-circuit Impedance Detection(15)	R_{SHORT}	28	64	100	mΩ

Notes
14. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.
15. Short-circuit impedance calculated from HS[0:3] to GND pins. Value guaranteed per design.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS3 (continued)					
Output Overcurrent Detection Levels (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)					A
28 W bit = 0	OCHI1_0	78	94.0	110	
	OCHI2_0	50	60.0	70	
	OC1_0	44.1	52.5	60.9	
	OC2_0	37.8	45.0	52.2	
	OC3_0	31.5	37.5	43.5	
	OC4_0	25.2	30.0	34.8	
	OCLO4_0	18.9	22.5	26.1	
	OCLO3_0	12.6	15.0	17.4	
	OCLO2_0	10.0	12.0	14.0	
	OCLO1_0	6.4	8.0	9.6	
28 W bit = 1	OCHI1_1	39	47.0	55	
	OCHI2_1	25	30.0	35	
	OC1_1	22.0	26.2	30.5	
	OC2_1	18.9	22.5	26.1	
	OC3_1	15.7	18.7	21.8	
	OC4_1	12.6	15.0	17.4	
	OCLO4_1	9.4	11.2	13.1	
	OCLO3_1	6.0	7.5	9.0	
	OCLO2_1	4.5	6.0	7.5	
	OCLO1_1	3.0	4.0	5.0	
Current Sense Ratio (6.0 V ≤ $_{HS[0:3]}$ ≤ 20 V, CSNS ≤ 5.0 V)[16]					–
28 W bit = 0					
CSNS_ratio bit = 0	C_{SR0_0}	–	1/8700	–	
CSNS_ratio bit = 1	C_{SR1_0}	–	1/53000	–	
28 W bit = 1					
CSNS_ratio bit = 0	C_{SR0_1}	–	1/4350	–	
CSNS_ratio bit = 1	C_{SR1_1}	–	1/26500	–	
Current Sense Ratio (C_{SR0}) Accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) with 28 W bit=0	$C_{SR0\_0\_ACC}$				%
Output Current					
12.5 A		-12	–	12	
5.0 A		-13	–	13	
3.0 A		-16	–	16	
1.5 A		-20	–	20	

Notes

16. Current sense ratio = I_{CSNS} / $I_{HS[0:3]}$

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS3 (continued)					
Current Sense Ratio (C_{SR0}) Accuracy (6.0 V ≤ V_{HS} ≤ 20 V) with 28 W bit=1 Output Current 3.0 A 1.5 A	$C_{SR0\_1\_ACC}$	 -16 -20	 – –	 16 20	%
C_{SR0} Current Recopy Accuracy with one calibration point (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)(17) Output Current 5.0 A	$C_{SR0\_0\_ACC(CAL)}$	-5.0	–	5.0	%
C_{SR0} Current Recopy Temperature Drift (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) with 28 W bit=0(18) Output Current 5.0 A	$\Delta(C_{SR0\_0})/\Delta(T)$			0.04	%/°C
Current Sense Ratio (C_{SR1}) Accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) with 28 W bit=0 Output Current 12.5 A 75 A	$C_{SR1\_0\_ACC}$	 -17 -12	 – –	 +17 +12	%
Current Sense Clamp Voltage CSNS Open; $I_{HS[0:3]}$ = 5.0 A with C_{SR0} ratio	$V_{CL(CSNS)}$	V_{DD}+0.25		V_{DD}+1.0	V
OFF Open-load Detection Source Current(19)	$I_{OLD(OFF)}$	30	–	100	µA
OFF Open-load Fault Detection Voltage Threshold	$V_{OLD(THRES)}$	2.0	3.0	4.0	V
ON Open-load Fault Detection Current Threshold	$I_{OLD(ON)}$	100	300	600	mA
ON Open-load Fault Detection Current Threshold with LED $V_{HS[0:3]}$ = V_{PWR} - 0.75 V	$I_{OLD(ON\_LED)}$	2.5	5.0	10	mA
Output Short to V_{PWR} Detection Voltage Threshold Output programmed OFF	$V_{OSD(THRES)}$	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V
Output Negative Clamp Voltage 0.5 A ≤ $I_{HS[0:3]}$ ≤ 5.0 A, Output programmed OFF	V_{CL}	-22	–	-16	V
Output Overtemperature Shutdown for 4.5 V < V_{PWR} < 28 V	T_{SD}	155	175	195	°C

Notes

17. Based on statistical analysis. It is not production tested.
18. Based on statistical data: delta(C_{SR0})/delta(T)={(measured I_{CSNS} at T_1 - measured I_{CSNS} at T_2) / measured I_{CSNS} at room} / {T_1-T_2}. No production tested.
19. Output OFF Open-load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open-load condition when the specific output is commanded OFF. Pull-up current is measured for V_{HS}=$V_{OLD(THRES)}$

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Logic High Voltage[20]	V_{IH}	2.0	–	V_{DD}+0.3	V
Input Logic Low Voltage[20]	V_{IL}	-0.3	–	0.8	V
Input Logic Pull-down Current (SCLK, SI)[23]	I_{DWN}	5.0	–	20	µA
Input Logic Pull-up Current ($\overline{CS}$)[24]	I_{UP}	5.0	–	20	µA
SO, $\overline{FS}$ Tri-state Capacitance[21]	C_{SO}	–	–	20	pF
Input Logic Pull-down Resistor ($\overline{RST}$, WAKE and IN[0:3])	R_{DWN}	125	250	500	kΩ
Input Capacitance[21]	C_{IN}	–	4.0	12	pF
Wake Input Clamp Voltage[22], $I_{CL(WAKE)}$ < 2.5 mA 10XS3412CHFK 10XS3412JHFK	$V_{CL(WAKE)}$	 19 20	 25 27	 32 35	V
Wake Input Forward Voltage $I_{CL(WAKE)}$ = -2.5 mA	$V_{F(WAKE)}$	 -2.0	 –	 -0.3	V
SO High state Output Voltage I_{OH} = 1.0 mA	V_{SOH}	 V_{DD}-0.4	 –	 –	V
SO and $\overline{FS}$ Low state Output Voltage I_{OL} = -1.0 mA	V_{SOL}	 –	 –	 0.4	V
SO, CSNS and $\overline{FS}$ Tri-state Leakage Current $\overline{CS}$ = V_{IH} and 0 V ≤ V_{SO} ≤ V_{DD}, or $\overline{FS}$ = 5.5 V, or CSNS=0.0 V	$I_{SO(LEAK)}$	 -2.0	 0	 2.0	µA
FSI External Pull-down Resistance[25] Watchdog Disabled Watchdog Enabled	RFS	 – 10	 0 Infinite	 1.0 –	kΩ

Notes

20. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3] and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage referenced to V_{PWR}.
21. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3] and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
22. The current must be limited by a series resistance when using voltages > 7.0 V.
23. Pull-down current is with V_{SI} ≥ 1.0 V and V_{SCLK} ≥ 1.0 V.
24. Pull-up current is with $V_{\overline{CS}}$ ≤ 2.0 V. $\overline{CS}$ has an active internal pull-up to V_{DD}.
25. In Fail Safe HS[0:3] depends respectively on ON[0:3]. FSI has an active internal pull-up to V_{REG} ~ 3.0 V.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS3					
Output Rising Medium Slew Rate (medium speed slew rate / SR[1:0]=00)[26] V_{PWR} = 14 V	SR_{R_00}	0.15	0.3	0.6	V/µs
Output Rising Slow Slew Rate (low speed slew rate / SR[1:0]=01)[26] V_{PWR} = 14 V	SR_{R_01}	0.07	0.15	0.3	V/µs
Output Falling Fast Slew Rate (high speed slew rate / SR[1:0]=10)[26] V_{PWR} = 14 V	SR_{R_10}	0.3	0.6	1.2	V/µs
Output Falling Medium Slew Rate (medium speed slew rate / SR[1:0]=00)[26] V_{PWR} = 14 V	SR_{F_00}	0.15	0.3	0.6	V/µs
Output Falling Slow Slew Rate (low speed slew rate / SR[1:0]=01)[26] V_{PWR} = 14 V	SR_{F_01}	0.07	0.15	0.3	V/µs
Output Rising Fast Slew Rate (high speed slew rate / SR[1:0]=10)[26] V_{PWR} = 14 V	SR_{F_10}	0.3	0.6	1.2	V/µs
HS[0,1] Output Turn-ON and Turn-OFF Delay Times[27] V_{PWR} = 14 V	t_{DLY_01}	45	70	95	µs
HS[2,3] Output Turn-ON and Turn-OFF Delay Times[27] V_{PWR} = 14 V	t_{DLY_23}	40	65	90	µs
Driver Output Matching Slew Rate (SR_R /SR_F) V_{PWR} = 14 V @ 25 °C and for medium speed slew rate (SR[1:0]=00)	ΔSR	0.8	1.0	1.2	
Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) V_{PWR} = 14 V, f_{PWM} = 240 Hz, PWM duty cycle = 50%, @ 25 °C for medium speed slew rate (SR[1:0]=00)	Δt_{RF}	-25	-5.0	15	µs

Notes

26. Rise and Fall Slew Rates measured across a 5.0 Ω resistive load at high side output = 30% to 70% (see Figure 4, page 20).
27. Turn-ON delay time measured from rising edge of any signal (IN[0:3] and $\overline{CS}$) that would turn the output ON to $V_{HS[0:3]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load. Turn-OFF delay time measured from falling edge of any signal (IN[0:3] and $\overline{CS}$) that would turn the output OFF to $V_{HS[0:3]}$ =V_{PWR} / 2 with R_L = 5.0 Ω resistive load.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS3 (CONTINUED)					
Fault Detection Blanking Time[28]	t_{FAULT}				µs
10XS3412CHFK		-	5.0	20	
10XS3412JHFK		-	5.0	10	
Output Shutdown Delay Time[29]	t_{DETECT}				µs
10XS3412CHFK		-	7.0	30	
10XS3412JHFK		-	7.0	20	
CSNS Valid Time[30]	t_{CNSVAL}	–	70	100	µs
Watchdog Timeout[31]	t_{WDTO}	217	310	400	ms
ON Open-load Fault Cyclic Detection Time with LED		-	f_{IN0} / 128	-	ms

Notes

28. Time necessary to report the fault to $\overline{FS}$ pin.
29. Time necessary to switch off the output in case of OT or OC or SC or UV fault detection (from negative edge of $\overline{FS}$ pin to HS voltage = 50% of V_{PWR}
30. Time necessary for CSNS to be within ±5% of the targeted value (from HS voltage = 50% of V_{PWR} to ±5% of the targeted CSNS value).
31. For FSI open, the Watchdog timeout delay measured from the rising edge of RST, to HS[0,2] output state depend on the corresponding input command.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Output Overcurrent Time Step for 28 W bit = 0					ms
OC[1:0]=00 (slow by default)	t_{OC1_00}	4.40	6.30	8.02	
	t_{OC2_00}	1.62	2.32	3.00	
	t_{OC3_00}	2.10	3.00	3.90	
	t_{OC4_00}	2.88	4.12	5.36	
	t_{OC5_00}	4.58	6.56	8.54	
	t_{OC6_00}	10.16	14.52	18.88	
	t_{OC7_00}	73.2	104.6	134.0	
OC[1:0]=01 (fast)	t_{OC1_01}	1.10	1.57	2.00	
	t_{OC2_01}	0.40	0.58	0.75	
	t_{OC3_01}	0.52	0.75	0.98	
	t_{OC4_01}	0.72	1.03	1.34	
	t_{OC5_01}	1.14	1.64	2.13	
	t_{OC6_01}	2.54	3.63	4.72	
	t_{OC7_01}	18.2	26.1	34.0	
OC[1:0]=10 (medium)	t_{OC1_10}	2.20	3.15	4.01	
	t_{OC2_10}	0.81	1.16	1.50	
	t_{OC3_10}	1.05	1.50	1.95	
	t_{OC4_10}	1.44	2.06	2.68	
	t_{OC5_10}	2.29	3.28	4.27	
	t_{OC6_10}	5.08	7.26	9.44	
	t_{OC7_10}	36.6	52.3	68.0	
OC[1:0]=11 (very slow)	t_{OC1_11}	8.8	12.6	16.4	
	t_{OC2_11}	3.2	4.6	21.4	
	t_{OC3_11}	4.2	6.0	7.8	
	t_{OC4_11}	5.7	8.2	10.7	
	t_{OC5_11}	9.1	13.1	17.0	
	t_{OC6_11}	20.3	29.0	37.7	
	t_{OC7_11}	146.4	209.2	272.0	

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Output Overcurrent Time Step for 28 W bit = 1					ms
OC[1:0]=00 (slow by default)	t_{OC1_00}	3.4	4.9	6.4	
	t_{OC2_00}	1.1	1.6	2.1	
	t_{OC3_00}	1.4	2.1	2.8	
	t_{OC4_00}	2.0	2.9	3.8	
	t_{OC5_00}	3.4	4.9	6.4	
	t_{OC6_00}	8.5	12.2	15.9	
	t_{OC7_00}	62.4	89.2	116.0	
OC[1:0]=01 (fast)	t_{OC1_01}	0.86	1.24	1.61	
	t_{OC2_01}	0.28	0.40	0.52	
	t_{OC3_01}	0.36	0.52	0.68	
	t_{OC4_01}	0.51	0.74	0.96	
	t_{OC5_01}	0.78	1.12	1.46	
	t_{OC6_01}	2.14	3.06	3.98	
	t_{OC7_01}	20.2	22.2	28.9	
OC[1:0]=10 (medium)	t_{OC1_10}	1.7	2.5	3.3	
	t_{OC2_10}	0.5	0.8	1.0	
	t_{OC3_10}	0.7	1.0	1.3	
	t_{OC4_10}	1.0	1.5	2.0	
	t_{OC5_10}	1.7	2.5	3.3	
	t_{OC6_10}	4.2	6.1	6.0	
	t_{OC7_10}	31.2	44.6	58.0	
OC[1:0]=11 (very slow)	t_{OC1_11}	6.8	9.8	12.8	
	t_{OC2_11}	2.2	3.2	16.7	
	t_{OC3_11}	2.9	4.2	5.5	
	t_{OC4_11}	4.0	5.8	7.6	
	t_{OC5_11}	6.8	9.8	12.8	
	t_{OC6_11}	17.0	24.4	31.8	
	t_{OC7_11}	124.8	178.4	232.0	

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Bulb Cooling Time Step for 28 W bit = 0					ms
CB[1:0]=00 or 11 (medium)	t_{BC1_00}	242	347	452	
	t_{BC2_00}	126	181	236	
	t_{BC3_00}	140	200	260	
	t_{BC4_00}	158	226	294	
	t_{BC5_00}	181	259	337	
	t_{BC6_00}	211	302	393	
CB[1:0]=01 (fast)	t_{BC1_01}	121	173	226	
	t_{BC2_01}	63	90	118	
	t_{BC3_01}	70	100	130	
	t_{BC4_01}	79	113	147	
	t_{BC5_01}	90	129	169	
	t_{BC6_01}	105	151	197	
CB[1:0]=10 (slow)					
	t_{BC1_10}	484	694	1904	
	t_{BC2_10}	252	362	472	
	t_{BC3_10}	280	400	520	
	t_{BC4_10}	316	452	588	
	t_{BC5_10}	362	518	674	
	t_{BC6_10}	422	604	786	
for 28 W bit = 1					
CB[1:0]=00 or 11 (medium)					
	t_{BC1_00}	291	417	542	
	t_{BC2_00}	156	224	292	
	t_{BC3_00}	178	255	332	
	t_{BC4_00}	208	298	388	
	t_{BC5_00}	251	359	467	
	t_{BC6_00}	314	449	584	
CB[1:0]=01 (fast)					
	t_{BC1_01}	146	209	272	
	t_{BC2_01}	78	112	146	
	t_{BC3_01}	88	127	166	
	t_{BC4_01}	101	145	189	
	t_{BC5_01}	126	180	234	
	t_{BC6_01}	226	324	422	
CB[1:0]=10 (slow)					
	t_{BC1_10}	583	834	1085	
	t_{BC2_10}	312	448	582	
	t_{BC3_10}	357	510	665	
	t_{BC4_10}	417	596	775	
	t_{BC5_10}	501	717	933	
	t_{BC6_10}	628	898	1170	

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PWM MODULE TIMING					
Input PWM Clock Range on IN0	f_{IN0}	7.68	–	51.2	kHz
Input PWM Clock Low Frequency Detection Range on IN0[32]	$f_{IN0(LOW)}$	1.0	2.0	4.0	kHz
Input PWM Clock High Frequency Detection Range on IN0[32]	$f_{IN0(HIGH)}$	100	200	400	kHz
Output PWM Frequency Range	f_{PWM}	–	–	1.0	kHz
Output PWM Frequency Accuracy using Calibrated Oscillator	$A_{FPWM(CAL)}$	-10	–	+10	%
Default Output PWM Frequency using Internal Oscillator	$f_{PWM(0)}$	84	120	156	Hz
$\overline{CS}$ Calibration Low Minimum Time Detection Range	$t_{CSB(MIN)}$	14	20	26	µs
$\overline{CS}$ Calibration Low Maximum Tine Detection Range	$t_{CSB(MAX)}$	140	200	260	µs
Output PWM Duty-cycle Range for fpwm = 1.0 kHz for High Speed Slew Rate[33]	R_{PWM_1k}	6.0	–	94	%
Output PWM Duty-cycle Range for fpwm = 400 Hz[33]	R_{PWM_400}	10	–	98	%
Output PWM Duty-cycle Range for fpwm = 200 Hz [33]	R_{PWM_200}	5.0	–	98	%
INPUT TIMING					
Direct Input Toggle Timeout	t_{IN}	175	250	325	ms
AUTORETRY TIMING					
Autoretry Period	t_{AUTO}	105	150	195	ms
TEMPERATURE ON THE GND FLAG					
Thermal Prewarning Detection[34]	T_{OTWAR}	110	125	140	°C
Analog Temperature Feedback at T_A = 25 °C with R_{CSNS}=2.5 kΩ	T_{FEED}	1.15	1.20	1.25	V
Analog Temperature Feedback Derating with R_{CSNS}=2.5 kΩ[35]	DT_{FEED}	-3.5	-3.7	-3.9	mV/°C

Notes

32. Clock Fail detector available for PWM_en bit is set to logic [1] and CLOCK_sel is set to logic [0].
33. The PWM ratio is measured at V_{HS} = 50% of V_{PWR} and for the default SR value. It is possible to put the device fully-on (PWM duty-cycle 100%) and fully-off (duty-cycle 0%). For values outside this range, a calibration is needed between the PWM duty-cycle programming and the PWM on the output with R_L = 5.0 Ω resistive load.
34. Typical value guaranteed per design.
35. Value guaranteed per statistical analysis.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS(36)					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	8.0	MHz
Required Low State Duration for $\overline{RST}$(37)	$t_{\overline{WRST}}$	10	–	–	µs
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time)(38)	$t_{\overline{CS}}$	–	–	1.0	µs
Rising Edge of $\overline{RST}$ to Falling Edge of $\overline{CS}$ (Required Setup Time)(38)	t_{ENBL}	–	–	5.0	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)(38)	t_{LEAD}	–	–	500	ns
Required High State Duration of SCLK (Required Setup Time)(38)	t_{WSCLKh}	–	–	50	ns
Required Low State Duration of SCLK (Required Setup Time)(38)	t_{WSCLKl}	–	–	50	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)(38)	t_{LAG}	–	–	60	ns
SI to Falling Edge of SCLK (Required Setup Time)(39)	$t_{SI(SU)}$	–	–	37	ns
Falling Edge of SCLK to SI (Required Setup Time)(39)	$t_{SI(HOLD)}$	–	–	49	ns
SO Rise Time C_L = 80 pF	t_{RSO}	 –	 –	 13	ns
SO Fall Time C_L = 80 pF	t_{FSO}	 –	 –	 13	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time(39)	t_{RSI}	–	–	13	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time(39)	t_{FSI}	–	–	13	ns
Time from Rising Edge of SCLK to SO Low-impedance(40)	$t_{SO(EN)}$	–	–	60	ns
Time from Rising Edge of SCLK to SO High-impedance(41)	$t_{SO(DIS)}$	–	–	60	ns

Notes

36. Parameters guaranteed by design.
37. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.
38. Maximum setup time required for the 10XS3412 is the minimum guaranteed time needed from the microcontroller.
39. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
40. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
41. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on $\overline{CS}$.

TIMING DIAGRAMS

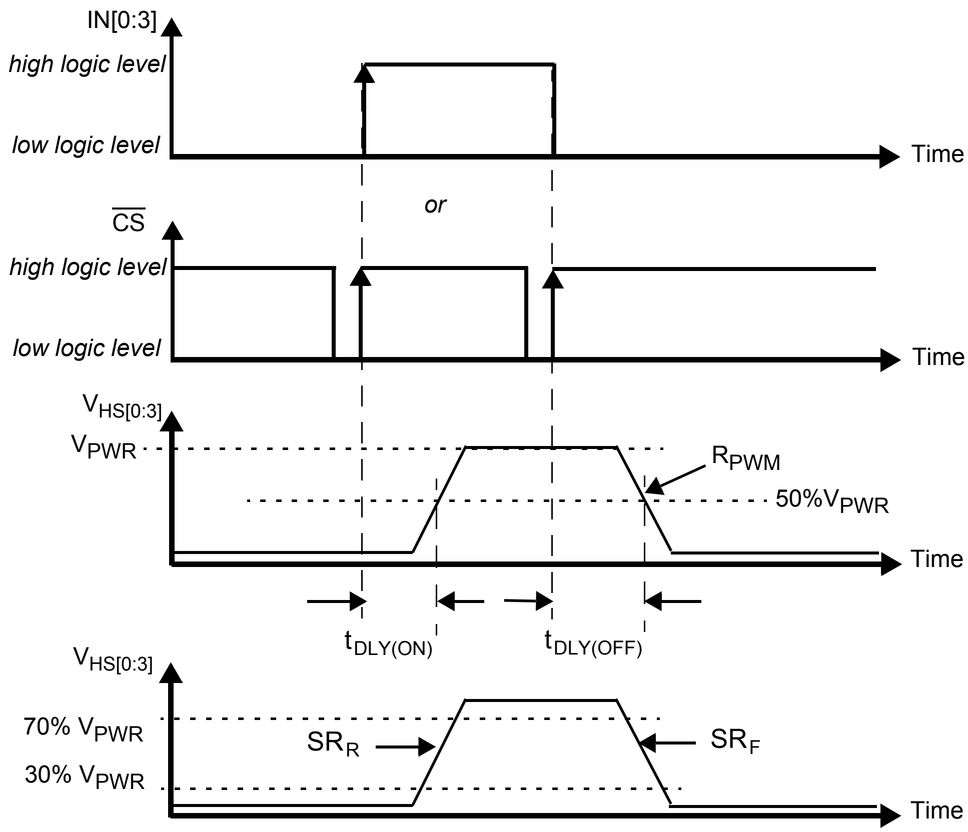


Figure 4. Output Slew Rate and Time Delays

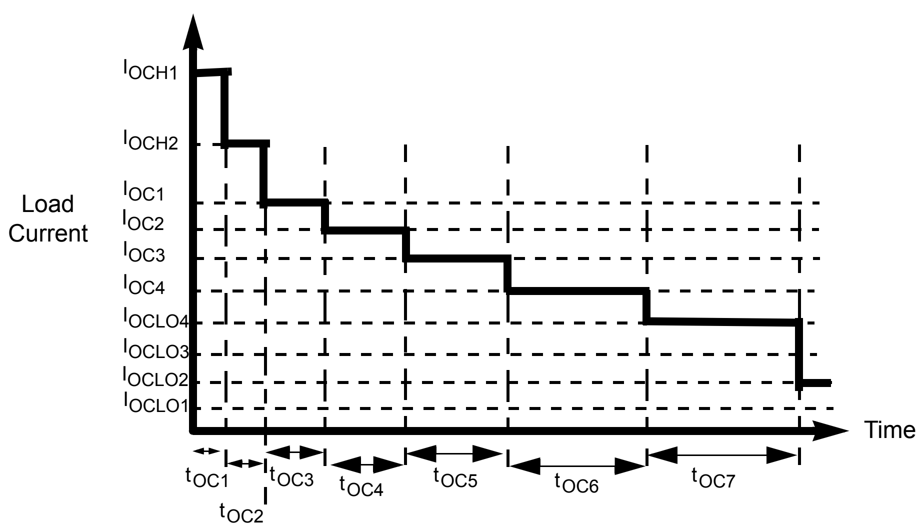


Figure 5. Overcurrent Shutdown Protection

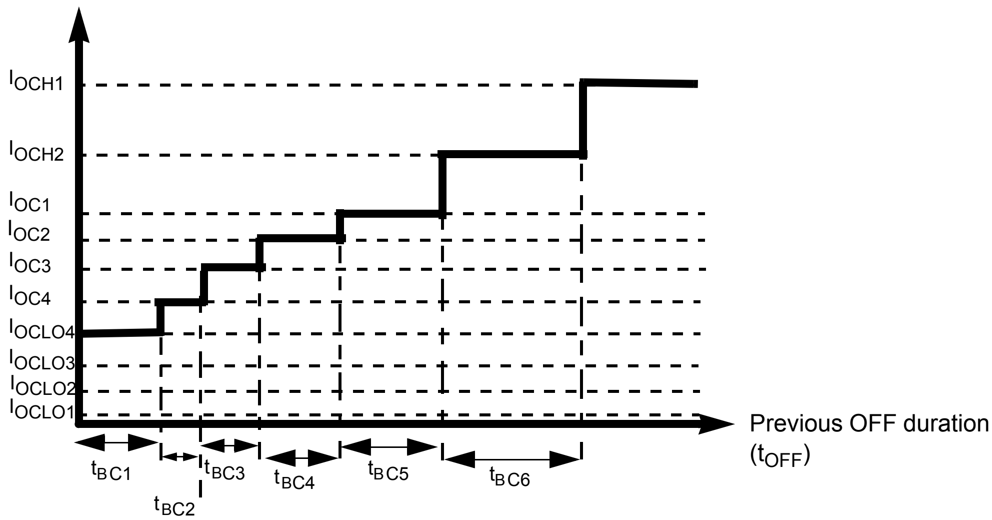


Figure 6. Bulb Cooling Management

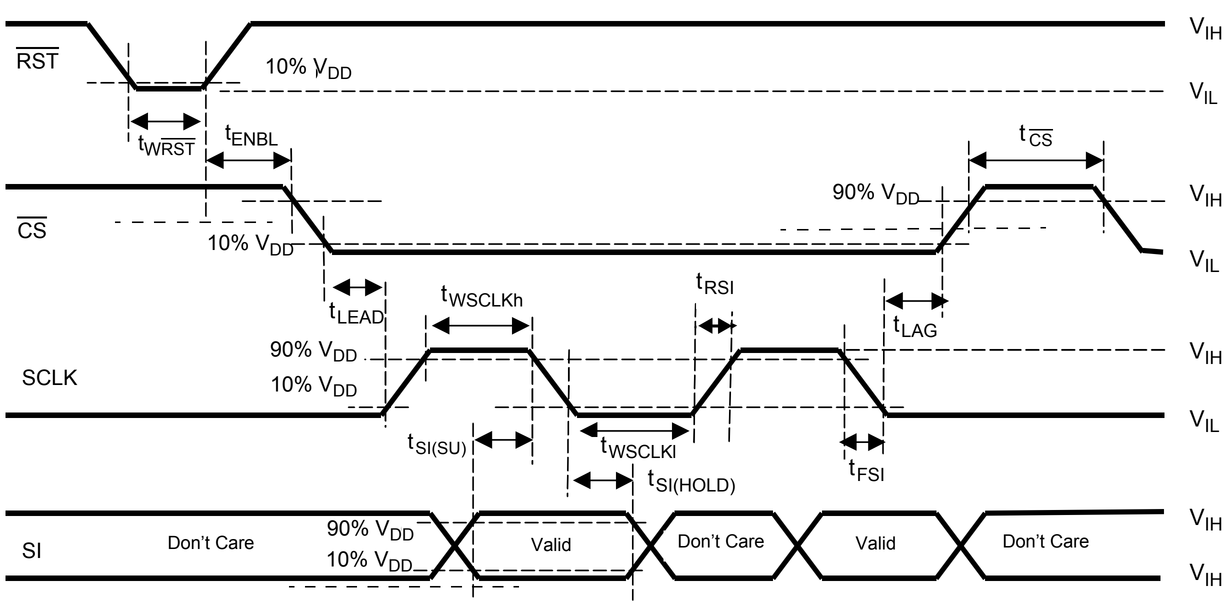


Figure 7. Input Timing Switching Characteristics

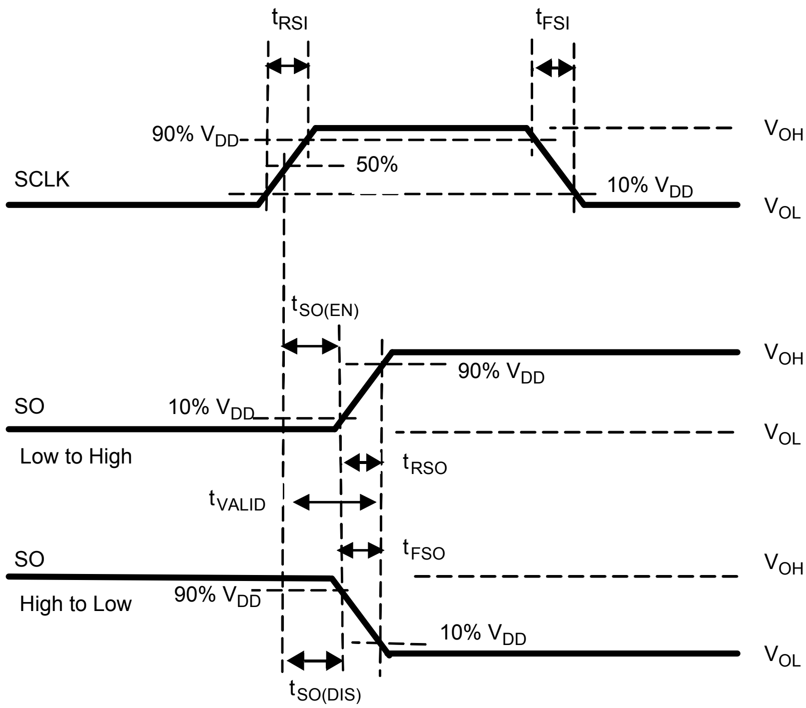


Figure 8. SCLK Waveform and Valid SO Data Delay Time

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 10XS3412 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(ON)}$ MOSFETs (dual 10 mΩ, dual 12 mΩ) can control four separate 55 W / 28 W bulbs and/or Xenon modules.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew-rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 10XS3412 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide functionality of the outputs in case of MCU damage.

FUNCTIONAL PIN DESCRIPTION

OUTPUT CURRENT MONITORING (CSNS)

The Current Sense pin provides a current proportional to the designated HS0:HS3 output or a voltage proportional to the temperature on the GND flag. That current is fed into a ground-referenced resistor (4.7 kΩ typical) and its voltage is monitored by an MCU's A/D. The output type is selected via the SPI. This pin can be tri-stated through the SPI.

DIRECT INPUTS (IN0, IN1, IN2, IN3)

Each IN input wakes the device. The IN0:IN3 high side input pins are also used to directly control HS0:HS3 high side output pins. In case of the outputs are controlled by PWM module, the external PWM clock is applied to IN0 pin. These pins are to be driven with CMOS levels, and they have a passive internal pull-down, R_{DWN}.

FAULT STATUS ($\overline{FS}$)

This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. If a device fault condition is detected, this pin is active LOW. Specific device diagnostics and faults are reported via the SPI SO pin.

WAKE

The wake input wakes the device. An internal clamp protects this pin from high damaging voltages with a series resistor (10 kΩ typ). This input has a passive internal pull-down, R_{DWN}.

RESET ($\overline{RST}$)

The reset input wakes the device. This is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin has a passive internal pull-down, R_{DWN}.

CHIP SELECT ($\overline{CS}$)

The $\overline{CS}$ pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 10XS3412 latches in data from the Input Shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an active internal pull-up from V_{DD}, I_{UP}.

SERIAL CLOCK (SCLK)

The SCLK pin clocks the internal shift registers of the 10XS3412 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic low state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an active internal pull-down. When $\overline{CS}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 9, page 26). SCLK input has an active internal pull-down, I_{DWN}.

SERIAL INPUT (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 (MSB) to D0 (LSB). The internal registers of the 10XS3412 are configured and controlled using a 5-bit addressing scheme described in Table 10. Register addressing and configuration are described in Table 11. The SI input has an active internal pull-down, I_{DWN}.

DIGITAL DRAIN VOLTAGE (VDD)

This pin is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost (V_{DD} Failure), the device goes to Fail Safe mode.

GROUND (GND)

These pins are the ground for the device.

POSITIVE POWER SUPPLY (VPWR)

This pin connects to the positive power supply and is the source of operational power for the device. The VPWR contact is the backside surface mount tab of the package.

SERIAL OUTPUT (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the $\overline{CS}$ pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, the state of the key inputs, etc. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. SO reporting descriptions are provided in Table 23.

HIGH SIDE OUTPUTS (HS3, HS1, HS0, HS2)

Protected 10 mΩ and 12 mΩ high side power outputs to the load.

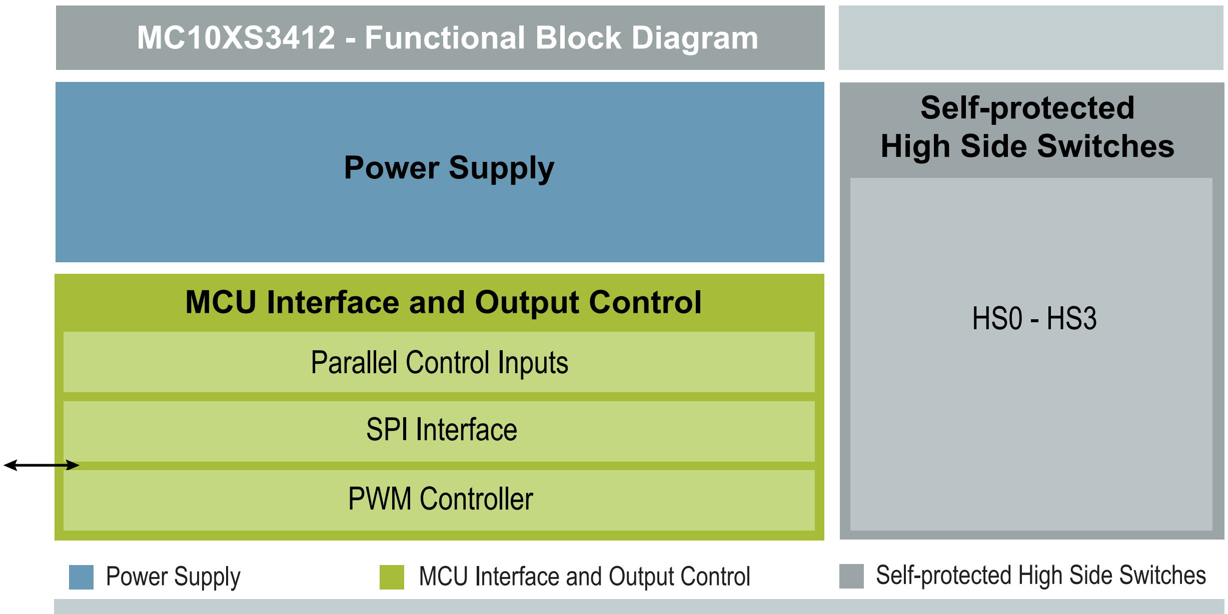
FAIL SAFE INPUT (FSI)

This pin incorporates an active internal pull-up current source from internal supply (V_{REG}). This enables the watchdog timeout feature.

When the FSI pin is opened, the watchdog circuit is enabled. After a Watchdog timeout occurs, the output states depends on IN[0:3].

When the FSI pin is connected to GND, the watchdog circuit is disabled. The output states depends on IN[0:3] in case of V_{DD} Failure condition, in case V_{DD} failure detection is activated (VDD_FAIL_en bit sets to logic [1]).

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



POWER SUPPLY

The 10XS3412 is designed to operate from 4.0 V to 28 V on the VPWR pin. Characteristics are provided from 6.0 V to 20 V for the device. The VPWR pin supplies power to internal regulator, analog, and logic circuit blocks. The V_{DD} supply is used for Serial Peripheral Interface (SPI) communication in order to configure and diagnose the device. This IC architecture provides a low quiescent current Sleep mode. Applying V_{PWR} and V_{DD} to the device will place the device in the Normal mode. The device will transit to Fail-safe mode in case of failures on the SPI or/and on V_{DD} voltage.

HIGH SIDE SWITCHES: HS0 – HS3

These pins are the high side outputs controlling automotive lamps located for the front of vehicle, such as 65 W/55 W bulbs and Xenon-HID modules. Those N-channel MOSFETs with 10 mΩ & 12 mΩ $R_{DS(ON)}$ are self-protected and present extended diagnostics in order to detect bulb outage and short-circuit fault condition. The HS output is actively clamped during turn off of inductive loads and inductive battery line. When driving DC motor or Solenoid loads demanding multiple switching, an external recirculation device must be used to maintain the device in its Safe Operating Area.

MCU INTERFACE AND OUTPUT CONTROL

In Normal mode, each bulb is controlled directly from the MCU through SPI. A pulse width modulation control module allows improvement of lamp lifetime with bulb power regulation (PWM frequency range from 100 to 400 Hz) and addressing the dimming application (day running light). An analog feedback output provides a current proportional to the load current or the temperature of the board. The SPI is used to configure and to read the diagnostic status (faults) of high side outputs. The reported fault conditions are: open load, short circuit to battery, short circuit to ground (overcurrent and severe short-circuit), thermal shutdown, and under/overvoltage. Thanks to accurate and configurable overcurrent detection circuitry and wire-harness optimization, the vehicle is lighter.

In Fail-safe mode, each lamp is controlled with dedicated parallel input pins. The device is configured in default mode.