



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Quad High Side Switch (Dual 10 mOhm, Dual 25 mOhm)

The 10XSC425 is one in a family of devices designed for low-voltage lighting or factory automation applications. Its four low  $R_{DS(ON)}$  MOSFETs (dual 10 m $\Omega$ /dual 25 m $\Omega$ ) can control four separate 55 W / 28 W bulbs, and/or Xenon modules, and/or LEDs, and/or DC low voltage motors.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew-rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 10XSC425 allows the user to program via the SPI the fault current trip levels and duration of acceptable inrush. The device has fail-safe mode to provide fail-safe functionality of the outputs in case of MCU damaged.

This device is powered by SMARTMOS technology.

## Features

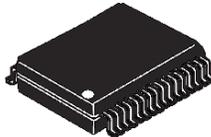
- Four protected 10 m $\Omega$  and 25 m $\Omega$  high side switches (at 25 °C)
- Operating voltage range of 6.0 to 20 V with sleep current < 5.0  $\mu$ A, extended mode from 4.0 to 28 V
- 8.0 MHz 16-bit 3.3 V and 5.0 V SPI control and status reporting with daisy chain capability
- PWM module using external clock or calibratable internal oscillator with programmable output delay management
- Smart overcurrent shutdown, severe short-circuit, overtemperature protections with time limited autoretry, and fail-safe mode, in case of MCU damage
- Output OFF or ON open-load detection compliant to bulbs or leds and short to battery detection.
- Analog current feedback with selectable ratio and board temperature feedback

10XSC425

---

HIGH SIDE SWITCH

---



EK SUFFIX (PB-FREE)  
98ASA00368D  
32-PIN SOICW-EP

## Applications

- Low-voltage industrial lighting
- Halogen lamps
- Incandescent bulbs
- Light-emitting diodes (LEDs)
- HID Xenon ballasts
- Low voltage factory automation

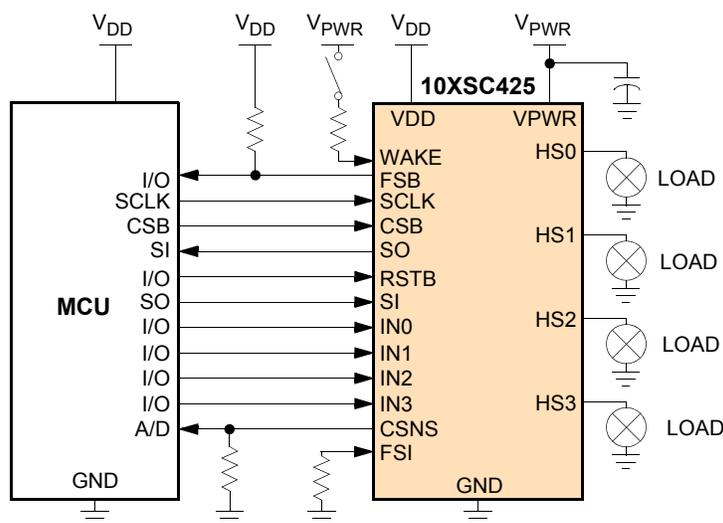


Figure 1. 10XSC425 Simplified Application Diagram

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.



# Table of Contents

1	Orderable Parts	5
2	Internal Block Diagram	6
3	Pin Connections	7
3.1	Pinout Diagram	7
3.2	Pin Definitions	7
4	Electrical Characteristics	9
4.1	Maximum Ratings	9
4.2	Static Electrical Characteristics	11
4.3	Dynamic Electrical Characteristics	18
4.4	Timing Diagrams	25
5	Functional Description	28
5.1	Introduction	28
5.2	Functional Pin Description	28
5.2.1	Output Current Monitoring (CSNS)	28
5.2.2	Direct Inputs (IN0, IN1, IN2, IN3)	28
5.2.3	Fault Status (FSB)	28
5.2.4	WAKE	28
5.2.5	Reset (RSTB)	28
5.2.6	Chip Select (CSB)	28
5.2.7	Serial Clock (SCLK)	29
5.2.8	Serial Input (SI)	29
5.2.9	Digital Drain Voltage (VDD)	29
5.2.10	Ground (GND)	29
5.2.11	Positive Power Supply (VPWR)	29
5.2.12	Serial Output (SO)	29
5.2.13	High Side Outputs (HS3, HS1, HS0, HS2)	29
5.2.14	Fail-safe Input (FSI)	29
5.3	Functional Internal Block Description	30
5.3.1	Power Supply	30
5.3.2	High Side Switches (HS0–HS3)	30
5.3.3	MCU Interface and Output Control	30
6	Functional Device Operation	31
6.1	SPI Protocol Description	31
6.2	Operational Modes	31
6.2.1	Sleep Mode	32
6.2.2	Normal Mode	33
6.2.3	Fail-safe Mode	34
6.2.4	Watchdog	34
6.2.5	Normal and Fail-safe Mode Transitions	35
6.2.6	Fault Mode	35
6.2.7	Start-up Sequence	35
6.3	Protection and Diagnostic Features	36
6.3.1	Protections	36
6.3.2	Auto-retry	38
6.3.3	Diagnostic	38
6.3.4	Analog Current Recopy and Temperature Feedbacks	39
6.3.5	Active Clamp ON VPWR	39

6.3.6	Reverse Battery ON VPWR	39
6.3.7	Ground Disconnect Protection	40
6.3.8	Loss of Supply Lines	40
6.3.9	EMC PERFORMANCES	40
6.4	LOGIC COMMANDS AND REGISTERS	40
6.4.1	Serial Input Communication	40
6.4.2	Device Register Addressing	42
6.4.3	Serial Output Communication (Device Status Return Data)	46
6.4.4	Serial Output Bit Assignment	47
7	Typical Applications	50
7.1	Introduction	50
8	Packaging	51
8.1	Soldering Information	51
8.2	Marking Information	51
8.3	Package Mechanical Dimensions	51
9	Revision History	55

# 1 Orderable Parts

This section describes the part numbers available to be purchased along with their differences.

**Table 1. Orderable Part Variations**

Part Number <sup>(1)</sup>	Temperature (T <sub>A</sub> )	Package
<b>Quad version</b>		
MC10XSC425EK	-40 to 125°C	32 pin SOIC exposed pad

Notes

1. To Order parts in Tape & Real, add the R2 suffix to the part number.

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers: 07XS and 17XS.

## 2 Internal Block Diagram

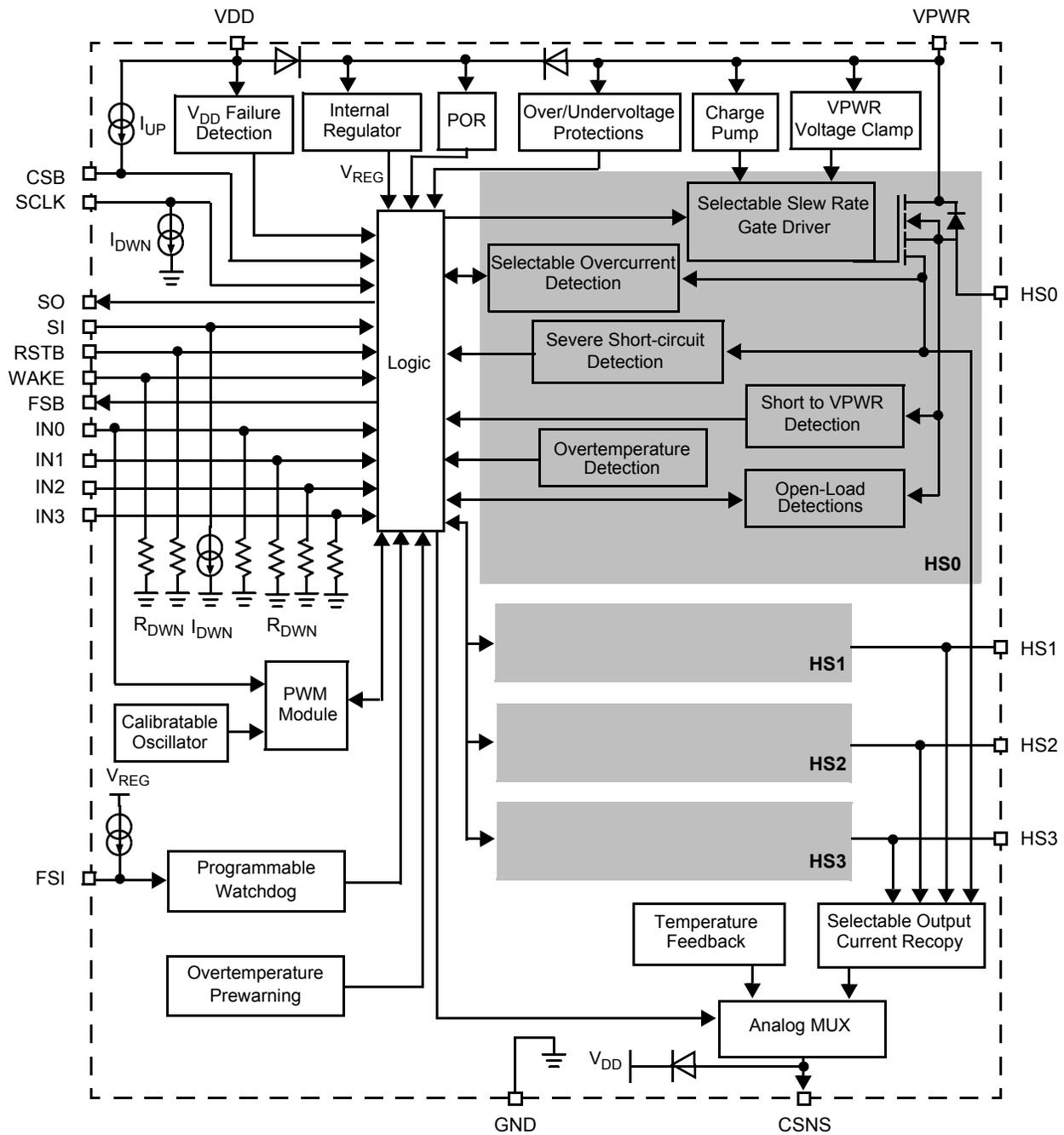


Figure 2. 10XSC425 Simplified Internal Block Diagram

## 3 Pin Connections

### 3.1 Pinout Diagram

Transparent Top View of Package

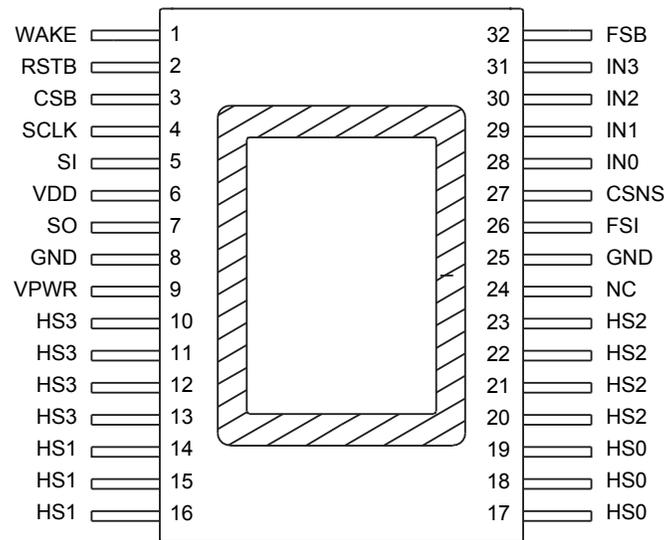


Figure 3. 10XSC425 Pin Connections

### 3.2 Pin Definitions

Table 2. 10XSC425 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page [28](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	WAKE	Input	Wake	This input pin controls the device mode.
2	RSTB	Input	Reset	This input pin is used to initialize the device configuration and fault registers, as well as drive the device into a low-current Sleep mode.
3	CSB	Input	Chip Select (Active Low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
4	SCLK	Input	Serial Clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.
5	SI	Input	Serial Input	This pin is a command data input pin connected to the SPI Serial Data Output of the MCU or to the SO pin of the previous device of a daisy-chain of devices.
6	VDD	Power	Digital Drain Voltage	This pin is an external voltage input pin used to supply power interfaces to the SPI bus.
7	SO	Output	Serial Output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device of a daisy-chain of devices.

**Table 2. 10XSC425 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Pin Description section beginning on page [28](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
8, 25	GND	Ground	Ground	These pins, internally shorted, are the ground for the logic and analog circuitry of the device. These ground pins must be also shorted in the board.
9, 33	VPWR	Power	Positive Power Supply	This pin connects to the positive power supply and is the source of operational power for the device. Pins 9 and 33 must be externally connected.
10, 11, 12, 13	HS3	Output	High Side Output	Protected 25 mΩ high side power output pins to the load.
14, 15, 16	HS1	Output	High Side Output	Protected 10 mΩ high side power output pins to the load.
17, 18, 19	HS0	Output	High Side Output	Protected 10 mΩ high side power output pins to the load.
20, 21, 22, 23	HS2	Output	High Side Output	Protected 25 mΩ high side power output pins to the load.
24	NC	N/A	No Connect	This pin may not be connected.
26	FSI	Input	Fail-safe Input	This input enables the watchdog timeout feature.
27	CSNS	Output	Output Current Monitoring	This pin reports an analog value proportional to the designated HS[0:3] output current or the temperature of the GND flag (pin 14). It is used externally to generate a ground-referenced voltage for the microcontroller (MCU). Current recopy and temperature feedback is SPI programmable.
28 29 30 31	IN0 IN1 IN2 IN3	Input	Direct Inputs	Each direct input controls the device mode. The IN[0:3] high side input pins are used to directly control HS0:HS3 high side output pins. The PWM frequency can be generated from IN0 pin to PWM module in case of external clock is set.
32	FSB	Output	Fault Status (Active Low)	This pin is an open drain configured output requiring an external pull-up resistor to VDD for fault reporting.

## 4 Electrical Characteristics

### 4.1 Maximum Ratings

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
<b>ELECTRICAL RATINGS</b>				
$V_{PWR(SS)}$	VPWR Supply Voltage Range <ul style="list-style-type: none"> <li>• Load Dump at 25 °C (400 ms)</li> <li>• Maximum Operating Voltage</li> <li>• Reverse Battery</li> </ul>	41 28 -18	V	
$V_{DD}$	VDD Supply Voltage Range	-0.3 to 5.5	V	
$V_{DIG}$	Input / Output Voltage	-0.3 to 5.5	V	(5)
$V_{SO}$	SO and CSNS Output Voltage	-0.3 to $V_{DD}+0.3$	V	
$I_{DIG}$	Digital Input/Output Current in Clamp Mode	100	μA	
$I_{CL(WAKE)}$	WAKE Input Clamp Current	2.5	mA	
$I_{CL(CSNS)}$	CSNS Input Clamp Current	2.5	mA	
$V_{HS[0:3]}$	HS [0:3] Voltage <ul style="list-style-type: none"> <li>• Positive</li> <li>• Negative</li> </ul>	41 -24	V	
$V_{PWR} - V_{HS}$	High Side Breakdown Voltage	47	V	
$I_{HS[0:3]}$	Output Current	6.0	A	(2)
$E_{CL[0:1]}$	HS[0,1] Output Clamp Energy using single pulse method	60	mJ	(3)
$E_{CL[2:3]}$	HS[2,3] Output Clamp Energy using single pulse method	25	mJ	(3)
$V_{ESD1}$ $V_{ESD2}$ $V_{ESD3}$ $V_{ESD4}$	ESD Voltage ( $V_{PWR}$ Pins 9 and 33 must be externally connected.) <ul style="list-style-type: none"> <li>• Human Body Model (HBM) for HS[0:3], VPWR and GND</li> <li>• Human Body Model (HBM) for other pins</li> <li>• Charge Device Model (CDM)               <ul style="list-style-type: none"> <li>Corner Pins (1, 13, 19, 21)</li> <li>All Other Pins (2-12, 14-18, 20, 22-24)</li> </ul> </li> </ul>	±8000 ±2000 ±750 ±500	V	(4)

**Notes**

- Continuous high side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
- Active clamp energy using single-pulse method ( $L = 2.0$  mH,  $R_L = 0 \Omega$ ,  $V_{PWR} = 14$  V,  $T_J = 150$  °C initial).
- Pins 9 and 33 must be externally connected. ESD testing is performed in accordance with the Human Body Model (HBM) ( $C_{ZAP} = 100$  pF,  $R_{ZAP} = 1500 \Omega$ ), the Machine Model (MM) ( $C_{ZAP} = 200$  pF,  $R_{ZAP} = 0 \Omega$ ), and the Charge Device Model (CDM), Robotic ( $C_{ZAP} = 4.0$  pF).
- Input / Output pins are: IN[0:3], RSTB, FSI, SI, SCLK, CSB, and FSB

**Table 3. Maximum Ratings (continued)**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
--------	---------	-------	------	-------

**THERMAL RATINGS**

T <sub>A</sub> T <sub>J</sub>	Operating Temperature		°C	(5)
	• Ambient	-40 to 125		
	• Junction	-40 to 150		
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C	

**THERMAL RESISTANCE**

R <sub>θJC</sub> R <sub>θJA</sub>	Thermal Resistance		°C/W	(7)
	• Junction to Case	<2.5		
	• Junction to Ambient	30		
T <sub>SOLDER</sub>	Peak Pin Reflow Temperature During Solder Mounting	260	°C	(8)

Notes

6. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
7. Device mounted on a 2s2p test board per JEDEC JESD51-2. 15 °C/W of R<sub>θJA</sub> can be reached in a real application case (4 layers board).
8. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

## 4.2 Static Electrical Characteristics

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>POWER INPUTS</b>						
$V_{PWR}$	Battery Supply Voltage Range <ul style="list-style-type: none"> <li>Fully Operational</li> <li>Extended mode</li> </ul>	6.0 4.0	– –	20 28	V	(9)
$V_{PWR}$ (CLAMP)	Battery Clamp Voltage	41	47	53	V	(10)
$I_{PWR(ON)}$	$V_{PWR}$ Operating Supply Current <ul style="list-style-type: none"> <li>Outputs commanded ON, HS[0:3] open, IN[0:3] &gt; <math>V_{IH}</math></li> </ul>	–	6.5	20	mA	
$I_{PWR(SBY)}$	$V_{PWR}$ Supply Current <ul style="list-style-type: none"> <li>Outputs commanded OFF, OFF Open-load Detection Disabled, HS[0:3] shorted to the ground with <math>V_{DD} = 5.5\text{ V}</math></li> <li>WAKE &gt; <math>V_{IH}</math> or RSTB &gt; <math>V_{IH}</math> and IN[0:3] &lt; <math>V_{IL}</math></li> </ul>	–	6.5	7.5	mA	
$I_{PWR(SLEEP)}$	Sleep State Supply Current <ul style="list-style-type: none"> <li><math>V_{PWR} = 12\text{ V}</math>, RSTB = WAKE = IN[0:3] &lt; <math>V_{IL}</math>, HS[0:3] shorted to ground</li> <li><math>T_A = 25\text{ }^\circ\text{C}</math></li> <li><math>T_A = 85\text{ }^\circ\text{C}</math></li> </ul>	– –	1.0 –	5.0 30	$\mu\text{A}$	
$V_{DD(ON)}$	$V_{DD}$ Supply Voltage	3.0	–	5.5	V	
$I_{DD(ON)}$	$V_{DD}$ Supply Current at $V_{DD} = 5.5\text{ V}$ <ul style="list-style-type: none"> <li>No SPI Communication</li> <li>8.0 MHz SPI Communication</li> </ul>	– –	1.6 5.0	2.2 –	mA	(11)
$I_{DD(SLEEP)}$	$V_{DD}$ Sleep State Current at $V_{DD} = 5.5\text{ V}$	–	–	5.0	$\mu\text{A}$	
$V_{PWR(OV)}$	Overvoltage Shutdown Threshold	28	32	36	V	
$V_{PWR}$ (OVHYS)	Overvoltage Shutdown Hysteresis	0.2	0.8	1.5	V	
$V_{PWR(UV)}$	Undervoltage Shutdown Threshold	3.3	3.9	4.3	V	(12)
$V_{SUPPLY}$ (POR)	$V_{PWR}$ and $V_{DD}$ Power on Reset Threshold	0.5	–	0.9	$V_{PWR}$ (UV)	
$V_{PWR(UV)}$ _UP	Recovery Undervoltage Threshold	3.4	4.1	4.5	V	
$V_{DD(FAIL)}$	$V_{DD}$ Supply Failure Threshold ( for $V_{PWR} > V_{PWR(UV)}$ )	2.2	2.5	2.8	V	

**Notes**

- In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
- Measured with the outputs open.
- Typical value guaranteed per design.
- Output will automatically recover with time limited autoretry to instructed state when  $V_{PWR}$  voltage is restored to normal as long as the  $V_{PWR}$  degradation level did not go below the undervoltage power-ON reset threshold. This applies to all internal device logic that is supplied by  $V_{PWR}$  and assumes that the external  $V_{DD}$  supply is within specification.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>OUTPUTS HS0 TO HS3</b>						
$R_{DS\_01(ON)}$	HS[0,1] Output Drain-to-Source ON Resistance ( $I_{HS} = 5.0\text{ A}$ , $T_A = 25\text{ }^\circ\text{C}$ ) <ul style="list-style-type: none"> <li>• <math>V_{PWR} = 4.5\text{ V}</math></li> <li>• <math>V_{PWR} = 6.0\text{ V}</math></li> <li>• <math>V_{PWR} = 10\text{ V}</math></li> <li>• <math>V_{PWR} = 13\text{ V}</math></li> </ul>	–	–	36	mΩ	
$R_{DS\_01(ON)}$	HS[0,1] Output Drain-to-Source ON Resistance ( $I_{HS} = 5.0\text{ A}$ , $T_A = 150\text{ }^\circ\text{C}$ ) <ul style="list-style-type: none"> <li>• <math>V_{PWR} = 4.5\text{ V}</math></li> <li>• <math>V_{PWR} = 6.0\text{ V}</math></li> <li>• <math>V_{PWR} = 10\text{ V}</math></li> <li>• <math>V_{PWR} = 13\text{ V}</math></li> </ul>	–	–	62	mΩ	
$R_{SD\_01(ON)}$	HS[0,1] Output Source-to-Drain ON Resistance ( $I_{HS} = -5.0\text{ A}$ , $V_{PWR} = -18\text{ V}$ ) <ul style="list-style-type: none"> <li>• <math>T_A = 25\text{ }^\circ\text{C}</math></li> <li>• <math>T_A = 150\text{ }^\circ\text{C}</math></li> </ul>	–	–	15	mΩ	(13)
$R_{DS\_23(ON)}$	HS[2,3] Output Drain-to-Source ON Resistance ( $I_{HS} = 5.0\text{ A}$ , $T_A = 25\text{ }^\circ\text{C}$ ) <ul style="list-style-type: none"> <li>• <math>V_{PWR} = 4.5\text{ V}</math></li> <li>• <math>V_{PWR} = 6.0\text{ V}</math></li> <li>• <math>V_{PWR} = 10\text{ V}</math></li> <li>• <math>V_{PWR} = 13\text{ V}</math></li> </ul>	–	–	90	mΩ	
$R_{DS\_23(ON)}$	HS[2,3] Output Drain-to-Source ON Resistance ( $I_{HS} = 5.0\text{ A}$ , $T_A = 150\text{ }^\circ\text{C}$ ) <ul style="list-style-type: none"> <li>• <math>V_{PWR} = 4.5\text{ V}</math></li> <li>• <math>V_{PWR} = 6.0\text{ V}</math></li> <li>• <math>V_{PWR} = 10\text{ V}</math></li> <li>• <math>V_{PWR} = 13\text{ V}</math></li> </ul>	–	–	153	mΩ	
$R_{SD\_23(ON)}$	HS[2,3] Output Source-to-Drain ON Resistance ( $I_{HS} = -5.0\text{ A}$ , $V_{PWR} = -18\text{ V}$ ) <ul style="list-style-type: none"> <li>• <math>T_A = 25\text{ }^\circ\text{C}</math></li> <li>• <math>T_A = 150\text{ }^\circ\text{C}</math></li> </ul>	–	–	37.5	mΩ	(13)
$R_{SHORT\_01}$	HS[0,1] Maximum Severe Short-circuit Impedance Detection	28	67	100	mΩ	(14)
$R_{SHORT\_23}$	HS[2,3] Maximum Severe Short-circuit Impedance Detection	70	160	200	mΩ	(14)
$I_{OFF}$	HS[0-3] Output Leakage Current in Off-state <ul style="list-style-type: none"> <li>• in sleep mode</li> <li>• in normal mode (<math>OS\_dis = 1</math> and <math>OLOFF\_dis = 1</math>)</li> </ul>	–	–	5.0	μA	
		–	–	30		

**Notes**

13. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity  $V_{PWR}$ .
14. Short-circuit impedance calculated from HS[0:3] to GND pins. Value guaranteed per design.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{\text{PWR}} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>OUTPUTS HS0 TO HS3 (CONTINUED)</b>						
OCHI1_0 OCHI2_0 OC1_0 OC2_0 OC3_0 OC4_0 OCLO4_0 OCLO3_0 OCLO2_0 OCLO1_0  OCHI1_1 OCHI2_1 OC1_1 OC2_1 OC3_1 OC4_1 OCLO4_1 OCLO3_1 OCLO2_1 OCLO1_1	HS[0,1] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{\text{HS}[0:3]} \leq 20\text{ V}$ ) • 28W bit = 0  • 28W bit = 1	77.6 46.4 43.6 40.2 31.6 26.2 19.2 12.1 10.3 6.2  38.8 23.2 21.8 18.6 15.8 13.1 4.6 4.6 4.6 2.9	101.6 62 55.6 48.8 40.4 33.2 24.3 15.3 13.1 8.3  50.8 31 27.8 23.8 20.2 16.6 6.3 6.3 6.3 4.1	125.6 77.6 67.6 57.4 49.2 40.2 29.4 18.4 15.9 10.3  62.8 38.8 33.8 29 24.6 20.1 8.0 8.0 8.0 5.3	A	
CSR0_0 CSR1_0  CSR0_1 CSR1_1	HS[0,1] Current Sense Ratio ( $6.0\text{ V} \leq V_{\text{HS}[0:3]} \leq 20\text{ V}$ , $\text{CSNS} \leq 5.0\text{ V}$ ) • 28W bit = 0 CSNS_ratio bit = 0 CSNS_ratio bit = 1 • 28W bit = 1 CSNS_ratio bit = 0 CSNS_ratio bit = 1	– –  – –	1/9900 1/58500  1/4950 1/29250	– –  – –	–	(15)
CSR0_0_ACC	HS[0,1] Current Sense Ratio ( $C_{\text{SR0}}$ ) Accuracy ( $6.0\text{ V} \leq V_{\text{HS}[0:1]} \leq 20\text{ V}$ ) with 28W bit = 0 At 25 °C and 125 °C • $I_{\text{HS}[0:1]} = 12.5\text{ A}$ • $I_{\text{HS}[0:1]} = 5.0\text{ A}$ • $I_{\text{HS}[0:1]} = 3.0\text{ A}$ • $I_{\text{HS}[0:1]} = 1.5\text{ A}$ At -40 °C • $I_{\text{HS}[0:1]} = 12.5\text{ A}$ • $I_{\text{HS}[0:1]} = 5.0\text{ A}$ • $I_{\text{HS}[0:1]} = 3.0\text{ A}$ • $I_{\text{HS}[0:1]} = 1.5\text{ A}$	–18 –21 –22 –25  –23 –26 –30 –35	– – – –  – – – –	18 21 22 25  23 26 30 35	%	

**Notes**

15. Current sense ratio =  $I_{\text{CSNS}} / I_{\text{HS}[0:3]}$

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>OUTPUTS HS0 TO HS3 (CONTINUED)</b>						
$C_{SR0\_0\_ACC}$ (CAL)	HS[0,1] Current Recopy Accuracy with one calibration point ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 0 • $I_{HS[0:1]} = 5.0\text{ A}$	-5.0	-	5.0	%	(16)
$\Delta(C_{SR0\_0})/\Delta(T)$	HS[0,1] $C_{SR0}$ Current Recopy Temperature Drift ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 0 • $I_{HS[0:1]} = 5.0\text{ A}$	-	-	0.04	%/ $^\circ\text{C}$	(17)
$C_{SR0\_1\_ACC}$	HS[0,1] Current Sense Ratio ( $C_{SR0}$ ) Accuracy ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 1 At $25\text{ }^\circ\text{C}$ and $125\text{ }^\circ\text{C}$ • $I_{HS[0:1]} = 3.0\text{ A}$ • $I_{HS[0:1]} = 1.5\text{ A}$ At $-40\text{ }^\circ\text{C}$ • $I_{HS[0:1]} = 3.0\text{ A}$ • $I_{HS[0:1]} = 1.5\text{ A}$	-22 -25 -30 -35	-	22 25 30 35	%	
$C_{SR0\_1\_ACC}$ (CAL)	HS[0,1] Current Recopy Accuracy with one calibration point ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 1 • $I_{HS[0:1]} = 3.0\text{ A}$	-5.0	-	5.0	%	(16)
$C_{SR1\_0\_ACC}$	HS[0,1] Current Sense Ratio ( $C_{SR1}$ ) Accuracy ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 0 At $25\text{ }^\circ\text{C}$ and $125\text{ }^\circ\text{C}$ • $I_{HS[0:1]} = 12.5\text{ A}$ • $I_{HS[0:1]} = 75\text{ A}$ At $-40\text{ }^\circ\text{C}$ • $I_{HS[0:1]} = 12.5\text{ A}$ • $I_{HS[0:1]} = 75\text{ A}$	-20 -18 -30 -25	-	20 18 30 25	%	
$C_{SR1\_0\_ACC}$ (CAL)	HS[0,1] Current Recopy Accuracy with one calibration point ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 0 • $I_{HS[0:1]} = 12.5\text{ A}$	-5.0	-	5.0	%	(16)
$C_{SR1\_1\_ACC}$	HS[0,1] Current Sense Ratio ( $C_{SR1}$ ) Accuracy ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 1 At $25\text{ }^\circ\text{C}$ and $125\text{ }^\circ\text{C}$ • $I_{HS[0:1]} = 12.5\text{ A}$ • $I_{HS[0:1]} = 37.5\text{ A}$ at $-40\text{ }^\circ\text{C}$ • $I_{HS[0:1]} = 12.5\text{ A}$ • $I_{HS[0:1]} = 37.5\text{ A}$	-22 -20 -27 -25	-	22 20 27 25	%	
$C_{SR1\_1\_ACC}$ (CAL)	HS[0,1] Current Recopy Accuracy with one calibration point ( $6.0\text{ V} \leq V_{HS[0:1]} \leq 20\text{ V}$ ) with 28W bit = 1 • $I_{HS[0:1]} = 12.5\text{ A}$	-5.0	-	5.0	%	(16)

Notes

- Based on statistical analysis. It is not production tested.
- Based on statistical data:  $\Delta(C_{SR0})/\Delta(T) = \{(\text{measured } I_{CSNS} \text{ at } T_1 - \text{measured } I_{CSNS} \text{ at } T_2) / \text{measured } I_{CSNS} \text{ at room}\} / \{T_1 - T_2\}$ .  
Not production tested.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>OUTPUTS HS0 TO HS3 (CONTINUED)</b>						
$V_{CL(CSNS)}$	Current Sense Clamp Voltage • CSNS Open; $I_{HS[0:3]} = 5.0\text{ A}$ with $C_{SR0}$ ratio	$V_{DD}+0.25$	–	$V_{DD}+1.0$	V	
$I_{OLD(OFF)}$	OFF OpenLoad Detection Source Current	30	–	100	$\mu\text{A}$	(18)
$V_{OLD(THRES)}$	OFF OpenLoad Fault Detection Voltage Threshold	2.0	3.0	4.0	V	
$I_{OLD(ON\_LED)}$	ON OpenLoad Fault Detection Current Threshold with LED ( $V_{HS[0:3]} = V_{PWR} - 0.75\text{ V}$ )	2.5	5.0	10	mA	
$I_{OLD(ON)}$	ON OpenLoad Fault Detection Current Threshold • HS[0,1] • HS[2,3]	80 55	360 165	660 330	mA	
$V_{OSD(THRES)}$	Output Short to $V_{PWR}$ Detection Voltage Threshold • Output programmed OFF	$V_{PWR}-1.2$	$V_{PWR}-0.8$	$V_{PWR}-0.4$	V	
$V_{CL}$	Output Negative Clamp Voltage • $0.5\text{ A} \leq I_{HS[0:3]} \leq 5.0\text{ A}$ , Output programmed OFF	-22	–	-16	V	
$T_{SD}$	Output Overtemperature Shutdown for $4.5\text{ V} < V_{PWR} < 28\text{ V}$	155	175	195	$^\circ\text{C}$	
OCHI1_1 OCHI2_1 OC1_1 OC2_1 OC3_1 OC4_1 OCLO4_1 OCLO3_1 OCLO2_1 OCLO1_1	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	38.8 23.2 21.8 17.3 14.7 12.2 9.2 5.8 4.6 2.9	50.8 31 27.3 22.9 19.2 15.8 11.9 7.6 6.3 4.1	62.8 38.8 32.8 28.4 23.7 19.4 14.5 9.3 8.0 5.3	A	
$C_{SR0\_x}$ $C_{SR1\_x}$	HS[2,3] Current Sense Ratio ( $6.0\text{ V} \leq V_{HS[2:3]} \leq 20\text{ V}$ , $CSNS \leq 5.0\text{ V}$ ) CSNS_ratio bit = 0 CSNS_ratio bit = 1	– –	1/4670 1/27270	– –	–	(19)

**Notes**

- Output OFF OpenLoad Detection Current is the current required to flow through the load for the purpose of detecting the existence of an OpenLoad condition when the specific output is commanded OFF. Pull-up current is measured for  $V_{HS} = V_{OLD(THRES)}$
- Current sense ratio =  $I_{CSNS} / I_{HS[0:3]}$

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>OUTPUTS HS0 TO HS3 (CONTINUED)</b>						
$C_{SR0\_x\_ACC}$	HS[2,3] Current Sense Ratio ( $C_{SR0}$ ) Accuracy ( $6.0\text{ V} \leq V_{HS[2:3]} \leq 20\text{ V}$ ) with 28W bit = x At 25 °C and 125 °C <ul style="list-style-type: none"> <li>• <math>I_{HS[2:3]} = 6.25\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 2.5\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 1.5\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 0.75\text{ A}</math></li> </ul> At -40 °C <ul style="list-style-type: none"> <li>• <math>I_{HS[2:3]} = 6.25\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 2.5\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 1.5\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 0.75\text{ A}</math></li> </ul>	-18 -21 -22 -25  -23 -26 -30 -35	- - - -  - - - -	18 21 22 25  23 26 30 35	%	
$C_{SR0\_x\_ACC}$ (CAL)	HS[2,3] Current Recopy Accuracy with one calibration point ( $6.0\text{ V} \leq V_{HS[2:3]} \leq 20\text{ V}$ ) <ul style="list-style-type: none"> <li>• <math>I_{HS[2:3]} = 2.5\text{ A}</math></li> </ul>	-5.0	-	5.0	%	(20)
$\Delta(C_{SR0\_x})/\Delta(T)$	HS[2,3] $C_{SR0}$ Current Recopy Temperature Drift ( $6.0\text{ V} \leq V_{HS[2:3]} \leq 20\text{ V}$ ) with 28W bit = 0 <ul style="list-style-type: none"> <li>• <math>I_{HS[2:3]} = 2.5\text{ A}</math></li> </ul>	-	-	0.04	%/°C	(20)
$C_{SR1\_x\_ACC}$	HS[2,3] Current Sense Ratio ( $C_{SR1}$ ) Accuracy ( $6.0\text{ V} \leq V_{HS[2:3]} \leq 20\text{ V}$ ) At 25 °C and 125 °C <ul style="list-style-type: none"> <li>• <math>I_{HS[2:3]} = 6.25\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 18.75\text{ A}</math></li> </ul> At -40 °C <ul style="list-style-type: none"> <li>• <math>I_{HS[2:3]} = 6.25\text{ A}</math></li> <li>• <math>I_{HS[2:3]} = 18.75\text{ A}</math></li> </ul>	-22 -25  -25 -27	- -  - -	+22 +25  +25 +27	%	
$C_{SR1\_x\_ACC}$ (CAL)	HS[2,3] Current Recopy Accuracy with one calibration point ( $6.0\text{ V} \leq V_{HS[2:3]} \leq 20\text{ V}$ ) <ul style="list-style-type: none"> <li>• <math>I_{HS[2:3]} = 6.2\text{ A}</math></li> </ul>	-5.0	-	5.0	%	(20)

**CONTROL INTERFACE**

$V_{IH}$	Input Logic High-voltage	2.0	-	$V_{DD}+0.3$	V	(21)
$V_{IL}$	Input Logic Low-voltage	-0.3	-	0.8	V	(21)
$I_{DWN}$	Input Logic Pull-down Current (SCLK, SI)	5.0	-	20	$\mu\text{A}$	(22)
$I_{UP}$	Input Logic Pull-up Current (CSB)	5.0	-	20	$\mu\text{A}$	(23)
$C_{SO}$	SO, FSB Tri-state Capacitance	-	-	20	pF	(24)

**Notes**

20. Based on statistical analysis. It is not production tested.
21. Upper and lower logic threshold voltage range applies to SI, CSB, SCLK, RSTB, IN[0:3], and WAKE input signals. The WAKE and RSTB signals may be supplied by a derived voltage referenced to  $V_{PWR}$ .
22. Pull-down current is with  $V_{SI} \geq 1.0\text{ V}$  and  $V_{SCLK} \geq 1.0\text{ V}$ .
23. Pull-up current is with  $V_{CSB} \leq 2.0\text{ V}$ . CSB has an active internal pull-up to  $V_{DD}$ .
24. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:3], and WAKE. This parameter is guaranteed by process monitoring but is not production tested.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>CONTROL INTERFACE (CONTINUED)</b>						
$R_{DWN}$	Input Logic Pull-down Resistor (RSTB, WAKE and IN[0:3])	125	250	500	$\text{k}\Omega$	
$C_{IN}$	Input Capacitance	–	4.0	12	$\text{pF}$	(26)
$V_{CL(WAKE)}$	Wake Input Clamp Voltage • $I_{CL(WAKE)} < 2.5\text{ mA}$	18	25	32	$\text{V}$	(25)
$V_{F(WAKE)}$	Wake Input Forward Voltage • $I_{CL(WAKE)} = -2.5\text{ mA}$	-2.0	–	-0.3	$\text{V}$	
$V_{SOH}$	SO High State Output Voltage • $I_{OH} = 1.0\text{ mA}$	$V_{DD}-0.4$	–	–	$\text{V}$	
$V_{SOL}$	SO and FSB Low State Output Voltage • $I_{OL} = -1.0\text{ mA}$	–	–	0.4	$\text{V}$	
$I_{SO(LEAK)}$	SO, CSNS and FSB Tri-state Leakage Current • $\text{CSB} = V_{IH}$ and $0.0\text{ V} \leq V_{SO} \leq V_{DD}$ , or $\text{FSB} = 5.5\text{ V}$ , or $\text{CSNS} = 0.0\text{ V}$	-2.0	0	2.0	$\mu\text{A}$	
RFS	FSI External Pull-down Resistance Watchdog Disabled Watchdog Enabled	– 10	0 Infinite	1.0 –	$\text{k}\Omega$	(27)

Notes

25. The current must be limited by a series resistance when using voltages  $> 7.0\text{ V}$ .
26. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:3], and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
27. In Fail-safe, HS[0:3] depends respectively on ON[0:3]. FSI has an active internal pull-up to  $V_{REG} \cong 3.0\text{ V}$ .

## 4.3 Dynamic Electrical Characteristics

**Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>POWER OUTPUT TIMING HS0 TO HS3</b>						
SR <sub>R00</sub>	Output Rising Medium Slew Rate (medium speed slew rate / SR[1:0] = 00)	300	650	1200	mV/μs	
SR <sub>F00</sub>	Output Falling Medium Slew Rate (medium speed slew rate / SR[1:0] = 00)	300	720	1200	mV/μs	
DS <sub>R_00</sub>	Driver Output Matching Slew Rate (SRR /SRF) • PWR = 14 V at 25 °C and for medium speed slew rate (SR[1:0] = 00) V	0.8	0.9	1.2		
SR <sub>R01</sub>	Output Rising Low Slew Rate (medium speed slew rate / SR[1:0] = 01)	150	330	600	mV/μs	
SR <sub>F01</sub>	Output Falling Low Slew Rate (medium speed slew rate / SR[1:0] = 01)	150	370	600	mV/μs	
SR <sub>R10</sub>	Output Rising Fast Slew Rate (medium speed slew rate / SR[1:0] = 10)	600	1250	2400	mV/μs	
SR <sub>F10</sub>	Output Falling Fast Slew Rate (medium speed slew rate / SR[1:0] = 10)	600	1450	2400	mV/μs	
t <sub>DLY_ON</sub>	HS[0:1] Outputs Turn-ON Delay Times • VPWR = 14 for medium speed slew rate (SR[1:0] = 00) V	40	64	100	μs	(28),(29)
t <sub>DLY_OFF</sub>	HS[0:1] Outputs Turn-OFF Delay Times • VPWR = 14 for medium speed slew rate (SR[1:0] = 00) V	10	32	60	μs	(28),(29)
Δt <sub>RF</sub>	HS[0:1] Driver Output Matching Time (t <sub>DLY(ON)</sub> - t <sub>DLY(OFF)</sub> ) • VPWR = 14 V, f <sub>PWM</sub> = 240 Hz, PWM duty cycle = 50%, at 25 °C for medium speed slew rate (SR[1:0] = 00)	10	32	60	μs	(28),(29)
SR <sub>R00</sub>	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	200	470	800	mV/μs	
SR <sub>F00</sub>	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	200	570	800	mV/μs	
DS <sub>R_00</sub>	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	0.6	0.8	1.0		
SR <sub>R01</sub>	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	100	230	400	mV/μs	
SR <sub>F01</sub>	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	100	300	400	mV/μs	

**Notes**

28. Turn ON delay time measured from rising edge of any signal (IN[0:3] and CSB) that would turn the output ON to  $V_{HS[0:3]} = V_{PWR} / 2$  with  $R_L = 5.0\ \Omega$  resistive load.
29. Turn OFF delay time measured from falling edge of any signal (IN[0:3] and CSB) that would turn the output OFF to  $V_{HS[0:3]} = V_{PWR} / 2$  with  $R_L = 5.0\ \Omega$  resistive load.

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>POWER OUTPUT TIMING HS0 TO HS3 (CONTINUED)</b>						
$SR_{R10}$	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	400	900	1600	mV/ $\mu\text{s}$	
$SR_{F10}$	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	400	1140	1600	mV/ $\mu\text{s}$	
$t_{DLY\_ON}$	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	40	87	160	$\mu\text{s}$	
$t_{DLY\_OFF}$	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	15	36	65	$\mu\text{s}$	
$\Delta t_{RF}$	HS[2,3] Output Overcurrent Detection Levels ( $6.0\text{ V} \leq V_{HS[0:3]} \leq 20\text{ V}$ )	10	51	110	$\mu\text{s}$	
$t_{FAULT}$	Fault Detection Blanking Time	1.0	5.0	20	$\mu\text{s}$	(30)
$t_{DETECT}$	Output Shutdown Delay Time	–	7.0	30	$\mu\text{s}$	(31)
$t_{CNSVAL}$	CSNS Valid Time	–	70	100	$\mu\text{s}$	(32)
$t_{WDTO}$	Watchdog Timeout	217	310	400	ms	(33)
$T_{OLD(LED)}$	ON OpenLoad Fault Cyclic Detection Time with LED	105	150	195	ms	

**Notes**

30. Time necessary to report the fault to FSB pin.
31. Time necessary to switch-off the output in case of OT, or OC, or SC, or UV fault detection (from negative edge of FSB pin to HS voltage = 50% of  $V_{PWR}$ ).
32. Time necessary for CSNS to be within  $\pm 5.0\%$  of the targeted value (from HS voltage = 50% of  $V_{PWR}$  to  $\pm 5.0\%$  of the targeted CSNS value).
33. For FSI open, the Watchdog timeout delay measured from the rising edge of RST, to HS[0,2] output state depend on the corresponding input command.

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{\text{PWR}} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>POWER OUTPUT TIMING HS0 TO HS3 (CONTINUED)</b>						
	HS[0,1] Output Overcurrent Time Step for 28W bit = 0				ms	
$t_{\text{OC1\_00}}$	• OC[1:0] = 00 (slow by default)	4.40	6.30	8.02		
$t_{\text{OC2\_00}}$		1.62	2.32	3.00		
$t_{\text{OC3\_00}}$		2.10	3.00	3.90		
$t_{\text{OC4\_00}}$		2.88	4.12	5.36		
$t_{\text{OC5\_00}}$		4.58	6.56	8.54		
$t_{\text{OC6\_00}}$		10.16	14.52	18.88		
$t_{\text{OC7\_00}}$		73.2	104.6	134.0		
$t_{\text{OC1\_01}}$	• OC[1:0] = 01 (fast)	1.10	1.57	2.00		
$t_{\text{OC2\_01}}$		0.40	0.58	0.75		
$t_{\text{OC3\_01}}$		0.52	0.75	0.98		
$t_{\text{OC4\_01}}$		0.72	1.03	1.34		
$t_{\text{OC5\_01}}$		1.14	1.64	2.13		
$t_{\text{OC6\_01}}$		2.54	3.63	4.72		
$t_{\text{OC7\_01}}$		18.2	26.1	34.0		
$t_{\text{OC1\_10}}$	• OC[1:0] = 10 (medium)	2.20	3.15	4.01		
$t_{\text{OC2\_10}}$		0.81	1.16	1.50		
$t_{\text{OC3\_10}}$		1.05	1.50	1.95		
$t_{\text{OC4\_10}}$		1.44	2.06	2.68		
$t_{\text{OC5\_10}}$		2.29	3.28	4.27		
$t_{\text{OC6\_10}}$		5.08	7.26	9.44		
$t_{\text{OC7\_10}}$		36.6	52.3	68.0		
$t_{\text{OC1\_11}}$	• OC[1:0] = 11 (very slow)	8.8	12.6	16.4		
$t_{\text{OC2\_11}}$		3.2	4.6	21.4		
$t_{\text{OC3\_11}}$		4.2	6.0	7.8		
$t_{\text{OC4\_11}}$		5.7	8.2	10.7		
$t_{\text{OC5\_11}}$		9.1	13.1	17.0		
$t_{\text{OC6\_11}}$		20.3	29.0	37.7		
$t_{\text{OC7\_11}}$		146.4	209.2	272.0		

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{\text{PWR}} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>POWER OUTPUT TIMING HS0 TO HS3 (CONTINUED)</b>						
	HS[0,1] Output Overcurrent Time Step for 28W bit = 1 HS[2,3] Output Overcurrent Time Step				ms	
$t_{\text{OC1\_00}}$	• OC[1:0] = 00 (slow by default)	3.4	4.9	6.4		
$t_{\text{OC2\_00}}$		1.1	1.6	2.1		
$t_{\text{OC3\_00}}$		1.4	2.1	2.8		
$t_{\text{OC4\_00}}$		2.0	2.9	3.8		
$t_{\text{OC5\_00}}$		3.4	4.9	6.4		
$t_{\text{OC6\_00}}$		8.5	12.2	15.9		
$t_{\text{OC7\_00}}$		62.4	89.2	116.0		
$t_{\text{OC1\_01}}$	• OC[1:0] = 01 (fast)	0.86	1.24	1.61		
$t_{\text{OC2\_01}}$		0.28	0.40	0.52		
$t_{\text{OC3\_01}}$		0.36	0.52	0.68		
$t_{\text{OC4\_01}}$		0.51	0.74	0.96		
$t_{\text{OC5\_01}}$		0.78	1.12	1.46		
$t_{\text{OC6\_01}}$		2.14	3.06	3.98		
$t_{\text{OC7\_01}}$		20.2	22.2	28.9		
$t_{\text{OC1\_10}}$	• OC[1:0] = 10 (medium)	1.7	2.5	3.3		
$t_{\text{OC2\_10}}$		0.5	0.8	1.0		
$t_{\text{OC3\_10}}$		0.7	1.0	1.3		
$t_{\text{OC4\_10}}$		1.0	1.5	2.0		
$t_{\text{OC5\_10}}$		1.7	2.5	3.3		
$t_{\text{OC6\_10}}$		4.2	6.1	6.0		
$t_{\text{OC7\_10}}$		31.2	44.6	58.0		
$t_{\text{OC1\_11}}$	• OC[1:0] = 11 (very slow)	6.8	9.8	12.8		
$t_{\text{OC2\_11}}$		2.2	3.2	16.7		
$t_{\text{OC3\_11}}$		2.9	4.2	5.5		
$t_{\text{OC4\_11}}$		4.0	5.8	7.6		
$t_{\text{OC5\_11}}$		6.8	9.8	12.8		
$t_{\text{OC6\_11}}$		17.0	24.4	31.8		
$t_{\text{OC7\_11}}$		124.8	178.4	232.0		

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{\text{PWR}} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>POWER OUTPUT TIMING HS0 TO HS3 (CONTINUED)</b>						
	HS[0,1] Bulb Cooling Time Step for 28W bit = 0				ms	
$t_{\text{BC1\_00}}$	• CB[1:0] = 00 or 11 (medium)	242	347	452		
$t_{\text{BC2\_00}}$		126	181	236		
$t_{\text{BC3\_00}}$		140	200	260		
$t_{\text{BC4\_00}}$		158	226	294		
$t_{\text{BC5\_00}}$		181	259	337		
$t_{\text{BC6\_00}}$		211	302	393		
$t_{\text{BC1\_01}}$	• CB[1:0] = 01 (fast)	121	173	226		
$t_{\text{BC2\_01}}$		63	90	118		
$t_{\text{BC3\_01}}$		70	100	130		
$t_{\text{BC4\_01}}$		79	113	147		
$t_{\text{BC5\_01}}$		90	129	169		
$t_{\text{BC6\_01}}$		105	151	197		
$t_{\text{BC1\_10}}$	• CB[1:0] = 10 (slow)	484	694	1904		
$t_{\text{BC2\_10}}$		252	362	472		
$t_{\text{BC3\_10}}$		280	400	520		
$t_{\text{BC4\_10}}$		316	452	588		
$t_{\text{BC5\_10}}$		362	518	674		
$t_{\text{BC6\_10}}$		422	604	786		
	HS[0,1] for 28W bit = 1 or for HS2-HS3					
	• CB[1:0] = 00 or 11 (medium)					
$t_{\text{BC1\_00}}$		291	417	542		
$t_{\text{BC2\_00}}$		156	224	292		
$t_{\text{BC3\_00}}$		178	255	332		
$t_{\text{BC4\_00}}$		208	298	388		
$t_{\text{BC5\_00}}$		251	359	467		
$t_{\text{BC6\_00}}$		314	449	584		
$t_{\text{BC1\_01}}$	• CB[1:0] = 01 (fast)	146	209	272		
$t_{\text{BC2\_01}}$		78	112	146		
$t_{\text{BC3\_01}}$		88	127	166		
$t_{\text{BC4\_01}}$		101	145	189		
$t_{\text{BC5\_01}}$		126	180	234		
$t_{\text{BC6\_01}}$		226	324	422		
$t_{\text{BC1\_10}}$	• CB[1:0] = 10 (slow)	583	834	1085		
$t_{\text{BC2\_10}}$		312	448	582		
$t_{\text{BC3\_10}}$		357	510	665		
$t_{\text{BC4\_10}}$		417	596	775		
$t_{\text{BC5\_10}}$		501	717	933		
$t_{\text{BC6\_10}}$		628	898	1170		

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{PWR} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>PWM MODULE TIMING</b>						
$f_{IN0}$	Input PWM Clock Range on IN0	7.68	–	30.72	kHz	
$f_{IN0(LOW)}$	Input PWM Clock Low Frequency Detection Range on IN0	1.0	2.0	4.0	kHz	(35)
$f_{IN0(HIGH)}$	Input PWM Clock High Frequency Detection Range on IN0	100	–	400	kHz	(35)
$f_{PWM}$	Output PWM Frequency Range using External Clock on IN0	31.25	–	781	Hz	
$A_{FPWM(CAL)}$	Output PWM Frequency Accuracy using Calibrated Oscillator	-10	–	+10	%	
$f_{PWM(0)}$	Default Output PWM Frequency using Internal Oscillator	84	120	156	Hz	
$t_{CSB(MIN)}$	CSB Calibration Low Minimum Time Detection Range	14	20	26	$\mu\text{s}$	
$t_{CSB(MAX)}$	CSB Calibration Low Maximum Time Detection Range	140	200	260	$\mu\text{s}$	
$R_{PWM\_1k}$	Output PWM Duty Cycle Range for $f_{PWM} = 1.0\text{ kHz}$ for high speed slew rate	10	–	94	%	(35)
$R_{PWM\_400}$	Output PWM Duty Cycle Range for $f_{PWM} = 400\text{ Hz}$	6.0	–	98	%	(35)
$R_{PWM\_200}$	Output PWM Duty Cycle Range for $f_{PWM} = 200\text{ Hz}$	5.0	–	98	%	(35)
<b>INPUT TIMING</b>						
$t_{IN}$	Direct Input Toggle Timeout	175	250	325	ms	
<b>AUTORETRY TIMING</b>						
$t_{AUTO}$	Autoretry Period	105	150	195	ms	
<b>TEMPERATURE ON THE GND FLAG</b>						
$T_{OTWAR}$	Thermal Prewarning Detection	110	125	140	$^\circ\text{C}$	(36)
$T_{FEED}$	Analog Temperature Feedback at $T_A = 25\text{ }^\circ\text{C}$ with $R_{CSNS} = 2.5\text{ k}\Omega$	1.15	1.20	1.25	V	
$DT_{FEED}$	Analog Temperature Feedback Derating with $R_{CSNS} = 2.5\text{ k}\Omega$	-3.5	-3.7	-3.9	$\text{mV}/^\circ\text{C}$	(37)

**Notes**

34. Clock Fail detector available for PWM\_en bit is set to logic [1] and CLOCK\_sel is set to logic [0].
35. The PWM ratio is measured at  $V_{HS} = 50\%$  of  $V_{PWR}$  and for the default SR value. It is possible to put the device fully on (PWM duty cycle 100%) and fully off (duty cycle 0%). For values outside this range, a calibration is needed between the PWM duty cycle programming and the PWM on the output with  $R_L = 5.0\ \Omega$  resistive load.
36. Typical value guaranteed per design.
37. Value guaranteed per statistical analysis.

**Table 5. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $6.0\text{ V} \leq V_{\text{PWR}} \leq 20\text{ V}$ ,  $3.0\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_{\text{A}} \leq 125\text{ }^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
<b>SPI INTERFACE CHARACTERISTICS<sup>(38)</sup></b>						
$f_{\text{SPI}}$	Maximum Frequency of SPI Operation	–	–	8.0	MHz	
$t_{\text{WRSTB}}$	Required Low State Duration for RSTB	10	–	–	$\mu\text{s}$	(39)
$t_{\text{CSB}}$	Rising Edge of CSB to Falling Edge of CSB (Required Setup Time)	–	–	1.0	$\mu\text{s}$	(40)
$t_{\text{ENBL}}$	Rising Edge of RSTB to Falling Edge of CSB (Required Setup Time)	–	–	5.0	$\mu\text{s}$	(40)
$t_{\text{LEAD}}$	Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	–	–	500	ns	(40)
$t_{\text{WSCLKh}}$	Required High State Duration of SCLK (Required Setup Time)	–	–	50	ns	(40)
$t_{\text{WSCLKl}}$	Required Low State Duration of SCLK (Required Setup Time)	–	–	50	ns	(40)
$t_{\text{LAG}}$	Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)	–	–	60	ns	(40)
$t_{\text{SI(SU)}}$	SI to Falling Edge of SCLK (Required Setup Time)	–	–	37	ns	(41)
$t_{\text{SI(HOLD)}}$	Falling Edge of SCLK to SI (Required Setup Time)	–	–	49	ns	(41)
$t_{\text{RSO}}$	SO Rise Time • $C_{\text{L}} = 80\text{ pF}$	–	–	13	ns	
$t_{\text{FSO}}$	SO Fall Time • $C_{\text{L}} = 80\text{ pF}$	–	–	13	ns	
$t_{\text{RSI}}$	SI, CSB, SCLK, Incoming Signal Rise Time	–	–	13	ns	(41)
$t_{\text{FSI}}$	SI, CSB, SCLK, Incoming Signal Fall Time	–	–	13	ns	(41)
$t_{\text{SO(EN)}}$	Time from Falling Edge of CSB to SO Low-impedance	–	–	60	ns	(42)
$t_{\text{SO(DIS)}}$	Time from Rising Edge of CSB to SO High-impedance	–	–	60	ns	(43)

**Notes**

38. Parameters guaranteed by design.
39. RSTB low duration measured with outputs enabled and going to OFF or disabled condition.
40. Maximum setup time required for the 10XSC425 is the minimum guaranteed time needed from the microcontroller.
41. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
42. Time required for output status data to be available for use at SO. 1.0 k $\Omega$  on pull-up on CSB.
43. Time required for output status data to be terminated at SO. 1.0 k $\Omega$  on pull-up on CSB.

## 4.4 Timing Diagrams

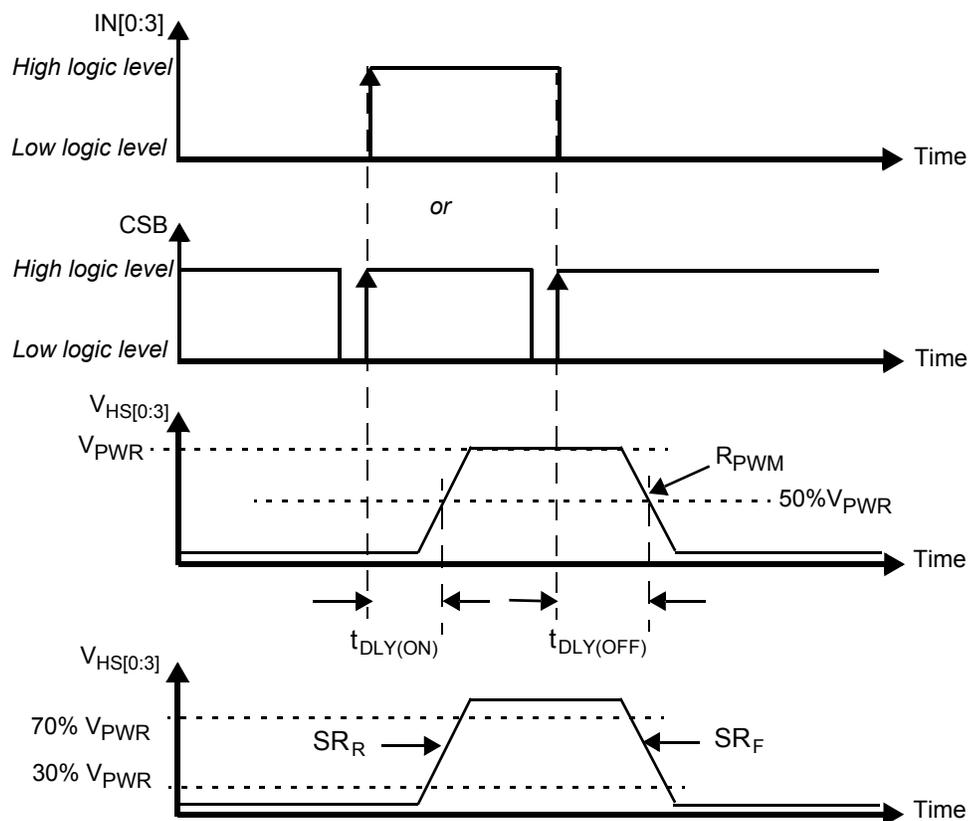


Figure 4. Output Slew Rate and Time Delays

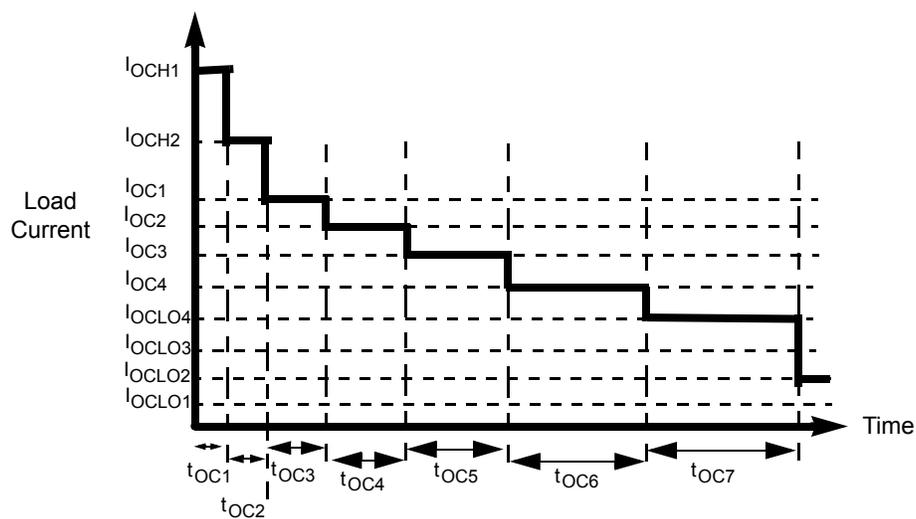


Figure 5. Overcurrent Shutdown Protection