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Document Number: MC10XSD200
Rev. 3.0, 12/2013

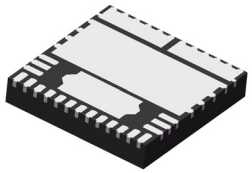
Dual 10 mOhm High Side Switch

10XSD200

HIGH SIDE SWITCH

The 10XSD200 device is part of a 36 V dual high side switch product family with integrated control, and a high number of protective and diagnostic functions. It has been designed for industrial applications. The low $R_{DS(ON)}$ channels (<10 mΩ) can control different load types; bulbs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit serial peripheral interface (SPI), allowing easy integration into existing applications. This device is powered by SMARTMOS technology.

Both channels can be controlled individually by external or internal clock signals, or by direct inputs. Using the internal clock allows fully autonomous device operation. Programmable output voltage slew-rates (individually programmable) helps improve electromagnetic compatibility (EMC) performance. To avoid shutting off the device upon inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Switching current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a Fail-safe operation mode, but remains operational, controllable, and protected.



FK SUFFIX (PB-FREE)
98ASA00428D
23 PIN PQFN (12 X12 mm)

Features

- Normal operating range: 8.0 - 36 V, extended range: 6.0 - 58 V
- Two fully protected 10 mΩ (@ 25 °C) high side switches
- Up to 6.0 A steady state current per channel
- Separate bulb and DC motor latched overcurrent handling
- Individually programmable internal/external PWM clock signals
- Overcurrent, short-circuit, and overtemperature protection with programmable autoretry functions
- Accurate temperature and current sensing
- OpenLoad detection (channel in OFF and ON state), also for LED applications (7.0 mA typ.)
- 3.3 V and 5.0 V compatible 16-bit SPI port for device control, configuration and diagnostics at rates up to 8.0 MHz

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC10XSD200FK	-40 to 125 °C	23 PQFN

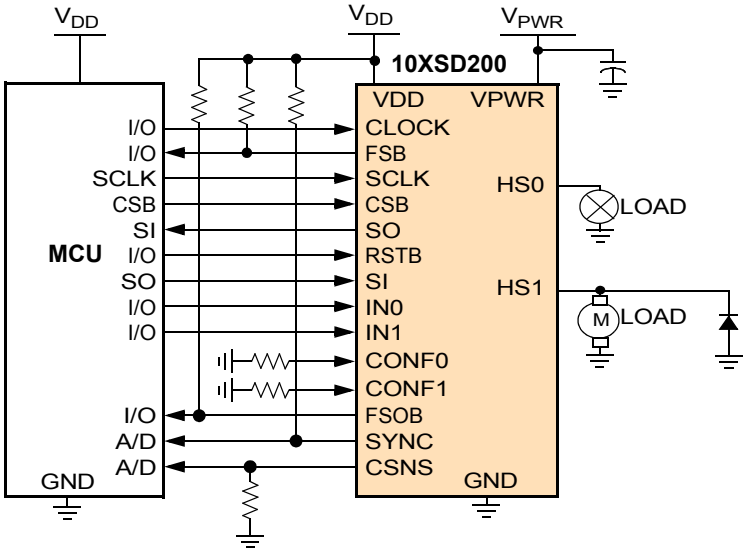


Figure 1. Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

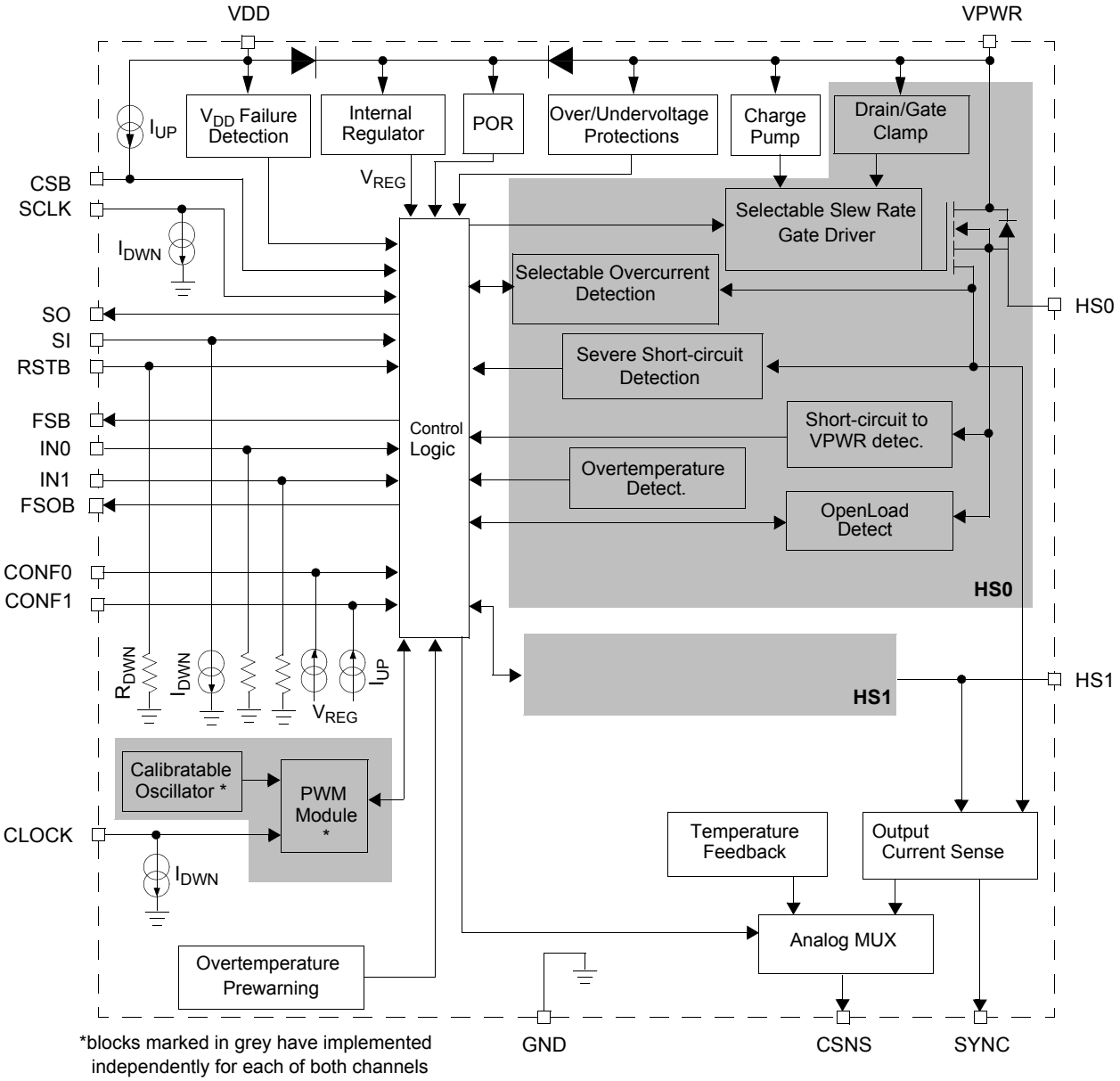


Figure 2. Internal Block Diagram

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PIN ASSIGNMENT

Transparent Top View

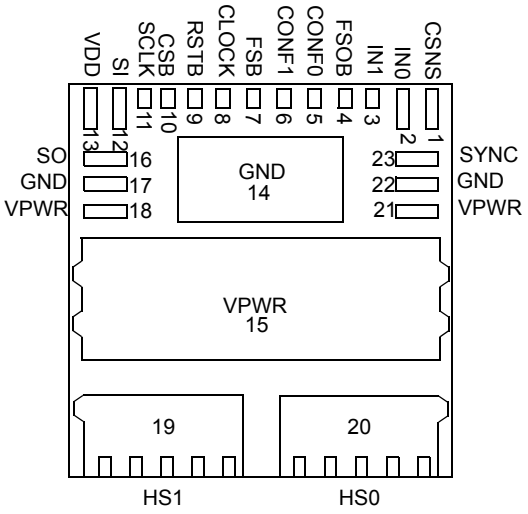


Figure 3. 10XSD200 Pin Assignments

Table 1. 10XSD200 Pin Description

The function of each pin is described in the section Functional Description

Pin Number	Pin Name	Function	Formal Name	Definition
1	CSNS	Output	Output Current/ Temperature Monitoring	This pin either outputs a current proportional to the channel's output current or a voltage proportional to the temperature of the GND pin (pin 14). Selection between current and temperature sensing, as well as setting the current sensing sensitivity, are performed through the SPI interface. An external pull-down resistor must be connected between CSNS and GND.
2 3	IN0 IN1	Input	Direct Inputs	The IN[0:1] input pins are used to directly control the switching state of both switches and consequently the voltage on the HS0:HS1 output pins. The pins are connected to GND by internal pull-down resistors
4	FSOB	Output	Fail-safe Output (Active Low)	FSOB is asserted (active-low) upon entering Fail-safe mode (see Functional Description) This open-drain output requires an external pull-up resistor to VPWR
5 6	CONF0 CONF1	Input	Configuration Input	The CONF[0:1] input pins are used to select the appropriate overcurrent detection profile (bulb /DC motor) for each of both channels. CONF requires a pull-down resistor to GND.
7	FSB	Output	Fault Status (Active Low)	This open-drain output pin (external pull-up resistor to VDD is required) is set when the device enters Fault mode (see Fault Mode)
8	CLOCK	Input	PWM Clock	The clock input gives the time-base when the device is operated in external clock/internal PWM mode. This pin has an internal pull-down current source.
9	RSTB	Input	Reset	This input pin is used to initialize the device's configuration - and fault registers. Reset puts the device in Sleep mode (low current consumption) provided it is not stimulated by direct input signals.This pin is connected to GND by an internal pull-down resistor.
10	CSB	Input	Chip Select (Active Low)	This input pin is connected to the SPI chip-select output of an external micro-controller. CSB is internally pulled up to V_{DD} by a current source I_{UP}.

Table 1. 10XSD200 Pin Description (continued)

The function of each pin is described in the section Functional Description

Pin Number	Pin Name	Function	Formal Name	Definition
11	SCLK	Input	Serial Clock	This input pin is to be connected to an external SPI Clock signal. The SCLK pin is internally connected to a pull-down current source I_{DWN}
12	SI	Input	Serial Input	This input pin receives the SPI input data from an external device (micro-controller or another extreme switch device in case of daisy-chaining). The SI pin is internally connected to a pull-down current source I_{DWN}
13	VDD	Power	Digital Drain Voltage	This is the positive supply pin of the SPI interface.
16	SO	Output	Serial Output	This output pin transmits SPI data to an external device (external micro-controller or the SI pin of the next SPI device in case of daisy-chaining). The pin doesn't require external pull-up or pull-down resistors, but a series resistor is recommended to limit current consumption in case of GND disconnection
14, 17, 22	GND	Ground	Ground	These pins, internally connected, are the ground pins for the logic and analog circuitry. It is recommended to also connect these pins on the PCB.
15,18,21	VPWR	Power	Positive Power Supply	These pins, internally connected, supply both the device's power and control circuitry (except the SPI port). The drain of both internal MOSFET switches is connected to them. Pin 15 is the device's primary thermal pad.
19 20	HS1 HS0	Output	Power Switch Outputs	Output pins of the switches, to be connected to the load.
23	SYNC	Output	Output Current Monitoring Synchronization	This output pin is asserted (logic low) when the Current Sense (CS) output signal is within the specified accuracy range. Reading the SYNC pin allows the external microprocessor to synchronize to the device when operating in autonomous operating mode. SYNC is open-drain and requires a pull-up resistor to VDD.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Parameter	Symbol	Maximum ratings	Unit
ELECTRICAL RATINGS			
VPWR Supply Voltage Range	V_{PWR}		V
Voltage Transient at 25 °C (500 ms)		58	
Reverse Voltage at 25 °C		-32	
Fast Negative Transient Pulses (ISO 7637-2 pulse #1, V_{PWR}=14 V & R_I=10 Ω)		-60	
VDD Supply Voltage Range	V_{DD}	-0.3 to 5.5	V
Voltage on Input pins [4] (except IN[0:1]) and Output pins [5] (except HS[0:1])	$V_{MAX,LOGIC}$[4]	-0.3 to 5.5	V
Voltage on Fail-safe Output (FSOB)	V_{FSO}	-0.3 to 58	V
Voltage on SO pin	V_{SO}	-0.3 to V_{DD}+0.3	V
Voltage (continuous, max. allowable) on IN[0:1] Inputs	$V_{IN,MAX}$	58	V
Voltage (continuous, max. allowable) on output pins (HS [0:1])	$V_{HS[0:1]}$	-32 to 58	V
Rated Continuous Output Current per channel[1]	$I_{HS[0:1]}$	6.0	A
Maximum allowable energy dissipation per channel and two parallel channels, single-pulse method[2]	$E_{CL[0:1]\_SING}$	128	mJ
ESD Voltage[3]			V
Human Body Model (HBM) for HS[0:1], VPWR and GND	V_{ESD1}	±8000	
Human Body Model (HBM) for other pins	V_{ESD2}	±2000	
Charge Device Model (CDM)			
Package Corner pins (1, 13, 19, 20)	V_{ESD3}	±750	
All Other pins	V_{ESD4}	±500	

Notes:

1. Output current rating valid as long as maximum junction temperature is not exceeded. For computation of the maximum allowable output current, the thermal resistance of the package & the underlying heatsink must be taken into account
2. Single pulse Energy dissipation, Single-pulse short-circuit method (L_L = 0.5 mH, R = 48 mΩ V_{PWR} = 28 V, T_J = 150 °C initial).
3. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
4. Concerned Input pins are: CONF[0:1], RSTB, SI, SCLK, Clock, and CSB.
5. Concerned Output pins are: CSNS, SYNC, and FSB.

Table 2. Maximum Ratings *(continued)*

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Parameter	Symbol	Maximum ratings	Unit
THERMAL RATINGS			
Operating Temperature [6] Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance Junction to Case Bottom/ VPWR Flag Surface	$R_{\theta JC}$	0.22	°C/W
Peak package reflow temperature during reflow[7],[8]	T_{PPRT}	Note 8	°C

Notes:

6. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
7. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
SUPPLY ELECTRICAL CHARACTERISTICS					
Supply Voltage Range: Full Specification compliant Extended Mode[9]	V_{PWR}	 8.0 6.0	 – –	 36 58	V
V_{PWR} Supply Current, device in wake-up mode, channel On, OpenLoad outputs in ON-state, HS[0:1] open, IN[0:1] > V_{IH}	$I_{PWR(ON)}$	–	6.5	8.0	mA
V_{PWR} Supply Current, device in wake-up mode (Standby), channel Off OpenLoad in OFF-state Detection Disabled, HS[0:1] shorted to ground with V_{DD} = 5.5 V and RSTB > V_{WAKE}	$I_{PWR(SBY)}$	–	6.5	8.0	mA
Sleep State Supply Current V_{PWR} = 24 V, RSTB = IN[0:1] < V_{WAKE}, HS[0:1] connected to ground T_A = 25 °C T_A = 125 °C	$I_{PWR(SLEEP)}$	 – –	 3.0 –	 10.0 60.0	µA
V_{DD} Supply Voltage	$V_{DD(ON)}$	3.0	–	5.5	V
V_{DD} Supply Current at V_{DD} = 5.5 V No SPI Communication 8.0 MHz SPI Communication[10]	$I_{DD(ON)}$	 – –	 – 5.0	 2.2 –	mA
V_{DD} Sleep State Current at V_{DD} = 5.5 V with or without V_{PWR}	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage Shutdown Threshold	$V_{PWR(OV)}$	39	42	45.5	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Shutdown Threshold[11]	$V_{PWR(UV)}$	5.0	–	6.0	V
V_{PWR} Power-On-Reset (POR) Voltage Threshold[11]	$V_{PWR(POR)}$	2.2	2.6	4.0	V
V_{DD} Power-On-Reset (POR) Voltage Threshold[11]	$V_{DD(POR)}$	1.5	2.0	2.5	V
V_{DD} Supply Failure Voltage Threshold (assumed V_{PWR} > $V_{PWR(UV)}$)	$V_{DD(FAIL)}$	2.2	2.5	2.8	V

Notes

9. In extended mode, several device functions (channel control, $R_{DS(ON)}$ and overtemperature protection) are guaranteed, but compliance with the specified values in this document is not. Below 6.0 V, the device is only protected from overheating (thermal shutdown). Above $V_{PWR(OV)}$, the channels can only be turned ON when the overvoltage detection function has been disabled.
10. Typical value guaranteed per design.
11. When the device recovers from undervoltage and returns to normal mode (6.0 V < V_{PWR} < 58 V) before the end of the auto-retry period (see Auto-retry), the device performs normally. When V_{PWR} drops below $V_{PWR(UV)}$, undervoltage is detected see Undervoltage Fault (Latchable Fault) and EMC Performances.

Table 3. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1)					
ON-Resistance, Drain-to-Source (I_{HS} = 3.0 A, T_J = 25 °C) CSNS_ratio = 0	$R_{DS(ON)25}$				mΩ
V_{PWR} = 8.0 V		–	–	10	
V_{PWR} = 28 V		–	–	10	
V_{PWR} = 36 V		–	–	10	
ON-Resistance, Drain-to-Source (I_{HS} = 3.0 A,T_J = 150 °C) CSNS_ratio = 0	$R_{DS(ON)150}$				mΩ
V_{PWR} = 8.0 V		–	–	18	
V_{PWR} = 28 V		–	–	18	
V_{PWR} = 36 V		–	–	18	
ON-Resistance, Drain-to-Source difference from one channel to the other in parallel mode (I_{HS} = 1.0 A,T_J = 150 °C) CSNS_ratio = X	$\Delta R_{DS(ON)150}$	-0.8	–	+0.8	mΩ
ON-Resistance, Source-Drain (I_{HS} = -3.0 A, T_J = 150 °C, V_{PWR} = -24 V)	$R_{SD(ON)150}$	–	–	18	mΩ
Max. detectable wiring length (2.5 mm²) for severe short-circuit detection	L_{SHORT}				cm
High slew rate selected					
Medium slew rate selected:		20	85	140	
Low slew rate selected:		50	160	300	
		100	280	600	
Overcurrent Detection thresholds with CSNS_ratio bit = 0 (CSR0)	OCH1_0	55	66	77	A
	OCH2_0	35	42	49	
	OCM1_0	22	26	31	
	OCM2_0	13	16	19.5	
	OCL1_0	9.0	10.8	12.6	
	OCL2_0	6.0	7.2	8.4	
	OCL3_0	3.0	3.6	4.2	
Overcurrent Detection thresholds with CSNS_ratio bit = 1(CSR1)	OCH1_1	18.3	22	26.5	A
	OCH2_1	11.7	14.0	16.3	
	OCM1_1	7.2	8.7	10.1	
	OCM2_1	4.4	5.3	6.2	
	OCL1_1	3.0	3.6	4.2	
	OCL2_1	2.0	2.4	2.8	
	OCL3_1	0.96	1.2	1.44	
Output pin leakage Current in sleep state (positive value = outgoing)	I_{OUT_LEAK}				µA
$V_{HS,OFF}$ = 0 V ($V_{HS,OFF}$ = output voltage in OFF state)		–	–	+11	
$V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 24 V)		-120	–	+5.0	
$V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 36 V)		-1400	–	+5.0	
Switch Turn-on threshold for Supply overvoltage (V_{PWR} -GND)	$V_{D\_GND(CLAMP)}$	58	–	66	V
Switch turn-on threshold for Drain-Source overvoltage (measured at I_{OUT} = 500 mA	$V_{DS(CLAMP)}$	58	–	66	V

Table 3. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)					
Current Sensing Ratio [12]					–
CSNS_ratio bit = 0 (high current mode)	C_{SR0}	–	1/3000	–	
CSNS_ratio bit = 1 (low current mode)	C_{SR1}	–	1/1000	–	
Minimum measurable load current with compensated error [13]	$I_{\_LOAD\_MIN}$	–	–	100	mA
CSNS leakage current in OFF state (CSNSx_en = 0, CSNS_ratio bit_x = 0)	I_{CSR_LEAK}	-4.0	–	+4.0	µA
Systematic offset error (see Current Sense Errors)	$I_{\_LOAD\_ERR\_SYS}$	–	-10	–	mA
Random offset error	$I_{\_LOAD\_ERR\_RAND}$	-150	–	150	mA
E_{SR0} Output Current Sensing Error (%, uncompensated[14] at output current level (Sense ratio C_{SR0} selected):	E_{SR0_ERR}				%
T_J=-40 °C					
6.0 A		-13	–	13	
3.0 A		-12	–	12	
1.5 A		-17	–	17	
0.75 A		-31	–	31	
T_J=125 °C					
6.0 A		-10	–	10	
3.0 A		-9.0	–	9.0	
1.5 A		-12	–	12	
0.75 A		-19	–	19	
T_J=25 to 125 °C					
6.0 A		-10	–	10	
3.0 A		-9.0	–	9.0	
1.5 A		-12	–	12	
0.75 A		-22	–	22	

Notes:

12. Current Sense Ratio C_{SRx} = I_{CSNS} / $I_{HS[x]}$
13. See note [14], but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and Use of Offset Compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration.
14. E_{SRx_ERR}=(I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRx}, ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current Sense Error Model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRx} - $I_{\_LOAD\_ERR\_SYS}$

Table 3. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
E_{SR0} Output Current Sensing Error (% after offset compensation[15] at output current level (Sense ratio C_{SR0} selected):	E_{SR0_ERR}(Comp)				%
T_J=-40 °C					
6.0 A		-10	–	10	
3.0 A		-10	–	10	
1.5 A		-10	–	10	
0.75 A		-10	–	10	
T_J=125 °C					
6.0 A		-9.0	–	9.0	
3.0 A		-8.0	–	8.0	
1.5 A		-8.0	–	8.0	
0.75 A		-9.0	–	9.0	
T_J=25 to 125 °C					
6.0 A		-9.0	–	9.0	
3.0 A		-8.0	–	8.0	
1.5 A		-8.0	–	8.0	
0.75 A		-9.0	–	9.0	
E_{SR1} Output Current Sensing Error (%, uncompensated [16] at output current level (Sense ratio C_{SR1} selected):	E_{SR1_ERR}				%
T_J=-40 °C					
1.5 A		-15	–	15	
T_J=125 °C					
1.5 A		-12	–	12	
T_J=25 to 125 °C					
1.5 A		-12	–	12	

Notes:

15. See note [14], but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and Use of Offset Compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration.
16. E_{SRx_ERR}=(I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRx}, ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current Sense Error Model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRx} - $I_{\_LOAD\_ERR\_SYS}$

Table 3. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)					
E_{SR1} Output Current Sensing Error (% (level) after offset compensation[17] at output current level (Sense ratio C_{SR1} selected):	E_{SR1_ERR}(Comp)				%
T_J=-40 °C					
1.5 A		-10	–	10	
0.5 A		-11	–	11	
0.25 A		-18	–	18	
0.15 A		-29	–	29	
T_J=125 °C					
1.5 A		-8.0	–	8.0	
0.5 A		-10	–	10	
0.25 A		-12	–	12	
0.15 A		-16	–	16	
T_J=25 to 125 °C					
1.5 A		-8.0	–	8.0	
0.5 A		-10	–	10	
0.25 A		-13	–	13	
0.15 A		-21	–	21	
E_{SR0} Output Current Sensing Error in parallel mode (%, uncompensated[18]) at outputs Current level (Sense ratio C_{SR0} selected):	$E_{SR0\_ERR\_PAR}$				%
T_J=-40 °C					
6.0 A (per channel)		-10	–	10	
3.0 A (per channel)		-11	–	11	
T_J=125 °C					
6.0 A (per channel)		-8.0	–	8.0	
3.0 A (per channel)		-8.0	–	8.0	
T_J=25 to 125 °C					
6.0 A (per channel)		-8.0	–	8.0	
3.0 A (per channel)		-8.0	–	8.0	

Notes:

17. See note [18], but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and Use of Offset Compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration.
18. E_{SRx_ERR}=(I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRx}, ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current Sense Error Model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRx} - $I_{\_LOAD\_ERR\_SYS}$

Table 3. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE OUTPUT STAGE (HS0 AND HS1) (CONTINUED)					
Current Sense Clamping Voltage (condition: R(CSNS) > 10 kOhm)	$V_{CL(CSNS)}$	5.5	–	7.5	V
OpenLoad detection Current threshold in OFF state [19]	$I_{OLD(OFF)}$	30	–	100	µA
OpenLoad Fault Detection Voltage Threshold [19]	$V_{OLD(THRES)}$	4.0	–	5.5	V
OpenLoad detection Current threshold in ON state (see OpenLoad Detection In On State (OL_ON)): CSNS_ratio bit = 0 CSNS_ratio bit = 1 (fast slew rate SR[1:0] = 10 mandatory for this function)	$I_{OLD(ON)}$	 80 5.0	 300 7.0	 600 10	mA
Time period of the periodically activated OpenLoad in ON state detection for CSNS_ratio bit = 1	t_{OLLED}	105	150	195	ms
Output Shorted-to-V_{PWR} Detection Voltage Threshold (channel in OFF state)	$V_{OSD(THRES)}$	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V
Switch turn-on threshold for Negative Output Voltages (protects against negative transients) - (measured at I_{OUT} = 100 mA, Channel in OFF state)	V_{CL}	-38	–	-32	V
Switch turn-on threshold for Negative Output Voltages difference from one channel to the other in parallel mode - (measured at I_{OUT} = 100 mA, Channel in OFF state)	ΔV_{CL}	-2.0	–	+2.0	V
Switching State (On/Off) discrimination thresholds	V_{HS_TH}	0.45*V_{PWR}	0.5*V_{PWR}	0.55*V_{PWR}	V
Shutdown temperature (Power MOSFET junction; 6.0 V < V_{PWR} < 58 V)	T_{SD}	160	175	190	°C
ELECTRICAL CHARACTERISTICS OF THE CONTROL INTERFACE PINS					
Logic Input Voltage, High[20]	V_{IH}	2.0	–	5.5	V
Logic Input Voltage, Low[20]	V_{IL}	-0.3	–	0.8	V
Wake-up Threshold Voltage (IN[0:1] and RSTB)[21]	V_{WAKE}	1.0	–	2.2	V
Internal Pull-down Current Source (on inputs: CLOCK, SCLK and SI)[22]	I_{DWN}	5.0	–	20	µA
Internal Pull-up Current Source (input CSB)[23]	I_{UP_CSB}	5.0	–	20	µA
Internal Pull-up Current Source (input CONF[0:1])[24]	I_{UP_CONF}	25	–	100	µA
Capacitance of SO, FSB and FSOB pins in Tri-state	C_{SO}	–	–	20	pF
Internal Pull-down Resistance (RSTB and IN[0:1])	R_{DWN}	125	250	500	kΩ
Input Capacitance[25]	C_{IN}	–	4.0	12	pF

Notes:

19. Minimum required value of OpenLoad impedance for detection of OpenLoad in OFF-state: 200 kΩ.($V_{OLD(THRES)}$ = V_{HS} @ $I_{OLD(OFF)}$)
20. High and low voltage ranges apply to SI, CSB, SCLK, RSTB, IN[0:1] and CLOCK input signals. The IN[0:1] signals may be derived from V_{PWR} and can tolerate voltages up to 58 V.
21. Voltage above which the device wakes up
22. Pull-down current-value for V_{SI} ≥ 0.8 V and V_{SCLK} ≥ 0.8 V and V_{CLOCK} ≥ 0.8 V.
23. Pull-up current-value for V_{CSB} ≤ 2.0 V. CSB has an internal pull-up current source connected to V_{DD}.
24. Pins CONF[0:1] are connected to an internal current source, connected itself to an internal voltage regulator (V_{REG} ~ 3.0 V).
25. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CONF[0:1], and CLOCK pins. This parameter is guaranteed by the manufacturing process but is not tested in production.

Table 3. Static Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

parameter	Symbol	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS OF THE CONTROL INTERFACE PINS (CONTINUED)					
SO High-state Output Voltage (I_{OH} = 1.0 mA)	V_{SOH}	V_{DD}-0.4	–	–	V
SYNC, SO, FSOB and FSB Low-state Output Voltage (I_{OL} = -1.0 mA)	V_{SOL}	–	–	0.4	V
SYNC, SO, CSNS, FSOB and FSB Tri-state Leakage Current: (0.0 V < V(SO) < V_{DD}, or V(FS) or V(SYNC) = 5.5 V, or V(FSO) = 36 V or V(CSNS) = 0 V	$I_{SO(LEAK)}$	-2.0	0.0	2.0	µA
CONF[0:1] Required values of the External Pull-down Resistor - Lighting applications - DC motor applications	R_{CONF}	 1.0 50	 – –	 10 Infinite	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
OUTPUT VOLTAGE SWITCHING CHARACTERISTICS					
Rising and Falling edges medium slew rate (SR[1:0] = 00)[26]	SR_{R_00}				V/µs
V_{PWR} = 16 V	SR_{F_00}	0.164	–	0.65	
V_{PWR} = 28 V		0.28	–	0.79	
V_{PWR} = 36 V		0.34	–	0.90	
Rising and Falling edges low slew rate (SR[1:0] = 01)[26]	SR_{R_01}				V/µs
V_{PWR} = 16 V	SR_{F_01}	0.081	–	0.32	
V_{PWR} = 28 V		0.14	–	0.395	
V_{PWR} = 36 V		0.17	–	0.45	
Rising and Falling edges high slew rate / SR[1:0] = 10)[26]	SR_{R_10}				V/µs
V_{PWR} = 16 V	SR_{F_10}	0.29	–	1.30	
V_{PWR} = 28 V		0.55	–	1.58	
V_{PWR} = 36 V		0.68	–	1.80	
Rising/Falling edge slew rate matching	SR_R/SR_F				
16 V < V_{PWR} < 36 V		0.65	1.0	1.35	
Edge slew rate difference from one channel to the other in parallel mode[26]	ΔSR				
16 V < V_{PWR} < 36 V					V/µs
SR[1:0] = 00		-0.12	0.0	+0.12	
SR[1:0] = 01		-0.06	0.0	+0.06	
SR[1:0] = 10		-0.2	0.0	+0.2	
Output Turn-ON and Turn-OFF Delays (medium slew rate: SR[1:0] = 00)[27]	t_{DLY_00}				µs
16 V < V_{PWR} < 36 V		30	–	160	
Output Turn-ON and Turn-OFF Delays (low slew rate / SR[1:0] = 01)[27]	t_{DLY_01}				µs
16 V < V_{PWR} < 36 V		50	–	300	
Output Turn-ON and Turn-OFF Delays (high slew rate / SR[1:0] = 10)[27]	t_{DLY_10}				µs
16 V < V_{PWR} < 36 V		15	–	80	
Turn-ON and Turn-OFF Delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)	Δt_{RF_00}				µs
f_{PWM} = 400 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 00		-25	0.0	25	
Turn-ON and Turn-OFF Delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)	Δt_{RF_01}				µs
f_{PWM} = 200 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 01		-90	0.0	90	
Turn-ON and Turn-OFF Delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)	Δt_{RF_10}				µs
f_{PWM} = 1.0 kHz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 10		-13	0.0	13	

Notes

26. Rising and Falling edge slew rates specified for a 20 to 80% voltage variation on a 10 Ω resistive load (see Figure 4).
27. Turn-on delay time measured as delay between a rising edge of the channel control signal (IN[0:1] = 1 or CSB) and the associated rising edge of the output voltage up to: $V_{HS[0:1]} = V_{PWR}$ / 2 (where R_L = 5.0 Ω). Turn-OFF delay time is measured as time between a falling edge of the channel control signal (IN[0:1] = 0 or CSB pin) and the associated falling edge of the output voltage up to the instant at which: $V_{HS[0:1]} = V_{PWR}$ / 2 (R_L = 5.0 Ω)

Table 4. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (CONTINUED)					
Delay time difference from one channel to the other in parallel mode[28] 16 V < V_{PWR} < 36 V SR[1:0] = 00 SR[1:0] = 01 SR[1:0] = 10	$\Delta t_{(DLY)}$	 -25 -50 -12	 0.0 0.0 0.0	 +25 +50 +12	µs
Fault Detection Delay Time[29]	t_{FAULT}	–	5.0	8.0	µs
Output Shutdown Delay Time[30]	t_{DETECT}	–	7.0	12	µs
Current sense output settling Time for SR[1:0] = 00 (medium slew rate) V_{PWR} = 28 V [31] 16 V < V_{PWR} < 36 V [31]	$t_{CSNSVAL\_00}$	 – 0.0	 104 –	 – 250	µs
Current sense output settling Time for SR[1:0] = 01(low slew rate) V_{PWR} = 28 V [31] 16 V < V_{PWR} < 36 V [31]	$t_{CSNSVAL\_01}$	 – 0.0	 167 –	 – 355	µs
Current sense output settling Time for SR[1:0] = 10 (high slew rate) V_{PWR} = 28 V [31] 16 V < V_{PWR} < 36 V [31]	$t_{CSNSVAL\_10}$	 – 0.0	 76 –	 – 210	µs
SYNC output signal delay for SR[1:0] = 00 (medium SR) [31]	$t_{SYNCVAL\_00}$	50	–	160	µs
SYNC output signal delay for SR[1:0] = 01 (low SR) [31]	$t_{SYNCVAL\_01}$	80	–	320	µs
SYNC output signal delay for SR[1:0] = 10 (high SR) [31]	$t_{SYNCVAL\_10}$	22	–	80	µs
Recommended sync_to_read delay SR[1:0] = 00 (medium slew rate) [31]	$t_{SYNREAD\_00}$	–	–	200	µs
Recommended sync_to_read delay SR[1:0] = 01 (low slew rate) [31]	$t_{SYNREAD\_01}$	–	–	300	µs
Recommended sync_to_read delay SR[1:0] = 10 (high slew rate) [31]	$t_{SYNREAD\_10}$	–	–	200	µs
Upper overcurrent threshold duration	t_{OCH1} t_{OCH2}	6.0 12.0	8.6 17.2	11.2 22.4	ms
Medium overcurrent threshold duration (CONF = 0; Lighting Profile)	t_{OCM1_L} t_{OCM2_L}	48 96	67 137	87 178	ms
Medium overcurrent threshold duration (CONF = 1; DC motor Profile)	t_{OCM1_M} t_{OCM2_M}	96 245	137 350	178 455	ms
FREQUENCY & PWM DUTY CYCLE RANGES [32](protections fully operational, see Protective Functions)					
Switching Frequency range - Direct Inputs	$f_{CONTROL}$	0.0	–	1000	Hz
Switching Frequency range - External clock with internal PWM (recommended)	f_{PWM_EXT}	20	–	1000	Hz
Switching Frequency range - Internal clock with internal PWM (recommended)	f_{PWM_INT}	60	–	1000	Hz
Duty Cycle range	$R_{CONTROL}$	0.0	–	100	%

Notes:

28. Rising and Falling edge slew rates specified for a 20 to 80% voltage variation on a 10 Ω resistive load (see Figure 4).
29. Time required to detect and report the fault to the FSB pin.
30. Time required to switch off the channel after detection of overtemperature (OT), overcurrent (OC), SC or UV error (time measured between start of the negative edge on the FSB pin and the falling edge on the output voltage until V(HS[0:1)) = 50% of V_{PWR}
31. Settling time (= $t_{CSNSVAL\_XX}$), SYNC output signal delay (= $t_{SYNCVAL\_XX}$) and Read-out delay (= $t_{SYNREAD\_XX}$) are defined for a stepped load current using a 10 Ω resistive load for CSNS_RATIO_s = 0. (see Figure 9 and Output Current Monitoring (CSNS)).
32. In Direct Input mode, the lower frequency limit is 0 Hz with RSTB=5.0 V and 4.0 Hz with RSTB=0 V. Duty-cycle applies to instants at which V_{HS} = 50% V_{PWR}. For low duty cycle values, the effective value also depends on the value of the selected slew rate.

Table 4. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
AVAILABILITY DIAGNOSTIC FUNCTIONS OVER DUTY-CYCLE AND SWITCHING FREQUENCY (protection & diagnostics both fully operational, see Diagnostic Features for the exact boundary values)					
Available Duty Cycle Range, f_{PWM} = 1.0 kHz high slew rate (Notes)	$R_{PWM\_1K\_H}$				%
OL_OFF		0.0	–	62	
OL_ON		35	–	100	
OS		0.0	–	90	
Available Duty Cycle Range, f_{PWM} = 400 Hz, medium slew rate mode(Notes)	$R_{PWM\_400\_M}$				%
OL_OFF		0.0	–	81	
OL_ON		21	–	100	
OS		0.0	–	88	
Available Duty Cycle Range, f_{PWM} = 400 Hz, high slew rate mode (Notes)	$R_{PWM\_400\_H}$				%
OL_OFF		0.0	–	84	
OL_ON		14	–	100	
OS		0.0	–	95	
Available Duty Cycle Range, f_{PWM} = 200 Hz, low slew rate mode(Notes)	$R_{PWM\_200\_L}$				%
OL_OFF		0.0	–	86	
OL_ON		15	–	100	
OS		0.0	–	93	
Available Duty Cycle Range, f_{PWM} = 200 Hz, medium slew rate mode(Notes)	$R_{PWM\_200\_M}$				%
OL_OFF		0.0	–	90	
OL_ON		11	–	100	
OS		0.0	–	94	
Available Duty Cycle Range, f_{PWM} = 100 Hz in low slew rate mode(Notes)	$R_{PWM\_100\_L}$				%
OL_OFF		0.0	–	93	
OL_ON		8.0	–	100	
OS		0.0	–	96	
Deviation of the internal clock PWM frequency after Calibration(34)	$A_{FPWM(CAL)}$	-10	–	+10	%
Default output frequency when using an uncalibrated oscillator	$f_{PWM(0)}$	280	400	520	Hz
Minimal required Low Time during Calibration of the Internal Clock through CSB	$t_{CSB(MIN)}$	1.0	1.5	2.0	µs
Maximal allowed Low Time during Calibration of the Internal Clock through CSB	$t_{CSB(MAX)}$	70	100	130	µs
Recommended external Clock Frequency Range (external clock/PWM Module)	f_{CLOCK}	15	–	512	kHz
Upper detection threshold for external Clock frequency monitoring	$f_{CLOCK(MAX)}$	512	730	930	kHz
Lower detection threshold for external Clock frequency monitoring	$f_{CLOCK(MIN)}$	5.0	7.0	10	kHz

Notes:

33. The device can be operated outside the specified duty cycle and frequency ranges (basic protective functions OC, SC, UV, OV, and OT remain active), but the availability of the diagnostic functions OL_ON, OL_OFF, and OS is affected. OL_OFF duty-cycle range is guaranteed by design characterization.
34. Values guaranteed from 60 Hz to 1.0 kHz (recommended switching frequency range).

Table 4. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
TIMING: SPI PORT, IN[0]/ IN[1] SIGNALS & AUTORETRY					
Required Low time allowing delatching or triggering sleep mode (direct inputs)	t_{IN}	175	250	325	ms
Watchdog Timeout for entering Fail-safe Mode due to loss of SPI contact[35]	t_{WDTO}	217	310	400	ms
Auto-Retry Repetition Period (when activated):					ms
Auto_period bits = 00	t_{AUTO_00}	105	150	195	
Auto_period bits = 01	t_{AUTO_01}	52.5	75	97.5	
Auto_period bits = 10	t_{AUTO_10}	26.2	37.5	47.8	
Auto_period bits = 11	t_{AUTO_11}	13.1	17.7	24.4	
GND PIN TEMPERATURE SENSING FUNCTION					
Thermal Prewarning Detection Threshold[36]	T_{OTWAR}	110	125	140	°C
Temperature Sensing output voltage @ T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)	T_{FEED}	918	1078	1238	mV
Gain Temperature Sensing output @ T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)[36]	DT_{FEED}	10.7	11.1	11.5	mV/°C
Temperature Sensing Error, range [-40 °C, 150 °C], default[36]	T_{FEED_ERROR}	-15	–	+15	°C
Temperature Sensing Error, [-40 °C, 150 °C] after 1 point calibration @ 25 °C[36]	$T_{FEED\_ERROR\_CAL}$	-5.0	–	+5.0	°C

Notes:

35. Only when the WD_dis bit set to logic [0] (default). Watchdog timeout defined from the rising edge on RST to rising edge HS[0,1]
36. Values were obtained after lab characterization

Table 4. Dynamic Electrical Characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min	Typ	Max	Unit
SPI INTERFACE ELECTRICAL CHARACTERISTICS(37)					
Maximum Operating Frequency of the Serial Peripheral Interface (SPI)(43)	f_{SPI}	–	–	8.0	MHz
Required Low-state Duration for reset RSTB(38)	t_{WRSTB}	10	–	–	µs
Required duration from the Rising to the Falling Edge of CSB (Required Setup Time)(39)	t_{CSB}	1.0	–	–	µs
Rising Edge of RSTB to Falling Edge of CSB (Required Setup Time)(39)	t_{ENBL}	5.0	–	–	µs
Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)(39)	t_{LEAD}	500	–	–	ns
Required High State Duration of SCLK (Required Setup Time)(39)	t_{WSCLKh}	50	–	–	ns
Required Low State Duration of SCLK (Required Setup Time)(39)	t_{WSCLKl}	50	–	–	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)(39)	t_{LAG}	60	–	–	ns
SI to Falling Edge of SCLK (Required Setup Time)(40)	$t_{SI(SU)}$	37	–	–	ns
Falling Edge of SCLK to SI (Required Setup Time)(40)	$t_{SI(HOLD)}$	49	–	–	ns
SO Rise Time C_L = 80 pF	t_{RSO}	–	–	20	ns
SO Fall Time C_L = 80 pF	t_{FSO}	–	–	20	ns
SI, CSB, SCLK, Max. Rise Time allowing operation at f_{SPI} = 8.0 MHz(40)	t_{RSI}	–	–	12	ns
SI, CSB, SCLK, Max. Fall Time allowing operation at f_{SPI} = 8.0 MHz(40)	t_{FSI}	–	–	12	ns
Time from Rising Edge of SCLK to the SO Low-level(41)	$t_{SO(EN)}$	–	–	73	ns
Time from Rising Edge of SCLK to the SO High-level(42)	$t_{SO(DIS)}$	–	–	73	ns

Notes

37. Parameters guaranteed by design. It is recommended to tie unused SPI pins to GND with resistors 1.0k < R <10 k
38. RSTB low duration defined as the minimum time required to switch off the channel when previously put ON in SPI mode (direct inputs inactive).
39. Minimum setup time required for the device is the minimum required time that the microcontroller must wait or remain in a given state.
40. Rise and Fall time of incoming SI, CSB, and SCLK signals.
41. Time required for output data to be available for use at SO, measured with a 1.0 kΩ series resistor connected CSB.
42. Time required for output data to be terminated at SO measured with a 1.0 kΩ series resistor connected CSB.
43. For clock frequencies > 4.0 MHz, series resistors on the SPI pins should preferably be removed. Otherwise, 470 pF ($V_{MAX.}$ > 40 V) ceramic speed-up capacitors in parallel with the >8.0 kΩ input resistors are required on pins SCLK, SI, SO, and CS.

TIMING DIAGRAMS

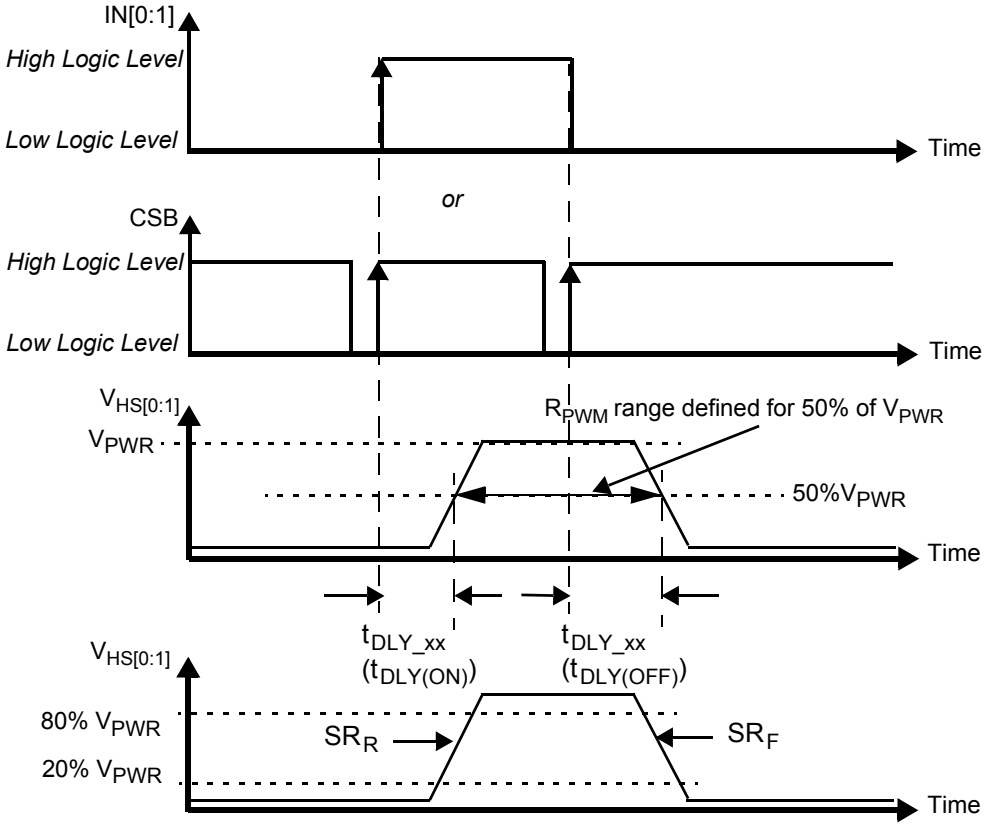


Figure 4. Output Voltage Slew Rate and Delay

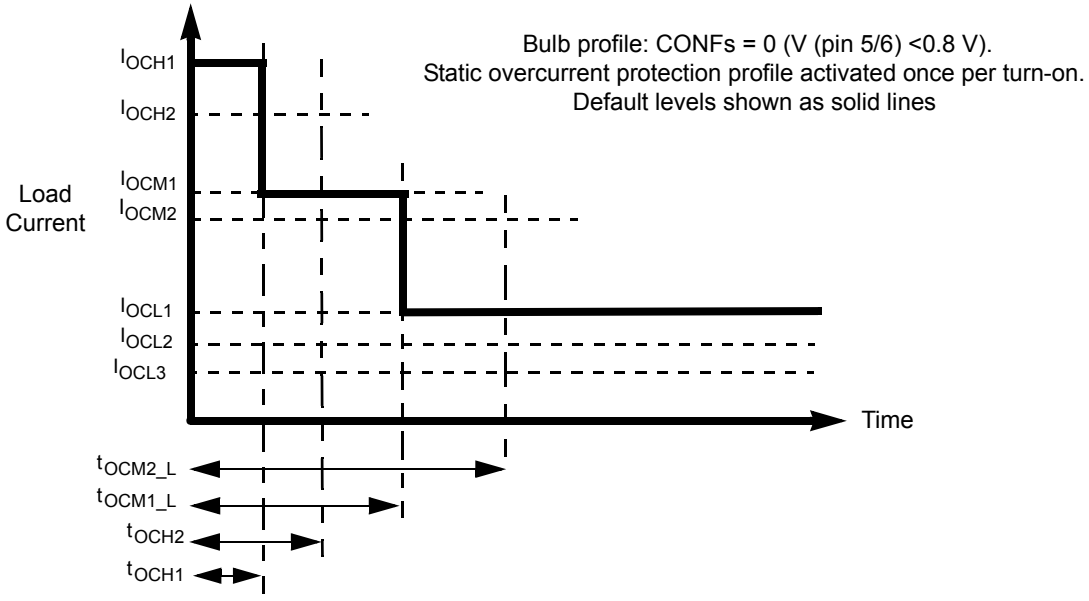


Figure 5. Overcurrent Protection Profile for Bulb Applications

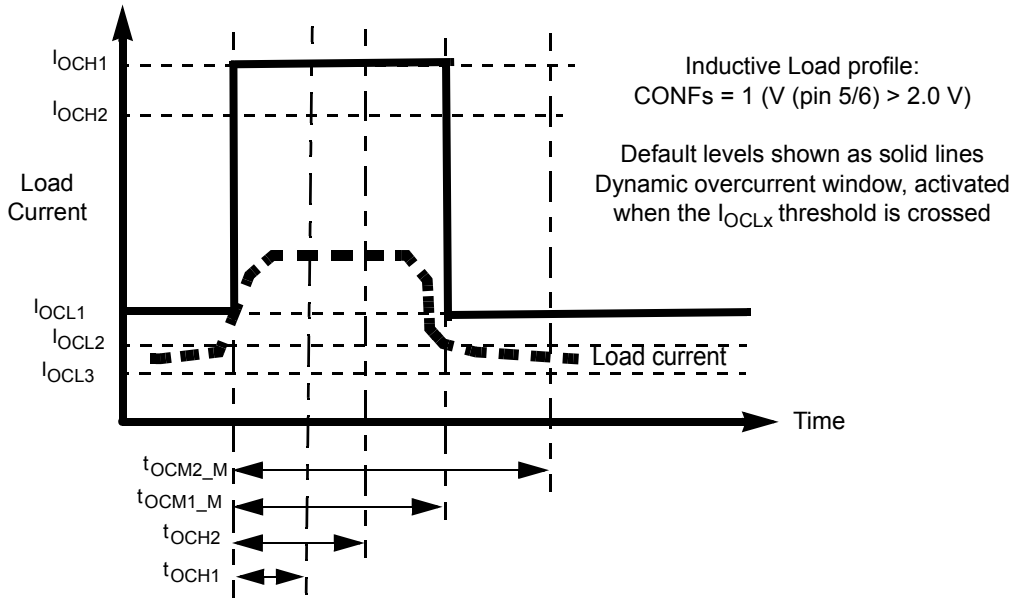


Figure 6. Overcurrent Protection Profile for Applications with Inductive Loads (DC motors, solenoids)

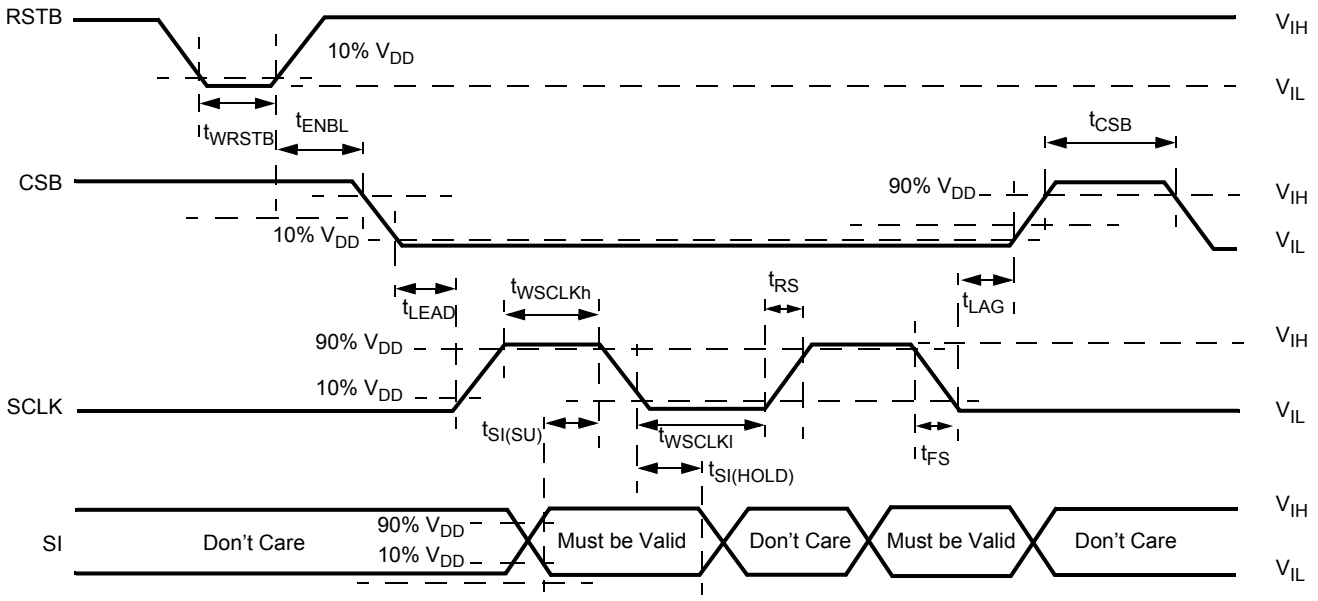


Figure 7. Timing Requirements During SPI Communication

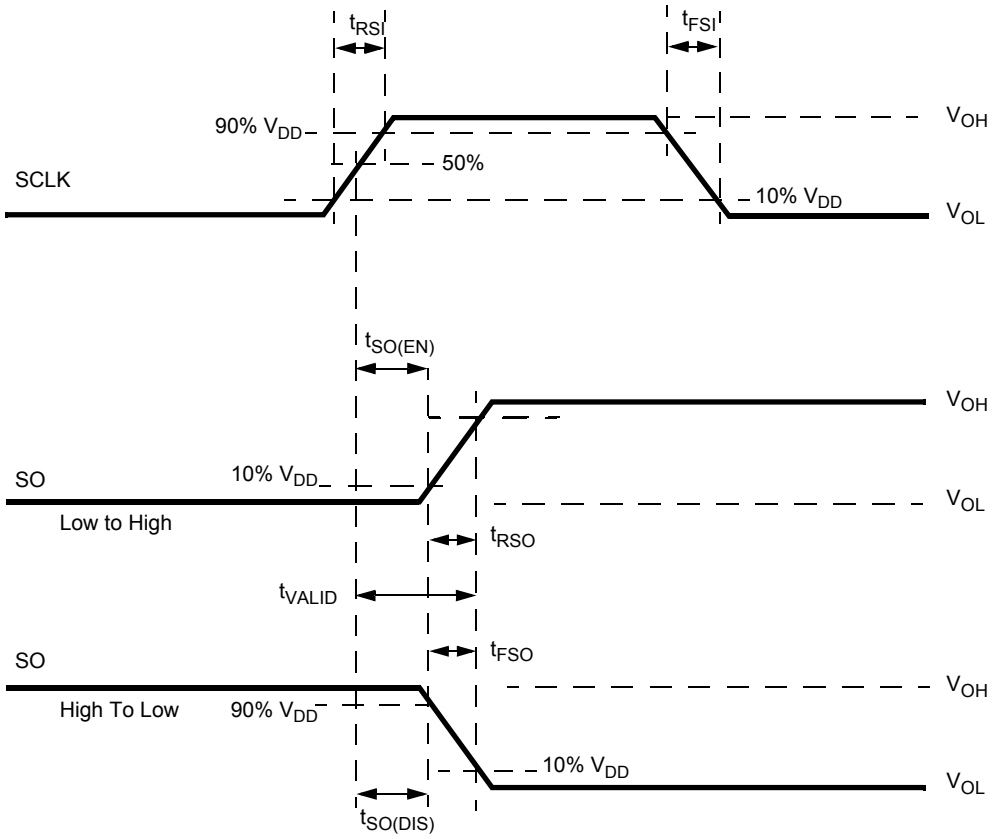


Figure 8. Timing Diagram for Serial Output (SO) Data Communication

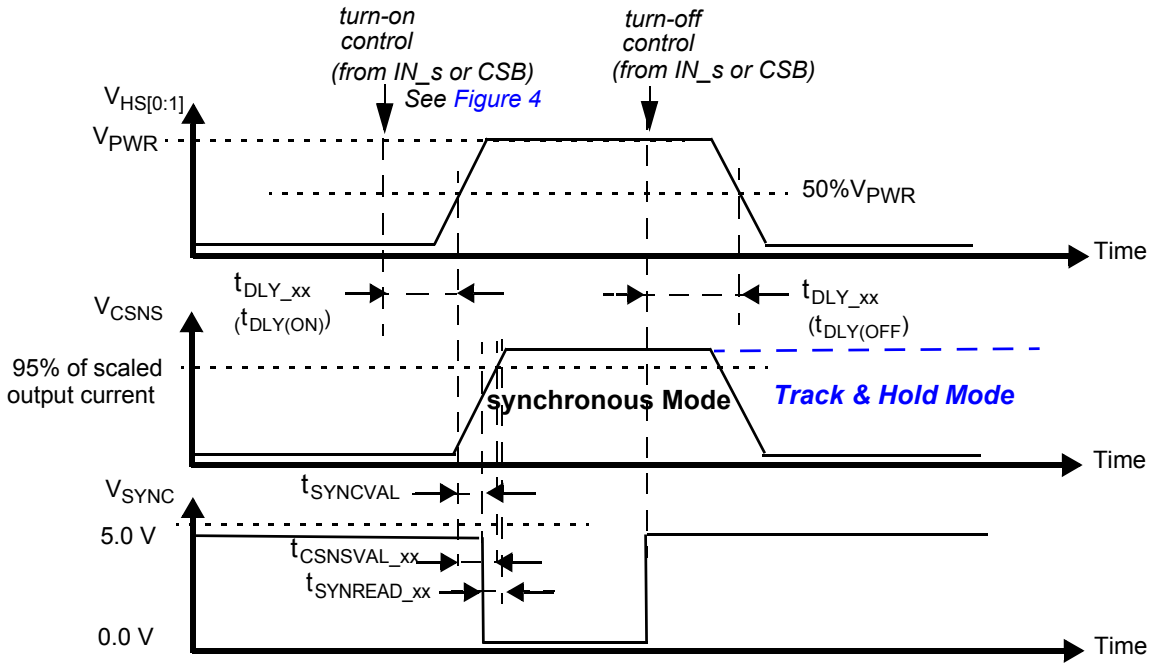


Figure 9. Synchronous & Track-and-Hold Current Sensing Modes: Associated Delay & Settling Times

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 10XSD200 is a two-channel, high side switch that can sustain up to 36 V, with integrated control and diagnostics designed for industrial applications. The device provides a high number of protective functions. Both low $R_{DS(ON)}$ channels (<10 mΩ) can independently drive various load types like light bulbs, solenoid actuators, or DC motors. Device control and diagnostics are configured through a 16-bit SPI port with daisy-chain capability.

Independently programmable output voltage slew rates allow satisfying electromagnetic compatibility (EMC) requirements.

Both channels can independently be operated in three different switching modes: internal clock and internal PWM mode (fully autonomous operation), external clock and internal PWM mode, and direct control switching mode.

Current sensing with an adjustable ratio is available on both channels, allowing both high-current (bulbs) and low-current (LED) monitoring. By activating the Track & Hold mode, current monitoring can be performed during the switch-Off phase. This allows random access to the current sense functionality. A patented offset compensation technique further enhances current sense accuracy.

To avoid turning off upon inrush current, while being able to monitor it, the device features a dynamic overcurrent threshold profile. For bulbs, this profile is a stair function with stages of which the height and width are programmable through the SPI port. DC motors can be protected from overheating by activating a specific window-shaped overcurrent profile that allow stall currents of limited duration.

Whenever communication with the external micro-controller is lost, the device enters Fail-safe Operation mode, but remains operational, controllable and protected.

PIN ASSIGNMENT AND FUNCTIONS

All logic input and output “pins” must be protected by series resistors of at least 1.0 kOhm, unless specified otherwise. Functions and register bits that are implemented independently for both channels have extension “_s”.

OUTPUT CURRENT MONITORING (CSNS)

The CS pin allows independent current monitoring of channel 0 or channel 1 up to the steady-state overcurrent threshold. It can also be used to sense the device temperature. The different functions are selected by setting bits CSNS1_en and CSNS0_en to the appropriate value (Table 22). When the CSNS pin is sensed during switch-off in the (optional) track & hold mode (see Figure 9), it outputs the scaled value of the load current as it was just before turn-Off. When several devices share the same pull-down resistor, the CSNS pins of devices, the current of which is not monitored, must be tri-stated. This is accomplished by setting CSNS0_en = 0 and CSNS1_en = 0 in their GCR register (Table 11). Settling time ($t_{CSNSVAL\_XX}$) is defined as the time between the instant at the middle of the output voltage’s rising edge (HS[0:1] = 50% of V_{PWR}), and the instant at which the voltage on the CSNS pin has settled to ±5.0% of its final value. Anytime an overcurrent window is active, the CSNS pin is disabled (see Overcurrent Detection on Resistive and Inductive Loads). The current and temperature sensing functions are unavailable in Fail-safe mode and in Normal mode when operating without the V_{DD} supply voltage. In order to generate a voltage output, this pin requires a pull-down resistor (R(CSNS)=1.0 kΩ typ. and 470 < R(CSNS) < 10 k). When the current sense resistor connected to the CSNS pin is disconnected, the CSNS voltage is clamped to $V_{CL(CSNS)}$. The CSNS pin can source currents up to about 5.6 mA.

CURRENT SENSE SYNCHRONIZATION (SYNC)

To synchronize current sensing with an external process, the SYNC signal can be connected to a digital input of an external MCU. An open-drain pull-down on SYNC indicates that the current sense signal is accurate and ready to be read. The current sense signal on the CSNS pin has the specified accuracy $t_{SYNREAD\_XX}$ seconds after the falling edge on the SYNC pin (Figure 9) and remains valid until a rising edge is generated. The rising edge that is generated by the SYNC pin at the turn-OFF instant (internal or external) may also be used to implement synchronization with the external MCU. Parameter $t_{SYNCVAL\_xx}$ is defined as the time between the instant at the middle of the output voltage rising edge (HS[0:1] = 50% of VPWR), and the instant at which the voltage on the SYNC-pin drops below 0.4 V (V_{SOL}). The SYNC pins of different devices can be connected together to save micro-controller input channels. However, in this configuration, the CSNS of only one device should be active at a time. Otherwise, the MCU is not be able to determine the source of the SYNC signal. The SYNC pin requires an external pull-up resistor to V_{DD}.

DIRECT CONTROL INPUTS (IN0 AND IN1)

The IN[0:1] pins allow direct control of both channels. A logic [0] level turns off the channel and a logic[1] level turns it on. When the device is in Sleep mode, a transition from logic 0 to logic 1 on any of these pins wakes it up (Channel configuration through the SPI). If it is desired to automatically turn on the channels after a transition to Fail-safe mode, inputs IN[0] and IN[1] must be externally connected to the VPWR pin by a pull-up resistor (e.g. 10 kΩ typ.). However,

this prevents the device from going into Sleep mode. Both IN pins are internally connected to a pull-down resistor.

CONFIGURATION INPUTS (CONF0 AND CONF1)

The CONF[0:1] input pins allow configuring both channels for the appropriate load type. CONF = 0 activates the bulb overcurrent protection profile, and CONF = 1 the DC motor profile. These inputs are connected to an internal voltage regulator of 3.3 V by an internal pull-up current source I_{UP}. Therefore, CONF = 1 is the default value when these pins are disconnected. Details on how to configure the channels are given in the table Overcurrent Profile Selection.

FAULT STATUS (FSB)

This open-drain output is asserted low when any of the following faults occurs (see Fault Mode): overcurrent (OC), overtemperature (OT), output connected to V_{PWR}, severe short-circuit (SC), OpenLoad in ON state (OL_ON), OpenLoad in OFF state (OL_OFF), external clock-fail (CLOCK_fail), overvoltage (OV), undervoltage (UV). Each fault type has its own assigned bit inside the STATR, FAULTR_s, or DIAGR_s register. Fault type identification and fault bit reset are accomplished by reading out these registers. The registers are part of the SO register (Table 12), and are accessed through the SPI port.

PWM CLOCK (CLOCK)

This pin is the input for an external clock signal that controls the internal PWM module.The clock signal is monitored by the device. The PWM module controls ON-time and turn-ON delay of the selected channels. The CLOCK pin should not be confused with the SCLK pin, which is the clock pin of the SPI interface. CLOCK has an internal pull-down current source (I_{DWN}) to GND.

RESET (RSTB)

All SPI register contents are reset when RSTB = 0. When RSTB = 0, the device returns to Sleep mode t_{IN} sec. after the last falling edge of the last active IN[0:1] signal. As long as the Reset input (RSTB pin) is at logic 0 and both direct input states remain low, the device remains in Sleep mode (Channel configuration through the SPI). A 0-to-1 transition on RSTB wakes the device and starts a watchdog timer to check the continuous presence of the SPI signals. To do this, the device monitors the contents of the first bit (WDIN bit) of all SPI words, following that transition (regardless the register it is contained in). When this contents is not alternated within a duration t_{WDTO}, SPI communication is considered lost, and Fail-safe mode is entered (Entering Fail-safe Mode). RSTB pin is internally pulled to GND by a R_{DWN} resistor.

CHIP SELECT (CSB)

Data communication over the SPI port is enabled when the CSB pin is in the logic [0] state. Data from the Input Shift registers are locked in the addressed SI registers on the rising edge of CSB. The device transfers the contents of one of the eight internal registers to the SO register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is at logic [0]. CSB is internally pulled up to V_{DD} through I_{UP}. (see Figure 7 and Figure 8).

SPI SERIAL CLOCK (SCLK)

The SCLK pin clocks the SPI data communication of the device. The serial input pin (SI) transfers data to the SI shift registers on the falling edge of the SCLK signal while data in the SO registers are transferred to the SO pin on the rising edge of the SCLK signal. The SCLK pin must be in low state when CSB makes any transition. For this reason, it is recommended to have the SCLK pin at a logic [0] state when the device is not accessed (CSB logic [1] state). When CSB is set to logic [1], signals at the SCLK and SI pins are ignored and the SO output is tri-stated (high-impedance). The SCLK pin is connected to an internal pull-down current source I_{DWN}.

SERIAL INPUT (SI)

Serial input (SI) data bits are shifted in at this pin. SI data is read on the falling edge of SCLK. 16-bit data packages are required on the SI pin (see Figure 7), starting with bit D15 (MSB) and ending with D0 (LSB). All the internal device registers are addressed and controlled by a 4-bit address (D9-D12) described in Table 10. Register addresses and function attribution are described in Table 11. The SI pin is internally connected to a pull-down current source, I_{DWN}.

SUPPLY OF THE DIGITAL CIRCUITRY (VDD)

This pin supplies the SPI circuit (3.3 V or 5.0 V). When lost, all circuitry is supplied by a V_{PWR} derived voltage, except the SPI's SO shift-register, which can no longer be read.

GROUND (GND)

This is the GND pin common for both the SPI and the other circuitry.

POSITIVE SUPPLY PIN (VPWR)

This pin is the positive supply and the common input pin of both switches. A 100 nF ceramic capacitor must be connected between VPWR and GND, close to the device. In addition, it is recommended to place a ceramic capacitor of at least 1.0 µF in parallel with this 100 nF capacitor.

SERIAL OUTPUT (SO)

The SO pin is a tri-stateable output pin that conveys data from one of the 13 internal SO registers, or from the previous SI register, to the outside world. The SO pin remains in a high-impedance state (tri-state) until the CSB pin becomes logic [0]. It then transfers the SPI data (device state, configuration, fault information). The SO pin changes state at the rising edge of the SCLK signal. For daisy-chaining, it can be read out on the falling edge of SCLK. V_{DD} must be present before the SO registers can be read. The SO register assignment is described in Table 12.

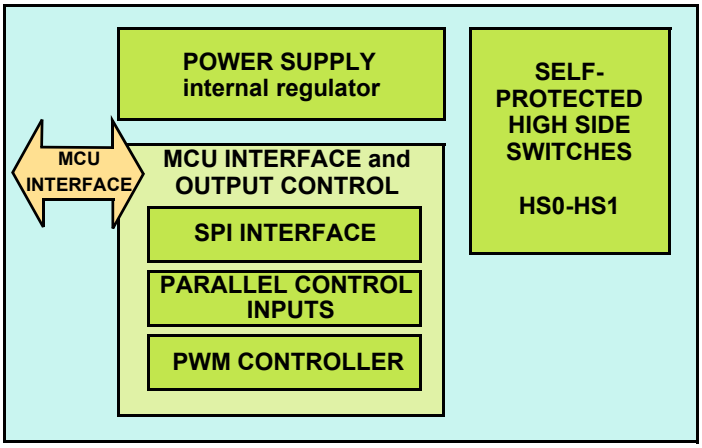
OUTPUT PINS (HS0 AND HS1)

HS0 and HS1 are the output pins of the power switches to be connected to the loads. A ceramic <= 22 nF (+/- 20%) capacitor is recommended between these pins and GND for optimal EMC performances.

FAIL-SAFE OUTPUT (FSOB)

This pin (active low) is used to indicate loss of SPI communication or loss of SPI supply voltage, V_{DD}. This open-drain output requires an external pull-up resistor to VPWR.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



POWER SUPPLY

The device operates with supply voltages from 6.0 to 58 V (V_{PWR}), but is full spec. compliant between 8.0 and 36 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VDD pin (5.0 V typ.) supplies the output register of the Serial Peripheral Interface (SPI). Consequently, the SPI registers cannot be read without presence of V_{DD}. The employed IC architecture guarantees a low quiescent current in Sleep mode.

SWITCH OUTPUT PINS HS0 & HS1

HS0 and HS1 are the output pins of the power switches. Both channels are protected against various kinds of short-circuits and have active clamp circuitry that may be activated when switching off inductive loads. Many protective and diagnostic functions are available. For large inductive loads, it is recommended to use a freewheeling diode. The device can be configured to control the output switches in parallel, which guarantees good switching synchronization.

COMMUNICATION INTERFACE AND DEVICE CONTROL

In Normal mode the output channels can either be controlled by the direct inputs or by the internal PWM module, which is configured by the data stored in the SPI registers. For bidirectional SPI communication, V_{DD} has to be in the authorized range. Failure diagnostics and configurations are also performed through the SPI port. The reported failure types are: OpenLoad, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, undervoltage, and overvoltage. The SPI port can be supplied either by a 5.0 V or by a 3.3 V voltage supply. For direct input control, V_{DD} is not required.

A Pulse Width Modulation (PWM) circuit allows driving loads at frequencies up to 1.0 kHz from an external or an internal clock. SPI communication is required to set these options.