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MC12311

Package Information
Case nnnn-xx
LGA-60 [8x8 mm]

Ordering Information

Device	Device Marking	Package
MC12311	MC12311	LGA-60

MC12311

Highly-integrated, cost-effective single-package solution for the sub-1 GHz, Wireless MBUS Standard

1 Introduction

The MC12311 is a highly-integrated, cost-effective, system-in-package (SIP), sub-1GHz wireless node solution with an FSK, GFSK, MSK, or OOK modulation-capable transceiver and low-power HCS08 8-bit microcontroller. The highly integrated RF transceiver operates over a wide frequency range including 315 MHz, 433 MHz, 470 MHz, 868 MHz, 915 MHz, 928 MHz, and 955 MHz in the license-free Industrial, Scientific and Medical (ISM) frequency bands. This configuration allows users to minimize the use of external components.

The MC12311 is targeted for the following low-power wireless applications:

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless MBUS Standard (EN13757-4:2005)

Contents

freescale™
semiconductor

Freescale supplements the MC12311 with tools and software that include hardware evaluation and development boards, software development IDE and applications, drivers, custom PHY usable with Freescale's IEEE 802.15.4 compatible MAC, SMAC and an available wireless MBUS solution.

2 Features

This section provides a simplified block diagram and highlights MC12311 features.

2.1 Block Diagram

Figure 1 shows a simplified block diagram of the MC12311.
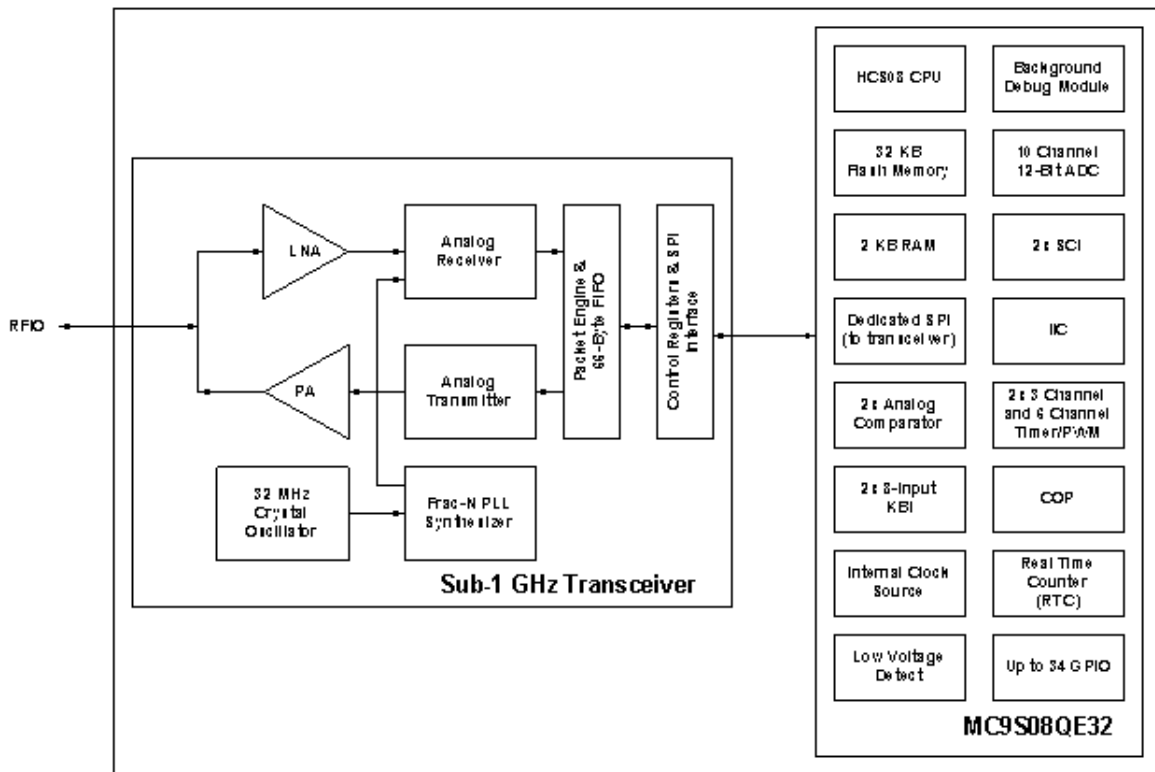
Figure 1. MC12311 Simplified Block Diagram

2.2 Features Summary

- RF Transceiver Features
  — High Sensitivity: down to -120 dBm at 1.2 kbps
  — High Selectivity: 16-tap FIR Channel Filter
  — Bullet-proof front end: IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB Blocking Immunity, no Image Frequency response
  — Low current: Rx = 16mA, 100nA register retention
  — Programmable Pout : -18 to +17 dBm in 1 dB steps
  — Constant RF performance over voltage range of chip

- — FSK bit rates up to 300 kbps
- — Fully integrated synthesizer with a resolution of 61 Hz
- — FSK, GFSK, MSK, GMSK and OOK modulations
- — Built-in Bit Synchronizer performing Clock recovery
- — Incoming Sync Word Recognition
- — Automatic RF Sense with ultra-fast AFC
- — Packet engine with CRC, AES-128 encryption and 66-byte FIFO
- — Built-in temperature sensor and Low battery indicator
- — 32 MHz crystal oscillator clock source
- 9S08QE32 MCU Features
  - — 8-Bit HCS08 Central Processor Unit (CPU) with CPU clock rate up to:
    - – 50.33 MHz at 3.6 V to 2.4V
    - – 40 MHz at 2.4V to 2.1V
    - – 20 MHz at 2.1V to 1.8V
  - — HC08 instruction set with added BGND instruction
  - — Support for up to 32 interrupt/reset sources
  - — 32 KB Flash and 2 KB RAM
  - — Low power modes (Wait plus Stop2 and Stop3 modes)
  - — Dedicated serial peripheral interface (SPI) connected internally to sub-1 GHz transceiver
  - — Multiple clock source options
    - – Internal clock generator (ICG) with 243 kHz oscillator that has +/-0.2% trimming resolution and +/-0.5% deviation across voltage.
    - – Startup oscillator of approximately 8 MHz
    - – External crystal or resonator
    - – External source from modem clock for very high accuracy source or system low-cost option
  - — In-circuit debug and FLASH programming available via on-chip background debug module (BDM)
  - — System protection features
    - – Programmable low voltage interrupt (LVI)
    - – Optional watchdog timer (COP)
    - – Illegal opcode detection
  - — Peripherals
    - – ADC — 10-channel, 12-bit resolution; 2.5 ms conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
    - – ACMPx — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3

- SCIx — Two serial communications interface modules with optional 13-bit break. Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake on active edge
- IIC — One IIC; up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
- TPMx — One 6-channel (TPM3) and two 3-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel;
- RTC — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components; runs in all MCU modes
— KBI — Two 8-bit port keyboard interrupt modules
— Input/Output
- Up to 33 GPIO including dedicated GPIO supporting transceiver
- 13 KBI interrupts with selectable polarity
- Hysteresis and configurable pullup device on all input pins; Configurable slew rate and drive strength on all output pins.
- 1.8 V to 3.6 V operating voltage with on-chip voltage regulators
- Temperature range of –40 °C to 85 °C
- 60-pin LGA (8x8 mm) Package

3 Software Solutions

Freescale will support the MC12311 platform with several software solutions:

- SMAC (Simple Media Access Controller) - This codebase provides simple communication and test apps based on drivers/PHY utilities available as source code. This environment is useful for hardware and RF debug, hardware standards certification, and developing proprietary applications.
- IEEE 802.15.4 MAC with custom PHY layer - The Freescale MAC is a robust, mature codebase useful for developing networking solutions. Freescale is implementing an IEEE 802.15.4 MAC-compatible custom sub-1 GHz PHY template that can be used across different frequency bands. This capability allows users to build powerful networking solutions on a known, stable codebase.
- Wireless MBUS stack - Freescale is porting an existing wireless MBUS codebase to the MC12311 platform which will be available through an external partner.

The Freescale MC12311 solutions are provided through a powerful software environment called the Freescale BeeKit Wireless Connectivity Toolkit. BeeKit is a comprehensive codebase of wireless networking libraries, application templates, and sample applications. The BeeKit Graphical User Interface (GUI), part of the BeeKit Wireless Connectivity Toolkit, allows users to create, modify, and update various wireless networking implementations. The MC12311 products are available as codebases within BeeKit; for the wireless MBUS stack, BeeKit will have simple demo apps only.

4   System-in-Package Sub-1 GHz Wireless Node

The MC12311 brings together a transceiver chip and an MCU chip on a single substrate to provide a small footprint, cost-effective sub-1 GHz wireless node. The transceiver is controlled by the MCU through a dedicated SPI interface. The SPI bus interface and some status signals are connected onboard the substrate to eliminate the need for external connections.

4.1   RF Transceiver

The transceiver (see Figure 2) is a single-chip integrated circuit ideally suited for today's high performance ISM band RF applications. Its advanced features set, including state of the art packet engine, greatly simplifies system design while the high level of integration reduces the external RF component bill of material (BOM) to a handful of passive de-coupling and matching components. It is intended for use as a high-performance, low-cost FSK and OOK RF transceiver for robust, frequency agile, half-duplex bi-directional RF links.

The MC12311 is intended for applications over a wide frequency range, including the 433 MHz and 868 MHz European and the 902-928 MHz North American ISM bands. Coupled with a link budget in excess of 135 dB, the transceiver advanced system features include a 66 byte TX/RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIOs which greatly enhance system flexibility while at the same time significantly reducing MCU requirements. The transceiver complies with both ETSI and FCC regulatory requirements.

Figure 2. MC12311 Transceiver Block Diagram
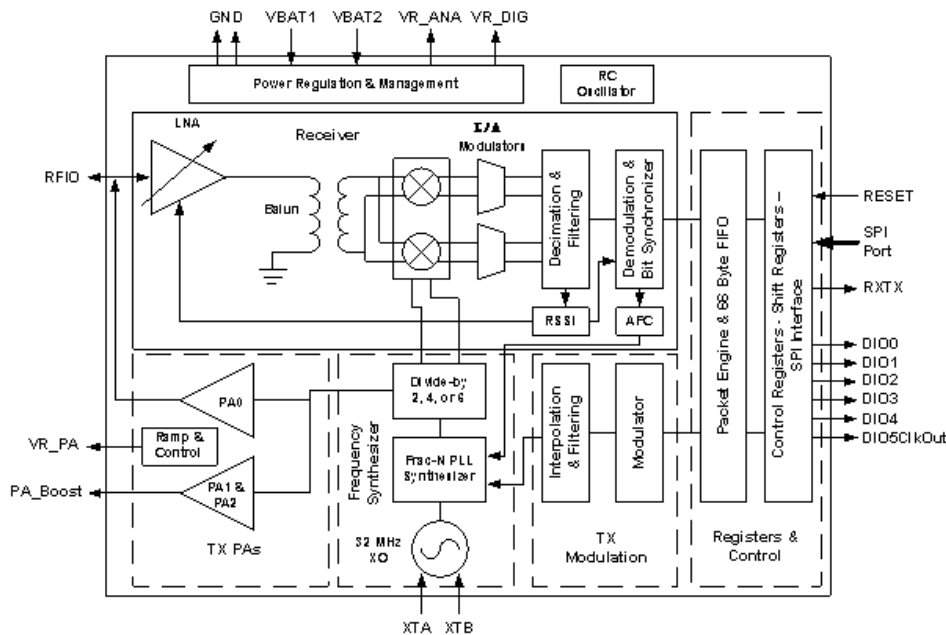
The major RF communication parameters of the MC12311 transceiver are programmable and most can be dynamically set. This feature offers the unique advantage of programmable narrow-band and wide-band communication modes without the need to modify external components. The transceiver is also optimized for low power consumption while offering high RF output power and channelized operation.

4.2   9S08QE32 MCU

The onboard 9S08QE32 MCU integrated circuit features an HC08 8-bit CPU, 2 KB RAM, 32 KB Flash memory, and a rich set of peripherals (see Section 2.2, "Features Summary"). The RF transceiver is controlled through the MCU SPI port which is dedicated to the RF device interface. Two of the transceiver status IO lines are also directly connected to the MCU GPIO to monitor the transceiver operation. In addition, the transceiver reset and additional status can be connected to the MCU through external connections.
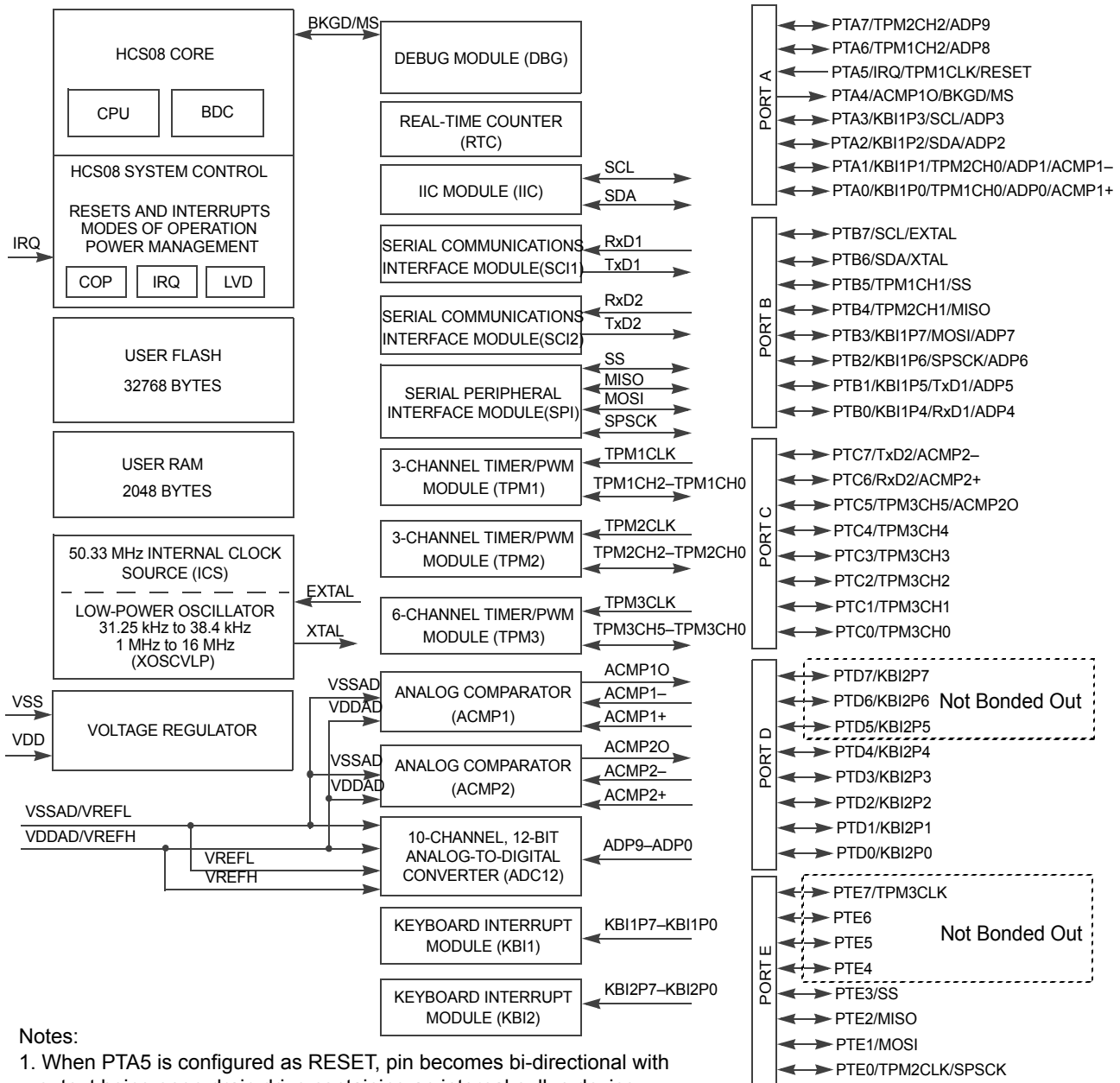
Notes:
1. When PTA5 is configured as RESET, pin becomes bi-directional with output being open-drain drive containing an internal pullup device.
2. When PTA4 is configured as BKGD, pin becomes bi-directional.
3. Pins PTD7-PTD5 and PTE7-PTE4 not bonded out.

Figure 3. MC12311 MCU Block Diagram

Operational modes of the MC12311 are determined by the software running on the MCU. The 9S08QE32 itself has its normal run mode as well as two low power modes (Stop2 and Stop3). The MCU in turn sets the operational mode of the transceiver which include sleep, standby, and radio operational modes.

Two common application scenarios are:

- Low power, battery-operated standalone wireless node - a common example of this configuration would be a remote sensor monitor. The wireless node programmed for standalone operation, typically has a low active-mode duty cycle, and is designed for long battery life, i.e., lowest power.

- Communication channel to a higher level controller - in this example, the wireless node implements the lower levels of a communications stack and is subordinate to the primary controller. Typically the MC12311 is connected to the controller through a command channel implemented via a UART/SCI port or other serial communication port.

4.3   System Clock Configuration

The MC12311 device allows for a wide array of system clock configurations:

- Pins are provided for a separate external clock source for the MCU. The external clock source can by derived from a crystal oscillator or from an external clock source

- Pins are provided for a 32 MHz crystal for the transceiver reference clock source (required)

- The transceiver can be programmed to provide a ClkOut programmable frequency clock output that can be used as an external source to the CPU. As a result, a single crystal system clock solution is possible (see Figure 4).

- The MCU provides a trimmable internal reference clock and also supports an external clock source. An optional onboard frequency locked loop (FLL) can be used with either clock source to support a CPU clock as high as 50 Mhz at 3.6 V to 2.4 V VDD.
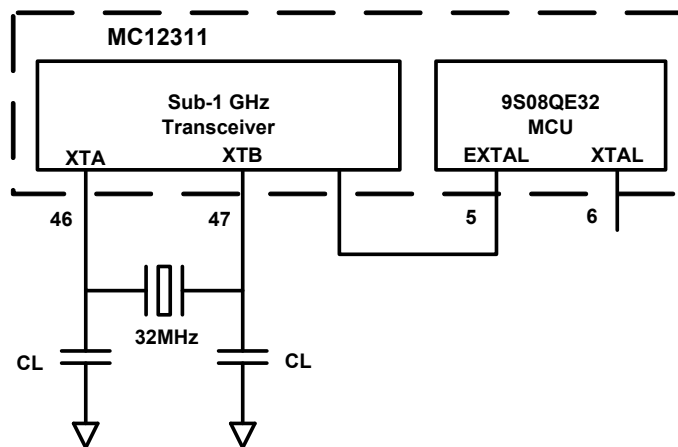
Figure 4. MC12311 Single Crystal System Clock Connection

5 MC12311 Pin Assignments and Connections

Figure 5 shows the MC12311 pinout.
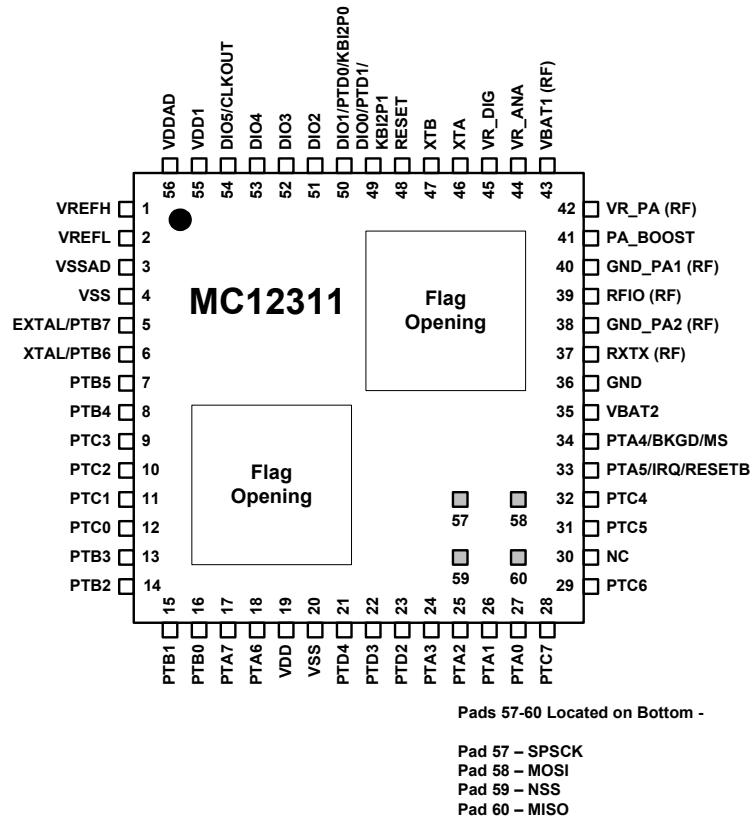
Figure 5. MC12311 Pinout (Top View)

Pads 57-60 Located on Bottom -

Pad 57 – SPSCK
Pad 58 – MOSI
Pad 59 – NSS
Pad 60 – MISO

5.1 Pin Definitions

Table 1 details the MC12311 pinout and functionality.

Table 1. Pin Function Description

Pin #	Pin Name	Type	Description	Functionality
1	VREFH	Input	MCU high reference voltage for ATD	
2	VREFL	Input	MCU low reference voltage for ATD	
3	VSSAD	Power Input	MCU ADC Ground	Connect to ground
4	VSS	Power Input	MCU Ground	Connect to ground
5	EXTAL/SCL/PTB7[1]	Input / Digital Input/Output	MCU Crystal Oscillator input / IIC bus clock / Port B Bit 7	• Normally used as MCU clock source • Driven from transceiver ClkOut (DIO5)
6	XTAL/SDA/PTB6[1]	Output / Digital Input/Output	MCU Crystal Oscillator output / IIC bus data / Port B Bit 6	

Table 1. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
7	PTB5/TPM1CH1[2]	Digital Input/Output	MCU Port B Bit 5 / TPM1 Channel 1	
8	PTB4/TPM2CH1[2]	Digital Input/Output	MCU Port B Bit 4 / TPM2 Channel 1	
9	PTC3/TPM3CH3	Digital Input/Output	MCU Port C Bit 3 / TPM3 Channel 3	
10	PTC2/TPM3CH2	Digital Input/Output	MCU Port C Bit 2/ TPM3 Channel 2	
11	PTC1/TPM3CH1	Digital Input/Output	MCU Port C Bit 1 / TPM3 Channel 1	
12	PTC0/TPM3CH0	Digital Input/Output	MCU Port C Bit 0 / TPM3 Channel 0	
13	PTB3/KBI1P7/ ADP7[2]	Digital Input/Output / Analog Input	MCU Port B Bit 3 / KBI1 Input Bit 7 / ADC Analog Channel 7	
14	PTB2/KBI1P6/ ADP6[2]	Digital Input/Output / Analog Input	MCU Port B Bit 2 / KBI1 Input Bit 6 / ADC Analog Channel 6	
15	PTB1/KBI1P5/TxD1 /ADP5	Digital Input/Output / Analog Input	MCU Port B Bit 1 / KBI1 Input Bit 5 / SCI1 TxD / ADC Analog Channel 5	
16	PTB0/KBI1P4/ RXD1/ADP4	Digital Input/Output / Analog Input	MCU Port B Bit 0 / KBI1 Input Bit 4 / SCI1 RXD / ADC Analog Channel 4	
17	PTA7/TPM2CH2/ ADP9	Digital Input/Output / Analog Input	MCU Port A Bit 7 / TPM2 Channel 2 / ADC Analog Channel 9	
18	PTA6/TPM1CH2/ ADP8	Digital Input/Output / Analog Input	MCU Port A Bit 6 / TPM1 Channel 2 / ADC Analog Channel 8	
19	VDD	Power Input	MCU VDD	Connect to MC12311 VDD supply
20	VSS	Power Input	MCU Ground	Connect to ground
21	PTD4/KBI2P4	Digital Input/Output	MCU Port D Bit 4 / KBI2 Input Bit 4	
22	PTD3/KBI2P3	Digital Input/Output	MCU Port D Bit 3 / KBI2 Input Bit 3	
23	PTD2/KBI2P2	Digital Input/Output	MCU Port D Bit 2 / KBI2 Input Bit 2	
24	PTA3/KBI1P3/ SCL/ADP3[1]	Digital Input/Output / Analog Input	MCU Port A Bit 3 / KBI1 Input Bit 3 / IIC bus clock / ADC Analog Channel 3	

Table 1. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
25	PTA2/KBI1P2/ SDA/ADP2[2]	Digital Input/Output / Analog Input	MCU Port A Bit 2 / KBI1 Input Bit 2 / IIC bus data / ADC Analog Channel 2	
26	PTA1/KBI1P1/ TPM2CH0/ADP1/ ACMP1-[3]	Digital Input/Output / Analog Input	MCU Port A Bit 1 / KBI1 Input Bit 1 / TPM2 Channel 0 / ADC Analog Channel 1 / ACMP1 Analog Input Minus	
27	PTA0/KBI1P0/ TPM1CH0/ADP0/ ACMP1+[3]	Digital Input/Output / Analog Input	MCU Port A Bit 0 / KBI1 Input Bit 0 / TPM1 Channel 0 / ADC Analog Channel 0 / ACMP1 Analog Input Plus	
28	PTC7/TXD2/ ACMP2-	Digital Input/Output / Analog Input	MCU Port C Bit 7 / SCI2 TXD / ACMP2 Analog Input Minus	
29	PTC6/RXD2/ ACMP2+	Digital Input/Output	MCU Port C Bit 6 / SCI2 RXD / ACMP2 Analog Input Plus	
30	NC		No Connect	
31	PTC5/TPM3CH5/ ACMP2O	Digital Input/Output	MCU Port C Bit 5 / TPM3 Channel 5 / ACMP2 Output	
32	PTC4/TPM3CH4	Digital Input/Output	MCU Port C Bit 5 / TPM3 Channel 5 / ACMP2 Output	
33	PTA5/IRQ/ TPM1CLK/RESETB	Digital Input/Output	MCU Port A Bit 5 / MCU IRQ / TPM1 Clock / MCU RESET	
34	PTA4/ACMP1O/ BKGD/MS	Digital Input/Output	MCU Port A Bit 4 / ACMP1 Output / Background Debug Port / Mode Select	
35	VBAT2	Power Input	Transceiver VDD	Connect to MC12311 VDD supply
36	GND	Power Input	Transceiver Ground	Connect to ground
37	RXTX (RF)	Digital Output	Transceiver Rx/Tx RF Switch Control Output; high when in TX	
38	GND_PA2 (RF)	Power Input	Transceiver RF Ground	Connect to ground
39	RFIO (RF)	RF Input/Output	Transceiver RF Input/Output	
40	GND_PA1 (RF)	Power Input	Transceiver RF Ground	Connect to ground
41	PA_BOOST	RF Output	Transceiver Optional High-Power PA Output	
42	VR_PA	Power Output	Transceiver regulated output voltage for VR_PA use.	
43	VBAT1 (RF)	Power Input	Transceiver VDD for RF circuitry	Connect to MC12311 VDD supply
44	VR_ANA	Power Output	Transceiver regulated output voltage for analog circuitry.	Decouple to ground with 100 nF capacitor

Table 1. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
45	VR_DIG	Power Output	Transceiver regulated output voltage for digital circuitry.	Decouple to ground with 100 nF capacitor
46	XTA	Xtal Osc	Transceiver crystal reference oscillator	Connect to 32 MHz crystal and load capacitor
47	XTB	Xtal Osc	Transceiver crystal reference oscillator	Connect to 32 MHz crystal and load capacitor
48	RESET	Digital Input	Transceiver hardware reset input	Typically driven from MCU GPIO
49	DIO0/PTD1/KBI2P1	Digital Input/Output	Transceiver GPIO Bit 0 / MCU Port D Bit 1 / MCU KBI2 Bit 1	MCU IO and Transceiver IO connected onboard MC12311
50	DIO1/PTD0/KBI2P0	Digital Input/Output	Transceiver GPIO Bit 1 / MCU Port D Bit 0 / MCU KBI2 Bit 0	MCU IO and Transceiver IO connected onboard MC12311
51	DIO2	Digital Input/Output	Transceiver GPIO Bit 2	
52	DIO3	Digital Input/Output	Transceiver GPIO Bit 3	
53	DIO4	Digital Input/Output	Transceiver GPIO Bit 4	
54	DIO5/CLKOUT	Digital Input/Output	Transceiver GPIO Bit 5 / ClkOut	Commonly programmed as ClkOut to supply MCU clock; connect to Pin 5
55	VDD1	Power Input	MCU VDD supply	Connect to MC12311 VDD supply
56	VDDAD	Power Input	MCU ADC VDD	Connect to MC12311 VDD supply
57	SPSCK[2]	Digital Input/Output	SPI Port Clock driven from MCU Port E Bit 0	• MCU IO and Transceiver IO connected onboard MC12311 • MCU IO must be configured for this connection
58	MOSI[2]	Digital Input/Output	SPI Port MOSI signal connected to MCU Port E Bit 1	• MCU IO and Transceiver IO connected onboard MC12311 • MCU IO must be configured for this connection
59	NSS[2]	Digital Input/Output	SPI Port $\overline{SS}$ signal connected to MCU Port E Bit 3	• MCU IO and Transceiver IO connected onboard MC12311 • MCU IO must be configured for this connection
60	MISO[2]	Digital Input/Output	SPI Port MISO signal connected to MCU Port E Bit 2	• MCU IO and Transceiver IO connected onboard MC12311 • MCU IO must be configured for this connection
FLAG	VSS	Power input	External package flag. Common VSS	Connect to ground.

[1] IIC pins, SCL and SDA can be repositioned using the IICPS bit in SOPT2; default locations are PTA3 and PTA2.

[2] The SPI Port pin selection must be configured by software by writing the SPIPS Bit in Register SOPT2

[3] If ADC and ACMP1 are both enabled, both modules have access to the pin.

5.2　Internal Functional Interconnects

The MCU provides control to the transceiver through the SPI Port and receives status from the transceiver from the DIOx pins. Certain interconnects between the devices are routed onboard the SiP. In addition, the signals are brought out to external pads.

Table 2. MC12311 Internal Functional Interconnects

Pin #	MCU Signal	Transceiver Signal	Description
49	PTD1/KBI2P1	DIO0	Transceiver DIO0 can be programmed to provide status to the MCU
50	PTD0/KBI2P0	DIO1	Transceiver DIO1 can be programmed to provide status to the MCU
57	PTE0/SPSCK	SCK	MCU SPI connection must be initiated, not default
58	PTE1/MOSI	MOSI	MCU SPI connection must be initiated, not default
59	PTE3/SS	NSS	MCU SPI connection must be initiated, not default
60	PTE2/MISO	MISO	MCU SPI connection must be initiated, not default

NOTE
- As shown in Table 2, the MCU SPI Port pin selection must be configured by software by writing the SPIPS bit in Register SOPT2
- The transceiver DIO pins must be programmed to provide desired status

5.3　External Functional Interconnects

In addition to the onboard device interconnection, other external connections between the MCU and the transceiver are common:

1. Freescale recommends programming the transceiver DIO5 signal as ClkOut - for lowest system cost, a single crystal configuration can be used where ClkOut can be used to supply the MCU clock by connection to EXTAL Pin 5. With a 32 MHz transceiver reference oscillator crystal, ClkOut can be programmed for frequencies of 32 MHz, 16 MHz, 8 MHz, 4 MHz, 2 MHz, and 1 MHz.

2. Freesacle recommends driving/controlling the transceiver reset from an MCU GPIO - This allows over-riding control of the transceiver from the system application.

3. The other DIO2-DIO4 status and RXTX signals can prove useful for monitoring the transceiver operation - the DIO4-DIO2 signals must be programmed to provide operational status. All signals must be connected externally to appropriate MCU GPIO for this function.

6　System and Power Management

The MC12311 consists of an independent transceiver and MCU. The MCU controls the transceiver through programming of the SPI Port, and sets its operational mode through this control channel. Total current draw for the MC12311 is dependent on the operation mode of both devices.

6.1 Modes of Operation

The MCU is the host controller and has the following primary modes of operation:

- Stop2 - provides lowest standby power consumption and maintains the contents of RAM and the current state of all of the I/O pins, but the main oscillator and most other digital circuitry are off. Wake-up is treated as a system recovery from reset.

- Stop3 - provides very low standby power consumption and maintains the contents of RAM, registers, and the current state of all of the I/O pins, but the main oscillator can be enabled or not. Wake-up is treated as an interrupt request, and this provides faster recovery time

- Wait - entered by executing a WAIT command, the CPU enters a low power state. This state can be used to save power over a normal RUN condition, but is not a true low power state such as Stop2 or Stop3

- Run - normal run condition for the CPU. Current draw is very dependent on the CPU clock frequency. Additional current can be saved but running at a lower clock rate if the software performance.

The transceiver has the following modes of operation:

- Sleep - provides lowest power consumption and is the full power down state

- Idle - provides very low standby power consumption and has the main voltage regulator and the RC oscillator enabled

- Standby - similar to Idle with low standby power consumption but has the main voltage regulator and the crystal oscillator enabled

- FS (Frequency synthesizer) - the frequency synthesizer is alive to shorten startup time to transmit or receive states

- Transmit - transmitter is active

- Receive - receiver is active

6.2 Power Management

The MC12311 power management is controlled through programming of the modes of operation. Different modes allow for different levels of power-down. Additional features include:

- Transceiver Sleep with MCU Stop2 is the lowest power state

- The transceiver mode is independent of the MCU

- The transceiver uses/powers-up the transmitter or receiver only as required

- MCU peripheral control clock gating can be disabled on a module-by-module basis to provide lowest power

- RTC can be used as wake-up timer

- Wake-up available through KBI asynchronous interrupts and UART activity

- Wake-up available with RTC

6.3 System Protection

The MC12311 provides several vehicles to maintain security or a high level of system robustness:

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- Flash block protection

7 Development Environment

Development support for the HCS08 on the MC12311 includes the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire debug interface to the MCU that provides a convenient interface for programming the on-chip FLASH and other storage. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

Address and data bus signals are not available on external pins. Debug is done through commands fed into the MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals. Features include:

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints)
- On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes

8 System Electrical Specification

This section details maximum ratings for the 60 pin LGA package and recommended operating conditions, DC characteristics, and AC characteristics for the modem, and the MCU.

8.1 SiP LGA Package Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum rating is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused

inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3 shows the maximum ratings for the 60 Pin LGA package.

Table 3. LGA Package Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Junction Temperature	T_J	95	°C
Storage Temperature Range	T_{stg}	-55 to 115	°C
Power Supply Voltage	V_{BATT}, V_{DDINT}	-0.3 to 3.8	Vdc
Digital Input Voltage	Vin	-0.3 to (V_{DDINT} + 0.3)	
RF Input Power	P_{max}	6	dBm

Note: Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the limits in the Electrical Characteristics
or Recommended Operating Conditions tables.
Note: Meets Human Body Model (HBM) = 2 kV. RF input/output pins have no ESD protection.

8.2   ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with the JESD22 Stress Test Qualification for Commercial Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

All latchup testing is in conformity with the JESD78 IC Latch-Up Test.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification.

Table 4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin[1]	—	1	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin[1]	—	1	
Latch-up	Minimum input voltage limit		– 1.8	V
	Maximum input voltage limit		4.32	V

[1] This number represents a minimum number for both positive pulse(s) and negative pulse(s)

Table 5. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 750	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	± 100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

8.3 Transceiver Electrical Characteristics

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1= VBAT2=VDD=3.3 V, temperature = 25 °C, FXOSC = 32 MHz, FRF = 915 MHz, Pout = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

NOTE

Unless otherwise specified, the performances in the other frequency bands are similar or better.

8.3.1 Transceiver Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BATT})		1.8		3.6	Vdc
Operating Temperature Range	T_A	-40	25	85	°C
Logic Input Voltage Low	V_{IL}	0	-	20% V_{BATT}	V
Logic Input Voltage High	V_{IH}	80% V_{BATT}	-	V_{BATT}	V
Logic Output Voltage Low (I_{max} = -1 mA)	V_{OL}	0	-	10% V_{BATT}	V
Logic Output Voltage High (I_{max} = 1 mA)	V_{OH}	90% V_{BATT}	-	V_{BATT}	V
Load capacitance on digital ports	C_L			25	pF
SPI Clock Rate	f_{SPI}	-	-	8.0	MHz
RF Input Power	P_{max}	-	-	0	dBm
Crystal Reference Oscillator Frequency	f_{ref}	32 MHz Only			

8.3.2 Transceiver Power Consumption

Table 7. Power Supply Current

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Supply current in Sleep mode		IDDSL	-	0.1	1	µA
Supply current in Idle mode	RC oscillator enabled	IDDIDLE	-	1.2	-	µA
Supply current in Standby mode	Crystal oscillator enabled	IDDST	-	1.25	1.5	mA
Supply current in Synthesizer mode		IDDFS	-	9	-	mA
Supply current in Receive mode		IDDR	-	16	-	mA
Supply current in Transmit mode with appropriate matching, stable across VDD range	RFOP = +17 dBm, on PA_BOOST RFOP = +13 dBm, on RFIO pin RFOP = +10 dBm, on RFIO pin RFOP = 0 dBm, on RFIO pin RFOP = -1 dBm, on RFIO pin	IDDT	- - - - -	95 45 33 20 16	- - - - -	mA mA mA mA mA

8.3.3 Transceiver Frequency Synthesis

Table 8. Frequency Synthesizer Specification

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Synthesizer Frequency Range	Programmable	FR	290 424 862	- - -	340 510 1020	MHz MHz MHz
Crystal oscillator frequency		FXOSC	-	32	-	MHz
Crystal oscillator wake-up time		TS_OSC	-	250	500	µs
Frequency synthesizer wake-up time to PllLock signal	From Standby mode	TS_FS	-	80	150	µs
Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	TS_HOP	- - - - - - -	20 20 50 50 80 80 80	- - - - - - -	µs µs µs µs µs µs µs
Frequency synthesizer step	$FSTEP = FXOSC/2^{19}$	FSTEP	-	61.0	-	Hz
RC Oscillator frequency	After calibration	FRC	-	62.5	-	kHz
Bit rate, FSK	Programmable	BRF	1.2	-	300	kbps
Bit rate, OOK	Programmable	BRO	1.2	-	32.768	kbps
Frequency deviation, FSK	Programmable FDA + BRF/2 =< 500 kHz	FDA	0.6	-	300	kHz

8.3.4   Receiver

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in RegRxBw, receiving a PN15 sequence with a BER of 0.1% (Bit Synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, by setting bit LnaZin in RegLna to 1. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level.

Table 9. Receiver Specification

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s	RFS_F	- - -	-118 -114 -105	- - -	dBm dBm dBm
	FDA = 5 kHz, BR = 1.2 kb/s [1]		-	-120	-	dBm
OOK sensitivity, highest LNA gain	BR = 4.8 kb/s	RFS_O	-	-112	-109	dBm
Co-Channel Rejection		CCR	-13	-10	-	dB
Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	ACR	- 37	42 42	- -	dB dB
Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	BI	- - -	-45 -40 -32	- - -	dBm dBm dBm
Blocking Immunity Wanted signal at sensitivity +16dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz		- - -	-36 -33 -25	- - -	dBm dBm dBm
AM Rejection , AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	AMR	- - -	-45 -40 -32	- - -	dBm dBm dBm
2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	IIP2	- -	+75 +35	- -	dBm dBm
3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	IIP3	- -23	+20 -18	- -	dBm dBm
Single Side channel filter BW	Programmable	BW_SSB	2.6	-	500	kHz
Image rejection in OOK mode	Wanted signal level = -106 dBm	IMR_OOK	27	30	-	dB
Receiver wake-up time, from PLL locked state to *RxReady*	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	TS_RE	- -	1.7 96	- -	ms µs
Receiver wake-up time, from PLL locked state, AGC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	TS_RE_AGC	-	3.0 163		ms µs
Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	TS_RE_AGC&AFC		4.8 265		ms µs
FEI sampling time	Receiver is ready	TS_FEI	-	$4.T_{bit}$	-	-
AFC Response Time	Receiver is ready	TS_AFC	-	$4.T_{bit}$	-	-

Table 9. Receiver Specification

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
RSSI Response Time	Receiver is ready		TS_RSSI	-	$2.T_{bit}$	-	-
RSSI Dynamic Range	AGC enabled	Min	DR_RSSI	-	-115	-	dBm
		Max		-	0	-	dBm

[1] Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver

8.3.5   Transmitter

Table 10. Transmitter Specidication

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
RF output power in 50 ohms On RFIO pin	Programmable with 1dB steps Max Min	RF_OP	- -	+13 -18	- -	dBm dBm
Max RF output power, on PA_BOOST pin	With external match to 50 ohms	RF_OPH	-	+17	-	dBm
RF output power stability	From VDD=1.8V to 3.6V	∆RF_OP	-	+/-0.3	-	dB
Transmitter Phase Noise	50 kHz Offset from carrier 868 / 915 MHz bands 434 / 315 MHz bands	PHN	- -	-95 -99	- -	dBc/Hz
Transmitter adjacent channel power (measured at 25 kHz offset)	BT=0.5 . Measurement conditions as defined by EN 300 220-1 V2.1.1	ACP	-	-	-37	dBm
Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10 µs, BR = 4.8 kb/s.	TS_TR	-	120	-	µs

8.4   MCU Electrical Characteristics

The following sections describe the electrical characteristics of the MC12311 MCU.

8.4.1   MCU DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 11. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage				1.8[2]		3.6	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	T				2.3 V, I_{Load} = –6 mA	V_{DD} – 0.5	—	—	
	C				1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	

Table 11. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	1.8 V, I_{Load} = 2 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = 10 mA	—	—	0.5	
	T				2.3 V, I_{Load} = 6 mA	—	—	0.5	
	C				1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
6	P	Input high voltage	all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
7	P	Input low voltage	all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C				V_{DD} >1.8 V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis	all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	all input only pins (Per pin)	$|I_{In|}$	V_{In} = V_{DD} or V_{SS}	—	—	1	μA
10	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$|I_{OZ|}$	V_{In} = V_{DD} or V_{SS}	—	—	1	μA
11	P	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$|I_{OZTOT}|$	V_{In} = V_{DD} or V_{SS}	—	—	2	μA
12	P	Pull-up resistors	all digital inputs, when enabled	R_{PU}		17.5	—	52.5	kΩ
13	D	DC injection current [3, 4, 5]	Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
14	C	Input Capacitance, all pins		C_{In}		—	—	8	pF
15	C	RAM retention voltage		V_{RAM}		—	0.6	1.0	V
16	C	POR re-arm voltage[6]		V_{POR}		0.9	1.4	1.79	V

Table 11. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
17	D	POR re-arm time	t_{POR}		10	—	—	µs
18	P	Low-voltage detection threshold — high range[7]	V_{LVDH}[8]	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
19	P	Low-voltage detection threshold — low range[7]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.86	1.82 1.90	1.91 1.99	V
20	P	Low-voltage warning threshold — high range[7]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
21	P	Low-voltage warning threshold — low range[7]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
22	C	Low-voltage inhibit reset/recover hysteresis[7]	V_{hys}		—	50	—	mV
23	P	Bandgap Voltage Reference[9]	V_{BG}		1.15	1.17	1.18	V

[1] Typical values are measured at 25°C. Characterized, not tested

[2] As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

[3] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[4] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[5] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[6] Maximum is highest voltage that POR is guaranteed.

[7] Low voltage detection and warning limits measured at 1 MHz bus frequency.

[8] Run at 1 MHz bus frequency

[9] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C
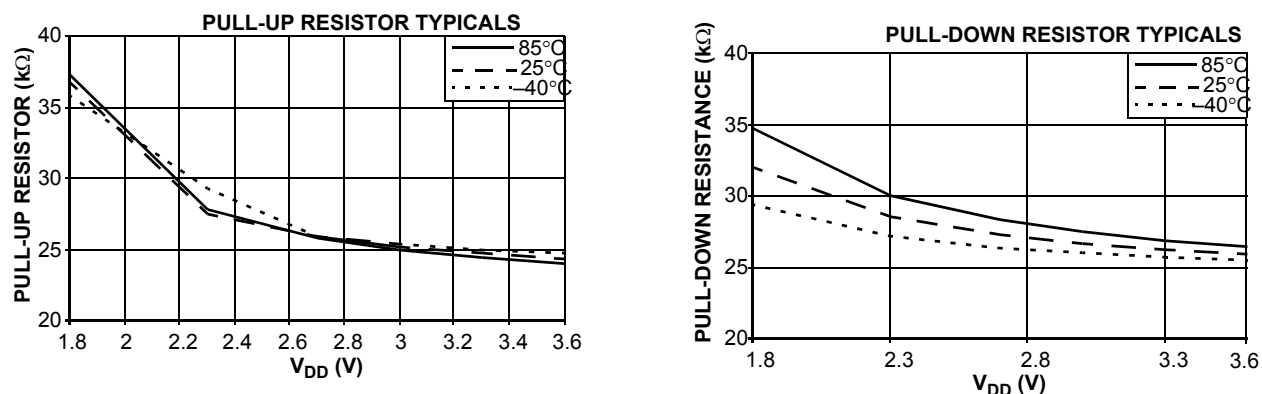
Figure 6. Pull-up and Pull-down Typical Resistor Values

TYPICAL V$_{OL}$ VS I$_{OL}$ AT V$_{DD}$ = 3.0 V
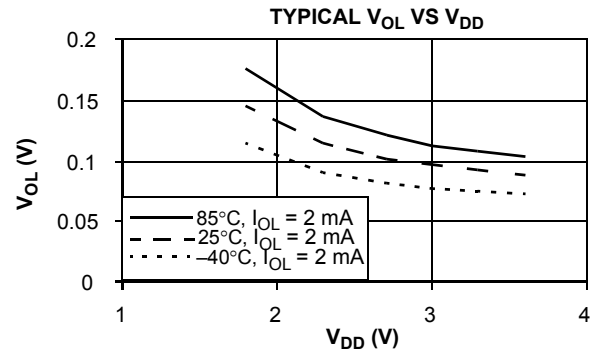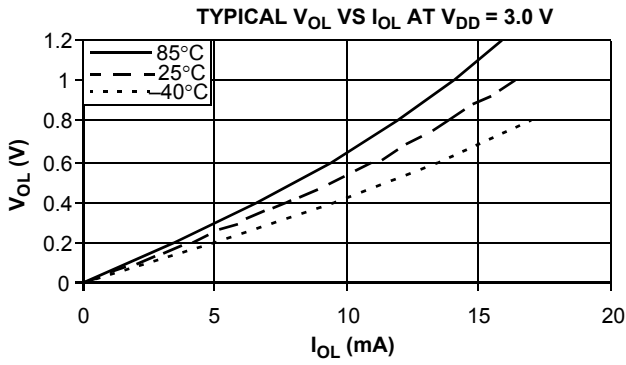
TYPICAL V$_{OL}$ VS V$_{DD}$

Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

TYPICAL V$_{OL}$ VS I$_{OL}$ AT V$_{DD}$ = 3.0 V

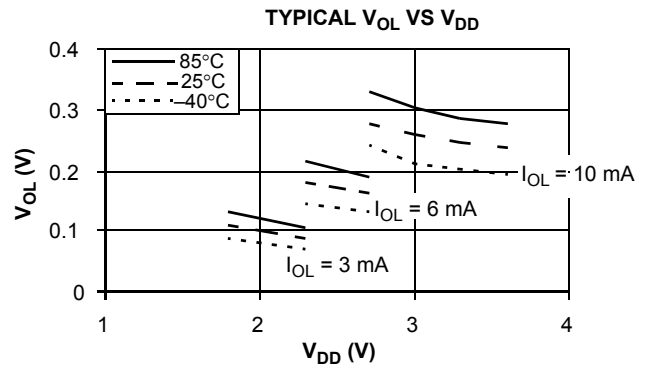**TYPICAL V$_{OL}$ VS V$_{DD}$**

Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)
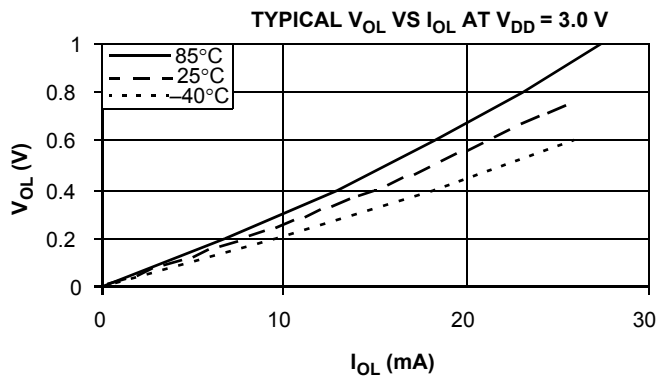
TYPICAL V$_{DD}$ − V$_{OH}$ VS I$_{OH}$ AT V$_{DD}$ = 3.0 V

TYPICAL V$_{DD}$ − V$_{OH}$ VS V$_{DD}$ AT SPEC I$_{OH}$
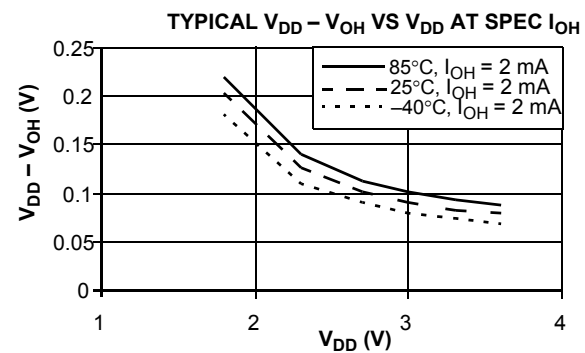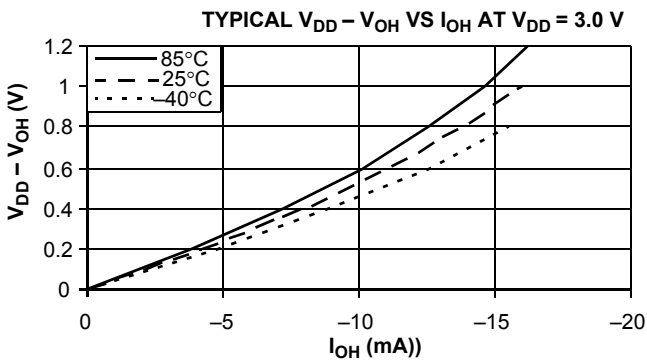
Figure 9. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

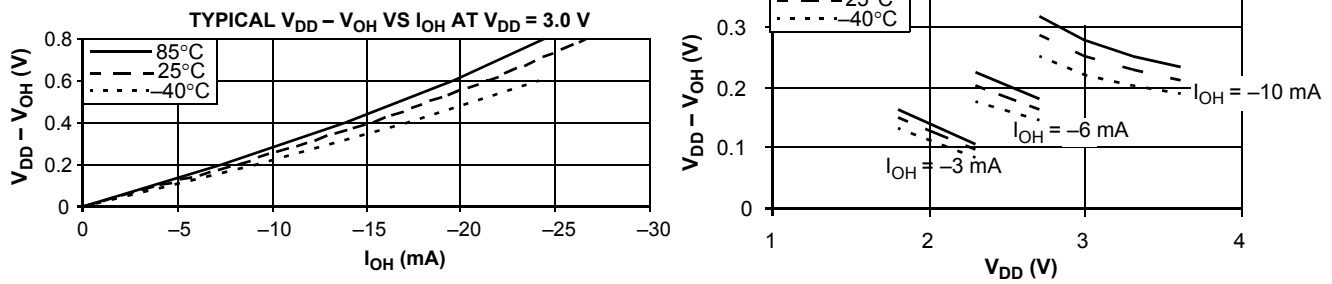**MC12311 Advance Information, Rev. 1.0**

Figure 10. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

8.4.2   MCU Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 12. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	13	184	mA	−40 to 25
	P					14	15		85
	T			20 MHz		13.75	—		−40 to 85
	T			8 MHz		5.59	—		
	T			1 MHz		1.03	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	11.5	12.3	mA	−40 to 85
	T			20 MHz		9.5	—		
	T			8 MHz		4.6	—		
	T			1 MHz		1.0	—		
3	T	Run supply current LPS=0, all modules off	RI_{DD}	16 kHz FBILP	3	152	—	μA	−40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	μA	0 to 70
							—		−40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		−40 to 85
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	5.74	6	mA	−40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		

Table 12. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current		$S2I_{DD}$	n/a	3	0.35	0.65	μA	–40 to 25
	C						0.8	1.0		70
	P						2.0	4.5		85
	C					2	0.25	0.5		–40 to 25
	C						0.65	0.85		70
	C						1.5	3.5		85
7	P	Stop3 mode supply current No clocks active		$S3I_{DD}$	n/a	3	0.45	1.0	μA	–40 to 25
	C						1.5	2.3		70
	P						4	8		85
	C					2	0.35	0.7		–40 to 25
	C						1	2		70
	C						3.5	6.0		85
8	T	Low power mode adders:	EREFSTEN=1		32 kHz	3	500		nA	–40 to 85
9	T		IREFSTEN=1		32 kHz		70		μA	
10	T		TPM PWM		100 Hz		12		nA	
11	T		SCI, SPI, or IIC		300 bps		15		μA	
12	T		RTC using LPO		1 kHz		200		μA	
13	T		RTC using ICSERCLK		32 kHz		1		μA	
14	T		LVD		n/a		100		μA	
15	T		ACMP		n/a		20		μA	

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 13. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	T	LPO		50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]		63	70	77	81	uA
4	T	RTC	does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	uA
6	T	ACMP[1]	not using the bandgap (BGBE = 0)	18	20	22	23	uA
7	T	ADC[1]	ADLPC = ADLSMP = 1 not using the bandgap (BGBE = 0)	95	106	114	120	uA

8.4.3 External Oscillator (XOSCVLP) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 14. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	f_{lo} f_{hi} f_{hi}	32 1 1	— — —	38.4 16 8	kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	— — —	— 10 1	— — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) $\geq$ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	— 0 100 0 0 0	— — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	t_{CSTL} t_{CSTH}	— — — —	200 400 5 15	— — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode FBELP mode	f_{extal}	0.03125 0	— —	40.0 50.33	MHz MHz

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

[2] Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

[3] See crystal or resonator manufacturer's recommendation.

[4] Proper PC board layout procedures must be followed to achieve specifications.