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Freescale Semiconductor
Technical Data

Document Number: MC1321x
Rev. 1.8 08/2009

MC1321x

Package Information
Case 1664-01
71-pin LGA [9x9 mm]

Ordering Information

Device	Device Marking	Package
MC13211[1]	13211	LGA
MC13212[1]	13212	LGA
MC13213[1]	13213	LGA

[1] See Table 1 for more details.

MC13211/212/213

ZigBee™- Compliant Platform - 2.4 GHz Low Power Transceiver for the IEEE® 802.15.4 Standard plus Microcontroller

1 Introduction

The MC1321x family is Freescale's second-generation ZigBee platform which incorporates a low power 2.4 GHz radio frequency transceiver and an 8-bit microcontroller into a single 9x9x1 mm 71-pin LGA package. The MC1321x solution can be used for wireless applications from simple proprietary point-to-point connectivity to a complete ZigBee mesh network. The combination of the radio and a microcontroller in a small footprint package allows for a cost-effective solution.

The MC1321x contains an RF transceiver which is an 802.15.4 Standard compliant radio that operates in the 2.4 GHz ISM frequency band. The transceiver includes a low noise amplifier, 1mW nominal output power, PA with internal voltage controlled oscillator (VCO), integrated transmit/receive switch, on-board power supply regulation, and full spread-spectrum encoding and decoding.

The MC1321x also contains a microcontroller based on the HCS08 Family of Microcontroller Units (MCU), specifically the HCS08 Version A, and can provide up to 60KB of flash memory and 4KB of RAM. The onboard

Contents

MCU allows the communications stack and also the application to reside on the same system-in-package (SIP). The MC1321x family is organized as follows:

- The MC13211 has 16KB of flash and 1KB of RAM and is an ideal solution for low cost, proprietary applications that require wireless point-to-point or star network connectivity. The MC13211 combined with the Freescale Simple MAC (SMAC) provides the foundation for proprietary applications by supplying the necessary source code and application examples to get users started on implementing wireless connectivity.
- The MC13212 contains 32K of flash and 2KB of RAM and is intended for use with the Freescale fully compliant 802.15.4 MAC. Custom networks based on the 802.15.4 Standard MAC can be implemented to fit user needs. The 802.15.4 Standard supports star, mesh and cluster tree topologies as well as beaconed networks.
- The MC13213 contains 60K of flash and 4KB of RAM and is also intended for use with the Freescale fully compliant 802.15.4 MAC and the fully ZigBee compliant Freescale BeeStack.

WARNING

- The MC1321x now uses an updated version of the 689S08A 8-bit microprocessor to correct errata associated with the onboard FLL and reset pin. Refer to the associated errata for this new device, *Document Number MSE9S08GB60A_4L11Y*, on the Freescale web site.
- The MC1321x also now uses an updated version of the transceiver device that is functionally fully compliant with earlier versions of the transceiver.

However, for proper performance of the radio the following modem registers must be over-programmed:

Register 0x31 to 0xA0C0

Register 0x34 to 0xFEC6

These registers must be over-programmed for MC1321x devices in which the modem Chip_ID Register 0x2C reads 0x6800.

Applications include, but are not limited to, the following:

- Residential and commercial automation
  - Lighting control
  - Security
  - Access control
  - Heating, ventilation, air-conditioning (HVAC)
  - Automated meter reading (AMR)
- Industrial Control
  - Asset tracking and monitoring
  - Homeland security
  - Process management
  - Environmental monitoring and control

- HVAC
- Automated meter reading

- Health Care
  - Patient monitoring
  - Fitness monitoring
- Consumer
  - Human interface devices (keyboard, mice, etc.)
  - Remote control
  - Wireless toys

1.1 Ordering Information

Table 1 provides additional details about the MC1321x family.

NOTE

The device marking for silicon revision 1.1 and newer is different than version 1.0 and older. For more details about the 71-pin LGA package used for the MC1321x family, see the *802.15.4/ZigBee Hardware Design Considerations Reference Manual* (ZHDCRM).

Table 1. Orderable Parts Details

Device	Operating Temp Range (TA.)	Package	Memory Options	Description
MC13211	-40° to 85° C	LGA	1KB RAM, 16KB Flash	Intended for proprietary applications and Freescale Simple MAC (SMAC)
MC13211R2	-40° to 85° C	LGA Tape and Reel	1KB RAM, 16KB Flash	Intended for proprietary applications and Freescale Simple MAC (SMAC)
MC13212	-40° to 85° C	LGA	2KB RAM, 32KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC
MC13212R2	-40° to 85° C	LGA Tape and Reel	2KB RAM, 32KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC
MC13213	-40° to 85° C	LGA	4KB RAM, 60KB Flash	Intended for 802.15.4 Standard compliant applications and the Freescale 802.15.4 MAC and fully ZigBee compliant Freescale BeeStack.
MC13213R2	-40° to 85° C	LGA Tape and Reel	4KB RAM, 60KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC and fully ZigBee compliant Freescale BeeStack.

1.2 General Platform Features

- 802.15.4 Standard compliant on-chip transceiver/modem
  - 2.4GHz
  - 16 selectable channels
  - Programmable output power
- Multiple power saving modes
- 2V to 3.4V operating voltage with on-chip voltage regulators
- -40°C to +85°C temperature range
- Low external component count
- Supports single 16 MHz crystal clock source operation or dual crystal operation
- Support for SMAC, IEEE 802.15.4 Standard-Compliant MAC, SynkroRF, BeeStack, BeeStack Consumer (ZigBee RF4CE) software solutions
- 9mm x 9mm x 1mm 71-pin LGA

1.3 Microcontroller Features

- Low voltage MCU with 40 MHz low power HCS08 CPU core
- Up to 60K flash memory with block protection and security and 4K RAM
  - MC13211: 16KB Flash, 1KB RAM
  - MC13212: 32KB Flash, 2KB RAM
  - MC13213: 60KB Flash, 4KB RAM
- Low power modes (Wait plus Stop2 and Stop3 modes)
- Dedicated serial peripheral interface (SPI) connected internally to 802.15.4 modem
- One external 4-channel (5-channel internal) 16-bit timer/pulse width modulator (TPM) module and one external 1-channel (3-channel internal) 16-bit timer/pulse width modulator module, each with selectable input capture, output capture, and PWM capability.
- 8-bit port keyboard interrupt (KBI)
- 8-channel 8-10-bit ADC
- Two independent serial communication interfaces (SCI)
- Multiple clock source options
  - Internal clock generator (ICG) with 243 kHz oscillator that has +/-0.2% trimming resolution and +/-0.5% deviation across voltage.
  - Startup oscillator of approximately 8 MHz
  - External crystal or resonator
  - External source from modem clock for very high accuracy source or system low-cost option
- Inter-integrated circuit (IIC) interface.
- In-circuit debug and flash programming available via on-chip background debug module (BDM)
  - Two comparator and 9 trigger modes
  - Eight deep FIFO for storing change-of-flow addresses and event-only data

  - Tag and force breakpoints
  - In-circuit debugging with single breakpoint
- System protection features
  - Programmable low voltage interrupt (LVI)
  - Optional watchdog timer (COP)
  - Illegal opcode detection
- Up to 32 MCU GPIO with programmable pullups

1.4 RF Modem Features

- Fully compliant 802.15.4 Standard transceiver supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode
- Operates on one of 16 selectable channels in the 2.4 GHz ISM band
- -1 dBm to 0 dBm nominal output power, programmable from -27 dBm to +3 dBm typical
- Receive sensitivity of <-92 dBm (typical) at 1% PER, 20-byte packet, much better than the 802.15.4 Standard of -85 dBm
- Integrated transmit/receive switch
- Dual PA ouput pairs which can be programmed for full differential single-port or dual-port operation that supports an external LNA and/or PA.
- Three low power modes for increased battery life
- Programmable frequency clock output for use by MCU
- Onboard trim capability for 16 MHz crystal reference oscillator eliminates need for external variable capacitors and allows for automated production frequency calibration
- Four internal timer comparators available to supplement MCU timer resources
- Supports both packet data mode and streaming data mode
- Seven GPIO to supplement MCU GPIO

1.5 Software Features

Freescale provides a wide range of software functionality to complement the MC1321x hardware. There are three levels of application solutions:

- SMAC
- IEEE 802.15.4 Standard-Compliant MAC
- SynkroRF
- BeeStack
- BeeStack Consumer (ZigBee RF4CE)

1.5.1 Simple Media Access Controller (SMAC)

- Small memory footprint (about 3 Kbytes typical)
- Supports point-to-point and star network configurations
- Proprietary networks
- Source code and application examples provided

1.5.2 802.15.4 Standard-Compliant MAC

- Supports star, mesh and cluster tree topologies
- Supports beaconed networks
- Supports GTS for low latency
- Multiple power saving modes (idle doze, hibernate)

1.5.3 SynkroRF

- Based on the IEEE 802.15.4 Standard
- Bi-directional Communication
- Interference Avoidance
- Channel Agility
- Low Latency Transmission for high duty cycle interferers
- Easy Device Pairing
- Fragmentation Support
- Standardized Command Set

1.5.4 BeeStack

- Based on the IEEE 802.15.4 Standard
- Supports ZigBee 2006 Specification
- Supports star, mesh and tree networks
- Advanced Encryption Standard (AES) 128-bit security
- Supports the ZigBee Home Automation Profile
- Supports the ZigBee Smart Energy Profile

1.5.5 BeeStack Consumer (ZigBee RF4CE)

- Based on the IEEE 802.15.4 Standard
- Supports application profiles that define standardized command sets for multi-vendor interoperability
- Supports vendor specific extensions to standard application profiles for vendor specific customizing
- Supports AES-128 bit encryption

- Provides a mechanism for secured key generation
- Specifies various power saving modes
- Provides a simple mechanism to pair devices (such as a remote to a TV)
- Ensures only authorized devices are able to communicate (a user's remote will not turn their neighbor's TV on or off)

1.6 System Block Diagram

Figure 1 shows a simplified block diagram of the MC1321x solution.

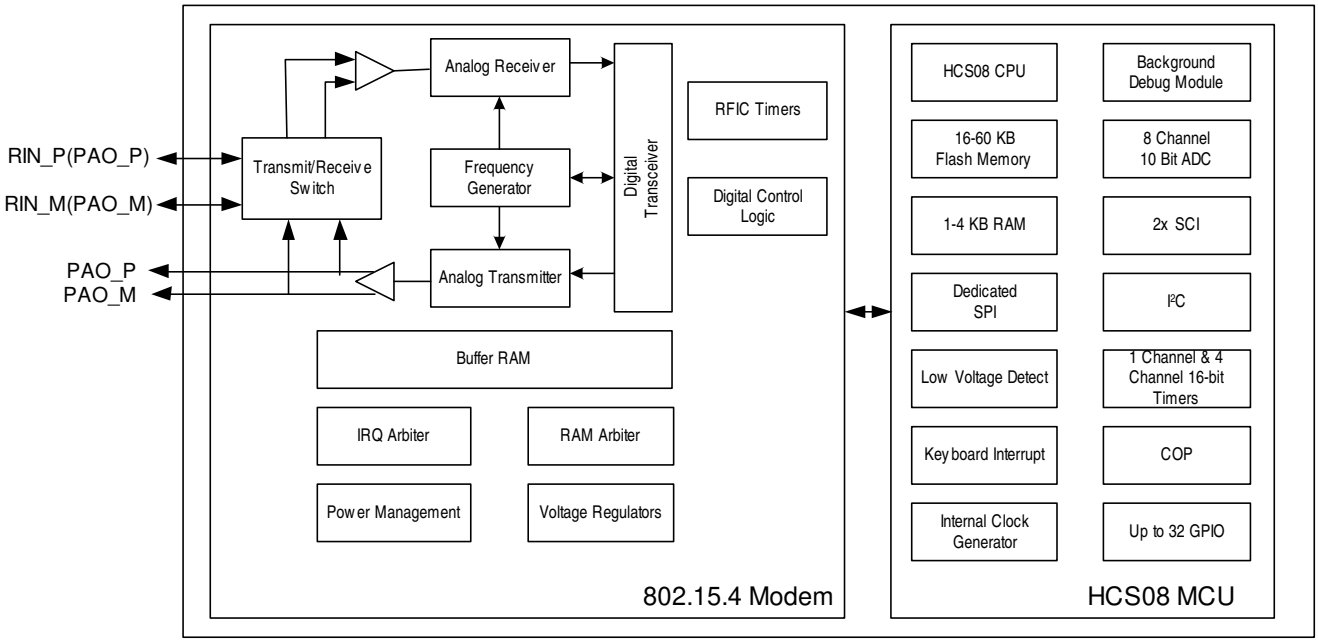


Figure 1. MC1321x System Level Block Diagram

1.7 System Clock Configuration

The MC321x device allows for a wide array of system clock configurations:

- Pins are provided for a separate external clock source for the CPU. The external clock source can by derived from a crystal oscillator or from an external clock source
- Pins are provided for a 16 MHz crystal for the modem clock source (required)
- The modem crystal oscillator frequency can be trimmed through programming to maintain the tight tolerances required by the 802.15.4 Standard
- The modem provides a CLKO programmable frequency clock output that can be used as an external source to the CPU. As a result, a single crystal system clock solution is possible
- Out of reset, the MCU uses an internally generated clock (approximately 8-MHz) for start-up. This allows recovery from stop or reset without a long crystal start-up delay
- The MCU contains an internal clock generator (which can be trimmed) that can be used to run the MCU for low power operation. This internal reference is approximately 243 kHz

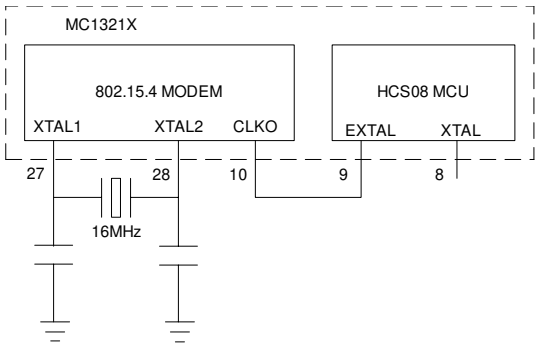


Figure 2. MC1321x Single Crystal System Clock Structure

2 MC1321x Pin Assignment and Connections

Figure 3 shows the MC1321x pinout.

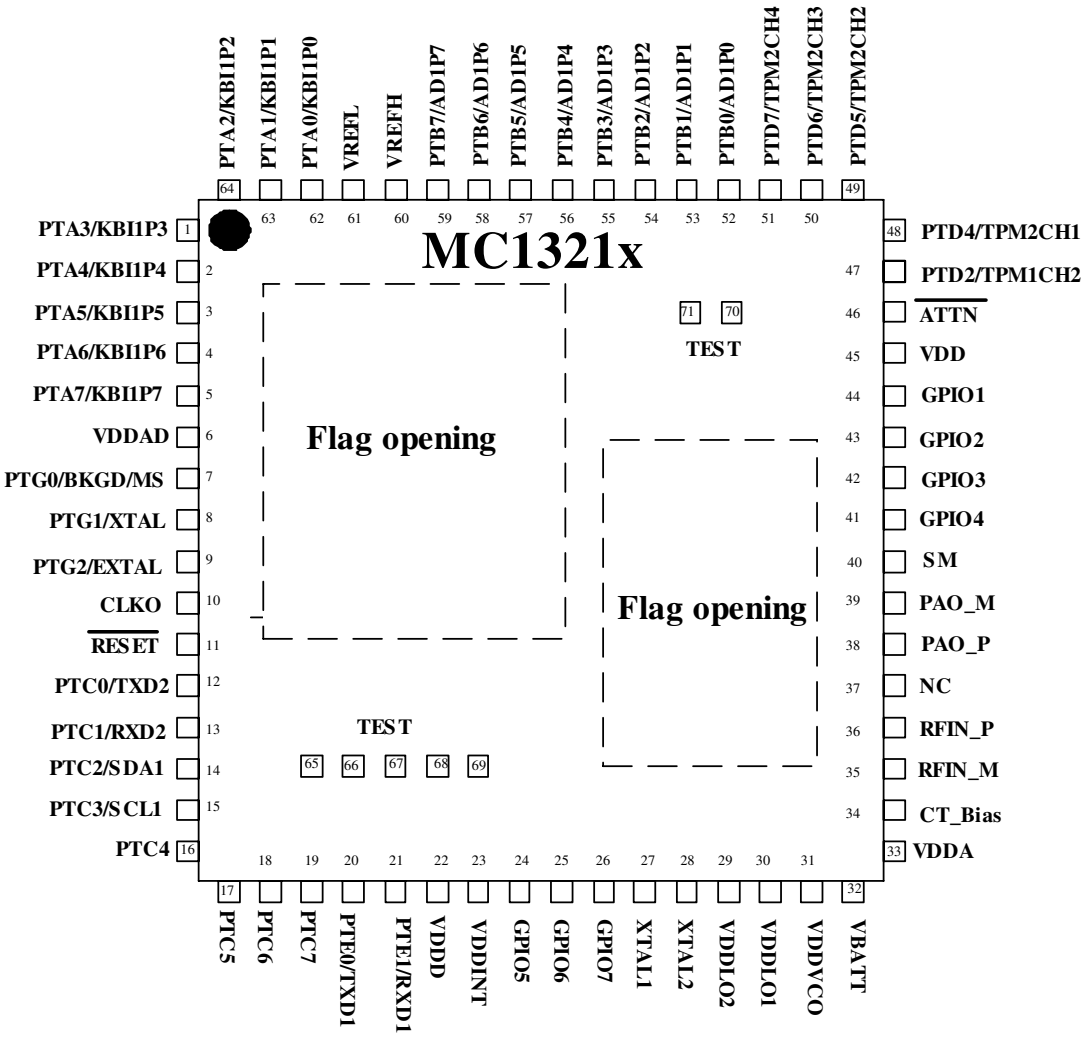


Figure 3. MC1321x Pinout (Top View)

2.1 Pin Definitions

Table 2 details the MC1321x pinout and functionality.

Table 2. Pin Function Description

Pin #	Pin Name	Type	Description	Functionality
1	PTA3/KBI1P3	Digital Input/Output	MCU Port A Bit 3 / Keyboard Input Bit 3	
2	PTA4/KBI1P4	Digital Input/Output	MCU Port A Bit 4 / Keyboard Input Bit 4	
3	PTA5/KBI1P5	Digital Input/Output	MCU Port A Bit 5 / Keyboard Input Bit 5	
4	PTA6/KBI1P6	Digital Input/Output	MCU Port A Bit 6 / Keyboard Input Bit 6	
5	PTA7/KBI1P7	Digital Input/Output	MCU Port A Bit 7 / Keyboard Input Bit 7	
6	VDDAD	Power Input	MCU power supply to ATD	Decouple to ground.
7	PTG0/BKGND/MS	Digital Input/Output/	MCU Port G Bit 0 / Background / Mode Select	PTG0 is output only. Pin is I/O when used as BDM function.
8	PTG1/XTAL	Digital Input/Output	MCU Port G Bit 1 / Crystal oscillator output	Full I/O when not used as clock source.
9	PTG2/EXTAL	Digital Input/Output/	MCU Port G Bit 2 / Crystal oscillator input	Full I/O when not used as clock source.
10	CLKO	Digital Output	Modem Clock Output	Programmable frequencies of: 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 62.5 kHz, 32.786+ kHz (default), and 16.393+ kHz.
11	$\overline{\text{RESET}}$	Digital Input/Output	MCU reset. Active low	
12	PTC0/TXD2	Digital Input/Output	MCU Port C Bit 0 / SCI2 TX data out	
13	PTC1/RXD2	Digital Input/Output	MCU Port C Bit 1/ SCI2 RX data in	
14	PTC2/SDA1	Digital Input/Output	MCU Port C Bit 1/ IIC bus data	
15	PTC3/SCL1	Digital Input/Output	MCU Port C Bit 1/ IIC bus clock	
16	PTC4	Digital Input/Output	MCU Port C Bit 4	
17	PTC5	Digital Input/Output	MCU Port C Bit 5	
18	PTC6	Digital Input/Output	MCU Port C Bit 6	

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
19	PTC7	Digital Input/Output	MCU Port C Bit 7	
20	PTE0/TXD1	Digital Input/Output	MCU Port E Bit 0 / SCI1 TX data out	
21	PTE1/RXD1	Digital Input/Output	MCU Port E Bit 1/ SCI1 RX data in	
22	VDDD	Power Output	Modem regulated output supply voltage	Decouple to ground.
23	VDDINT	Power Input	Modem digital interface supply	2.0 to 3.4 V. Decouple to ground. Connect to Battery.
24	GPIO5[1]	Digital Input/Output	General Purpose Input/Output 5.	See Footnote 1
25	GPIO6[1]	Digital Input/Output	Modem General Purpose Input/Output 6	See Footnote 1
26	GPIO7[1]	Digital Input/Output	Modem General Purpose Input/Output 7	See Footnote 1
27	XTAL1	Input	Modem crystal reference oscillator input	Connect to 16 MHz crystal and load capacitor.
28	XTAL2	Input/Output	Modem crystal reference oscillator output	Connect to 16 MHz crystal and load capacitor. Do not load this pin by using it as a 16 MHz source. Measure 16 MHz output at CLKO, programmed for 16 MHz.
29	VDDLO2	Power Input	Modem LO2 VDD supply	Connect to VDDA externally.
30	VDDLO1	Power Input	Modem LO1 VDD supply	Connect to VDDA externally.
31	VDDVCO	Power Output	Modem VCO regulated supply bypass	Decouple to ground.
32	VBATT	Power Input	Modem voltage regulators' input	Decouple to ground. Connect to Battery.
33	VDDA	Power Output	Modem analog regulated supply output	Decouple to ground. Connect to directly VDDLO1 and VDDLO2 externally and to PAO_P and PAO_M through a bias network.
34	CT_Bias	RF Control Output	Modem bias voltage/control signal for RF external components	When used with internal T/R switch, provides ground reference for RX and VDDA reference for TX. Can also be used as a control signal with external LNA, antenna switch, and/or PA (high level is VDDA).
35	RFIN_M	RF Input (Output)	Modem RF input/output negative	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA
36	RFIN_P	RF Input (Output)	Modem RF input/output positive	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA
37	NC		Not used	May be grounded or left open

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
38	PAO_P	RF Output	Modem power amplifier RF output positive	Open drain. Connect to VDDA through a bias network when used with external balun. Not used when internal T/R switch is used.
39	PAO_M	RF Output	Modem power amplifier RF output negative	Open drain. Connect to VDDA through a bias network when used with external balun. Not used when internal T/R switch is used.
40	SM	Input	Test Mode pin	Must be grounded for normal operation
41	GPIO4[1]	Digital Input/ Output	General Purpose Input/Output 4.	See Footnote 1
42	GPIO3[1]	Digital Input/Output	Modem General Purpose Input/Output 3	See Footnote 1
43	GPIO2	Test Point	MCU Port E Bit 6 / Modem General Purpose Input/Output 2	Internally connected pins. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO2 functions as a “CRC Valid” indicator.
44	GPIO1	Test Point	MCU Port E Bit 7 / Modem General Purpose Input/Output 1	Internally connected pins. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO1 functions as an “Out of Idle” indicator.
45	VDD	Power Input	MCU main power supply	Decouple to ground.
46	$\overline{\text{ATTN}}$[2]	Digital Input	Active Low Attention. Transitions IC from either Hibernate or Doze Modes to Idle.	See Footnote 2
47	PTD2/TPM1CH2	Digital Input/Output	MCU Port D Bit 2 / TPM1 Channel 2	
48	PTD4/TPM2CH1	Digital Input/Output	MCU Port D Bit 4 / TPM2 Channel 1	
49	PTD5/TPM2CH2	Digital Input/Output	MCU Port D Bit 5 / TPM2 Channel 2	
50	PTD6/TPM2CH3	Digital Input/Output	MCU Port D Bit 6 / TPM2 Channel 3	
51	PTD7/TPM2CH4	Digital Input/Output	MCU Port D Bit 7 / TPM2 Channel 4	
52	PTB0/AD1P0	Input/Output	MCU Port B Bit 0 / ATD analogChannel 0	
53	PTB1/AD1P1	Input/Output	MCU Port B Bit 1 / ATD analog Channel 1	
54	PTB2/AD1P2	Input/Output	MCU Port B Bit 2 / ATD analog Channel 2	
55	PTB3/AD1P3	Input/Output	MCU Port B Bit 3 / ATD analog Channel 3	
56	PTB4/AD1P4	Input/Output	MCU Port B Bit 4 / ATD analog Channel 4	

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
57	PTB5/AD1P5	Input/Output	MCU Port B Bit 5 / ATD analog Channel 5	
58	PTB6/AD1P6	Input/Output	MCU Port B Bit 6 / ATD analog Channel 6	
59	PTB7/AD1P7	Input/Output	MCU Port B Bit 7 / ATD analog Channel 7	
60	VREFH	Input	MCU high reference voltage for ATD	
61	VREFL	Input	MCU low reference voltage for ATD	
62	PTA0/KBI1P0	Digital Input/Output	MCU Port A Bit 0 / Keyboard Input Bit 0	
63	PTA1/KBI1P1	Digital Input/Output	MCU Port A Bit 1 / Keyboard Input Bit 1	
64	PTA2/KBI1P2	Digital Input/Output	MCU Port A Bit 2 / Keyboard Input Bit 2	
65	PTE5/SPSCK1	SPICLK	MCU SPI master SPI clock output drives modem SPICLK slave clock input.	Normally factory test. Do not connect
66	PTE4/MOSI1	MOSI	MCU SPI master MOSI output drives modem slave MOSI input	Normally factory test. Do not connect
67	PTE3/MISO1	MISO	Modem SPI slave MISO output drives MCU master MISO input	Normally factory test. Do not connect
68	PTE2/$\overline{SS1}$	CE	MCU SPI master SS output drives modem slave $\overline{CE}$ input	Normally factory test. Do not connect
69	IRQ	M_IRQ	Modem interrupt request $\overline{M\_IRQ}$ output drives MCU IRQ input	Normally factory test. Do not connect
70	PTD1	RXTXEN	MCU Port D Bit 1 drives the RXTXEN input to the modem to enable TX or RX or CCA operations.	Normally factory test. Do not connect
71	PTD3	M_RST	MCU Port D Bit 3 drives the reset $\overline{M\_RST}$ input to the modem.	Normally factory test. Do not connect
FLAG	VSS	Power input	External package flag. Common VSS	Connect to ground.

1 The transceiver GPIO pins default to inputs at reset. There are no programmable pullups on these pins. Unused GPIO pins should be tied to ground if left as inputs, or if left unconnected, they should be programmed as outputs set to the low state.

2 During low power modes, input must remain driven by MCU.

2.2 Internal Functional Interconnects

The MCU provides control for the 802.15.4 modem. The required interconnects between the devices are routed onboard the SiP. In addition, the signals are brought out to external pads primarily for use as test points. These signals can be useful when writing and debugging software.

Table 3. Internal Functional Interconnects

Pin #	MCU Signal	Modem Signal	Description
43	PTE6	GPIO2	Modem GPIO2 output acts as “CRC Valid” status indicator for Stream Data Mode to MCU.
44	PTE7	GPIO1	Modem GPIO1 output acts as “Out of Idle” status indicator for Stream Data Mode to MCU.
46	PTD0	$\overline{\text{ATTN}}$	MCU Port D Bit 0 drives the attention ($\overline{\text{ATTN}}$) input of the modem to wake modem from Hibernate or Doze Mode.
	PTE5/SPSCK1	SPICLK[1]	MCU SPI master SPI clock output drives modem SPICLK slave clock input.
	PTE4/MOSI1	MOSI[1]	MCU SPI master MOSI output drives modem slave MOSI input
	PTE3/MISO1	MISO[2]	Modem SPI slave MISO output drives MCU master MISO input
	PTE2/$\overline{\text{SS1}}$	$\overline{\text{CE}}$[1]	MCU SPI master SS output drives modem slave $\overline{\text{CE}}$ input
	IRQ	$\overline{\text{M\_IRQ}}$	Modem interrupt request $\overline{\text{M\_IRQ}}$ output drives MCU IRQ input
	PTD1	RXTXEN[1]	MCU Port D Bit 1 drives the RXTXEN input to the modem to enable TX or RX or CCA operations.
	PTD3	$\overline{\text{M\_RST}}$	MCU Port D Bit 3 drives the reset $\overline{\text{M\_RST}}$ input to the modem.

1 During low power modes, input must remain driven by MCU.

2 By default MISO is tri-stated when $\overline{\text{CE}}$ is negated. For low power operation, miso_hiz_en (Bit 11, Register 07) should be set to zero so that MISO is driven low when $\overline{\text{CE}}$ is negated.

NOTE

To use the MCU and modem signals as described in Table 3, the MCU needs to be programmed appropriately for the stated function.

3 MC1321x Serial Peripheral Interface (SPI)

The MC1321x modem and CPU communicate primarily through the onboard SPI command channel. Figure 4 shows the SiP internal interconnects with the SPI bus highlighted. The MCU has a single SPI module that is dedicated to the modem SPI interface. The modem is a slave only and the MCU SPI must be programmed and used as a master only. Further, the SPI performance is limited by the modem constraints of 8 MHz SPI clock frequency, and use of the SPI must be programmed to meet the modem SPI protocol.

3.1 SiP Level SPI Pin Connections

The SiP level SPI pin connections are all internal to the device. Figure 4 shows the SiP interconnections with the SPI bus highlighted.

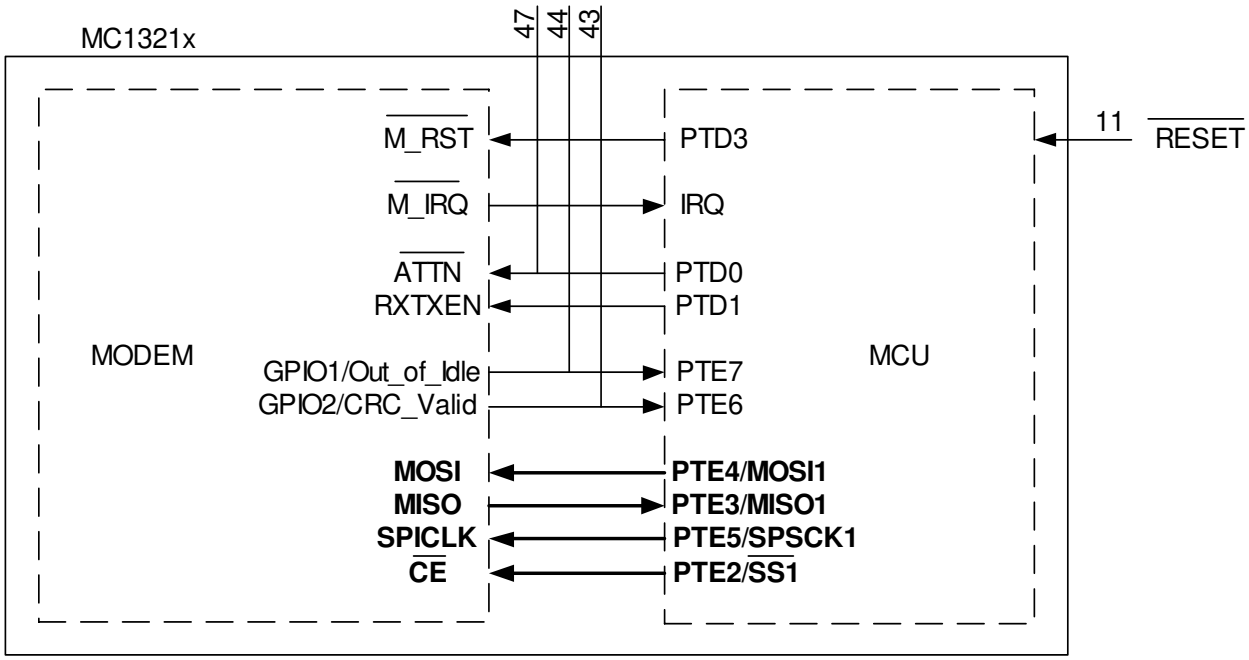


Figure 4. MC1321x Internal Interconnects Highlighting SPI Bus

Table 4. MC1321x Internal SPI Connections

MCU Signal	Modem Signal	Description
PTE5/SPSCK1	SPICLK	MCU SPI master SPI clock output drives modem SPICLK slave clock input.
PTE4/MOSI1	MOSI	MCU SPI master MOSI output drives modem slave MOSI input
PTE3/MISO1	MISO	Modem SPI slave MISO output drives MCU master MISO input
PTE2/$\overline{SS1}$	$\overline{CE}$	MCU SPI master SS output drives modem slave $\overline{CE}$ input

3.2 SPI Features

- MCU bus master
- Modem bus slave
- Programmable SPI clock rate; maximum rate is 8 MHz
- Double-buffered transmit and receive at MCU
- Serial clock phase and polarity must meet modem requirements (MCU control bits
- Slave select programmed to meet modem protocol

3.3 SPI System Block Diagram

Figure 5 shows the SPI system level diagram.

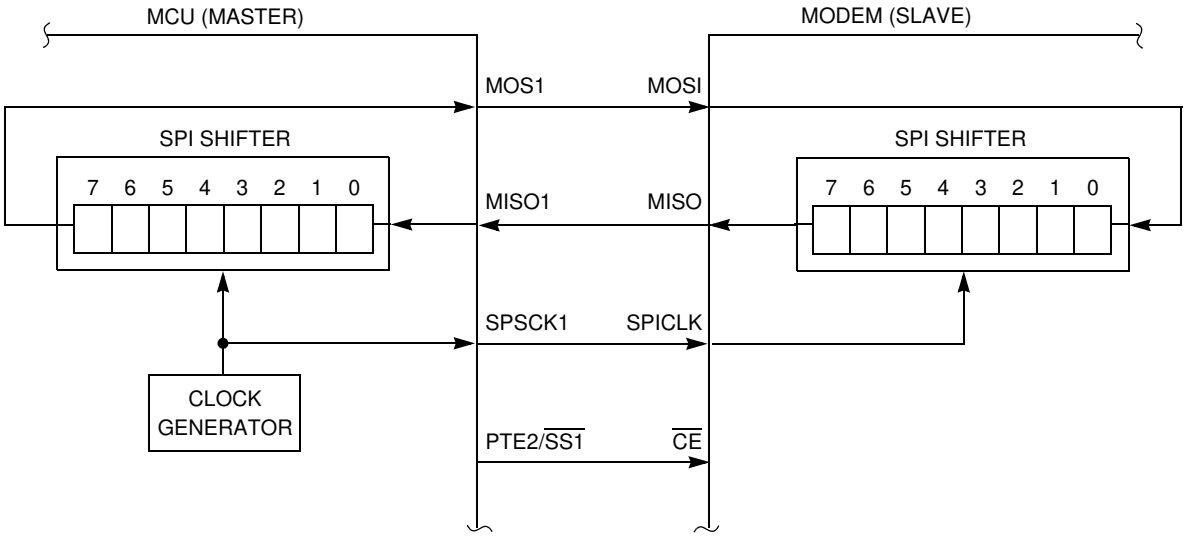


Figure 5. SPI System Block Diagram

Figure 5 shows the SPI modules of the MCU and modem in the master-slave arrangement. The MCU (master) initiates all SPI transfers. During a transfer, the master shifts data out (on the MOSI pin) to the slave while simultaneously shifting data in (on the MISO pin) from the slave. Although the SPI interface supports simultaneous data exchange between master and slave, the modem SPI protocol only uses data exchange in one direction at a time. The SPSCK signal is a clock output from the master and an input to the slave. The slave device must be selected by a low level on the slave select input ($\overline{SS1}$ pin).

4 802.15.4 Standard Modem

4.1 Block Diagram

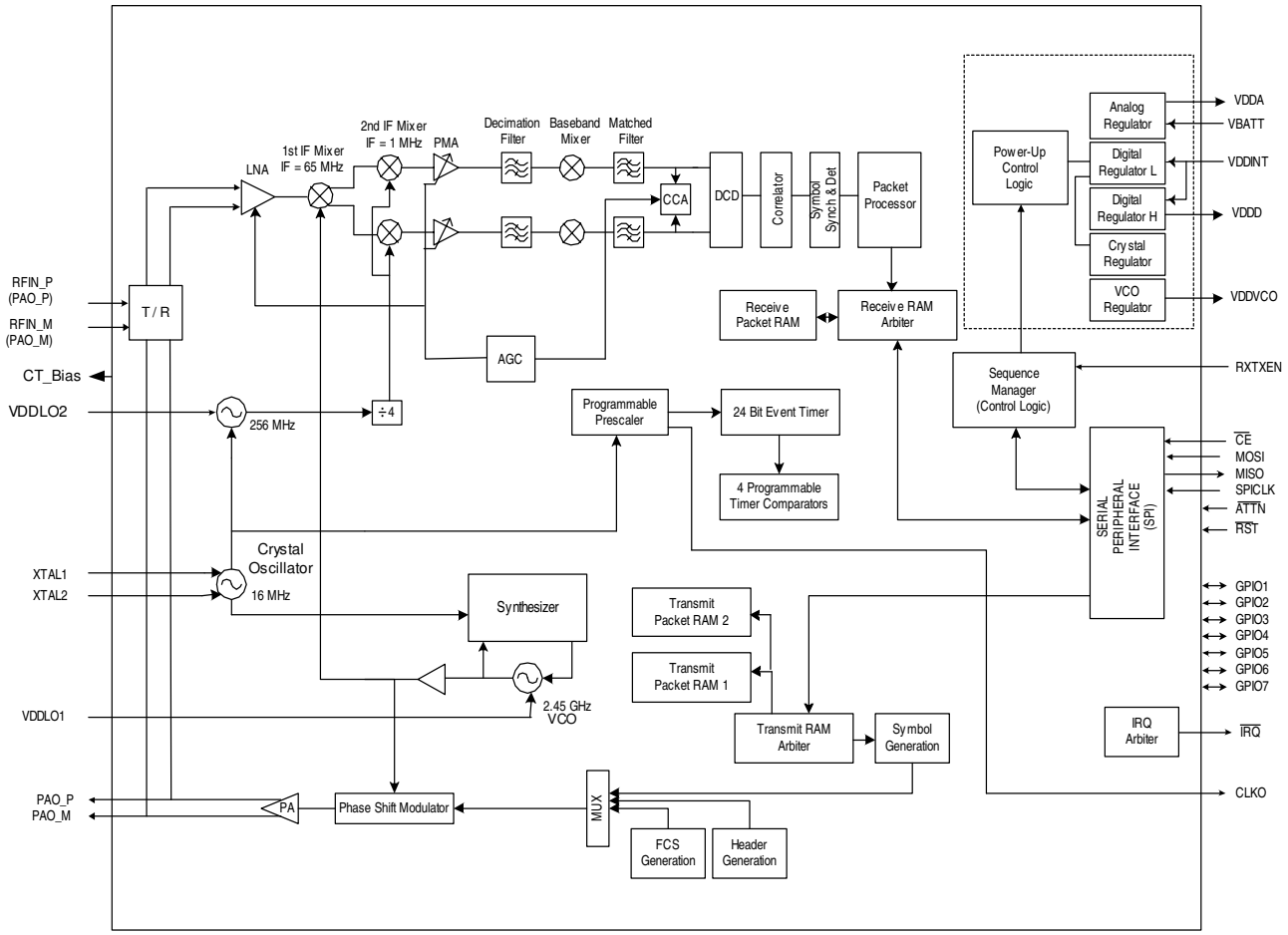


Figure 6. 802.15.4 Standard Modem Block Diagram

4.2 Data Transfer Modes

The 802.15.4 modem has two data transfer modes:

1. Packet Mode — Data is buffered in on-chip RAM
2. Streaming Mode — Data is processed word-by-word

The Freescale 802.15.4 MAC software only supports the streaming mode of data transfer. For proprietary applications, packet mode can be used to conserve MCU resources.

4.3 Packet Structure

Figure 7 shows the packet structure of the 802.15.4 modem. Payloads of up to 125 bytes are supported. The 802.15.4 modem adds a four-byte preamble, a one-byte Start of Frame Delimiter (SFD), and a one-byte Frame Length Indicator (FLI) before the data. A Frame Check Sequence (FCS) is calculated and appended to the end of the data.

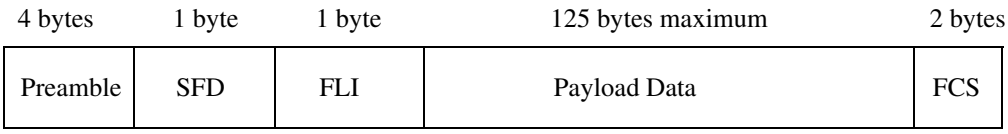


Figure 7. 802.15.4 modem Packet Structure

4.4 Receive Path Description

In the receive signal path, the RF input is converted to low IF In-phase and Quadrature (I & Q) signals through two down-conversion stages. A Clear Channel Assessment (CCA) can be performed based upon the baseband energy integrated over a specific time interval. The digital back end performs Differential Chip Detection (DCD), the correlator “de-spreads” the Direct Sequence Spread Spectrum (DSSS) Offset QPSK (O-QPSK) signal, determines the symbols and packets, and detects the data.

The preamble, SFD, and FLI are parsed and used to detect the payload data and FCS (which are stored in RAM in Packet Mode). A two-byte FCS is calculated on the received data and compared to the FCS value appended to the transmitted data, which generates a Cyclical Redundancy Check (CRC) result. A parameter of received energy during the reception called the Link Quality Indicator is measured over a 64 µs period after the packet preamble and stored in an SPI register.

If the 802.15.4 modem is in Packet Mode, the data is stored in RAM and processed as an entire packet. The MCU is notified that an entire packet has been received via an interrupt.

If the 802.15.4 modem is in streaming mode, the MCU is notified by a recurring interrupt on a word-by-word basis.

Figure 8 shows CCA reported power level versus input power. Note that CCA reported power saturates at about -57 dBm input power which is well above 802.15.4 Standard requirements.

NOTE

For both graphs, the required 802.15.4 Standard accuracy and range limits are shown. A 3.5 dBm offset has been programmed into the CCA reporting level to center the level over temperature in the graphs.

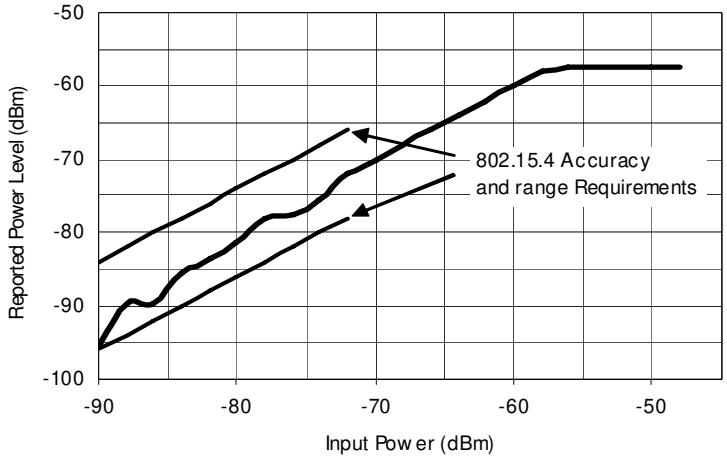


Figure 8. Reported Power Level versus Input Power in Clear Channel Assessment Mode

Figure 9 shows energy detection/LQI reported level versus input power.

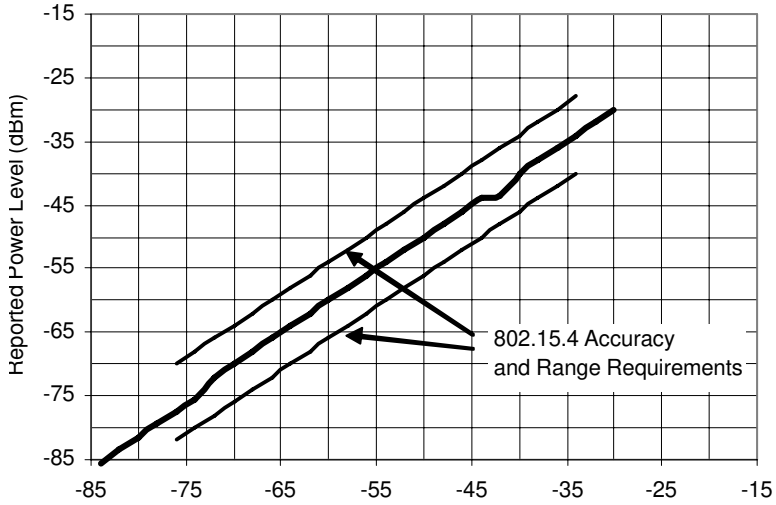


Figure 9. Reported Power Level Versus Input Power for Energy Detect or Link Quality Indicator

4.5 Transmit Path Description

For the transmit path, the TX data that was previously written to the internal RAM is retrieved (packet mode) or the TX data is clocked in via the SPI (stream mode), formed into packets per the 802.15.4 PHY, spread, and then up-converted to the transmit frequency.

If the 802.15.4 modem is in packet mode, data is processed as an entire packet. The data is first loaded into the TX buffer. The MCU then requests that the modem transmit the data. The MCU is notified via an interrupt when the whole packet has successfully been transmitted.

In streaming mode, the data is fed to the 802.15.4 modem on a word-by-word basis with an interrupt serving as a notification that the 802.15.4 modem is ready for more data. This continues until the whole packet is transmitted.

In both modes, a two-byte FCS is calculated in hardware from the payload data and appended to the packet. This done without intervention from the user.

4.6 Functional Description

The following sections provide a detailed description of the MC1321x functionality including the operating modes and the Serial Peripheral Interface (SPI).

4.6.1 802.15.4 Modem Operational Modes

The 802.15.4 modem has a number of operational modes that allow for low-current operation. Transition from the Off to Idle mode occurs when $\overline{\text{M\_RST}}$ is negated. Once in Idle, the SPI is active and is used to control the IC. Transition to Hibernate and Doze modes is enabled via the SPI. These modes are summarized, along with the transition times, in Table 5. Current drain in the various modes is listed in Table 8, DC Electrical Characteristics.

Table 5. 802.15.4 Modem Mode Definitions and Transition Times

Mode	Definition	Transition Time To or From Idle
Off	All IC functions Off, Leakage only. $\overline{\text{M\_RST}}$ asserted. Digital outputs are tri-stated including $\overline{\text{IRQ}}$	10 - 25 ms to Idle
Hibernate	Crystal Reference Oscillator Off. (SPI not functional.) IC Responds to $\overline{\text{ATTN}}$. Data is retained.	7 - 20 ms to Idle
Doze	Crystal Reference Oscillator On but CLKO output available only if Register 7, Bit 9 = 1 for frequencies of 1 MHz or less. (SPI not functional.) Responds to $\overline{\text{ATTN}}$ and can be programmed to enter Idle Mode through an internal timer comparator.	(300 + 1/CLKO) µs to Idle
Idle	Crystal Reference Oscillator On with CLKO output available. SPI active.	
Receive	Crystal Reference Oscillator On. Receiver On.	144 µs from Idle
Transmit	Crystal Reference Oscillator On. Transmitter On.	144 µs from Idle

4.6.2 Serial Peripheral Interface (SPI)

The MCU directs the 802.15.4 modem, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the 802.15.4 modem occurs as multiple 8-bit bursts on the SPI. The modem SPI signals are:

1. Chip Enable ($\overline{CE}$) - A transaction on the SPI port is framed by the active low $\overline{CE}$ input signal. A transaction is a minimum of 3 SPI bursts and can extend to a greater number of bursts.
2. SPI Clock (SPICLK) - The host drives the SPICLK input to the 802.15.4 modem. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

NOTE

For the MCU, the SPI clock format is the clock phase control bit CPHA = 0 and the clock polarity control bit CPOL = 0.

3. Master Out/Slave In (MOSI) - Incoming data from the host is presented on the MOSI input.
4. Master In/Slave Out (MISO) - The 802.15.4 modem presents data to the master on the MISO output.

Although the SPI port is fully static, internal memory, timer and interrupt arbiters require an internal clock (CLK_{core}), derived from the crystal reference oscillator, to communicate from the SPI registers to internal registers and memory.

4.6.2.1 SPI Burst Operation

The SPI port of the MCU transfers data in bursts of 8 bits with most significant bit (MSB) first. The master (MCU) can send a byte to the slave (transceiver) on the MOSI line and the slave can send a byte to the master on the MISO line. Although an 802.15.4 modem transaction is three or more SPI bursts long, the timing of a single SPI burst is shown in Figure 10. The maximum SPI clock rate is 8 Mhz from the MCU because the modem is limited by this number.

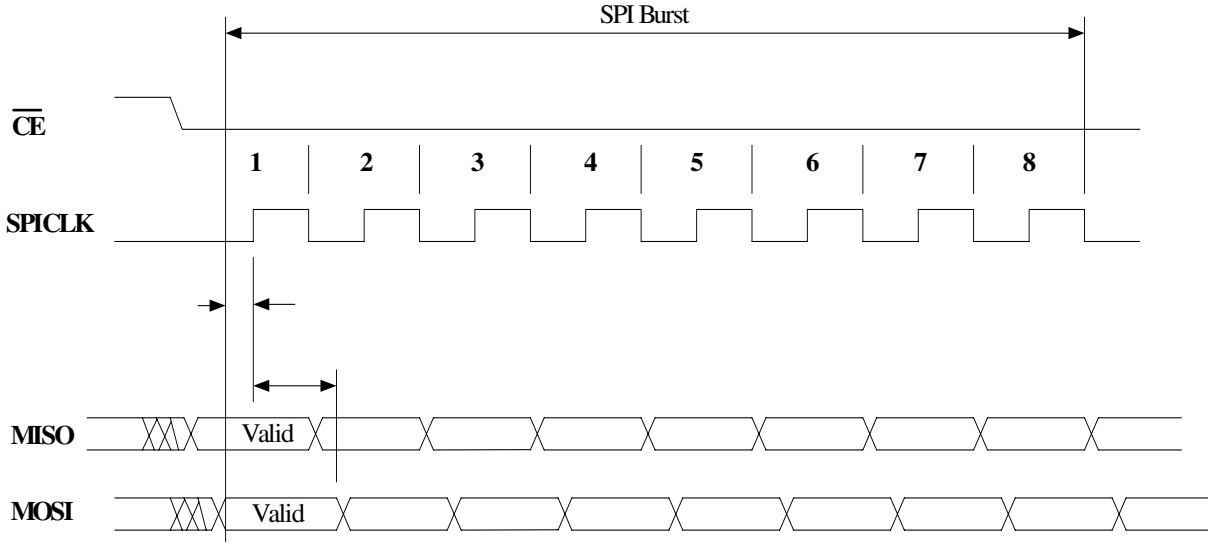


Figure 10. SPI Single Burst Timing Diagram

4.6.2.2 SPI Transaction Operation

Although the SPI port of the MCU transfers data in bursts of 8 bits, the 802.15.4 modem requires that a complete SPI transaction be framed by $\overline{CE}$, and there will be three (3) or more bursts per transaction. The assertion of $\overline{CE}$ to low signals the start of a transaction. The first SPI burst is a write of an 8-bit header to the transceiver (MOSI is valid) that defines a 6-bit address of the internal resource being accessed and identifies the access as being a read or write operation. In this context, a write is data written to the 802.15.4 modem and a read is data written to the SPI master. The following SPI bursts will be either the write data (MOSI is valid) to the transceiver or read data from the transceiver (MISO is valid).

Although the SPI bus is capable of sending data simultaneously between master and slave, the 802.15.4 modem never uses this mode. The number of data bytes (payload) will be a minimum of 2 bytes and can extend to a larger number depending on the type of access. After the final SPI burst, $\overline{CE}$ is negated to high to signal the end of the transaction.

An example SPI read transaction with a 2-byte payload is shown in Figure 11.

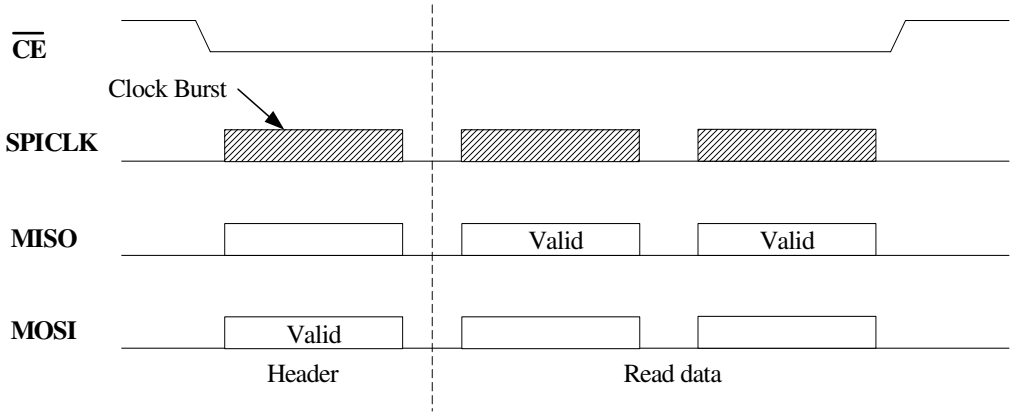


Figure 11. SPI Read Transaction Diagram

4.7 Modem Crystal Oscillator

The modem crystal oscillator uses the following external pins as shown in Figure 12.

1. XTAL1 - reference oscillator input.
2. XTAL2 - reference oscillator output. Note that this pin should not be loaded as a reference source or to measure frequency; instead use CLKO to measure or supply 16 MHz.

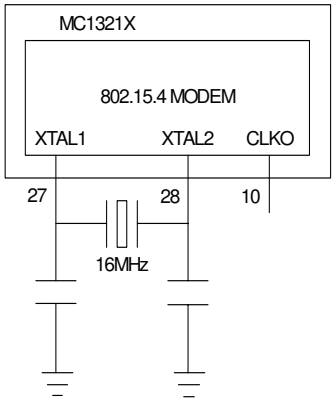


Figure 12. Modem Crystal Oscillator

The 802.15.4 Standard requires that several frequency tolerances be kept within ± 40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The primary determining factor in meeting the 802.15.4 Standard is the tolerance of the crystal oscillator reference frequency. A number of factors can contribute to this tolerance and a crystal specification will quantify each of them:

1. The initial (or make) tolerance of the crystal resonant frequency itself.
2. The variation of the crystal resonant frequency with temperature.
3. The variation of the crystal resonant frequency with time, also commonly known as aging.
4. The variation of the crystal resonant frequency with load capacitance, also commonly known as pulling. This is affected by:
   a) The external load capacitor values - initial tolerance and variation with temperature
   b) The internal trim capacitor values - initial tolerance and variation with temperature
   c) Stray capacitance on the crystal pin nodes - including stray on-chip capacitance, stray package capacitance and stray board capacitance; and its initial tolerance and variation with temperature

Freescale has specified that a 16 MHz crystal with a <9 pF load capacitance is required. The 802.15.4 modem does not contain a reference divider, so 16 MHz is the only frequency that can be used. A crystal requiring higher load capacitance is prohibited because a higher load on the amplifier circuit may compromise its performance. The crystal manufacturer defines the load capacitance as that total external capacitance seen across the two terminals of the crystal. The oscillator amplifier configuration used in the 802.15.4 modem requires two balanced load capacitors from each terminal of the crystal to ground. As such, the capacitors are seen to be in series by the crystal, so each must be <18 pF for proper loading.

The modem uses the 16 MHz crystal oscillator as the reference oscillator for the system and a programmable warp capability is provided. It is controlled by programming CLKO_Ctl Register 0A, Bits

15-8 (xtal_trim[7:0]). The trimming procedure varies the frequency by a few hertz per step, depending on the type of crystal. The high end of the frequency spectrum is set when xtal_trim[7:0] is set to zero. As xtal_trim[7:0] is increased, the frequency is decreased. Accuracy of this feature can be observed by varying xtal_trim[7:0] and using a spectrum analyzer or frequency counter to track the change in frequency of the crystal signal. The reference oscillator frequency can be measured at the CLKO contact by programming CLKO_Ctl Register 0A, Bits 2-0, to value 000.

Figure 13 shows typical oscillator frequency decrease versus the value programmed in xtal_trim[7:0].

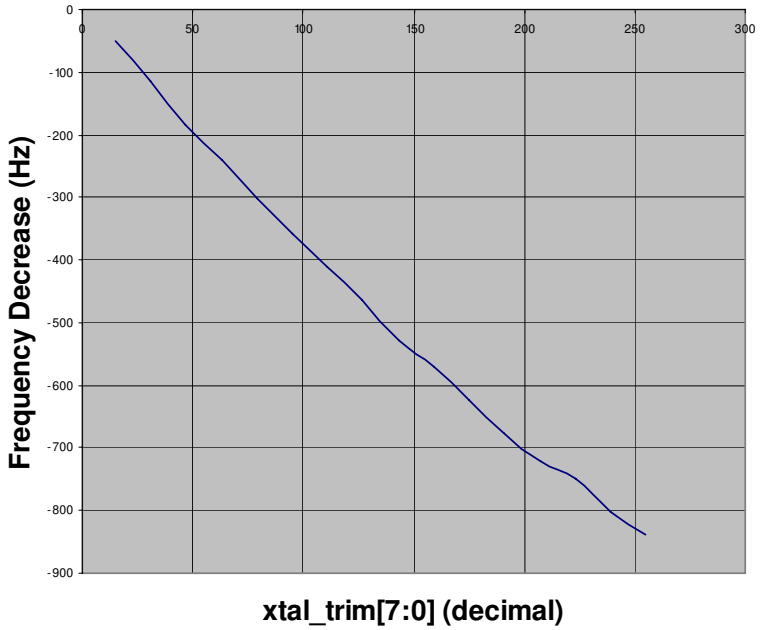


Figure 13. Crystal Frequency Variation vs. xtal_trim[7:0]

4.8 Radio Usage

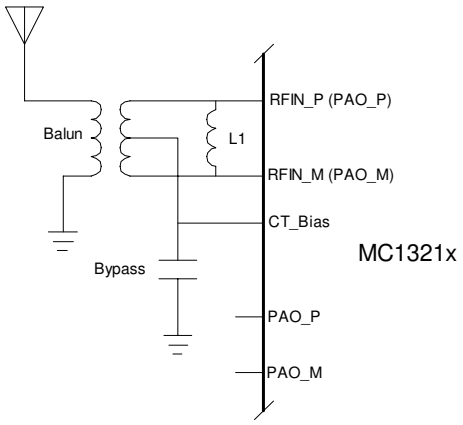
The MC1321x RF analog interface has been designed to provide maximum flexibility as well as low external part count and cost. An on-chip transmit/receive (T/R) switch with bias switch (CT_Bias) can be used for a simple single antenna interface with a balun. Alternately, separate full differential RFIN and PAO outputs can be utilized for separate RX and TX antennae or external LNA and PA designs.

Figure 14 shows three possible configurations for the transceiver radio RF usage.

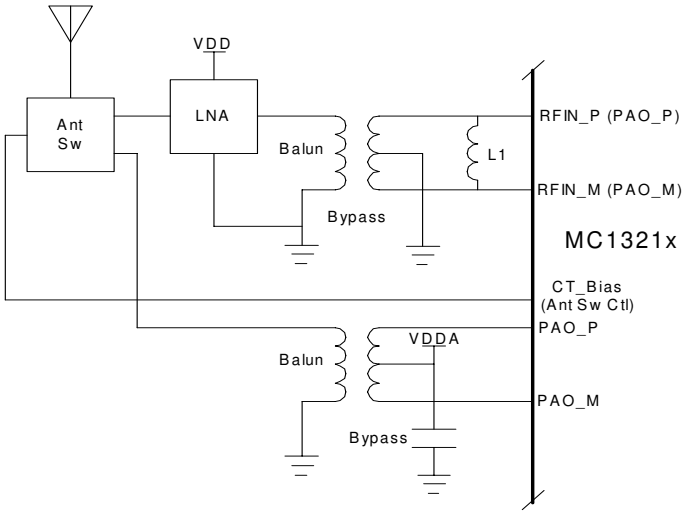
1. Figure 14A shows a single antenna configuration in which the MC1321x internal T/R switch is used. The balun converts the single-ended antenna to differential signals that interface to the RFIN_x (PAO_x) pins of the radio. The CT_Bias pin provides the proper bias point to the balun depending on operation, that is, CT_Bias is at VDDA voltage for transmit and is at ground for receive. The internal T/R switch enables the signal to an onboard LNA for receive and enables the onboard PAs for transmit.
2. Figure 14B shows a single antenna configuration with an external low noise amplifier (LNA) for greater range. An external antenna switch is used to multiplex the antenna between receive and transmit. An LNA is in the receive path to add gain for greater receive sensitivity. Two external baluns are required to convert the single-ended antenna switch signals to the differential signals

required by the radio. Separate RFIN and PAO signals are provided for connection with the baluns, and the CT_Bias signal is programmed to provide the external switch control. The polarity of the external switch control is selectable.

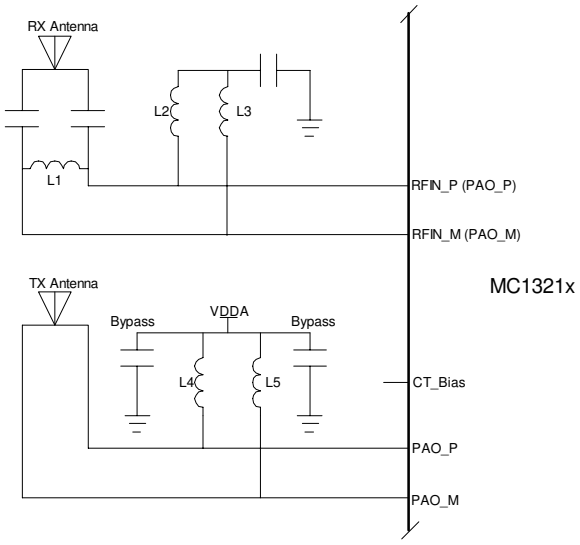
3. Figure 14C shows a dual antenna configuration where there is a RX antenna and a TX antenna. For the receive side, the RX antenna is ac-coupled to the differential RFIN inputs and these capacitors along with inductor L1 form a matching network. Inductors L2 and L3 are ac-coupled to ground to form a frequency trap. For the transmit side, the TX antenna is connected to the differential PAO outputs, and inductors L4 and L5 provide dc-biasing to VDDA but are ac isolated.



14A) Using Onboard T/R Switch



14B) Using External Antenna Switch With LNA

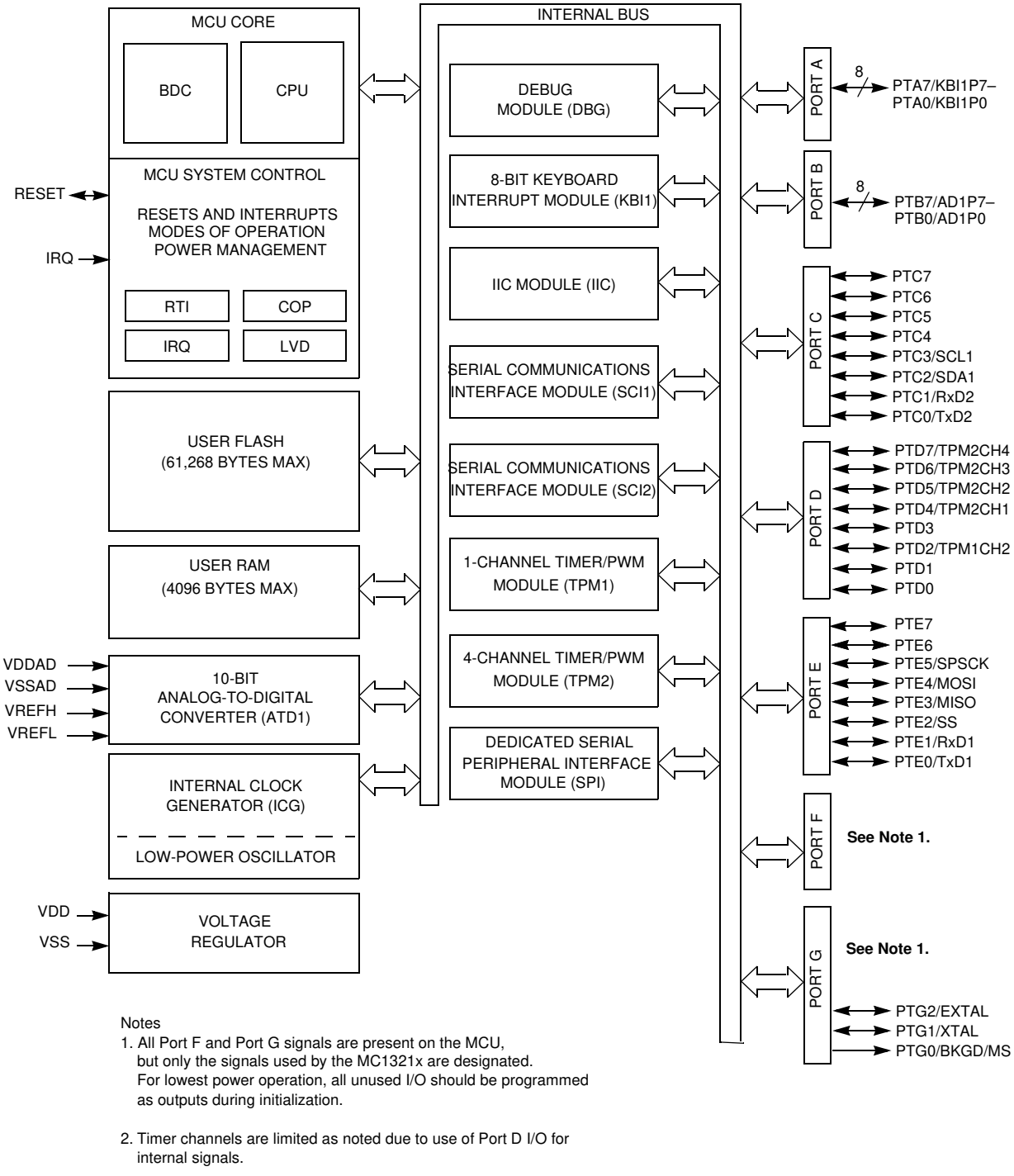


14C) Using Dual Antennae

Figure 14. Using the MC1321x with External RF Components

5 MCU

5.1 MCU Block Diagram



Notes
1. All Port F and Port G signals are present on the MCU, but only the signals used by the MC1321x are designated. For lowest power operation, all unused I/O should be programmed as outputs during initialization.

2. Timer channels are limited as noted due to use of Port D I/O for internal signals.

Figure 15. MCU Block Diagram (HCS08, Version A)