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Freescale Semiconductor
Technical Data

Document Number: MC1322x
Rev. 1.3 10/2010

MC1322x

MC1322x

Advanced ZigBee™- Compliant Platform-in-Package (PiP) for the 2.4 GHz IEEE® 802.15.4 Standard

Package Information
Case 1901-01
99-Pin [9.5X9.5X1.2mm]

Ordering Information

Device	Device Marking	Package
MC13224V[1]	MC13224V	LGA
MC13224VR2[1]	MC13224V	LGA
MC13226V[1]	MC13226V	LGA
MC13226VR2[1]	MC13226V	LGA

[1] See Table 1 for more details.

Contents

1 Introduction

The MC1322x family is Freescale's third-generation ZigBee platform which incorporates a complete, low power, 2.4 GHz radio frequency transceiver, 32-bit ARM7 core based MCU, hardware acceleration for both the IEEE 802.15.4 MAC and AES security, and a full set of MCU peripherals into a 99-pin LGA Platform-in-Package (PiP).

The MC1322x solution can be used for wireless applications ranging from simple proprietary point-to-point connectivity to complete ZigBee mesh networking. The MC1322x is designed to provide a highly integrated, total solution, with premier processing capabilities and very low power consumption.

The MC1322x MCU resources offer superior processing power for ZigBee applications. A full 32-bit ARM7TDMI-S core operates up to 26 MHz. A 128 Kbyte FLASH memory is mirrored into a 96 Kbyte RAM for upper stack and applications software. In addition, an 80 Kbyte ROM is available for boot software, standardized IEEE 802.15.4 MAC and

communications stack software. A full set of peripherals and Direct Memory Access (DMA) capability for transceiver packet data complement the processor core.

The RF radio interface provides for low cost and the high density as shown in Figure 1. An onboard balun along with a TX/RX switch allows direct connection to a single-ended 50-Ω antenna. The integrated PA provides programmable output power typically from -30 dBm to +4 dBm, and the RX LNA provides -96 dBm sensitivity. In addition, separate complementary PA outputs allow use of an external PA and/or an external LNA for extended range applications. The device also has onboard bypass capacitors and crystal load capacitors for the smallest footprint in the industry. All components are integrated into the package except the crystal and antenna.

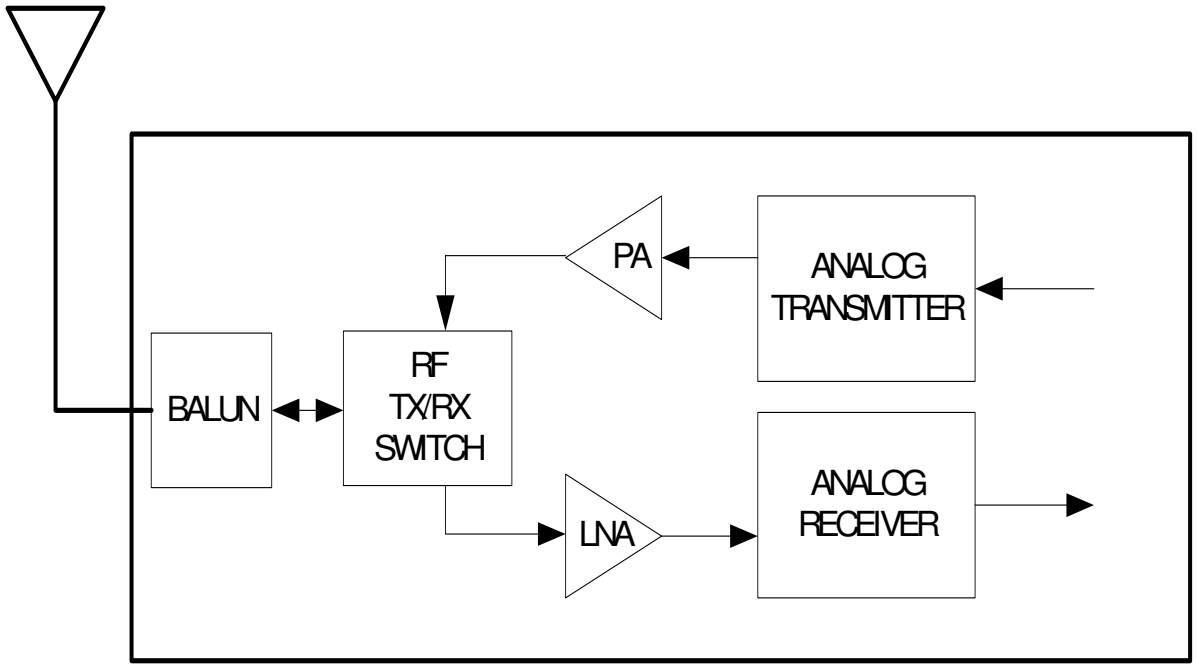

Figure 1. MC1322x RF Radio Interface

In addition to the best-in-class MCU performance and power, the MC1322x also provides best-in-class power savings. Typical transmit current is 29 mA and typical receive current is 22 mA with the CPU at 2 MHz operation and even lower with the bus stealing enabled. Onboard power supply regulation is provided for source voltages from 2.0 Vdc to 3.6 Vdc. Numerous low current modes are available to maximize battery life including sleep or restricted performance operation.

Applications include, but are not limited to, the following:

- Residential and commercial automation
  - Lighting control
  - Security
  - Access control
  - Heating, ventilation, air-conditioning (HVAC)
  - Automated meter reading (AMR)
- Industrial Control

- Asset tracking and monitoring
- Homeland security
- Process management
- Environmental monitoring and control
- HVAC
- Automated meter reading

- Health Care
  - Patient monitoring
  - Fitness monitoring
- Consumer
  - Remote control
  - Entertainment systems
  - Cellular phone attach

1.1 Available Devices

The MC1322x family is available as two part numbers. These device types differ only in their ROM contents, all other device hardware, performance, and specifications are identical:

- MC13224V - this is the original version and is the generic part type.
  - The MC13224V is intended for most IEEE 802.15.4 applications including MAC-based, ZigBee-2007 Profile 1, and ZigBee RF4CE targets.
  - It has a more complete set of peripheral drivers in ROM.
- MC13226V - this is a more recent version and is provided specifically for ZigBee-2007 Profile 2 (Pro) applications. Only the onboard ROM image has been changed to optimize ROM usage for the ZigBee Pro profile and maximize the amount of available RAM for application use.
  - The IEEE MAC/PHY functionality has been streamlined to include only that functionality required by the ZigBee specification. The MAC functionality is 802.15.4 compatible.
  - For a typical application, up to 20 kbytes more of RAM is available versus the M13224V
  - Some drivers present in the MC13224 ROM have been removed and these include the ADC, LCDfont, and SSI drivers. These drivers are still available as library functions, but now compile into the RAM space.
  - The Low Level Component (LLC) functionality has also been streamlined for the ZigBee specification

NOTE

- When running the Freescale IEEE 802.15.4 MAC (or a related stack) on the MC1322x platform, neither beaconing or GTS are supported.
- See the MC1322x Reference Manual (Document No MC1322xRM), for information on using applications on these devices.

1.2 Ordering Information

Table 1 provides additional details about the MC1322x

Table 1. Orderable Parts Details

Device	Operating Temp Range (TA.)	Package	Memory Options	Description
MC13224V	-40° to 105° C	LGA	96KB RAM, 128KB Flash	Intended for 802.15.4 Standard compliant applications, Freescale 802.15.4 MAC, and Freescale BeeStack™.
MC13224VR2	-40° to 105° C	LGA Tape and Reel		
MC13226V	-40° to 105° C	LGA	96KB RAM, 128KB Flash	Intended specifically for Freescale BeeStack™ Pro applications.
MC13226VR2	-40° to 105° C	LGA Tape and Reel		

2 Features

This section provides a simplified block diagram and highlights MC1322x features.

2.1 Block Diagram

Figure 2 shows a simplified block diagram of the MC1322x.

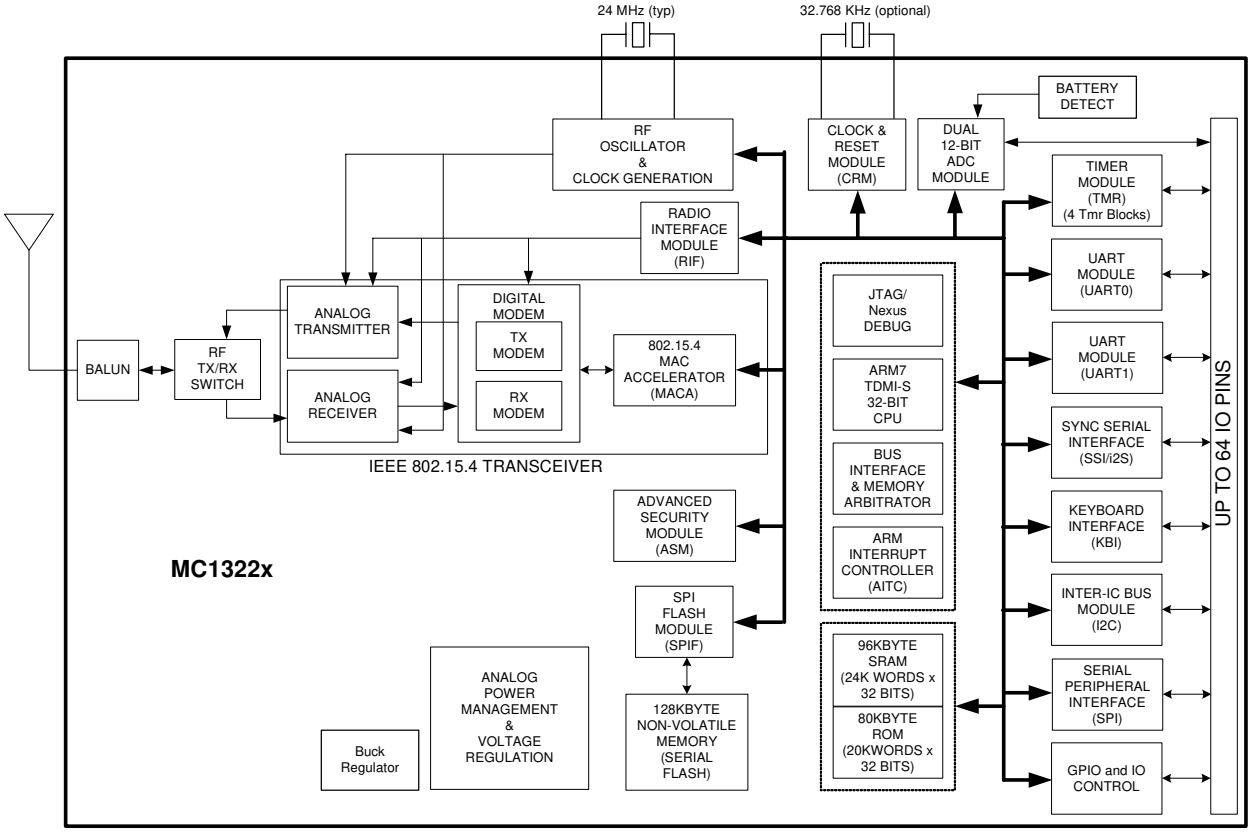

Figure 2. MC1322x Simplified Block Diagram

2.2 Features Summary

- IEEE 802.15.4 standard compliant on-chip transceiver/modem
  - 2.4 GHz ISM Band operation
  - 16 selectable channels
  - Programmable transmitter output power (-30 dBm to +4 dBm typical)
  - World-class receiver sensitivity
    - < -96 dBm typical receiver sensitivity using DCD mode (<1% PER, 20-byte packets)
    - < -100 dBm typical receiver sensitivity using NCD mode (<1% PER, 20-byte packets)
- Hardware acceleration for IEEE 802.15.4 applications
  - MAC accelerator (sequencer and DMA interface)
  - Advanced encryption/decryption hardware engine (AES 128-bit)
- Supports standard IEEE 802.15.4 signaling with 250 kbps data rate
- 32-bit ARM7TDMI-S CPU core with programmable performance up to 26 MHz (24 MHz typical)
- Extensive on-board memory resources
  - 128 Kbyte serial FLASH memory (will be mirrored into RAM)
  - 96 Kbyte SRAM
  - 80 Kbyte ROM
- Best-in-class power dissipation
  - 22 mA typical RX current draw (DCD mode) with radio and MCU active
  - 29 mA typical TX current draw with radio and MCU active (coin cell capable)
  - 3.3 mA typical current draw with MCU active (radio off)
  - 0.8 mA typical current with MCU idle (radio off)
  - 0.85 µA typical Hibernate current (retain 8 Kbyte SRAM contents)
  - 0.4 µA maximum Off current (device in reset)
- Extensive sleep mode control and variation
  - Hibernate and Doze low power modes
  - Programmable degree of power down
  - Clock management
  - Onboard 2 kHz oscillator for wake-up timer.
  - Optional 32.768 kHz crystal oscillator for accurate real-time sleep mode timing and wake-up with a possible sleep period greater than 36.4 hours
  - Wake-up through programmable timer, external real-time interrupts, or ADC timer
- Extensive MCU peripherals set
  - Dedicated 802.15.4 modem/radio interface module (RIF)
  - Dedicated NVM SPI interface for managing FLASH memory
  - Two dedicated UART modules capable of 2 Mbps with CTS/RTS support
  - SPI port with programmable master and slave operation

  - 8-pin keyboard interface (KBI) supports up to a 4x4 matrix. Also, provides up to four asynchronous interrupt inputs for wake-up
  - Two 12-bit analog-to-digital converters (ADCs) share 8 input channels
  - Four independent 16-bit timers with PWM capability. These can cascade in combinations up to 64-bit operation
  - Inter-integrated circuit (I^2C) interface
  - Synchronous Serial Interface (SSI) with I^2S and SPI capability and FIFO data buffering
  - Up to 64 programmable I/O shared by peripherals and GPIO
- Powerful In-circuit debug and FLASH programming available via on-chip debug ports
  - JTAG debug port
  - Nexus extended feature debug port
- System protection features
  - Low battery detect
  - Watchdog timer (COP)
  - Sleep mode timer
- Low external component count
  - Only antenna needed for single-ended 50-Ω RF interface (balun in package)
  - Only a single crystal is required for the main oscillator; programmable crystal load capacitors are on-chip
  - All bypass capacitors in package
- Supports single crystal reference clock source (typical 24 MHz crystal with 13 - 26 MHz usable) with on-chip programmable crystal load capacitance or external frequency source. Also provides onboard 2 kHz oscillator for wake-up timing or an optional 32.768 kHz crystal for accurate low power timing.
- 2.0 V to 3.6 V operating voltage with on-chip voltage regulators.
- Optional buck converter for better battery life.
- -40 °C to +105 °C temperature range
- RoHS-compliant 9.5mm x 9.5mm x 1.2mm 99-pin LGA package

2.3 Software Solutions

Freescale provides a powerful software environment called the Freescale BeeKit Wireless Connectivity Toolkit. BeeKit is a comprehensive codebase of wireless networking libraries, application templates, and sample applications. The BeeKit Graphical User Interface (GUI), part of the BeeKit Wireless Connectivity Toolkit, allows users to create, modify, and update various wireless networking implementations. A wide range of software functionality is available to complement the MC1322x and these are provided as codebases within BeeKit. The following sections describe the available tools.

NOTE

The MC13226V is intend specifically for use with the BeeStack codebase, see Section 2.3.4.2, "Using BeeStack on the MC1322x Platform".

2.3.1 Simple Media Access Controller (22xSMAC)

The Freescale Simple Media Access Controller (22xSMAC) is a simple ANSI C based code stack available as sample source code. The SMAC can be used for developing proprietary RF transceiver applications using the MC1322x.

- Supports point-to-point and star network configurations
- Proprietary networks
- Source code and application examples provided

2.3.2 IEEE 802.15.4 2006 Standard-Compatible MAC

The Freescale 802.15.4 Standard MAC is a code stack available as object code. The 802.15.4 MAC is used in two ways:

- The 802.15.4 MAC is the heart of all Freescale non-SMAC codebases. All higher level stacks are built on the MAC services
- Customers also use the MAC for developing networking applications based on the full IEEE® 802.15.4 Standard but having custom Network Layer and application services.

NOTE

The basic MAC is fully 802.15.4 compliant on the HCS08 platform; however, on the MC1322x ARM platform, beaconing and GTS are not supported. This has no impact on ZigBee stacks as these do not utilize these features.

Features of the 22x MAC include

- Supports star, mesh and cluster tree topologies
- Does not support beaconed networks
- Does not supports GTS
- Multiple power saving modes
- AES-128 Security module
- 802.15.4 Sequence support

- 802.15.4 Receiver Frame filtering.
- Binaries and application examples provided

2.3.3 SynkroRF Platform

The SynkroRF Network is a general purpose, proprietary networking layer that sits on top of the IEEE® 802.15.4 MAC and PHY layers. It is designed for Wireless Personal Area Networks (WPANs) and conveys information over short distances among the participants in the network. It enables small, power efficient, inexpensive solutions to be implemented for a wide range of applications. Some key characteristics of an SynkroRF Network are:

- An over-the-air data rate of 250 kbit/s in the 2.4 GHz band.
- 3 independent communication channels in the 2.4 GHz band (15, 20, and 25).
- 2 network node types, controller and controlled nodes.
- Channel Agility mechanism.
- Low Latency Tx mode automatically enabled in conditions of radio interference.
- Fragmented mode transmission and reception, automatically enabled in conditions of radio interference.
- Robustness and ease of use.
- Essential functionality to build and support a CE network.

The SynkroRF Network layer uses components from the standard HC(S)08 Freescale platform, which is also used by the Freescale's implementations of 802.15.4. MAC and ZigBee™ layers. For more details about the platform components, see the *Freescale Platform Reference Manual*.

2.3.4 ZigBee-Based Stacks

Freescale has two independent codebases to support the two ZigBee standard specifications:

- BeeStack™ - supports ZigBee-2007 and ZigBee Pro extensions
- BeeStack Consumer - supports ZigBee RF4CE

2.3.4.1 BeeStack

Freescale's BeeStack architecture implements the ZigBee-2007 protocol stack including both Stack Profile 1 and Stack Profile 2 (Pro). Based on the OSI Seven-Layer model, the ZigBee stack ensures inter-operability among networked devices. The physical (PHY), media access control (MAC), and network (NWK) layers create the foundation for the application (APL) layers. BeeStack defines additional services to improve the communication between layers of the protocol stack.

At the Application Layer, the application support layer (ASL) facilitates information exchange between the Application Support Sub-Layer (APS) and application objects. Finally, ZigBee Device Objects (ZDO), in addition to other manufacturer-designed applications, allow for a wide range of useful tasks applicable to home and industrial automation.

BeeStack uses the IEEE 802.15.4-compatible MAC/PHY layer that is not part of ZigBee itself. The NWK layer defines routing, network creation and configuration, and device synchronization. The application framework (AF) supports a rich array of services that define ZigBee functionality. ZigBee Device Objects (ZDO) implement application-level services in all nodes via profiles. A security service provider (SSP) is available to the layers that use encryption (NWK and APS), i.e., Advanced Encryption Standard (AES) 128-bit security.

The complete Freescale BeeStack protocol stack includes the following components:

- ZigBee Device Objects (ZDO) and ZigBee Device Profile (ZDP)
- Application Support Sub-Layer (APS)
- Application Framework (AF)
- Network (NWK) Layer
- Security Service Provider (SSP)
- IEEE 802.15.4-compatible MAC and Physical (PHY) Layer

NOTE

For more details on the ZigBee model and protocol, the user is directed to the *ZigBee Specification* at www.zigbee.org.

In addition to the use of two Stack Profiles, ZigBee also embraces the concept of application profiles. The profiles are intended to assure interoperability between like devices for a specific application from different vendors. The application profile specifies a device description and its messaging protocol such that it defines the type, shape, and features of the network. The ZigBee Alliance defines each profile and targets a specific market. Examples include Smart Energy, Home Automation, Health Care, and Remote Control.

Freescale's BeeStack supports a number of these application profiles through demonstration software projects. These projects can be used as a starting point for the user to develop their specific application.

For more information on Freescale supported application profiles see AN3403, *Freescale IEEE 802.15.4/ZigBee Software Selector Guide*.

2.3.4.2 Using BeeStack on the MC1322x Platform

When using the BeeStack codebases on the MC1322x platform, the application should be targeted to the proper part number:

- MC13224V should be used for ZigBee Profile 1 applications
- MC13226V should be used for ZigBee Profile 2 (Pro) applications

BeeStack for the MC1322x platform is a single codebase, device selection is determined by a configuration wizard when the BeeKit project is first developed.

2.3.4.3 BeeStack Consumer

In response to significant market opportunity in the consumer electronics remote control market, the ZigBee Alliance adapted the ZigBee RF4CE Specification in 2009. Freescale's BeeStack Consumer stack implements the ZigBee RF4CE protocol. It is also a networking layer that sits on top of the IEEE®

802.15.4 MAC. It is designed for standards-based Wireless Personal Area Networks (WPANs) of home entertainment products and conveys information over short distances among the participants in the network. It enables small, power efficient, inexpensive solutions to be implemented for a wide range of applications. Targeted applications include DTV, set top box, A/V receivers, DVD players, security, and other consumer products.

Some key characteristics of a BeeStack Consumer network are:

- Based on IEEE 802.15.4 Standard
- Use 3 of the standard 802.15.4 communication channels in the 2.4 GHz band, namely, Channels 15, 20, and 25
- 2 network node types, controller node and target node
- Channel Agility mechanism
- Provides robustness and ease of use
- Includes essential functionality to build and support a CE network
- Binaries, and application examples provided

3 High Density, Low Component Count, Integrated IEEE 802.15.4 Solution

The MC1322x is more than a high performance, low power platform-in-a-package IEEE 802.15.4 solution. Not only are the transceiver (radio) and MCU on an SoC, the packaged solution contains a 128 Kbyte serial FLASH memory, onboard bypass capacitors for critical nodes, and RF components that present a single-ended 50-Ω interface for an external antenna. The radio is a full differential design with an on-chip transmit/receive (TX/RX) switch, and the PiP also has an onboard balun for differential to singled-ended conversion. On-chip RF matching is also provided to present the proper impedance to the antenna.

To further simplify the application, single crystal operation (optimized for 24 MHz) is supported for full radio and MCU operation. If the default 24 MHz crystal is not used, the device supports 13-26 MHz crystals also. The load capacitance to the crystal oscillator is supplied on-chip to eliminate the need for the otherwise required external capacitors.

3.1 Integrated IEEE 802.15.4 Transceiver (Radio and Modem)

The MC1322x IEEE 802.15.4 fully-compliant transceiver provides a complete 2.4 GHz radio with 250 kbps Offset-Quadrature Phase Shift Keying (O-QPSK) data in 5.0 MHz channels and full spread-spectrum encode and decode. The modem supports transmit, receive, clear channel assessment (CCA), Energy Detect (ED), and Link Quality Indication (LQI) as required by the 802.15.4 Standard.

3.1.1 RF Interface and Usage

The MC1322x RF interface provides for a single-ended, 50-Ω port that connects directly to an antenna. There is an onboard balun that converts the single-ended interface to a full differential, bi-directional, on-chip interface with transmit/receive switch, LNA, and complementary PA outputs. The required port

impedance matching is also onboard. This combination allows for a very small footprint and a very low cost RF solution.

The MC1322x also provides a secondary set of complementary PA outputs that can be used with external RF circuitry such as a additional PA for higher TX power to the antenna. The single-ended port continues as the receive input for this circuit configuration.

The receiver demodulator includes a module called the Differential Chip Detector which has two modes of operation:

- Non-coherent Detection (NCD) with automatic frequency control (AFC)
- Non-coherent Differential Chip Detection (DCD) without AFC

The IEEE 802.15.4 standard allows a maximum clock drift of ±40 ppm (which equals ±80 ppm station-to-station). The MC1322x 802.15.4 demodulator includes two different methods of operating in the presence of such large frequency errors:

NCD Mode	Provides an increased ~3.5 dB of sensitivity. However, the addition of the AFC increases the demodulator current drain about 3 mA.
DCD Mode	Default receive mode at lower current.

For longer range applications where external amplification may be desired (LNA and/or PA), additional ports are provided for secondary complementary PA outputs. These can be used as a separate PA interface while the single-ended port through the balun is used as an input only. Also, four control pins and a regulated 20mA voltage source are provided to control external components and supply power to the PA outputs.

The RF Interface functionality can be summarized as follows:

- Programmable output power — 0 dBm nominal output power, programmable from -30 to +4 dBm
- Receive sensitivity (at 1% PER, 20-byte packet) -
  - — < -96 dBm (typical) DCD receive (well above IEEE 802.15.4 specification of -85 dBm)
  - — < -100 dBm (typical) NCD receive (higher current)
- Single-ended 50-Ω antenna port — Uses integrated transmit/receive (T/R) switch, LNA, and onboard balun. Impedance matching onboard.
- Maximum flexibility — The optional single-ended port becomes RF input only and a separate set of full differential PA outputs are provided. Separate input and outputs allow for a variety of RF configurations including external LNA and PA for increased range
- Four control signals for external RF components such as a LNA or PA
- Regulated voltage source for PA biasing and powering external components

3.1.2 Modem

The modem supports the full requirement of the IEEE 802.15.4 Standard to transmit and receive data packets. In additional, the mechanism is present to measure received signal level to provide CCA, ED, and LQI as required by the 802.15.4 Standard.

3.2 High Performance, Low Power 32-Bit ARM7 Processor

- The ARM7TDMI-S processor is a member of the 32-bit ARM family of general-purpose 32-bit microprocessors that offers high performance with very low-power consumption
- A three stage instruction pipeline (fetch, decode, execute) increases the speed of the flow of instructions to the processor
- Data access can be 8-bit bytes, 16-bit half words, or 32-bit words. Words must be aligned to 4-byte boundaries. Half words must be aligned to 2-byte boundaries
- The ARM7TDMI-S processor supports two instruction sets, the 32-bit ARM instruction set and the 16-bit Thumb instruction set. The Thumb mode incorporates 16-bit instructions for higher code density while retaining all the benefits of a 32-bit architecture, such as the full 32-bit registers, 32-bit operations, and 32-bit memory transfer. The use of the instruction sets can be intermixed for maximizing performance while retaining higher code density

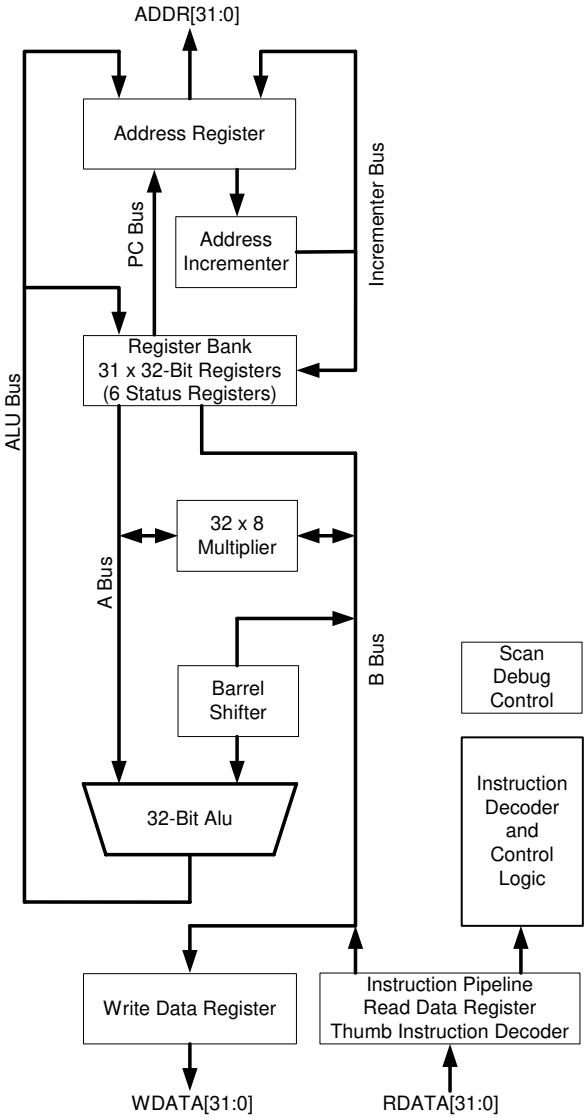

Figure 3. ARM7TDMI-S 32-Bit CPU Core

3.3 Low Power Operation and Power Management

The MC1322x is inherently a very low power device, but it also has extensive power management and an onboard buck regulator option to maximize battery life.

3.3.1 Operating Current

The MC1322x operating currents are a function of operating mode. There are two basic low power modes of Hibernate and Doze, and both have options of how much RAM contents are retained. The difference between Hibernate and Doze is that Doze mode keeps the primary reference oscillator running.

Highest operating current is when the radio is active for transmit or receive. Refer to Section 7.4, “Supply Current Characteristics” for more details and specifications.

3.3.2 Power Management

The MC1322x power management is controlled through the Clock and Reset Module (CRM). The CRM is a dedicated module to handle MCU clock, reset, and power management functions which includes control of the power regulators. All these functions have impact on attaining lowest power.

3.3.2.1 CRM Features

The CRM features include:

- Control of system reset
- Control clock gating for power savings
- Sleep mode (Hibernate and Doze) management
  - Degree of chip power down
  - Retention of programmed parameters
  - Programmable retention of RAM contents
  - Clock management
- Wake-up management
  - Graceful power-up
  - Clock management
  - Wake-up via programmable timer or external interrupts.
- Wake-up timer
  - Hibernate mode - based on onboard 2 kHz oscillator or optional 32.768 kHz crystal oscillator
  - Doze mode - based on main reference oscillator, typically 24 MHz
- Controls reference clocks based on default 24 MHz crystal oscillator or optional 13-26 MHz oscillator with PLL (external filter) for 24 MHz frequency synthesis.
- MCU watchdog timer (COP)
- Software initiated reset
- Management control of onboard linear regulators and optional buck regulator

3.3.2.2 CRM Operation

The CRM has primary control of the entire system:

- Reset and power up — After release of the hardware RESETB signal, the CRM will perform a power up sequence of the MCU. The linear regulators and clock sources are managed for a graceful start-up of the MCU and its resources. The radio is not powered until needed
- Normal operation of MCU — The clock management of the MCU and its resources are controlled by the CRM. The processor clock is programmable from low frequencies up to the maximum reference frequency (13-26 MHz optional w/24 MHz standard) to allow the application to trade-off processing speed versus power savings
- Sleep modes and recovery — There are two sleep modes of Hibernate and Doze. The primary difference is that Doze mode keeps the reference oscillator running. Both modes can retain critical programmed parameters and have selectable sizes of RAM retention. Hibernate has lowest power, but Doze allows high accuracy sleep timing. The CRM manages the recovery from low power, similar to power-up from reset, providing regulator and clock management.
  - Wake-up can be based on external interrupts through 4 KBI inputs
  - Wake-up can be from internal interrupts
  - Wake-up can be based on an RTI (wake-up) timer.
- The RTI timer has two possible frequency sources that provide a very low power wake-up option from sleep
  - One option is an onboard, low accuracy 2 kHz oscillator
  - A second option is to add an external 32.768 kHz crystal for the RTI clock source
  - A 32-bit timer allows greater than a 36.4 hour wake-up delay with the 32.768 crystal oscillator
- Other features of the CRM:
  - An optional COP watchdog timer to monitor CPU program activity
  - A programmable software reset

3.3.3 Optional Buck Regulator

For battery based applications, an optional buck regulator is provided to maximize battery life. Figure 4 shows the configuration of the buck regulator versus the normal connection. An onboard MOSFET is used as a switch with an external 100µH inductor and 10µF capacitor when the buck regulator is enabled.

The buck regulator drops the higher battery voltage to 1.8 - 2.0 Vdc that is applied to the onboard linear regulators. This allows lower net current from the battery to maximize the life of the battery.

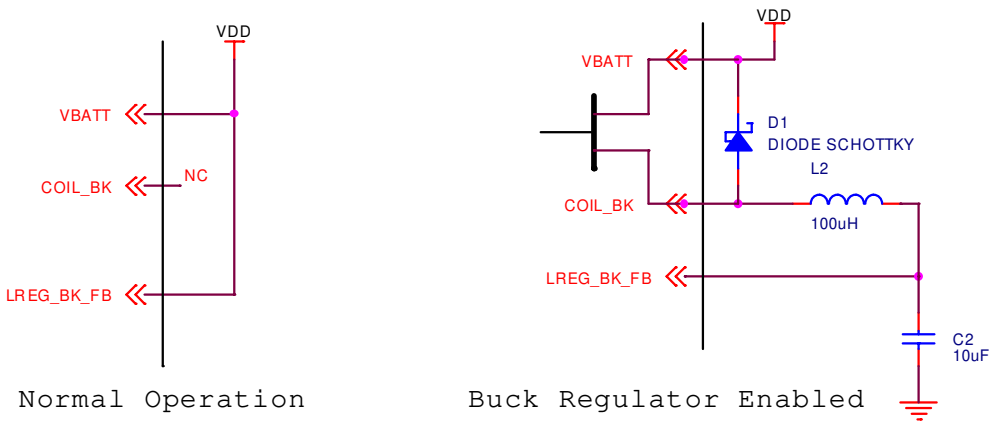

Figure 4. Optional Buck Regulator

3.3.4 Battery Voltage Monitor

An optional feature of the ADC module is a battery voltage monitor capability. An onboard 1.2 Vdc reference voltage can be sampled by the ADC module. The battery-sourced supply voltage is used as the high reference voltage for the ADC and as the supply voltage lowers due to battery usage, the onboard reference voltage reading will become greater because this fixed voltage is a higher percentage of the reduced supply voltage.

Programmable high and low thresholds are provided for an ADC analog sample channel to monitor the reference voltage. This feature can be used as a trigger to provide low battery indication, protection for data that may be lost due to end-of-life for the battery, monitoring charging, and controlling buck regulator operation.

3.4 IEEE 802.15.4 Acceleration Hardware

The MC1322x provides acceleration hardware for IEEE 802.15.4 applications and this hardware includes 802.15.4 MAC acceleration and AES encryption/decryption.

3.4.1 802.15.4 MAC Accelerator (MACA) Overview

The MC1322x contains a hardware block that provides a low-level MAC and PHY link controller, which together with software running on the ARM core, implements the baseband protocols and other low-level link routine control and link control. Components of the MACA include a sequencer/controller (with timers), TX and RX packet buffers, DMA block, frame check sequence (FCS) generator/checker, and control registers. Figure 5 shows a MACA simplified block diagram.

As part of the 802.15.4 protocol, packets are generated and transmitted, packets are received and verified, and channel energy is measured via a clear channel assessment (CCA). Also, combinations or sequences of events are required as part of the protocol such as an ACK response following a received packet. The MACA facilitates these activities via control of the transceiver and off loads the functions from the CPU. A dedicated DMA function moves data between the MACA buffers and RAM on a cycle steal basis and does not require intervention from the CPU.

The MACA is responsible for construction of packets for TX including FCS, and for parsing the received packets. The MACA will also handle ACKs and TxPoll sequences independent of the ARM processor. During TX the MACA will construct the entire packet. This includes preamble and SFD (start of frame delimiter). During receive, the modem will recognize preamble and SFD, then the MACA will begin receiving the packet with the first bit of frame length, and finally, will check the FCS.

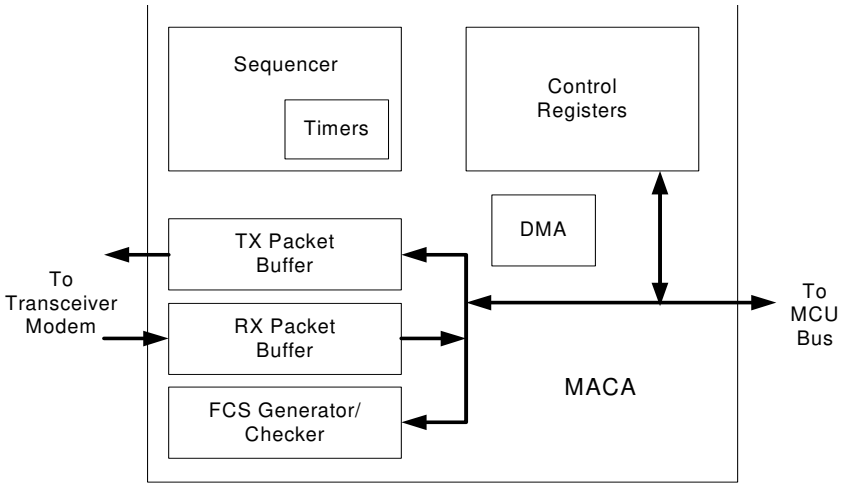

Figure 5. MAC Accelerator Simplified Block Diagram

3.4.1.1 MACA Features

In order to reduce CPU load, the MACA module has embedded features for controlling parts of the IEEE 802.15.4 PHY and MAC layer requirements. The MACA core features include:

- Sequence Manager sequences / auto sequences
  - RX only
  - TX only
  - Automatic acknowledgment frame reception on transmitted packets
  - Automatic acknowledgment frame transmission on received packets
  - Auto-RX for continuous reception as coordinator
  - Auto sequence for transmitted MAC data.request
  - Assist for efficient response to MAC data.request
  - Embedded channel assessment in sequence
  - Support for sequences with slotted mode access
  - Timer triggered and immediately executed actions
  - Support for extended RX for reception in random backoff and battery life extension
  - Support for promiscuous mode
- Programmable auto sequence timing - Each CCA, RX, or TX event is an independent operation. The radio gets through a power-up or “warm-up” sequence for each operation (including VCO), and there is also a power-down or “warm-down” time. Sequences are combinations of radio operations and are highly configurable.
  - RX warm-up is 72 µs

— TX warm-up is 92 µs
— Turnaround times
  – The IEEE 802.15.4 Standard requires a TX-to-RX or a RX-to-TX turnaround time to be less than or equal to 12 symbols times (192 µs).
  – Best practice for maximum station-to-station performance is to minimize TX-to-RX turnaround time and to maximize (within spec) RX-to-TX turnaround time.
  – Auto sequences should use recommended turnaround times of:
    a) 11 symbols times (176 µs) RX-to-TX
    b) 96 µs TX-to-RX.

- Dedicated DMA for transfer of TX/RX data from/to RAM (minimum bus clock of 2 MHz for 802.15.4 modem operation)
- Maskable, event-driven interrupt generation
- Address header filtering for received packets. A promiscuous mode allows bypass of the filtering for monitoring network traffic
- Packet manager
  — Handles preamble data
  — Handles frame check sequence (FCS) a.k.a CRC
  — Embedded header filter for received packets
- Control/status registers mapped into CPU memory map
- 32-Bit random number generator — Runs at the bus clock rate, a 32-bit Linear Feedback Shift Register (LFSR) can be set with a seed value and uses a 32-bit primitive polynomial. A 32-bit random number is fetched with every read of the proper control register

3.4.2 Advanced Security Module (ASM)

The IEEE 802.15.4 Standard and the ZigBee Standard both provide for optional use of data encryption.The ASM engine is a hardware block that accelerates encryption/decryption using the Advanced Encryption Standard (AES). The engine can perform “Counter” (CTR) and Cipher Block Chaining (CBC) encryption. The combination of these two modes of encryption are known as CCM mode encryption. CCM is short for Counter with CBC-MAC. CCM is a generic authenticate and encrypt block cipher mode. CCM is only defined for use with 128 bit block ciphers, such as AES. The definition of CCM mode encryption is documented in the NIST publication SP800-38C.

The ASM has the following features:

- 32-Bit wide bus interface
- CTR encryption in 13 clock cycles
- CBC encryption in 13 clock cycles
- Encrypts 128 bits as a unit
- The 128-bit registers are aligned on quad word boundaries (16 byte)
- Self-test mode
- Maskable “action complete” interrupt

4 Memory

The MC1322x memory resources consist of RAM, ROM, and serial FLASH.

4.1 RAM and ROM

The RAM and ROM features include:

- 96 Kbytes RAM.
  - RAM0: 8 Kbytes, 2 Kwords (2048 x 32 bits)
  - RAM1: 24 Kbytes, 6 Kwords (6144 x 32 bits)
  - RAM2: 32 Kbytes, 8 Kwords (8192 x 32 bits)
  - RAM3: 32 Kbytes, 8 Kwords (8192 x 32 bits)
- All read or write accesses require a minimum of two system clock cycles
- Stall signal generated for read after write cycles
- Clock is enabled only on the accessed memory device for low power consumption
- RAMs have been divided to allow for power savings. While sleeping, the above RAM blocks can be turned off (combinations include 8, 32, 64, and 96 Kbytes active) and the RAM remainder can be placed in a low voltage mode for data retention. If more RAMs are turned on, then less battery life will be achieved. Depending on the amount of RAM powered during sleep, the boot time may be longer with less RAM as the non-powered RAM must be reloaded from FLASH.
- 80 Kbytes ROM
  - 20 Kwords (20480 x 32 bits)
  - Initially contains bootstrap code, 802.15.4 MAC and drivers. The MAC software builds on the lower level hardware capability of the transceiver and MACA. All code except the bootstrap is “patchable”.

4.2 Serial FLASH (NVM)

The MC1322x also contains a 128 Kbyte serial FLASH memory that can be mirrored into the 96 Kbyte RAM. The serial FLASH is accessed via an internal dedicated SPI module (SPIF). The FLASH erase, program, and read capability are programmed through the SPIF port. The FLASH is accessed at boot time to load/initialize RAM. All actual CPU program and data access is from RAM or ROM.

5 MCU Peripherals

The MC1322x has a rich set of MCU peripherals. Figure 6 shows the peripheral modules.

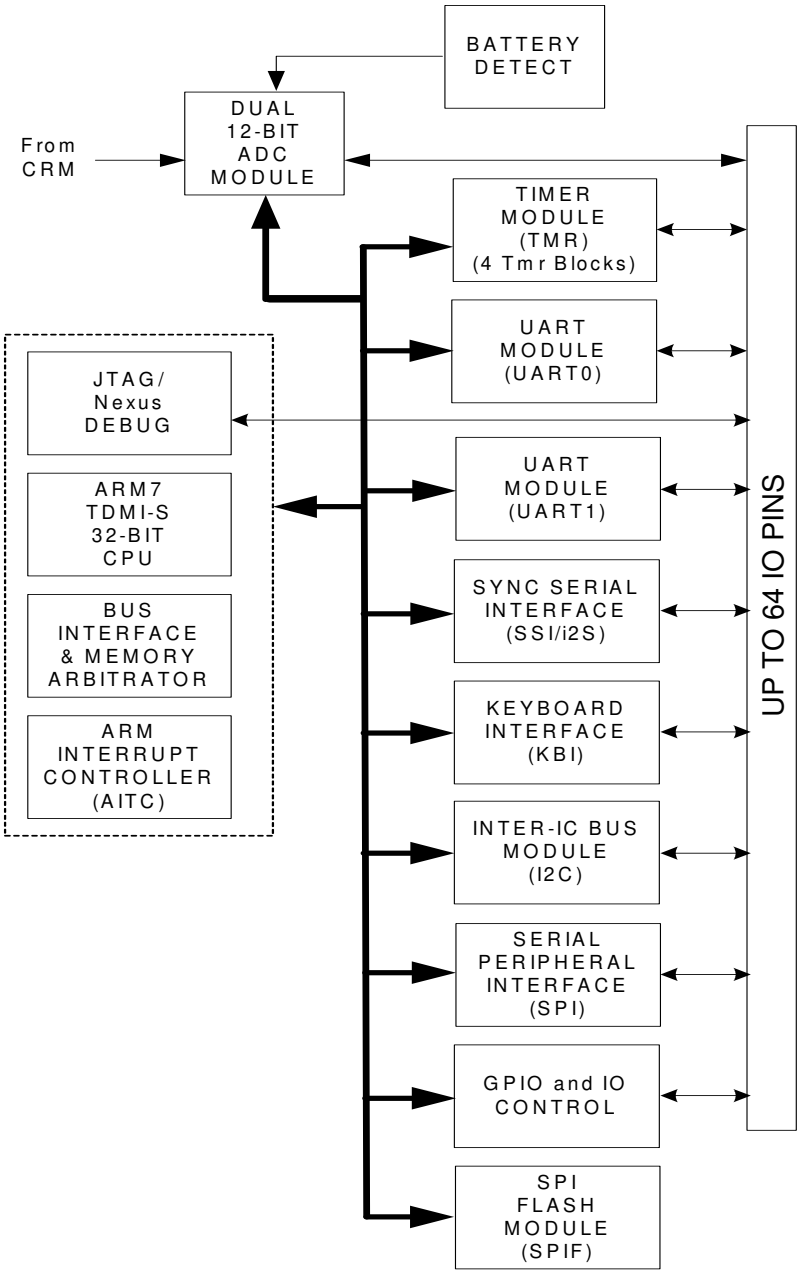

Figure 6. MCU Peripherals

5.1 Parallel IO (GPIO)

The parallel I/O features include:

- A total of 64 general-purpose I/O pins
- Individual control (direction and output state) for each pin when in GPIO mode
- Pad hysteresis enables
- Software-controlled pull-ups/pull-downs on each input pin
- When not used as GPIO, the IO provide alternative functions
  - Debug ports for JTAG (four signals) and Nexus (fourteen signals) modules
  - Four control signals for external RF components such as an LNA, PA, and antenna switch
  - Eight analog inputs for ADC input channels
  - Four signals for ADC reference voltages
  - Eight signals for UART1 and UART2
  - Two I^2C signals
  - Four timer block signals
  - Four SPI block signals
  - Four SSI block signals
  - Eight KBI signals
- Eight KBI pins are kept alive during Hibernate or Doze. Four KBI are output and four are inputs. The input can be used as wake-up interrupts

5.2 Keyboard Interface (KBI)

The MC1322x designates 8 pins (KBI_0 to KBI_7) as a keyboard interface, where four of these signals typically are outputs and four are inputs (KBI_4 to KBI_7) that support interrupts. These 8 pins could typically be used as a matrix interface to support up to 16 switches or buttons, such as a keypad. These signals can also be used as general purpose IO if a keyboard is not present.

During Hibernate or Doze, the KBI are unique in that they are kept alive. Four KBI are outputs and four KBI are inputs. The inputs can be enabled as asynchronous interrupts to wake-up the MC1322x from the sleep mode.

5.3 Timer (TMR) Module

The MC1322x provides a timer module (TMR) that contains four identical counter/timer groups. Each group is capable of many variants of input capture, output compare and pulse-width modulation. The wide range of operational modes is useful for many control and sensor applications.

Figure 7 shows a block diagram of an individual timer group.

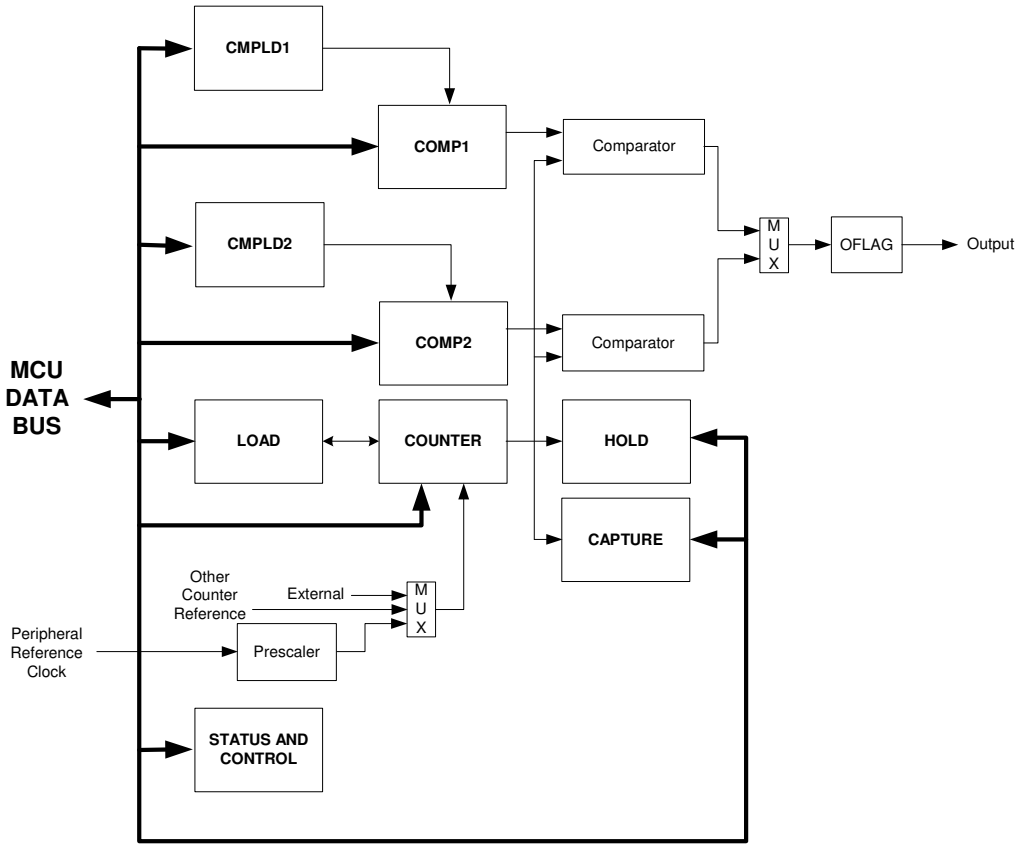

Figure 7. Timer Group Block Diagram

Each 16-bit counter/timer group contains a prescaler, a counter, a load register, a hold register, a capture register, two compare registers, and status and control registers.

- Load Register — Provides the initialization value to the counter when the counter's terminal value has been reached
- Hold Register — Captures the counter's value when other counters are being read. This feature supports the reading of cascaded counters
- Capture Register — Enables an external signal to take a snap shot of the counter's current value
- COMP1 and COMP2 Registers — Provides the values to which the counter is compared. If a match occurs, the OFLAG signal can be set, cleared, or toggled. At match time, an interrupt is generated (if enabled), and the new compare value is loaded into the COMP1 or COMP2 registers from CMPLD1 and CMPLD2 if enabled
- The Prescaler provides different time bases useful for clocking the counter/timer

- The Counter provides the ability to count internal or external events
- Control and Status Registers — Provides operational mode control of the counter, status, clock source control, interrupt control, and external interface control

Four GPIO pins (TMR0 -TMR3) are programmable and can be used with any counter/timer group.

The TMR module feature include:

- Four 16-bit counters/timers groups
- Up/down count
- Counters are cascadable for up to 64-bit delay counter
- Programmable count modulo.
- Peripheral reference clock is same as bus clock
- External clock max count rate equals peripheral clock divided by 2
- Internal clock max count rate equals peripheral clock.
- Count once or repeatedly
- Counters are preloadable
- Compare registers are preloadable
- Counters share available four GPIO pins (programmable as inputs or outputs and programmable for falling or rising edge)
- Separate prescaler for each counter
- Each counter has capture and compare capability
- Optional input glitch filter
- Functional modes include stop, count, edge-count, gated-count, quadrature-count, signed-count, triggered-count, one-shot, cascade-count, pulse-output, fixed frequency PWM, and variable-frequency PWM

5.4 UART Modules

The MC1322x has two universal asynchronous receiver/transmitter (UART) modules. Each UART has an independent fractional divider, baud rate generator that is clocked by the peripheral bus clock (typically 24 MHz) which enables a broad range of baud rates up to 1,843.2 kbaud. Transmit and receive use a common baud rate for each module.

Each UART provides the following features:

- 8-bit only data
- One or two stop bits
- Programmable parity (even, odd, and none)
- Full duplex four-wire serial interface (RXD, TXD, RTS, and CTS)
- Hardware flow control support for RTS and CTS signals
- 32-byte receive FIFO and 32-byte transmit FIFO
- Programmable sense for RTS/CTS pins (high true/low true)

- Status flags for various flow control and FIFO states
- Receiver detects framing errors, start bit error, break characters, parity errors, and overrun errors.
- Voting logic for improved noise immunity (16X/8X oversampling)
- Maskable interrupt request
- Time-out counter, which times out after eight non-present characters
- Receiver and transmitter enable/disable
- Low-power modes
- Baud rate generator to provide any multiple-of-2 baud rate between 1.2 kbaud and 1,843.2 kbaud

5.5 Inter-Integrated Circuit (I^2C) Module

The MC1322x provides an Inter-Integrated Circuit (I^2C) module for the I^2C which is a two-wire, serial data (SDA) and serial clock (SCL), bidirectional serial bus. The I^2C allows for data exchange between the MC1322x and other devices such as MCUs, serial EEPROM, serial ADC and DAC devices, and LCDs. The I^2C minimizes interconnections between devices and is a synchronous, multi-master bus that allows additional devices to be connected and still handle system expansion and development. The bus includes collision detection and arbitration to prevent data corruption if two or more masters attempt to simultaneously control the I^2C.

The I^2C module is driven by the peripheral bus clock (typically 24 MHz) and the SCL bit clock is generated from a prescaler. The prescaler divide ratio can be programmed from 61,440 to 160 (decimal) which gives a maximum bit clock of 150 kbps.

The I^2C module supports the following features:

- Two-wire (SDA and SCL) interface
- Multi-master operation
- Master or slave mode
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation/detection
- Acknowledge bit generation/detection
- Bus busy detection
- Software-programmable bit clock frequency up to 150 kbps
- Software-selectable acknowledge bit
- On-chip filtering for spikes on the bus

5.6 Serial Peripheral Interface (SPI) Modules

The MC1322x has two SPI modules that use a common architecture

5.6.1 External SPI Module

The MC1322x offers a dedicated Serial Peripheral Interface (SPI) module for external use. The SPI is a high-speed synchronous serial data input/output port used for interfacing with serial memories, peripheral devices, or other processors. The SPI allows a serial bit stream of a programmed length (1 to 32 bits) to be shifted simultaneously into and out of the device at a programmed bit-transfer rate (called 4-wire mode). There are four pins associated with the SPI port (SPI_SCK, SPI_MOSI, SPI_MISO, and SPI_SS).

The SPI module can be programmed for master or slave operation. It also supports a 3-wire mode where for master mode the MOSI becomes MOMI, a bidirectional data pin, and for slave mode the MISO becomes SISO, a bidirectional data pin. In 3-wire mode, data is only transferred in one direction at a time.

The SPI bit clock is derived from the peripheral reference clock (typically 24 MHz with a maximum of 26 MHz). A prescaler divides the peripheral reference clock with a programmed divide ratio from 2 to 256. Typical bit clock range will be from 12 MHz to 93.75 kHz.

The SPI has the following features:

- Master or slave mode operation
- Data buffer is 4 bytes (32 bits) in length
- SPI transfer length programmable from 1 to 32 bits
- MSB-first shifting
- Programmable transmit bit rate (typically 12 MHz max)
- Serial clock phase and polarity options
- Full-duplex (4-wire) or bidirectional data (3-wire) operation
- SPI transaction can be polled or interrupt driven
- Slave select signal
- Low Power (SPI Master uses gated clocks. SPI Slave clock derived completely from SPI_SCK.)

5.6.2 SPI FLASH Module (SPIF)

The SPIF is an internal SPI block dedicated to control, reading, and writing of the serial FLASH memory (NVM). It uses the same architecture as the general SPI block, but is limited by the characteristics of the FLASH SPI interface.

5.7 Synchronous Serial Interface (SSI) Module

The MC1322x provides a versatile Synchronous Serial Interface (SSI) which is a full-duplex, serial port that allows communication with a variety of serial devices. These serial devices can be digital signal processors (DSPs), MCUs, peripherals, popular industry audio CODECs, and devices that implement the Inter-Integrated Circuit sound bus standard (I^2S).

The SSI typically transfers samples in a periodic manner and it consists of independent transmitter and receiver sections with common clock generation and frame synchronization. The external signals include the bit clock (SSI_BITCK), frame sync (SSI_FSYN), RX data (SSI_RX), and TX data (SSI_TX). The SSI has the following basic operating modes all with synchronous protocol:

- Normal mode — The simplest SSI mode transfers data in one time slot per frame
- Network mode — Creates a Time Division Multiplexed (TDM) network, such as a TDM CODEC network or a network of DSPs
- Gated Clock mode — Connects to SPI-type interfaces on MCUs or external peripheral chips

With its multi-modes, the SSI can be programmed for two very useful functions:

- A second SPI port augmenting the MC1322x SPI module
- I^2S interface - the SSI is capable of generating the required clock frequencies and data format to drive a serial stereo audio DAC

The SSI includes the following features:

- Synchronous transmit and receive sections with shared internal/external clocks and frame syncs, operating in Master or Slave mode.
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as thirty-two time slots
- Gated Clock mode operation requiring no frame sync
- SSI clock source is Peripheral Clock (typically 24 MHz); maximum SSI transfer rate is 6.0 MHz
- Separate Transmit and Receive FIFOs. Each of which is 8x24 bits
- Programmable data interface modes including I^2S, LSB, MSB aligned
- Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)
- Program options for frame sync and clock generation
- Programmable I^2S modes (Master, Slave)
- Programmable internal clock divider
- Time Slot Mask Registers for reduced CPU overhead (for Tx and Rx both)
- SSI power-down feature