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Freescale Semiconductor
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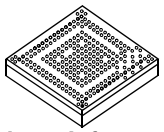
RoHS

MC13783



Package Information
Plastic Package
10 × 10 mm package

Ordering Information

Device	Device Marking or Operating Temperature Range	Package
MC13783	–30 to +85°C	MAPBGA-247

MC13783

Power Management and Audio Circuit

1 Introduction

The MC13783 is a highly integrated power management and audio component dedicated to handset and portable applications covering GSM, GPRS, EDGE, and UMTS standards. The MC13783 implements high-performance audio functions suited to high-end applications such as smartphones and UMTS handsets.

The MC13783 provides the following key benefits:

- Full power management and audio functionality in one module optimizes system size.
- High level of integration reduces the power management and audio system bill of materials.
- Versatile solution offers large possibilities of flexibility through simple programming (64 registers of 24-bit data).
- Implemented DVS saves significant battery resources in every mode (compatibility with a large number of processors).
- Dual channel voice ADC improves intelligibility.

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freescale semiconductor

The detailed block diagram of the MC13783 in Figure 1 shows the wide functionality of the MC13783, including the following features:

- Battery charger interface for wall charging and USB charging
- 10 bit ADC for battery monitoring and other readout functions
- Buck switchers for direct supply of the processor cores
- Boost switcher for backlight and USB on the go supply
- Regulators with internal and external pass devices
- Transmit amplifiers for two handset microphones and a headset microphone
- Receive amplifiers for earpiece, loudspeaker, headset and line out
- 13 bit Voice CODEC with dual ADC channel and both narrow and wide band sampling
- 13 bit Stereo recording from an analog input source such as FM radio
- 16 bit Stereo DAC supporting multiple sample rates
- Dual SSI audio bus with network mode for connection to multiple devices
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry
- Dual SPI control bus with arbitration mechanism
- Multiple backlight drivers and LED control including funlight support
- USB FS/LS transceiver with OTG and CEA-936-A Carkit support
- Touchscreen interface

The main functions of the MC13783 are described in the following sections. A detailed block diagram is shown in Figure 1, on page 3.

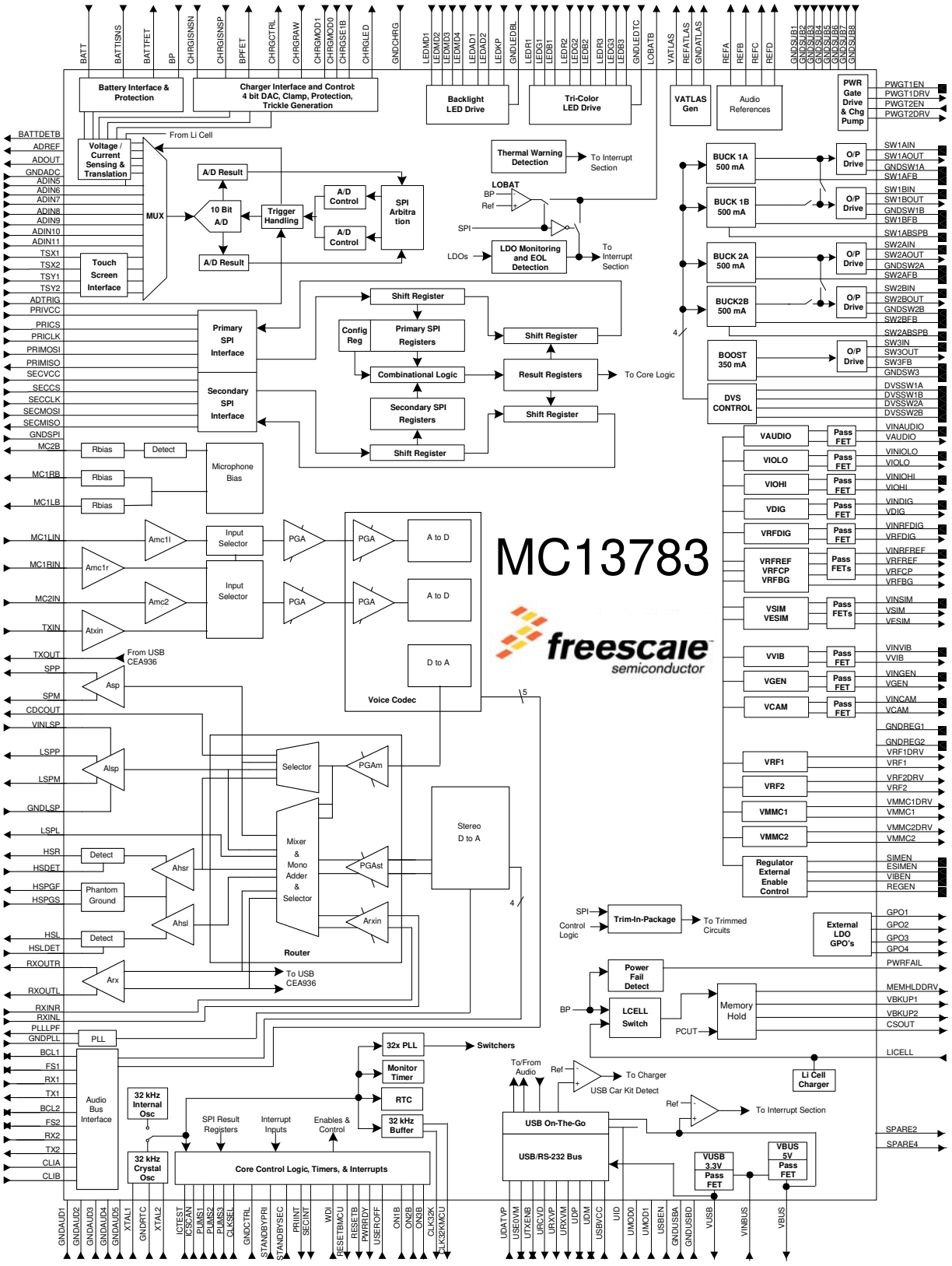

Figure 1. MC13783 Detailed Block Diagram

1.1 Audio

The audio section is composed of microphone amplifiers and speaker amplifiers, a voice CODEC, and a stereo DAC.

Three microphone amplifiers are available for amplification of two handset microphones and of the headset microphone. The feedback networks are fully integrated for a current input arrangement. A line input buffer amplifier is provided for connecting external sources. All microphones have their own stabilized supply with an integrated microphone sensitivity setting. The microphone supplies can be disabled. The headset microphone supply has a fully integrated microphone detection.

Several speaker amplifiers are provided. A bridged earpiece amplifier is available to drive an earpiece. Also, a battery supplied bridged amplifier with thermal protection is included to drive a low ohmic speaker for speakerphone and alert functionality. The performance of this amplifier allows it to be used as well for earpiece drive to support applications with a single transducer combining earpiece, speakerphone and alert functionality, thus avoiding the use of multiple transducers.

A left audio out is provided which in combination with a discrete power amplifier and the integrated speaker amplifier allows for a stereo speaker application. Two, single-ended amplifiers are included for the stereo headset drive including headset detection. The stereo headset return path is connected to a phantom ground which avoids the use of large DC decoupling capacitors. The additional stereo receive signal outputs can be used for connection to external accessories like a car kit. Via a stereo line in, external sources such as an FM radio or standalone midi ringer can be applied to the receive path.

A voice CODEC with a dual path ADC is implemented following GSM audio requirements. Both narrow band and wide band voice is supported. The dual path ADC allows for conversion of two microphone signal sources at the same time for noise cancellation or stereo applications as well as for stereo recording from sources like FM radio. A 16-bit stereo DAC is available which supports multi-clock modes. An on-board PLL ensures proper clock generation. The voice CODEC and the stereo DAC can be operated at the same time via two interchangeable buses supporting master and slave mode, network mode, as well as the different protocols like I2S.

Volume control is included in both transmit and receive paths. The latter also includes a balance control for stereo. The mono adder in the receive path allows for listening to a stereo source on a mono transducer. The receive paths for stereo and mono are separated to allow the two sources to be played back simultaneously on different outputs. The different sources can be analog mixed and two sources on the SSI configured in network mode can be mixed as well.

1.2 Switchers and Regulators

The MC13783 provides most of the telephone reference and supply voltages.

Four down converters and an up converter are included. The down, or buck, converters provide the supply to the processors and to other low voltage circuits such as IO and memory. The four down converters can be combined into two higher power converters. Dynamic voltage scaling is provided on each of the down converters. This allows under close processor control to adapt the output voltage of the converters to minimize processor current drain. The up, or boost, converter supplies the white backlight LEDs and the

regulators for the USB transceiver. The boost converter output has a backlight headroom tracking option to reduce overall power consumption.

The regulators are directly supplied from the battery or from the switchers and include supplies for IO and peripherals, audio, camera, multi media cards, SIM cards, memory and the transceivers. Enables for external discrete regulators are included as well as a vibrator motor regulator. A dedicated preamplifier audio output is available for multifunction vibrating transducers.

Drivers for power gating with external NMOS transistors are provided including a fully integrated charge pump. This will allow to power down parts of the processor to reduce leakage current.

1.3 Battery Management

The MC13783 supports different charging and supply schemes including single path and serial path charging. In single path charging, the phone is always supplied from the battery and therefore always has to be present and valid. In a serial path charging scheme, the phone can operate directly from the charger while the battery is removed or deeply discharged.

The charger interface provides linear operation via an integrated DAC and unregulated operation like used for pulsed charging. It incorporates a standalone trickle charge mode in case of a dead battery with LED indicator driver. Over voltage, short circuit and under voltage detectors are included as well as charger detection and removal. The charger includes the necessary circuitry to allow for USB charging and for reverse supply to an external accessory. The battery management is completed by a battery presence detector and an A to D converter that serves for measuring the charge current, battery and other supply voltages as well as for measuring the battery thermistor and die temperature.

1.4 Logic

The MC13783 is fully programmable via SPI bus. Additional communication is provided by direct logic interfacing. Default startup of the device is selectable by hard-wiring the power up mode select pins.

Both the call processor and the applications processor have full access to the MC13783 resources via two independent SPI busses. The primary SPI bus is able to allow the secondary SPI bus to control all or some of the registers. On top of this an arbitration mechanism is built in for the audio, the power and ADC functions. This together will avoid programming conflicts in case of a dual processor type of application.

The power cycling of the phone is driven by the MC13783. It has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures the supply of the memory and other circuits from the coin cell in case of brief power failures. A charger for the coin cell is included as well. Several pre-selectable power modes are provided such as SDRAM self refresh mode and user off mode.

The MC13783 provides the timekeeping based on an integrated low power oscillator running with a standard watch crystal. This oscillator is used for internal clocking, the control logic, and as a reference for the switcher PLL. The timekeeping includes time of day, calendar and alarm. The clock is put out to the processors for reference and deep sleep mode clocking.

1.5 Miscellaneous Functions

The drivers and comparators for a USB On-the-Go and a CEA-936-A compatible USB carkit including audio routing, as well as RS232 interfaces are provided. Special precautions are taken to allow for specific booting and accessory detection modes.

Current sources are provided to drive tricolored funlights and signaling LEDs. The funlights have preprogrammed lighting patterns. The wide programmability of the tricolored LED drivers allows for applications such as audio modulation. Three backlight drivers with auto dimming are included as well for keypad and dual display backlighting.

A dedicated interface in combination with the A to D converter allow for precise resistive touchscreen reading. Pen touch wake up is included.

2 Signal Descriptions

The below pinout description gives the pin name per functional block with its row-column coordinates, its maximum voltage rating, and a functional description.

Table 1. Pinout Listing

Pin	Location	Rating*	Function
Charger			
CHRGRAW	A18 A19 B19	EHV	1. Charger input 2. Output to battery supplied accessories
CHRGCTRL	C18	EHV	Driver output for charger path FETs M1 and M2
BPFET	B15	EHV	1. Driver output for dual path regulated BP FET M4 2. Driver output for separate USB charger path FETs M5 and M6
CHRGISNSP	B17	MV	Charge current sensing point 1
CHRGISNSN	C14	MV	Charge current sensing point 2
BP	B13	MV	1. Application supply point 2. Input supply to the MC13783 core circuitry 3. Application supply voltage sense
BATTFET	A12	MV	Driver output for battery path FET M3
BATTISNS	A14	MV	Battery current sensing point 1
BATT	D15	MV	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
CHRGMOD0	D17	LV	Selection of the mode of charging
CHRGMOD1	A16	LV	Selection of the mode of charging

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- MV for Medium Voltage (4.65 V)
- LV for Low Voltage (3.1 V)

Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
CHRGSE1B	F15	LV	Charger forced SE1 detection input
CHRGLED	D13	EHV	Trickle LED driver output
GNDCHRG	J11	—	Ground for charger interface
LED Drivers			
LEDMD1	B8	EMV	Main display backlight LED driver output 1
LEDMD2	F9	EMV	Main display backlight LED driver output 2
LEDMD3	E9	EMV	Main display backlight LED driver output 3
LEDMD4	C9	EMV	Main display backlight LED driver output 4
LEDAD1	C8	EMV	Auxiliary display backlight LED driver output 1
LEDAD2	E8	EMV	Auxiliary display backlight LED driver output 2
LEDKP	C7	EMV	Keypad lighting LED driver output
LEDR1	B10	EMV	Tricolor red LED driver output 1
LEDG1	E11	EMV	Tricolor green LED driver output 1
LEDB1	F11	EMV	Tricolor blue LED driver output 1
LEDR2	E10	EMV	Tricolor red LED driver output 2
LEDG2	F10	EMV	Tricolor green LED driver output 2
LEDB2	G10	EMV	Tricolor blue LED driver output 2
LEDR3	F8	EMV	Tricolor red LED driver output 3
LEDG3	C10	EMV	Tricolor green LED driver output 3
LEDB3	B9	EMV	Tricolor blue LED driver output 3
GNDLEDBL	H10	—	Ground for backlight LED drivers
GNDLEDTC	J10	—	Ground for tricolor LED drivers
MC13783 Core			
VATLAS	C12	LV	Regulated supply output for the MC13783 core circuitry
REFATLAS	B11	LV	Main bandgap reference
GNDATLAS	H11	—	Ground for the MC13783 core circuitry
Switchers			
SW1AIN	K18	MV	Switcher 1A input
SW1AOUT	K17	MV	Switcher 1A output
SW1AFB	L18	LV	Switcher 1A feedback

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
DVSSW1A	J15	LV	Dynamic voltage scaling logic input for switcher 1A
GNDSW1A	L17	—	Ground for switcher 1A
SW1BIN	N18	MV	Switcher 1B input
SW1BOUT	N17	MV	Switcher 1B output
SW1BFB	M18	LV	Switcher 1B feedback
DVSSW1B	K15	LV	Dynamic voltage scaling logic input for switcher 1B
GNDSW1B	M17	—	Ground for switcher 1B
SW2AIN	P18	MV	Switcher 2A input
SW1ABSPB	P11	LV	SW1 mode configuration
SW2AOUT	R18	MV	Switcher 2A output
SW2AFB	P15	LV	Switcher 2A feedback
DVSSW2A	H15	LV	Dynamic voltage scaling logic input for switcher 2A
GNDSW2A	P17	—	Ground for switcher 2A
SW2BIN	U18	MV	Switcher 2B input
SW2BOUT	T18	MV	Switcher 2B output
SW2BFB	R17	LV	Switcher 2B feedback
DVSSW2B	J14	LV	Dynamic voltage scaling logic input for switcher 2B
GNDSW2B	T17	—	Ground for switcher 2B
SW2ABSPB	R12	LV	SW2 mode configuration
SW3IN	J17	HV	Switcher 3 input
SW3OUT	H18	HV	Switcher 3 output
SW3FB	H17	HV	Switcher 3 feedback
GNDSW3	J18	—	Ground for switcher 3
Power Gating			
PWGT1EN	L14	LV	Power gate driver 1 enable
PWGT1DRV	M15	EMV	Power gate driver 1 output
PWGT2EN	L15	LV	Power gate driver 2 enable
PWGT2DRV	K14	EMV	Power gate driver 2 output
Regulators			
VINAUDIO	U12	MV	Input regulator audio

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
VAUDIO	U10	LV	Output regulator audio
VINIOLO	U13	MV	Input regulator low voltage IO
VIOLO	V13	LV	Output regulator low voltage IO
VINIOHI	B7	MV	Input regulator high voltage IO
VIOHI	B6	LV	Output regulator high voltage IO
VINDIG	R11	MV	Input regulator general digital
VDIG	U11	LV	Output regulator general digital
VINRFDIG	K5	MV	Input regulator transceiver digital
VRFDIG	K2	LV	Output regulator transceiver digital
VINRFREF	K7	MV	Input regulator transceiver reference
VRFREF	G3	LV	Output regulator transceiver reference
VRFCP	G2	LV	Output regulator transceiver charge pump
VRFBG	C11	LV	Bandgap reference output for transceiver
VINSIM	F2	MV	Input regulator SIM card and eSIM card
VSIM	E3	LV	Output regulator SIM card
VESIM	F3	LV	Output regulator eSIM card
VINVIB	G5	MV	Input regulator vibrator motor
VVIB	E2	LV	Output regulator vibrator motor
VINGEN	G17	MV	Input regulator graphics accelerator
VGEN	G18	LV	Output regulator graphics accelerator
VINCAM	V12	MV	Input regulator camera
VCAM	V11	LV	Output regulator camera
VRF2DRV	J6	MV	Drive output regulator transceiver
VRF2	J5	LV	Output regulator transceiver
VRF1DRV	K8	MV	Drive output regulator transceiver
VRF1	J3	LV	Output regulator transceiver
VMMC1DRV	L7	MV	Drive output regulator MMC1 module
VMMC1	K6	LV	Output regulator MMC1 module
VMMC2DRV	J2	MV	Drive output regulator MMC2 module
VMMC2	K3	LV	Output regulator MMC2 module

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- LV for Low Voltage (3.1 V)

Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
SIMEN	D19	LV	VSIM enable input
ESIMEN	F16	LV	VESIM enable input
VIBEN	E19	LV	VVIB enable input
REGEN	E18	LV	Regulator enable input
GPO1	G8	LV	General purpose output 1 to be used for enabling a discrete regulator
GPO2	F6	LV	General purpose output 2 to be used for enabling a discrete regulator
GPO3	E5	LV	General purpose output 3 to be used for enabling a discrete regulator
GPO4	G9	LV	General purpose output 4 to be used for enabling a discrete regulator
GNDREG1	N12	—	Ground for regulators 1
GNDREG2	K10	—	Ground for regulators 2
USB/RS232			
UDP	C2	EMV	1. USB transceiver cable interface, D+ 2. RS232 transceiver cable interface, transmit output or receive input signal
UDM	D2	EMV	1. USB transceiver cable interface, D- 2. RS232 transceiver cable interface, receive input or transmit output signal
UID	F7	EMV	USB on the go transceiver cable ID resistor connection
UDATVP	C5	LV	1. USB processor interface transmit data input (logic level version of D+/D-) or transmit positive data input (logic level version of D+) 2. Optional USB processor interface receive data output (logic level version of D+/D-) 3. RS232 processor interface
USE0VM	C6	LV	1. USB processor interface transmit single ended zero signal input or transmit minus data input (logic level version of D-) 2. Optional USB processor interface received single ended zero output 3. Optional RS232 processor interface
UTXENB	C4	LV	1. USB processor interface transmit enable bar
URCVD	B5	LV	Optional USB receiver processor interface differential data output (logic level version of D+/D-)
URXVP	B3	LV	Optional USB receiver processor interface data output (logic level version of D+)
URXVM	B2	LV	1. Optional USB receiver processor interface data output (logic level version of D-) 2. Optional RS232 processor interface
UMOD0	H7	LV	USB transceiver operation mode selection at power up 0
UMOD1	G6	LV	USB transceiver operation mode selection at power up 1
USBEN	C3	LV	Bootmode enable for USB/RS232 interface
VINBUS	B4	EMV	Input for VBUS and VUSB regulators for USB on the go mode

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
VBUS	D3	EHV EMV	When in common input configuration, shorted to CHRGRAW 1. USB transceiver cable interface VBUS 2. Output VBUS regulator in USB on the go mode When in separate input configuration, not shorted to CHRGRAW 1. USB transceiver cable interface VBUS 2. Output VBUS regulator in USB on the go mode
VUSB	F5	MV	Output VUSB regulator as used by the USB transceiver
USBVCC	E7	LV	Supply for processor interface
GNDUSBA	A1 A2 B1	—	Ground for USB transceiver and USB cable
GNDUSBD	K9	—	Ground for USB processor interface
Control Logic			
ON1B	E16	LV	Power on/off button connection 1
ON2B	E15	LV	Power on/off button connection 2
ON3B	G14	LV	Power on/off button connection 3
WDI	F17	LV	Watchdog input
RESETB	G15	LV	Reset output
RESETBMCU	F18	LV	Reset for the processor
STANDBYPRI	H14	LV	Standby input signal from primary processor
STANDBYSEC	J13	LV	Standby input signal from secondary processor
LOBATB	N14	LV	Low battery indicator signal or end of life indicator signal
PWRRDY	U17	LV	Power ready signal after DVS and power gate transition
PWRFAIL	F13	LV	Powerfail indicator output to processor or system
USEROFF	E14	LV	User off signaling from processor
MEMHLDDRV	G12	LV	Memory hold FET drive for power cut support
CSOUT	G11	LV	Chip select output for memory
LICELL	C16	MV	1. Coincell supply input 2. Coincell charger output
VBKUP1	E12	LV	Backup output voltage for memory
VBKUP2	F12	LV	Backup output voltage for processor core
GNDCTRL	J12	—	Ground for control logic

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
Oscillator and Real Time Clock			
XTAL1	V16	LV	32.768 kHz Oscillator crystal connection 1
XTAL2	V14	LV	32.768 kHz Oscillator crystal connection 2
CLK32K	R14	LV	32 kHz Clock output
CLK32KMCU	E13	LV	32 kHz Clock output to the processor
CLKSEL	U16	LV	Enables the RC clock routing to the outputs
GNDRTC	V15	—	Ground for the RTC block
Power Up Select			
PUMS1	H6	LV	Power up mode supply setting 1
PUMS2	J7	LV	Power up mode supply setting 2
PUMS3	H5	LV	Power up mode supply setting 3
ICTEST	F14	LV	Test mode selection
ICSCAN	U14	LV	Scan mode selection
SPI Interface			
PRIVCC	N2	LV	Supply for primary SPI bus and audio bus 1
PRICLK	N5	LV	Primary SPI clock input
PRIMOSI	N8	LV	Primary SPI write input
PRIMISO	P7	LV	Primary SPI read output
PRICS	N6	LV	Primary SPI select input
PRIINT	P5	LV	Interrupt to processor controlling the primary SPI bus
SECVCC	N3	LV	Supply for secondary SPI bus and audio bus 2
SECCLK	P6	LV	Secondary SPI clock input
SECMOSI	R6	LV	Secondary SPI write input
SECMISO	R5	LV	Secondary SPI read output
SECCS	P8	LV	Secondary SPI select input
SECINT	R7	LV	Interrupt to processor controlling the secondary SPI bus
GNDSPI	L9	LV	Ground for SPI interface
A to D Converter			
BATTDETB	K13	LV	Battery thermistor presence detect output
ADIN5	M14	LV	ADC generic input channel 5, group 1

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
ADIN6	U15	LV	ADC generic input channel 6, group 1
ADIN7	R15	LV	ADC generic input channel 7, group 1
ADIN8	P14	LV	ADC generic input channel 8, group 2
ADIN9	V17	LV	ADC generic input channel 9, group 2
ADIN10	V18	LV	ADC generic input channel 10, group 2
ADIN11	V19 W18 W19	LV	ADC generic input channel 11, group 2
TSX1	P13	LV	ADC generic input channel 12 or touchscreen input X1, group 2
TSX2	L13	LV	ADC generic input channel 13 or touchscreen input X2, group 2
TSY1	P12	LV	ADC generic input channel 14 or touchscreen input Y1, group 2
TSY2	M13	LV	ADC generic input channel 15 or touchscreen input Y2, group 2
ADREF	R13	LV	Reference for ADC and touchscreen interface
ADTRIG	N15	LV	ADC trigger input
ADOUT	E6	LV	ADC trigger output
GNDADC	L12	—	Ground for A to D circuitry
Audio Bus			
BCL1	M7	LV	Bit clock for audio bus 1. Input in slave mode, output in master mode
FS1	M9	LV	Frame synchronization clock for audio bus 1. Input in slave mode, output in master mode
RX1	L5	LV	Receive data input for audio bus 1
TX1	M6	LV	Transmit data output for audio bus 1
BCL2	M8	LV	Bit clock for audio bus 2. Input in slave mode, output in master mode
FS2	M2	LV	Frame synchronization clock for audio bus 2. Input in slave mode, output in master mode
RX2	M3	LV	Receive data input for audio bus 2
TX2	M5	LV	Transmit data output for audio bus 2
CLIA	L6	LV	Clock input for audio bus 1 or 2
CLIB	L3	LV	Clock input for audio bus 1 or 2
Audio Transmit			
MC1RB	R2	LV	Handset primary or right microphone supply output with integrated bias resistor
MC1LB	P3	LV	Handset secondary or left microphone supply output with integrated bias resistor

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
MC2B	P2	LV	Headset microphone supply output with integrated bias resistor and detect
MC1RIN	V2	LV	Handset primary or right microphone amplifier input
MC1LIN	U2	LV	Handset secondary or left microphone amplifier input
MC2IN	U3	LV	Headset microphone amplifier input
TXIN	U4	LV	General purpose line level transmit input
TXOUT	V3	LV	Buffered output of CEA-936-A microphone signal
Audio Receive			
SPP	V9	LV	Handset earpiece speaker amplifier output positive terminal
SPM	V10	LV	Handset earpiece speaker amplifier output minus terminal
VINLSP	V6	MV	Handset loudspeaker and alert amplifier supply input
LSPP	V5	MV	Handset loudspeaker and alert amplifier positive terminal
LSPM	V4	MV	Handset loudspeaker and alert amplifier minus terminal
GNDLSP	V1 W1 W2	—	Ground for loudspeaker amplifier
LSPL	U5	LV	Low power output for discrete loudspeaker amplifier, associated to left channel audio
CDCOUT	U6	LV	Low power output for discrete amplifier, associated to voice CODEC channel
HSL	V8	LV	Headset left channel amplifier output
HSR	U9	LV	Headset right channel amplifier output
HSPGF	V7	LV	Headset phantom ground power line (force)
HSPGS	P10	LV	Headset phantom ground feedback line (sense)
HSDET	R10	LV	Headset sleeve detection input
HSLDET	R8	LV	Headset left detection input
RXOUTR	U7	LV	Low power receive output for accessories right channel
RXOUTL	P9	LV	Low power receive output for accessories left channel
RXINR	R9	LV	General purpose receive input right channel
RXINL	U8	LV	General purpose receive input left channel
Audio Other			
REFA	R3	LV	Reference for audio amplifiers
REFB	T3	LV	Reference for low noise audio bandgap
REFC	T2	LV	Reference for voice CODEC

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- EMV for Extended Medium Voltage (5.5 V)
- MV for Medium Voltage (4.65 V)
- LV for Low Voltage (3.1 V)

Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
REFD	L2	LV	Reference for stereo DAC
PLLLPF	H2	LV	Connection for the stereo DAC PLL low pass filter.
GNDPLL	H3	—	Dedicated ground for the stereo DAC PLL block.
GNDAUD1	L10	—	Ground for audio circuitry 1 (analog)
GNDAUD2	M10	—	Ground for audio circuitry 2 (analog)
GNDAUD3	M11	—	Ground for audio circuitry 3 (analog)
GNDAUD4	M12	—	Ground for audio circuitry 4 (digital)
GNDAUD5	H9	—	Ground for audio circuitry 5 (digital)
Thermal Grounds			
GNDSUB1	N11	—	Non critical signal ground and thermal heatsink
GNDSUB2	K12	—	Non critical signal ground and thermal heatsink
GNDSUB3	K11	—	Non critical signal ground and thermal heatsink
GNDSUB4	H12	—	Non critical signal ground and thermal heatsink
GNDSUB5	J9	—	Non critical signal ground and thermal heatsink
GNDSUB6	J8	—	Non critical signal ground and thermal heatsink
GNDSUB7	L8	—	Non critical signal ground and thermal heatsink
GNDSUB8	L11	—	Non critical signal ground and thermal heatsink
Future Use			
SPARE2	H8	TBD	Spare ball for future use
SPARE4	H13	TBD	Spare ball for future use

* The maximum voltage rating is given per category of pins:
- EHV for Extended High Voltage (20 V)
- HV for High Voltage (7.5 V)
- EMV for Extended Medium Voltage (5.5 V)
- MV for Medium Voltage (4.65 V)
- LV for Low Voltage (3.1 V)

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 2 gives the maximum allowed voltages, current and temperature ratings which can be applied to the IC. Exceeding these ratings could damage the circuit.

Table 2. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Charger Input Voltage	-0.3	—	+20	V
USB Input Voltage if Common to Charger	-0.3	—	+20	V
USB Input Voltage if Separate from Charger	-0.3	—	+5.50	V
Battery Voltage	-0.3	—	+4.65	V
Coincell Voltage	-0.3	—	+4.65	V
Ambient Operating Temperature Range	-30	—	+85	°C
Operating Junction Temperature Range	-30	—	+125	°C
Storage Temperature Range	-65	—	+150	°C
ESD Protection Human Body Model	2.0	—	—	kV

3.2 Current Consumption

The current consumption of the individual blocks is described in detail throughout this specification. For convenience, below a summary table is included with the main characteristics. Note that the external loads are not taken into account.

Table 3. Summary of Current Consumption

Mode	Typ	Max	Unit
RTC	5	6	µA
OFF	30	45	µA
Power Cut	35	52	µA
User OFF	60	91	µA
ON Standby	135	220	µA
ON Default	620	1000	µA
ON Audio Call	7.3	9.9	mA
ON Stereo Playback	9.5	12.1	mA

4 Functional Description

4.1 Logic

The logic portions of the MC13783 includes the following:

- Section 4.1.1, “Programmability,” on page 17 includes a description of the dual SPI interface.
- Section 4.1.2, “Clock Generation and Real Time Clock,” on page 21 includes a description of the 32.768 kHz real time clock generation.
- Section 4.1.3, “Power Control System,” on page 22 describes the power control logic, including interface and operated modes.

4.1.1 Programmability

4.1.1.1 SPI Interface

The MC13783 IC contains two SPI interface ports which allow parallel access by both the call processor and the applications processor to the MC13783 register set. Via these registers the MC13783 resources can be controlled. The registers also provide status information about how the MC13783 IC is operating as well as information on external signals. The SPI interface is comprised of the signals listed below.

Table 4. SPI Interface Pin Description

	Description
SPI Bus	
PRICLK	Primary processor clock input line, data shifting occurs at the rising edge.
PRIMOSI	Primary processor serial data input line.
PRIMISO	Primary processor serial data output line.
PRICS	Primary processor clock enable line, active high.
SECCLK	Secondary processor clock input line, data shifting occurs at the rising edge.
SECMOSI	Secondary processor serial data input line.
SECMISO	Secondary processor serial data output line.
SECCS	Secondary processor clock enable line, active high.
Interrupt	
PRIINT	Primary processor interrupt.
SECINT	Secondary processor interrupt.
Supply	
PRIVCC	Primary processor SPI bus supply.
SECVCC	Secondary processor SPI bus supply

Both SPI ports are configured to utilize 32-bit serial data words, using 1 read/write bit, 6 address bits, 1 null bit, and 24 data bits. The SPI ports’ 64 registers correspond to the 6 address bits.

4.1.1.2 Register Set

The register set is given in Table 5.

Table 5. Register Set

Register		Register		Register		Register	
0	Interrupt Status 0	16	Regen Assignment	32	Regulator Mode 0	48	Charger
1	Interrupt Mask 0	17	Control Spare	33	Regulator Mode 1	49	USB 0
2	Interrupt Sense 0	18	Memory A	34	Power Miscellaneous	50	Charger USB 1
3	Interrupt Status 1	19	Memory B	35	Power Spare	51	LED Control 0
4	Interrupt Mask 1	20	RTC Time	36	Audio Rx 0	52	LED Control 1
5	Interrupt Sense 1	21	RTC Alarm	37	Audio Rx 1	53	LED Control 2
6	Power Up Mode Sense	22	RTC Day	38	Audio Tx	54	LED Control 3
7	Identification	23	RTC Day Alarm	39	SSI Network	55	LED Control 4
8	Semaphore	24	Switchers 0	40	Audio Codec	56	LED Control 5
9	Arbitration Peripheral Audio	25	Switchers 1	41	Audio Stereo DAC	57	Spare
10	Arbitration Switchers	26	Switchers 2	42	Audio Spare	58	Trim 0
11	Arbitration Regulators 0	27	Switchers 3	43	ADC 0	59	Trim 1
12	Arbitration Regulators 1	28	Switchers 4	44	ADC 1	60	Test 0
13	Power Control 0	29	Switchers 5	45	ADC 2	61	Test 1
14	Power Control 1	30	Regulator Setting 0	46	ADC 3	62	Test 2
15	Power Control 2	31	Regulator Setting 1	47	ADC 4	63	Test 3

4.1.1.3 Interface Requirements

4.1.1.3.1 SPI Interface Description

The operation of both SPI interfaces is equivalent. Therefore, all SPI bus names without prefix PRI or SEC correspond to both the PRISPI and SECSPI interfaces.

The control bits are organized into 64 fields. Each of these 64 fields contains 32 bits. A maximum of 24 data bits is used per field. In addition, there is one “dead” bit between the data and address fields. The remaining bits include 6 address bits to address the 64 data fields and one write enable bit to select whether the SPI transaction is a read or a write.

For each SPI transfer, first a one is written to the read/write bit if this SPI transfer is to be a write. A zero is written to the read/write bit if this is to be a read command only. If a zero is written, then any data sent after the address bits are ignored and the internal contents of the field addressed do not change when the 32nd CLK is sent. Next the 6-bit address is written, MSB first. Finally, data bits are written, MSB first. Once all the data bits are written then the data is transferred into the actual registers on the falling edge of the 32nd CLK.

The default CS polarity is active high. The CS line must remain active during the entire SPI transfer. In case the CS line goes inactive during a SPI transfer all data is ignored. To start a new SPI transfer, the CS line must go inactive and then go active again. The MISO line will be tri-stated while CS is low.

Note that not all bits are truly writable. Refer to the individual subcircuit descriptions to determine the read/write capability of each bit. All unused SPI bits in each register must be written to a zero. SPI readbacks of the address field and unused bits are returned as zero. To read a field of data, the MISO pin will output the data field pointed to by the 6 address bits loaded at the beginning of the SPI sequence.

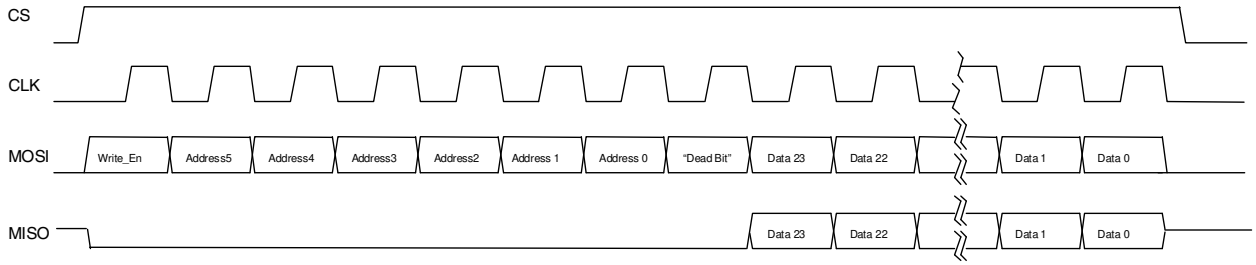

Figure 2. SPI Transfer Protocol Single Read/Write Access

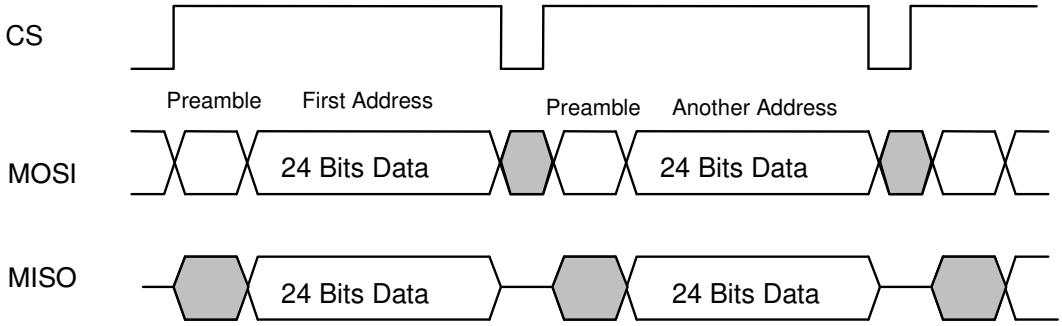

Figure 3. SPI Transfer Protocol Multiple Read/Write Access

4.1.1.3.2 SPI Requirements

The requirements for both SPI interfaces are equivalent. Therefore, all SPI bus names without prefix PRI or SEC correspond to both SPI interfaces. The below diagram and table summarize the SPI electrical and timing requirements. The SPI input and output levels are set independently via the PRIVCC and SECVCC pins by connecting those to the proper supply.

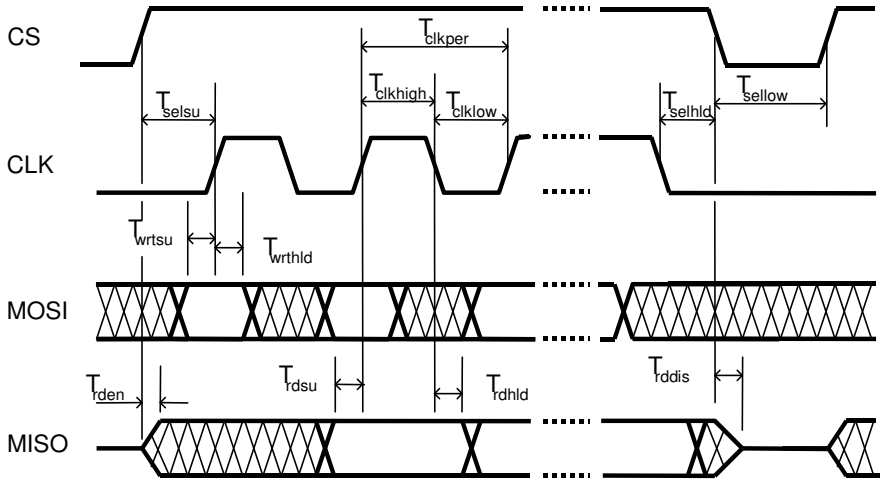

Figure 4. SPI Interface Timing Diagram

Table 6. SPI Interface Timing Specifications

Parameter	Description	T min (ns)
T_{selsu}	Time CS has to be high before the first rising edge of CLK	20
T_{selhld}	Time CS has to remain high after the last falling edge of CLK	20
T_{sellow}	Time CS has to remain low between two transfers	20
T_{clkper}	Clock period of CLK[1]	50
$T_{clkhigh}$	Part of the clock period where CLK has to remain high	20
T_{clklow}	Part of the clock period where CLK has to remain low	20
T_{wrtsu}	Time MOSI has to be stable before the next rising edge of CLK	5
T_{wrthld}	Time MOSI has to remain stable after the rising edge of CLK	5
T_{rdsu}	Time MISO will be stable before the next rising edge of CLK	5
T_{rdhld}	Time MISO will remain stable after the falling edge of CLK	5
T_{rden}	Time MISO needs to become active after the rising edge of CS	5
T_{rddis}	Time MISO needs to become inactive after the falling edge of CS	5

1 Equivalent to a maximum clock frequency of 20 MHz.

Table 7. SPI Interface Logic IO Specifications

Parameter	Condition	Min	Max	Units
Input High CS, MOSI, CLK	—	0.7*VCC	VCC+0.5	V
Input Low CS, MOSI, CLK	—	0	0.3*VCC	V
Output Low MISO, INT	Output sink 100 μA	0	0.2	V
Output High MISO, INT	Output source 100 μA	VCC-0.2	VCC	V
Note: VCC refers to PRIVCC and SECVCC respectively.				

4.1.2 Clock Generation and Real Time Clock

4.1.2.1 Clock Generation

The MC13783 generates a 32.768 kHz clock as well as several 32.768 kHz derivative clocks that are used internally for control. In addition, a 32.768 kHz square wave is output to external pins.

4.1.2.1.1 Clocking Scheme

The MC13783 contains an internal RC oscillator powered from VATLAS that delivers a 32 kHz nominal frequency (±20%) at its output when an external 32.768 kHz crystal is not present. The RC oscillator will then be used to run the debounce logic, the PLL for the switchers, the real time clock (RTC) and internal control logic, and can also be output on the CLK32K pin.

4.1.2.2 Real Time Clock

This section provides an overview of the Real Time Clock (RTC).

4.1.2.2.1 Time and Day Counters

The real time clock runs from the 32 kHz clock. This clock is divided down to a 1 Hz time tick which drives a 17 bit time of day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399 and will then roll over to 0. When the roll over occurs, it increments the 15-bit DAY counter. The DAY counter can count up to 32767 days. The 1Hz time tick can be used to generate an 1HZI interrupt. The 1HZI can be masked with corresponding 1HZM mask bit.

If the TOD and DAY registers are read at a point in time in which DAY is incremented, then care must be taken that, if DAY is read first, DAY has not changed before reading TOD.

In order to guarantee stable TOD and DAY data, all SPI reads and writes to TOD and DAY data should happen immediately after the 1HZI interrupt occurs. Alternatively, TOD or DAY readbacks could be double-read and then compared to verify that they haven't changed. This requirement results from the fact that the 32.768 kHz clock is completely independent of the SPI clock and the two cannot be synchronized.

4.1.2.2.2 Time of Day Alarm

A Time Of Day (TOD) alarm function can be used to turn on the phone and alert the processor. If the phone is already on, the processor will be interrupted. The TODA and DAYA registers are used to set the alarm time. When the TOD counter is equal to the value in TODA and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

MC13783 makes it convenient to schedule multiple daily events, where a single list could be used, or to skip any number of days.

4.1.3 Power Control System

The power control system on MC13783 interfaces with the processors via different IO signals and the SPI bus. It also uses on-chip signals and detector outputs. It supports a system with different operating modes as described below.

Table 8. MC13783 Operating Modes

Mode	Description
Off	Only the MC13783 core circuitry at VATLAS and the RTC module are powered. To exit the Off mode requires a turn on event.
Cold Start	The switchers and regulators are powered up sequentially to limit the inrush current. At the end of the start-up phase, the RESETB and RESETBMCU will be made high and the circuit transitions to On.
On	The circuit is fully powered and under SPI control. To stay in this mode, the WDI pin has to be high and remain high. If not, the part will transition to Off mode.
Memory Hold	All switchers and regulators are powered off except for VBKUP1 and VBKUP2. The RESETB and RESETBMCU are low. The MC13783 enters Cold Start mode when a turn on event occurs.
User Off	All switchers and regulators are powered off except for VBKUP1 and VBKUP2. RESETB is low and RESETBMCU is kept high. The 32 kHz output signal CLK32KMCU can be maintained in this mode as well. The MC13783 enters Warm Start mode when a turn on event occurs.
Warm Start	The switchers and regulators are powered up sequentially to limit the inrush current. The reset signals RESETB is kept low and RESETBMCU is kept high and CLK32KMCU can be kept active. At the end of the warm start up phase, the RESETB will be made high and the circuit transitions to On.
Power Cuts	Defined as a momentary loss of power. This can be caused by battery contact bounce or a user-initiated battery swap. The memory and the processor core are automatically backed up in that case by the coin cell depending on the power cut support mode selected. The maximum duration of a power cut as well as the maximum number of power cuts to be supported are programmable. When exiting the power cut mode due to reapplication of power the system will start up again on the main battery and revert back to the battery supplied modes.
Turn On Events	If the MC13783 is in Off, User Off or Memory Hold mode, the circuit can be powered on via a turn-on event. The turn-on events are listed below. To indicate to the processor which turn-on event occurred, an interrupt bit is associated with each of the turn-on events. ON1B, ON2B or ON3B pulled low, a power on/off button is connected here. • CHRGRAW pulled high which is equivalent to plugging in a charger. • BP crossing the minimum operating threshold which corresponds to attaching a charged battery to the phone. • VBUS pulled high which is equivalent to plugging in a supplied USB cable. • Time of day alarm which allows powering up a phone at a preset time.

The default power up state and sequence of the MC13783 is controlled by the power up mode select pins PUMS1, PUMS2 and PUMS3. In total three different sequences and five different default voltage setting combinations are provided. At power up all regulators and switchers are sequentially enabled at equidistant steps of 2ms to limit the inrush current.

4.2 Switchers and Regulators

4.2.1 Supply Flow

The switch mode power supplies and the linear regulators are dimensioned to support a supply flow based upon Figure 5.

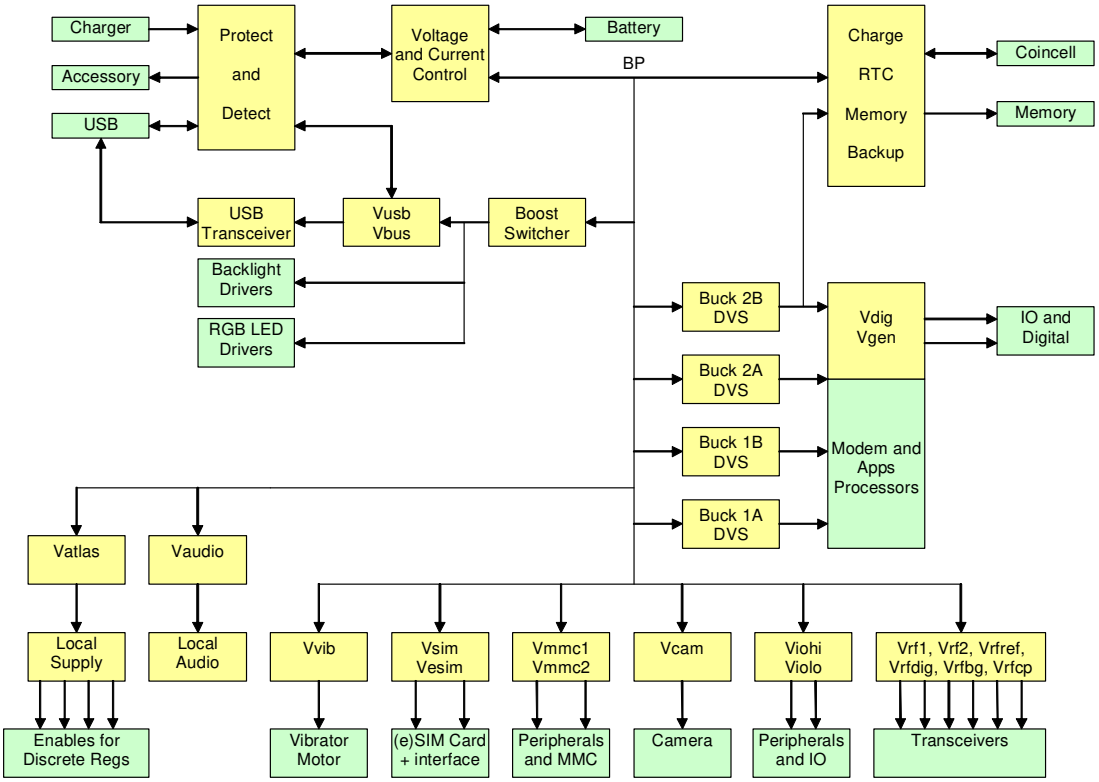

Figure 5. Supply Distribution

The minimum operating voltage for the supply tree, while maintaining the performance as specified, is 3.0 V. For lower voltages the performance may be degraded.

Table 9 summarizes supply output voltages.

Table 9. Regulator Output Voltages

Supply	Output (V)	Load (mA)	
SW1A	0.900 - 1.675 in 25 mV steps, 1.700 - 2.200 in 100 mV steps	500	1A
SW1B		500	
SW2A		500	1A
SW2B		500	
SW3	5.0 / 5.5	350/300	
VAUDIO	2.775	200	
VIOHI	2.775	200	

Table 9. Regulator Output Voltages (continued)

Supply	Output (V)	Load (mA)
VIOLO	1.2/1.3/1.5/.18	150 (Vout < 1.5V)/200 (Vout ≥ 1.5V)
VDIG	1.2/1.3/1.5/.18	150 (Vout < 1.3V)/200 (Vout ≥ 1.3V)
VRFDIG	1.2/1.5/1.8/1.875	150 (Vout < 1.8V)/200 (Vout ≥ 1.8V)
VGEN	1.1/1.2/1.3/1.5/1.8/2.0/2.4/2.775	150 (Vout < 1.5V)/200 (Vout ≥ 1.5V)
VCAM	1.5/1.8/2.5/2.55/2.6/2.75/2.8/3.0	150
VRFBG	1.250	0.1
VRFREF	2.475/2.600/2.700/2.775	50
VRFCP	2.700/2.775	50
VSIM	1.8/2.9	60
VESIM	1.8/2.9	60
VVIB	1.3/1.8/2.0/3.0	200
VUSB	2.775/3.3	50
VBUS	5.0	50
VRF1	1.5/1.875/2.7/2.775	350
VRF2	1.5/1.875/2.7/2.775	350
VMMC1	1.6/1.8/2.0/2.6/2.7/2.8/2.9/3.0	350
VMMC2	1.6/1.8/2.0/2.6/2.7/2.8/2.9/3.0	350

Table 10 lists characteristics that apply to MC13783 regulators. Table 11 on page 25 lists characteristics that apply only to the buck switchers.

Table 10. Regulator General Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operating Input Voltage Range Vinmin to Vinmax	—	Vnom + 0.3		4.65	V
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom - 3%	Vnom	Vnom + 3%	V
Load Regulation	1mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	µA
Low Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	µA
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz Vin = Vnom + 1V	50	60	—	dB

Table 10. Regulator General Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Minimum Bypass Capacitor Value	Used as a condition for all other parameters.	-35%	2.2	+35%	µF
Minimum Bypass Capacitor Value for: VRFREF, VRFCP, VIOHI, VSIM, VESIM	Used as a condition for all other parameters.	-35%	1	—	µF
Bypass Capacitor Value for VAUDIO	Used as a condition for all other parameters.	-35%	1	+35%	µF
Bypass Capacitor Value for VRFBG	Used as a condition for all other parameters.	—	100	—	nF
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω

Table 11. Buck Switcher Characteristics

Parameter	Condition	Min	Typ	Max	Units
Output Voltage	2.8 V < BP < 4.65 V 0 < IL < 500 mA	0.900 V to 1.675 V in 25 m V steps 1.700 V to 2.200 V in 100 V steps			V
Output Accuracy	PWM Mode, including ripple and load regulation	-50	—	+50	mV
Transient Load Response	IL from 5 mA to 400 mA in 1µs IL from 400 mA to 5 mA in 1µs	—	—	+/- 25	mV
Effective Quiescent Current Consumption	PWM MODE	—	50	—	µA
	PFM MODE	—	15	—	µA
External Components	Inductor	-20%	10	+20%	µH
	Inductor Resistance	—	—	0.16	Ω
	Bypass Capacitor	-35%	22	+35%	µF
	Bypass Capacitor ESR	0.005	—	0.1	Ω

The buck switchers support dynamic voltage scaling (DVS). The buck switchers are designed to directly supply the processor cores. To reduce overall power consumption, core voltages of processors may be varied depending on the mode the processor is in. The DVS scheme of the buck switchers allows to transition between the different set points in a controlled and smooth manner.

For reduced current drain in low power modes, parts of a processor may be power gated, that is to say, the supply to that part of the processor is disabled. To simplify the supply tree and to reduce the number of external components while maintaining flexibility, power gate switch drivers are included.