Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Freescale Semiconductor
Technical Data

Document Number: MC13853
Rev. 1.8, 8/2008

RoHS

MC13853

MC13853

Tri-Band Low Noise Amplifiers with Bypass Switches

Package Information
Plastic Package
(QFN–16)

Ordering Information

Device	Device Marking or Operating Temperature Range	Package
MC13853	853	QFN-16

1 Introduction

The MC13853 is a SPI controlled, tri-band, high gain LNA with extremely low noise figure, designed for cellular band applications. Integrated bypass switches are included to preserve input intercept performance. The input and output match are external to allow maximum design flexibility. The MC13853 is fabricated using Freescale's advanced RF BiCMOS process using the SiGe:C option and is packaged in the QFN-16 leadless package.

1.1 Features

- RF input frequency: 800 MHz to 2.4 GHz
- Gain: 13.5 dB (typical) at 1960 MHz, 15 dB (typical) at 2140 MHz, and 13.5 dB (typical) at 880 MHz
- Input 3rd order intercept point (IIP3): -3 dBm (typical) at 880 MHz, -4.0 dBm (typical) at 1960 MHz, and -3.0 dBm (typical) at 2140 MHz
- Noise figure (NF): 1.5 dB (typical) at 880 MHz, 1.5 dB (typical) at 1960 MHz, and 1.6 dB (typical) at 2140 MHz

Contents

freescale semiconductor

- Current Settings are SPI controllable
- Freescale's IP3 boost circuitry
- Bypass mode included for improved intercept point performance
- Total supply current:
  LB – 9.7 mA in current setting 6
  HB1 – 9.2 mA in current setting 6
  HB2 – 6.5 mA in current setting 2
  10 µA (typical) in bypass mode
- Bias stabilized for device and temperature variations
- QFN-16 leadless package with low parasitics
- SiGe technology ensures lowest possible noise figure
- SPI controlled
- At POR, all bands default to bypass mode. In deep sleep mode, all bands are set to disable mode.

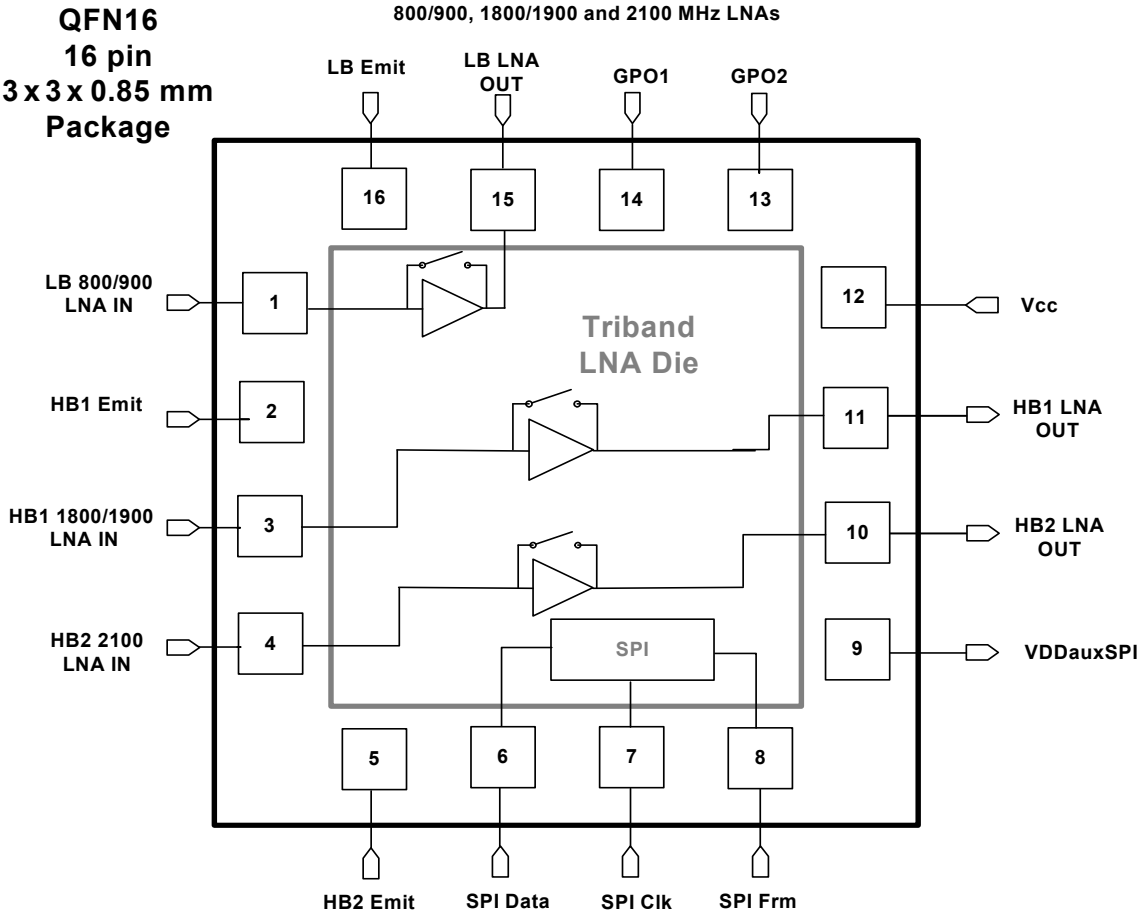


Figure 1. Simplified Block Diagram

2 Electrical Specifications

Table 1. Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.3	V
Storage Temperature Range	T_{stg}	-65 to 150	°C
Operating Ambient Temperature Range	T_A	-30 to 85	°C
RF Input Power	P_{rf}	10	dBm
Power Dissipation	P_{dis}	100	mW
Thermal Resistance, Junction to Case	$R_{\theta JC}$	24	C/W
Thermal Resistance, Junction to Ambient, 4 Layer Board	$R_{\theta JA}$	90	C/W
ESD Rating HBM RF Pins		100	V
ESD Rating HBM non-RF Pins		550	V

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
RF Frequency Range	f_{RF}	800		2400	MHz
Supply Voltage	V_{CC} VDDauxSPI	2.6 1.5	2.775 1.8	3 2.1	V
Logic Voltage Input High Voltage Input Low Voltage		 1.25 0	 – –	 V_{CC} 0.8	V

NOTES: 1.Supply voltage Vcc must be on before VDDauxSPI.

Table 3. Electrical Characteristics in Frequency Specific Tuned Circuits
(V_{CC} = 2.775 V, 25°C)

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
880 MHz (Refer to Figure 4)					
Frequency	f	869	880	894	MHz
Active Gain Band V Band VI	G	 12.5 12.5	 13.5 13.5	 14.5 14.5	dB
Active Noise Figure	NF	–	1.4	1.5	dB
Active Input Third Order Intercept Point	IIP3	-3	-2.5	–	dBm
Active Input 1 dB Compression Point	P_{1dB}	-9.5	-9	–	dBm
Active Current @ 2.75 V in current setting 6	I_{CC}	–	8.6	10.2	mA

Table 3. Electrical Characteristics in Frequency Specific Tuned Circuits (continued)
(V_{CC} = 2.775 V, 25°C)

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Bypass Gain	G	-10	-9.5	–	dB
Bypass Input Third Order Intercept Point	IIP3	16	22	–	dBm
Bypass Current		–	10	20	µA
950 MHz (Refer to Figure 5)					
Frequency	f	925	950	960	MHz
Active Gain	G	11.0	12.0	13.0	dB
Active Noise Figure	NF	–	1.45	1.5	dB
Active Input Third Order Intercept Point	IIP3	-3	-2.5	–	dBm
Active Input 1 dB Compression Point	P_{1dB}	-9	-8.5	–	dBm
Active Current @ 2.75 V in current setting 6	I_{CC}	–	8.6	10.2	mA
Bypass Gain	G	-10	-9.5	–	dB
Bypass Input Third Order Intercept Point	IIP3	16	22	–	dBm
Bypass Current		–	10	20	µA
1850 MHz (Refer to Figure 6)					
Frequency	f	1805	1850	1880	MHz
Active Gain	G	12.5	13.5	14.5	dB
Active Noise Figure	NF	–	1.55	1.6	dB
Active Input Third Order Intercept Point	IIP3	-3	-2.5	–	dBm
Active Input 1 dB Compression Point	P_{1dB}	-12.5	-11.7	–	dBm
Active Current @ 2.75 V in current setting 6	I_{CC}	–	7.8	9.7	mA
Bypass Gain	G	-9.5	-9	–	dB
Bypass Input Third Order Intercept Point	IIP3	16	22	–	dBm
Bypass Current		–	10	20	µA
1960 MHz (Refer to Figure 7)					
Frequency	f	1930	1960	1990	MHz
Active Gain	G	12.5	13.5	14.5	dB
Active Noise Figure	NF	–	1.55	1.6	dB
Active Input Third Order Intercept Point	IIP3	-3	-2.5	–	dBm
Active Input 1 dB Compression Point	P_{1dB}	-12.5	-12	–	dBm
Active Current @ 2.75 V in current setting 6	I_{CC}	–	7.8	9.7	mA
Bypass Gain	G	-9.5	-9	–	dB
Bypass Input Third Order Intercept Point	IIP3	20	22	–	dBm
Bypass Current		–	10	20	µA

Table 3. Electrical Characteristics in Frequency Specific Tuned Circuits (continued)
(V_{CC} = 2.775 V, 25°C)

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
2140 MHz (Refer to Figure 8)					
Frequency	f	2110	2140	2170	MHz
Active Gain	G	14	15	16	dB
Active Noise Figure	NF	–	1.55	1.6	dB
Active Input Third Order Intercept Point	IIP3	-3	-2.5	–	dBm
Active Input 1 dB Compression Point	P_{1dB}	-12	-11	–	dBm
Active Current @ 2.75 V in current setting 2	I_{CC}	–	6.0	7.0	mA
Bypass Gain	G	-6.5	-6	–	dB
Bypass Input Third Order Intercept Point	IIP3	20	22	–	dBm
Bypass Current		–	10	20	µA

Table 4. Electrical Characteristics Over Temperature (-30°C to 85°C)

Characteristic	Symbol	Minimum	Maximum	Unit
High Gain Mode Current	Icc			mA
LNA1 HB2		–	8.3	
LNA2 HB1		–	11.5	
LNA3 LB		–	10.2	
Bypass Mode Current	Icc		30	µA
Active Gain Variation Across Temperature	G			dB
85°C relative to 25°C		-1.0	+0.5	
-30°C relative to 25°C		-0.5	+1.0	
	G			dB
85°C relative to 25°C		-1.0	+0.5	
-30°C relative to 25°C		-0.5	+1.0	
Noise Figure relative to 25°C	NF		+0.4	dB
Active Input Third Order Intercept relative to 25°C	IIP3	-2.0	–	dBm

Table 5. Truth Table for SPI Operation

Mode	Gain Bit	Enable Bit
Active	1	1
Bypass Gain	0	0
Disable	1	0
Not Used	0	1
Note: At power on reset (POR), the mode is set to bypass gain on all LNAs.		

Table 6. SPI Programmable Current Draw (25°C)

SPI bit			Typical Current (mA)			Current Setting
Current 2	Current 1	Current 0	LNA 1 HB2	LNA 2 HB1	LNA3 LB	
0	0	0	7.4	8.0	8.6	0
0	0	1	4.4	4.5	5.0	1
0	1	0	5.3	5.6	6.2	2
0	1	1	9.1	9.8	10.8	3
1	0	0	1.8	2.2	2.0	4
1	0	1	6.2	6.5	7.2	5
1	1	0	7.1	7.7	8.3	6
1	1	1	9.8	11.0	11.9	7
Default current setting shown in gray for each band						

Table 7. Maximum Current

	25°C	-30°C to 85°C	Unit
Deep Sleep Mode - Vcc on and VDDauxSPI off	1	5	µA
VDDauxSPI during a read operation	400	400	µA

SPI bit word

Clock →		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
		Address structure														**Data Structure**															
Bit # →		**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Not Variable →			**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**																			
Variable ↓		**Write / Read Bit**	**Device Type is LNA**	**Device Type is LNA**	**Device Type is LNA**	**Device is Iota**	**Device is Iota**	**Device is Iota**	**Device is Iota**	**Device is Iota**	**LNA Selector PA4**	**LNA Selector PA3**	**LNA Selector PA2**	**LNA Selector PA1**	**LNA Selector PA0**										**Current 2**	**Current 1**	**Current 0**		**Enable**	**Gain**	
SPI Data	Write	**0**																													
	Read	**1**																													
LNA Selector	LNA1 HB2												**0**	**0**	**0**																
	LNA2 HB1												**0**	**0**	**1**																
	LNA3 LB												**0**	**1**	**0**																
	GPO (Ext LNA)												**1**	**0**	**0**																
Mode Selector	Active																												**1**	**1**	
	Bypass																												**0**	**0**	
	Disable																												**0**	**1**	
	Not Used																												**1**	**0**	
Current Selector (default)	LNA1 HB2																								**0**	**1**	**0**				
	LNA2 HB1																								**1**	**1**	**0**				
	LNA3 LB																								**1**	**1**	**0**				
																													GPO2	**GPO1**	
Mode Selector for GPO (External LNA)	Active																												**1**	**1**	
	Bypass																												**1**	**0**	
	Disable																												**0**	**0**	
	Disable																												**0**	**1**	

Read Mode

		Address structure															**Data Structure**														
Bit # →		**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**		**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Not Variable →			**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**																				
Variable ↓																**one extra clock cycle in read mode**								**HID 8**	**HID 7**	**HID 6**	**HID 5**	**HID 4**	**HID 3**	**HID 2**	**HID 1**	**HID 0**
SPI Data	Read	**1**																														
LNA Selector																																
	For Hardware Read												**0**	**1**	**1**																	

Figure 2. SPI Bit Word

Table 8. SPI Used for Dual-, Tri-, and Quad-Band Configurations

					SPI Inputs								
					LNA Selector			Enable	Gain	Outputs			
		PATH #	Bit 22	Bit 21	PA2	PA1	PA0	D2	D1	GPO1	GPO2	Mode	
Dual- or Tri-band Config	Tri-band LNA #1	1	0	1	0	0	0	1	1	No Connect	No Connect	LNA1 Active	LNAs 1, 2, and 3 or LNAs 1 and 2
		1	0	1	0	0	0	0	0	No Connect	No Connect	LNA1 Bypass	
		1	0	1	0	0	0	0	1	No Connect	No Connect	LNA1 Off	
		2	0	1	0	0	1	1	1	No Connect	No Connect	LNA2 Active	
		2	0	1	0	0	1	0	0	No Connect	No Connect	LNA2 Bypass	
		2	0	1	0	0	1	0	1	No Connect	No Connect	LNA2 Off	
		3	0	1	0	1	0	1	1	No Connect	No Connect	LNA3 Active	
		3	0	1	0	1	0	0	0	No Connect	No Connect	LNA3 Bypass	
		3	0	1	0	1	0	0	1	No Connect	No Connect	LNA 3 Off	
Note: This is an SPI-controlled, tri-band MC13853 LNA.													
Quad-band Config	Tri-band LNA #1	1	0	1	0	0	0	1	1	To Ext LNA	To Ext LNA	LNA1 Active	LNAs 1, 2, 3, and 4
		1	0	1	0	0	0	0	0	To Ext LNA	To Ext LNA	LNA1 Bypass	
		1	0	1	0	0	0	0	1	To Ext LNA	To Ext LNA	LNA1 Off	
		2	0	1	0	0	1	1	1	To Ext LNA	To Ext LNA	LNA2 Active	
		2	0	1	0	0	1	0	0	To Ext LNA	To Ext LNA	LNA2 Bypass	
		2	0	1	0	0	1	0	1	To Ext LNA	To Ext LNA	LNA2 Off	
		3	0	1	0	1	0	1	1	To Ext LNA	To Ext LNA	LNA3 Active	
		3	0	1	0	1	0	0	0	To Ext LNA	To Ext LNA	LNA3 Bypass	
		3	0	1	0	1	0	0	1	To Ext LNA	To Ext LNA	LNA3 Off	
	Single LNA	4	0	1	1	0	0	1	1	NA	NA	LNA4 Active	
		4	0	1	1	0	0	**1**	**0**	NA	NA	LNA4 Bypass	
		4	0	1	1	0	0	**0**	**0**	NA	NA	LNA4 Off	
Note: This is one SPI-controlled, tri-band MC13853 LNA and one external LNA (not a MC13853) controlled by GPO from the MC13853 LNA.													

The different banding LNA combinations are:
- Dual band (using one MC13853)
- Tri-band (using one MC13853)
- Quad-band (using one MC13853 and one single-band GPO-controlled external LNA (not a MC13853))

3 Application Information

The MC13853 SiGe:C LNA is designed for applications in the 800 MHz to 2.1 GHz range. It has three different modes: High Gain, Low Gain (Bypass) and Disabled. The IC mode is programmable through the Gain and Enable bits. The current setting is also SPI programmable. The logic truth table is given in Table 5.

In these application examples a balance is made between the competing RF performance characteristics of I_{CC}, NF, gain, IP3 and return losses with unconditional stability. Conjugate matching is not used for the input or output. Instead, matching which achieves a trade-off in RF performance qualities is utilized. For a particular application or spec requirement, the matching can be changed to achieve enhanced performance of one parameter at the expense of other parameters.

Application information for 880, 950, 1800, 1960, and 2140 MHz are shown. Measurements are made at a bias of V_{CC} = 2.775 V. Freq. spacing for IP3 measurements is 800 kHz for 2G and 10 MHz for 3GPP. The board loss corrections for these boards are: Input 0.16 dB, Output 0.2 dB. NF results incorporate these corrections in order to better reflect the actual performance of the device.

Two MC13853 devices can also be used with common SPI control lines for a quad-band application, as shown in Figure 3. In this application, LB and HB1 are used on LNA1 and HB2 is used on LNA2. In active mode, both LNAs are active, but only one is connected in the circuit. Depending on which band is selected in the connected LNA, the corresponding un-connected LNA which would also become active when the SPI command is sent to the connected LNA will draw <1 mA for LB, <1.2 mA for HB1 and <1mA for HB2 in active mode over temperature.

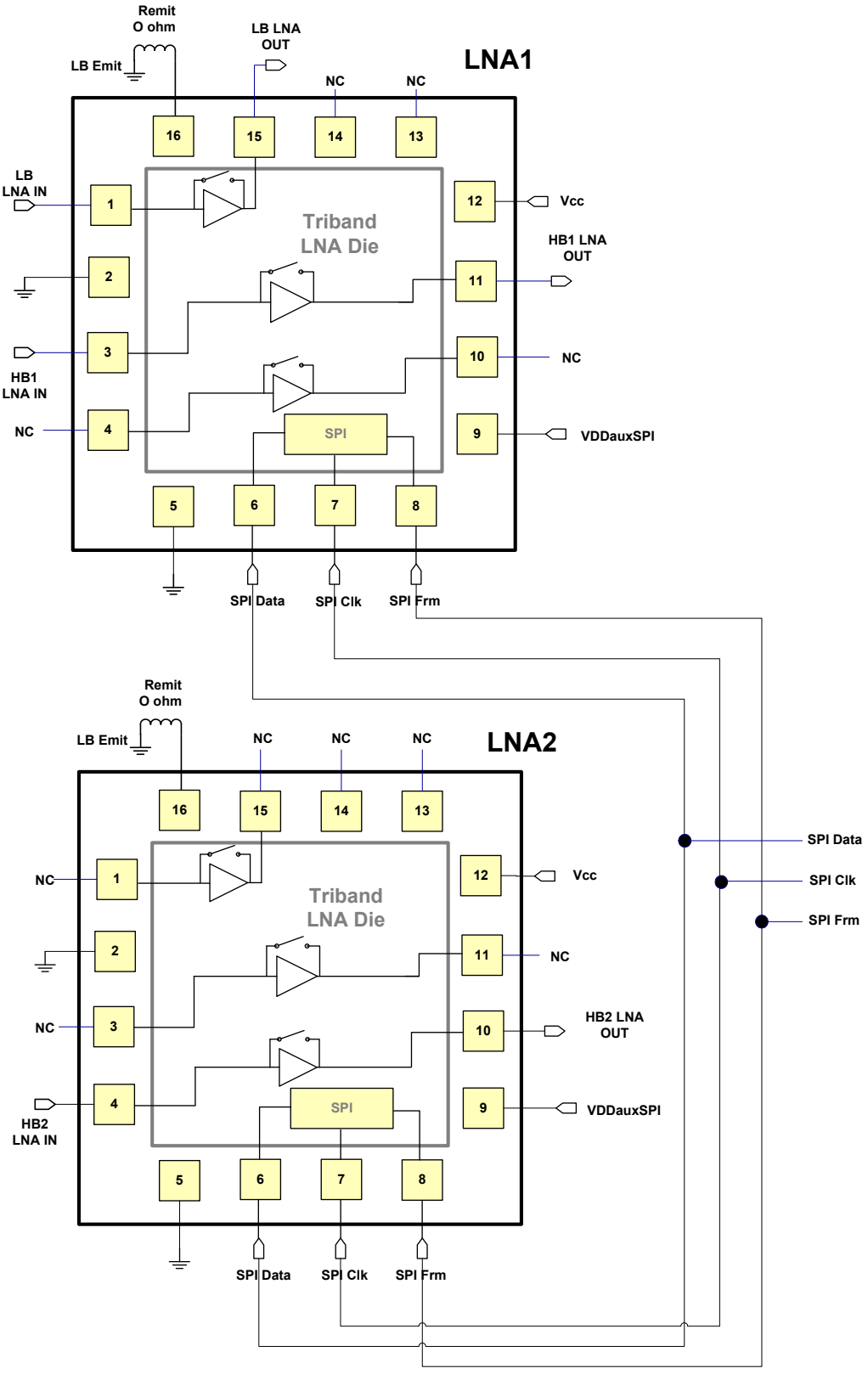


Figure 3. Application Circuit with Two MC13853s Controlled by Common SPI Lines

3.1 880 MHz Application

This application circuit was designed to provide NF 1.5 dB, typical S21 gain of 13.5 dB, IIP3 of -3 dBm. Typical performance that can be expected from this circuit at 2.775 V V_{CC} is listed in Table 9. The component values can be changed to enhance the performance of a particular parameter, but usually at the expense of another.

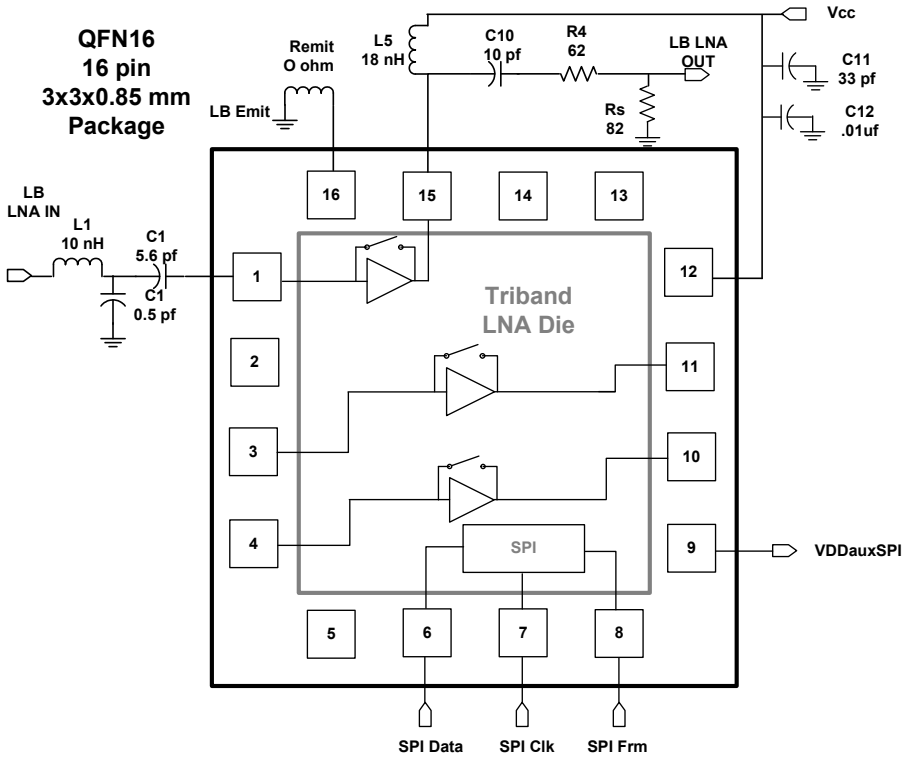


Figure 4. 880 MHz LNA Application Schematic

Table 9. Typical 880 MHz LNA Demo Board Performance (25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	869	880	894	MHz
Power Gain High Gain Band V High Gain Band VI Bypass	G	 12.5 12.5 -10	 13.5 13.5 -9.5	 14.5 14.5 –	dB
Input Third Order Intercept Point High Gain Bypass	IIP3	 -3 16	 -2.5 22	 – –	dBm
In Ref P1dB High Gain Bypass	P_{1dBin}	 -9.5 0	 -9 3.5	 – –	dBm
Noise Figure High Gain Bypass	NF	 – –	 1.45 3	 1.5 6	dB

Table 9. Typical 880 MHz LNA Demo Board Performance (continued)(25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Drain in current setting 6 High Gain Bypass	I_{CC}	 – –	 8.5 10	 10.2 20	 mA µA
Input Return Loss High Gain Bypass	S11	 -10 -3	 -11 -3.5	 – –	dB
Gain High Gain Bypass	S21	 12.5 -10	 13.5 -9.5	 14.5 –	dB
Reverse Isolation High Gain Bypass	S12	 -20 –	 -22 -4	 – –	dB
Output Return Loss High Gain Bypass	S22	 -10 -3	 -11 -3.5	 – –	dB
P_{IN} IM2 F_{INT} = RX/2 at -40 dBm	IM2	 -56	 -58	 –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = TX +RX at -49 dBm		 -62 –	 -63 –	 – –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = RX -TX at -54 dBm		 -55 –	 -54 –	 – –	dBm
Switching Time from 20% top 90% of VIH	TRISE TFALL	– –	– –	5 5	µs

3.2 950 MHz Application

This application circuit was designed to provide NF < 1.5 dB, S21 gain of 12 dB, IIP3 of -3 dBm. Typical performance that can be expected from this circuit at 2.775 V V_{CC} is listed in Table 10. The component values can be changed to enhance the performance of a particular parameter, but usually at the expense of another.

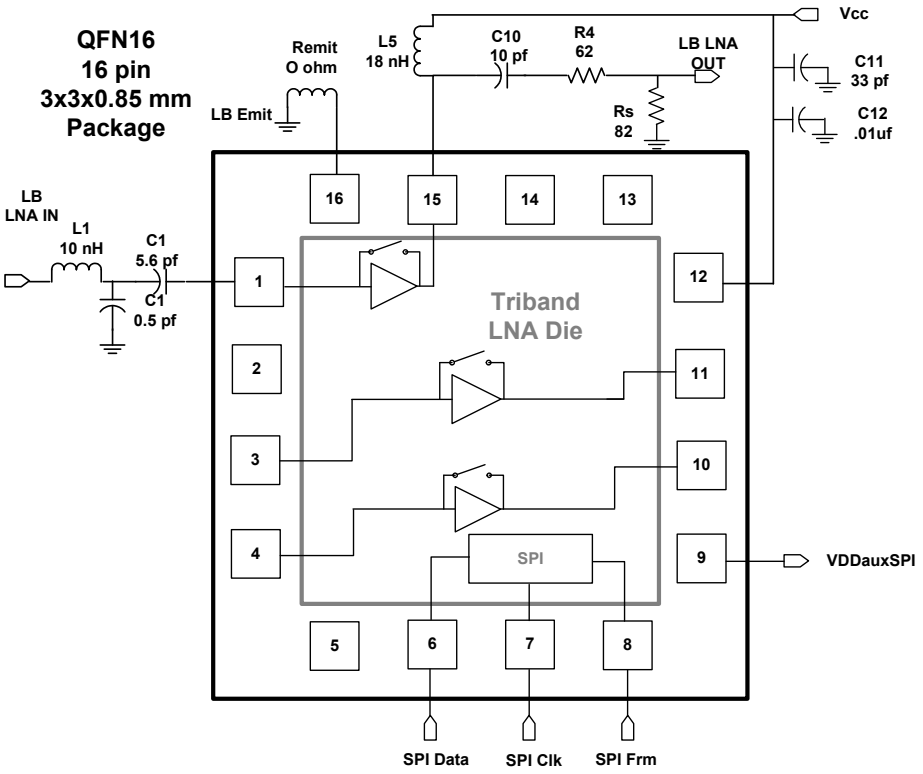


Figure 5. 950 MHz LNA Application Schematic

Table 10. Typical 950 MHz LNA Demo Board Performance (25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	925	950	960	MHz
Power Gain High Gain Bypass	G	 11 -10	 12 -9.5	 13 –	dB
Input Third Order Intercept Point High Gain Bypass	IIP3	 -3 16	 -2.5 22	 – –	dBm
In Ref P1dB High Gain Bypass	P_{1dBin}	 -9 0	 -8.5 3.5	 – –	dBm
Noise Figure High Gain Bypass	NF	 – –	 1.45 3	 1.5 6	dB

Table 10. Typical 950 MHz LNA Demo Board Performance (25°C) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Drain in current setting6 High Gain Bypass	I_{CC}	 – –	 8.5 10	 10.2 20	 mA µA
Input Return Loss High Gain Bypass	S11	 -10 -3	 -11 -3.5	 – –	dB
Gain High Gain Bypass	S21	 11 -10	 12 -9.5	 13 –	dB
Reverse Isolation High Gain Bypass	S12	 -20 –	 -22 -4	 – –	dB
Output Return Loss High Gain Bypass	S22	 -10 -3	 -11 -3.5	 – –	dB
P_{IN} IM2 F_{INT} = RX/2 at -40 dBm	IM2	 -56	 -57	 –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = TX +RX at -49 dBm		 -62 –	 -63 –	 – –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = RX -TX at -54 dBm		 -55 –	 -56 –	 – –	dBm
Switching Time From 20% top 90% of VIH From 20% top 90% of VIL	 TRISE TFALL	 – –	 – –	 5 5	µs

3.3 1850 MHz Application

This application circuit is designed to demonstrate performance at 1850 MHz. Typical performance that can be expected from this circuit at 2.775 V V_{CC} is listed in Table 11. The match consists of a highpass match on the output and a simple inductor-capacitor network on the LNA input.

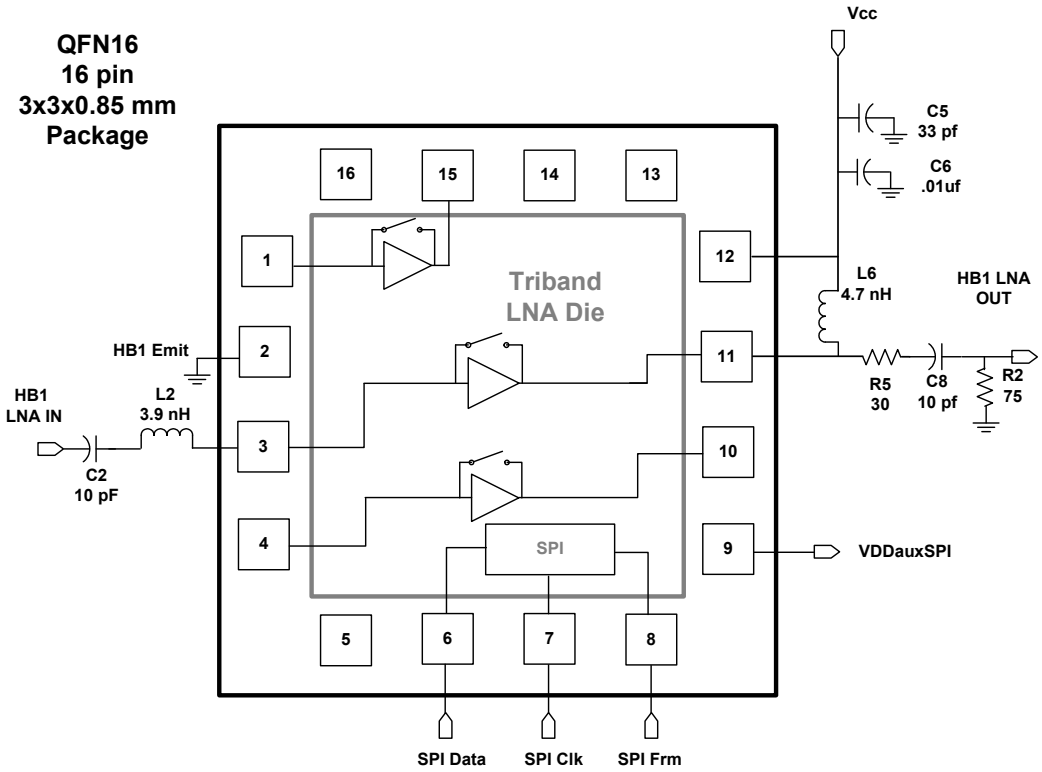


Figure 6. 1850 MHz LNA Application Schematic

Table 11. Typical 1850 MHz LNA Demo Board Performance (25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	1805	1850	1880	MHz
Power Gain High Gain Bypass	G	 12.5 -9.5	 13.5 -9	 14.5 –	dB
Input Third Order Intercept Point High Gain Bypass	IIP3	 -3 16	 -2.5 22	 – –	dBm
In Ref P1dB High Gain Bypass	P_{1dBin}	 -12.5 0	 -11.7 3.5	 – –	dBm
Noise Figure High Gain Bypass	NF	 – –	 1.55 3	 1.6 6	dB

Table 11. Typical 1850 MHz LNA Demo Board Performance (25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Drain in current setting 6 High Gain Bypass	I_{CC}	 – –	 7.9 10	 9.7 20	 mA µA
Input Return Loss High Gain Bypass	S11	 -10 -3	 -11 -3.5	 – –	dB
Gain High Gain Bypass Disabled	S21	 12.5 -9.5 –	 13.5 -9 -15	 14.5 – –	dB
Reverse Isolation High Gain Bypass	S12	 -20 -3	 -22 -4	 – –	dB
Output Return Loss High Gain Bypass	S22	 -10 -3	 -11 -3.5	 – –	dB
P_{IN} IM2 P_{INT} = RX/2 @ -40 dBm	IM2	 -56	 -57	 –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = TX +RX at -49 dBm		 -62 –	 -63 –	 – –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = RX -TX at -54 dBm		 -55 –	 -56 –	 – –	dBm
Switching Time From 20% top 90% of VIH From 20% top 90% of VIL	 TRISE TFALL	 – –	 – –	 5 5	µs

3.4 1960 MHz Application

This application circuit is designed to demonstrate performance at 1960 MHz. Typical performance that can be expected from this circuit at 2.775 V V_{CC} is listed in Table 12. The match consists of a highpass match on the output and a simple inductor-capacitor network on the LNA input.

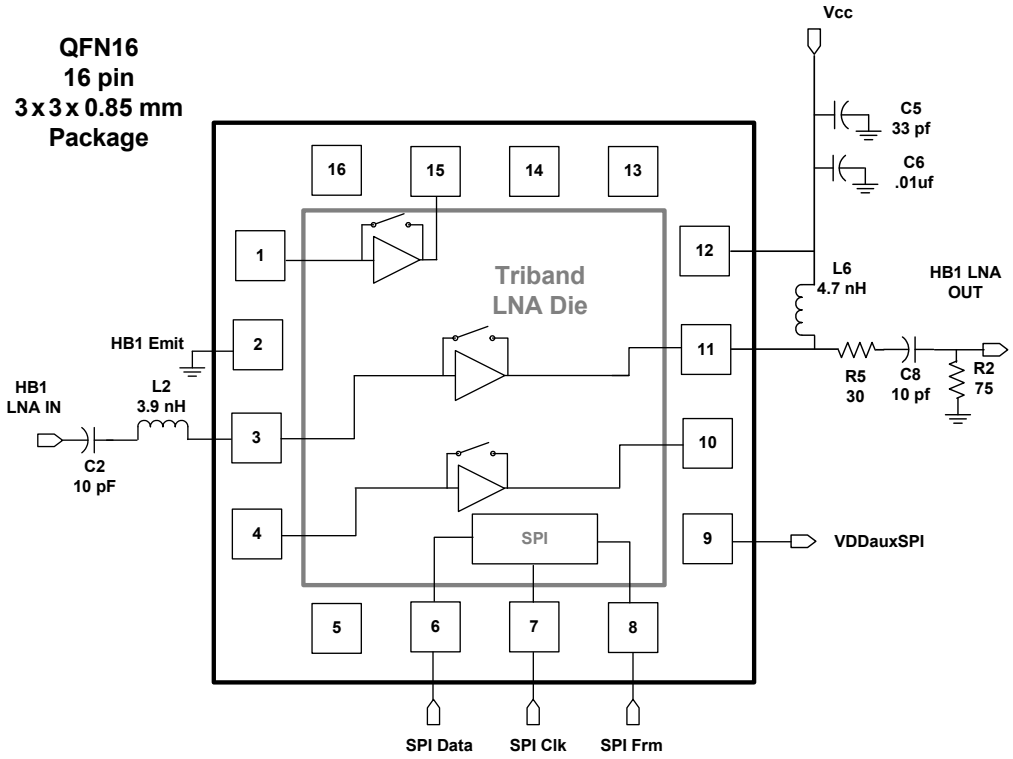


Figure 7. 1960 MHz LNA Application Schematic

Table 12. Typical 1960 MHz LNA Demo Board Performance (25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	1930	1850	1990	MHz
Power Gain High Gain Bypass	G	 12.5 -9.5	 13.5 -9	 14.5 –	dB
Input Third Order Intercept Point High Gain Bypass	IIP3	 -3 16	 -2.5 22	 – –	dBm
In Ref P1dB High Gain Bypass	P_{1dBin}	 -12.5 0	 -12 3.5	 – –	dBm
Noise Figure High Gain Bypass	NF	 – –	 1.6 3	 1.7 6	dB

Table 12. Typical 1960 MHz LNA Demo Board Performance (25°C) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Drain in current setting 6 High Gain Bypass	I_{CC}	 – –	 7.9 10	 9.7 20	 mA µA
Input Return Loss High Gain Bypass	S11	 -10 -3	 -11 -3.5	 – –	dB
Gain High Gain Bypass Disabled	S21	 12.5 -9.5 –	 13.5 -9 -15	 14.5 – –	dB
Reverse Isolation High Gain Bypass	S12	 -20 -3	 -22 -4	 – –	dB
Output Return Loss High Gain Bypass	S22	 -10 -3	 -11 -3.5	 – –	dB
P_{IN} IM2 P_{INT} = RX/2 @ -40 dBm	IM2	 -56	 -57	 –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = TX +RX at -49 dBm		 -62 –	 -63 –	 – –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = RX -TX at -54 dBm		 -55 –	 -56 –	 – –	dBm
Switching Time From 20% top 90% of VIH From 20% top 90% of VIL	 TRISE TFALL	 – –	 – –	 5 5	µs

3.5 2140 MHz Application

These application circuits demonstrate performance at 2140 MHz. Typical performance that can be expected from this circuit at 2.775 V V_{CC} is listed in Table 13.

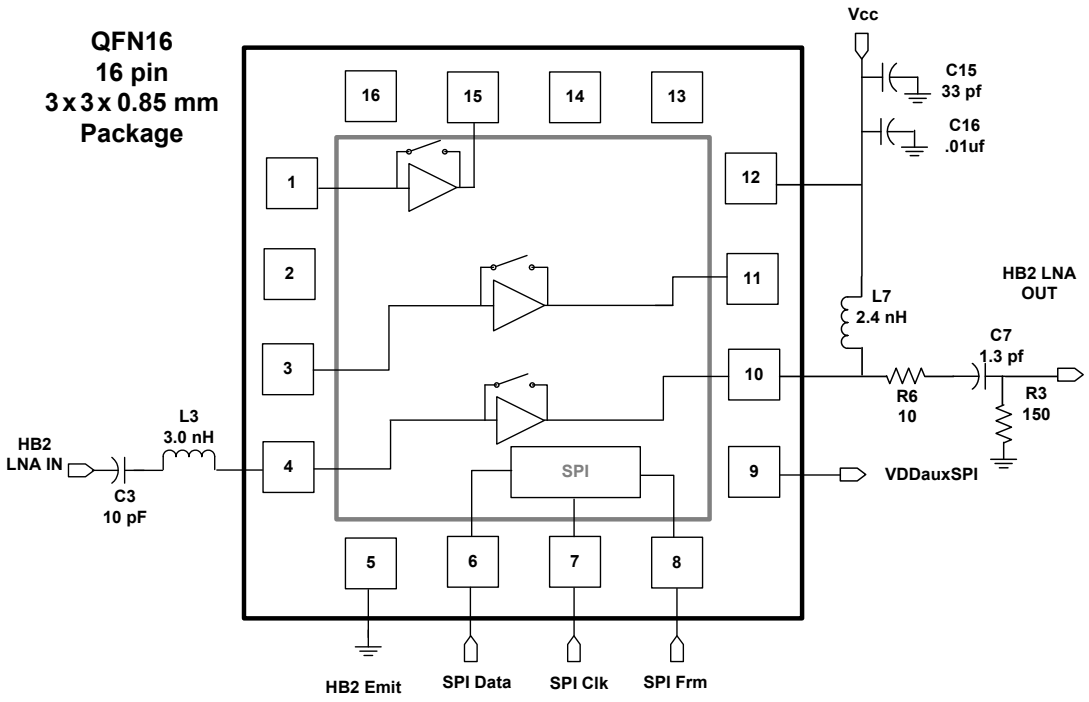


Figure 8. 2140 MHz LNA Application Schematic

Table 13. Typical 2140 MHz LNA Demo Board Performance (25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	2110	2140	2170	MHz
Power Gain High Gain Bypass	G	 14 -6.5	 15 -6	 16 –	dB
Input Third Order Intercept Point High Gain Bypass	IIP3	 -3 20	 3 22	 – –	dBm
In Ref P1dB High Gain Bypass	P_{1dBin}	 -12 0	 -11 3.5	 – –	dBm
Noise Figure High Gain Bypass	NF	 – –	 1.55 3	 1.6 6	dB
Current Drain in current setting 2 High Gain Bypass	I_{CC}	 – –	 6.0 10	 7.0 20	 mA µA

Table 13. Typical 2140 MHz LNA Demo Board Performance (25°C) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Return Loss High Gain Bypass	S11	 -10 -3	 -11 -3.5	 – –	dB
Gain High Gain Bypass	S21	 14 -6.5	 15 -6	 16 –	dB
Reverse Isolation High Gain Bypass	S12	 -20 -3.5	 -20 -4	 – –	dB
Output Return Loss High Gain Bypass	S22	 -10 -3	 -11 -3.5	 – –	dB
P_{IN} IM2 P_{INT} = RX/2 @ -40 dBm	IM2	 -56	 -57		dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = TX +RX at -49 dBm		 -62 –	 -63 –	 – –	dBm
P_{IN} IM2 F_{INT1} = TX at -27 dBm F_{INT2} = RX -TX at -54 dBm		 -55 –	 -56 –	 – –	dBm
Switching Time From 20% top 90% of VIH From 20% top 90% of VIL	 TRISE TFALL	 – –	 – –	 5 5	µs

Table 14. Bill of Materials

Component	Value	Case	Manufacturer	Comments
880 MHz				
C1	5.6 pF	402	Murata	Input match
C19	0.5 pF	402	Murata	Input match
C10	10 pF	402	Taiyo Yuden	Output match
C11	33 pF	402	Murata	RF bypass
C12	.01 µF	402	Murata	Low freq bypass
L1	10 nH	402	TOKO	Input match
L5	18 nH	402	TOKO	DC feed/output match
R4	62 Ω	402	KOA	Stability/reduce gain
RS	82 Ω	402	KOA	Stability
Remit	0Ω	402	KOA	Stability
Q1	MC13853	QFN-16	Freescale	

Table 14. Bill of Materials (continued)

Component	Value	Case	Manufacturer	Comments
950 MHz				
C1	5.6 pF	402	Murata	Input match
C19	0.5 pF	402	Murata	Input match
C10	10 pF	402	Taiyo Yuden	Output match
C11	33 pF	402	Murata	RF bypass
C12	.01 µF	402	Murata	Low freq bypass
L1	10 nH	402	TOKO	Input match
L5	18 nH	402	TOKO	DC feed/output match
R4	62 Ω	402	KOA	Stability/reduce gain
RS	82 Ω	402	KOA	Stability
Remit	0Ω	402	KOA	Stability
Q1	MC13853	QFN-16	Freescale	
1800 MHz				
C2	10 pF	402	Murata	Input match
C5	33 pF	402	Murata	RF bypass
C6	.01 µF	402	Murata	Low freq bypass
C8	10 pF	402	Murata	Output match
L2	3.9 nH	402	TOKO	Input match
L6	4.7 nH	402	TOKO	Output match/DC feed
R2	75 Ω	402	KOA	Stability
R5	30 Ω	402	KOA	Stability
Q1	MC13853	QFN-16	Freescale	

Table 14. Bill of Materials (continued)

Component	Value	Case	Manufacturer	Comments
1960 MHz				
C2	10 pF	402	Murata	Input match
C5	33 pF	402	Murata	RF bypass
C6	.01 µF	402	Murata	Low freq bypass
C8	10 pF	402	Murata	Output match
L2	3.9 nH	402	TOKO	Input match
L6	4.7 nH	402	TOKO	Output match/DC feed
R2	75 Ω	402	KOA	Stability
R5	30 Ω	402	KOA	Stability
Q1	MC13853	QFN-16	Freescale	
2140 MHz				
C3	10 pF	402	Murata	Input match
C15	33 pF	402	Murata	RF bypass
C16	.01 µF	402	Murata	Low freq bypass
C7	5 pF	402	Murata	Output match
L3	3.0 nH	402	TOKO	Input match
L7	2.4 nH	402	TOKO	Output match/DC feed
R3	150 Ω	402	KOA	Stability
R6	10 Ω	402	KOA	Stability
Q1	MC13853	QFN-16	Freescale	

4 Packaging

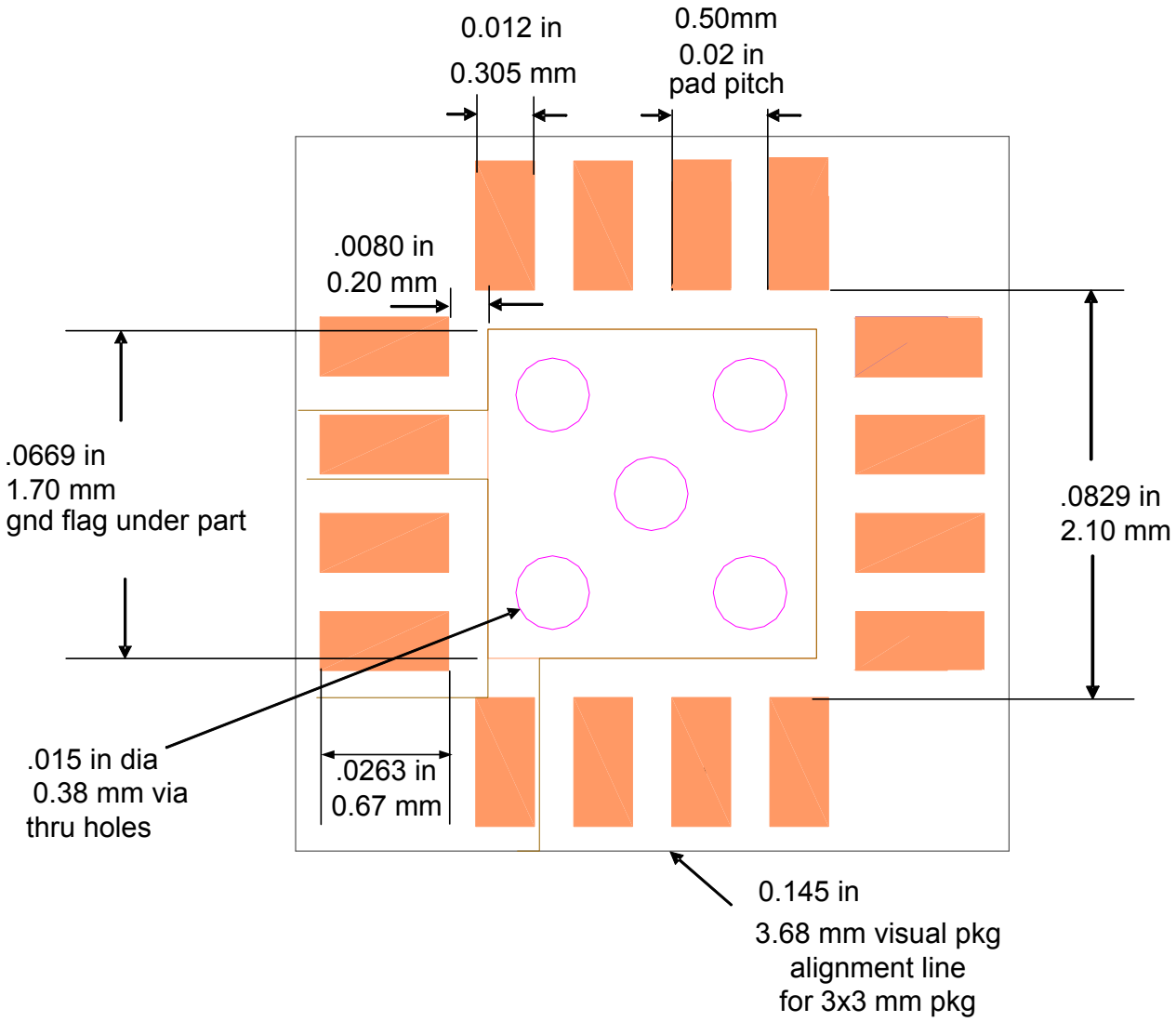
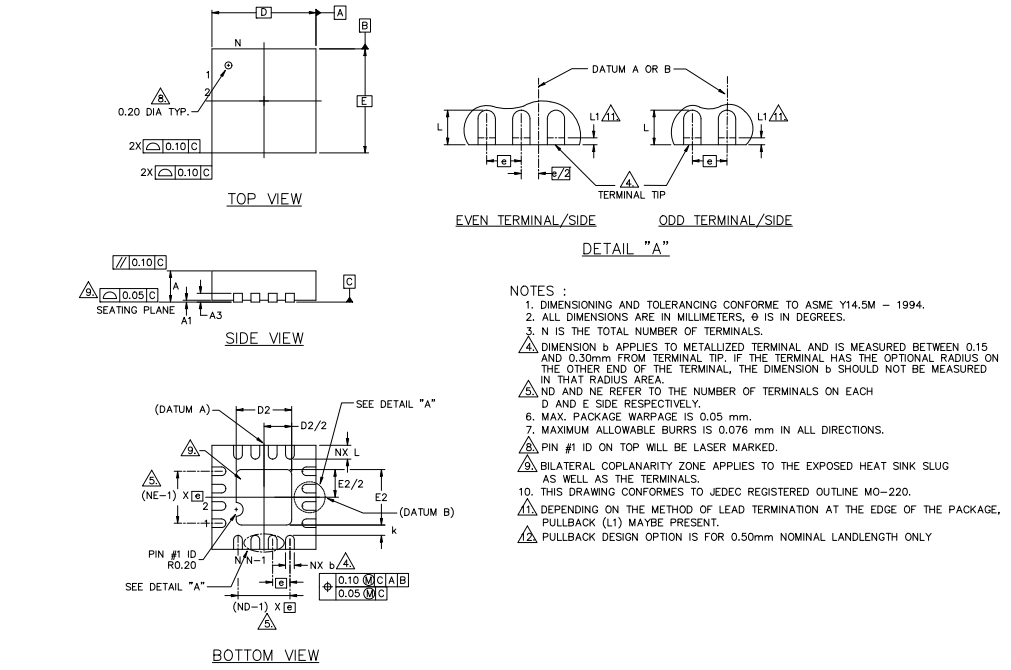


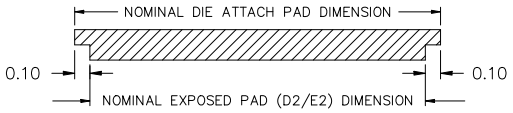
Figure 9. Board Layout Dimensions



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
θ	0	——	12	2
K		0.20 MIN.		
D		3.0 BSC		
E		3.0 BSC		
L1		0.15 mm MAX		11

SYMBOL	0.50 mm LEAD PITCH VARIATION E			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC.		
N		16		3
ND		4		5
NE		4		5
L	0.35	0.40	0.45	12
b	0.18	0.25	0.30	4
D2	1.50	1.60	1.70	
E2	1.50	1.60	1.70	

GENERAL ; NOMINAL EXPOSED PAD DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION–0.20



<DIE ATTACH PAD X–SECTION VIEW>

Unless otherwise specified
Dimensions are in millimeters
Decimal Angular
X.X +/– 0.1 +/– 1deg
X.XX +/– .05
X.XXX +/– .025
Interpret dim and tol per
ASME Y14.5M – 1994

Title:
Package Outline, MLF 3.0 x 3.0 mm Body
Saw Singulate Design

Figure 10. Outline Dimensions for QFN-16

5 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

Table 15 summarizes revisions to this document since the previous release (Rev. 1.7).

Table 15. Revision History

Location	Revision
Figure 2 - SPI Bit Word	Revised diagram to remove penta-band info.
Table 8 - SPI Used for Dual-, Tri-, and Quad-Band Configurations	Removed penta-band data, other revisions to table data.
Section 3, “Application Information”	Added new paragraph 4, revised paragraph 3.
Figure 3 - Application Circuit with Two MC13853s Controlled by Common SPI Lines	New figure.
Figure 5 950 MHz LNA Application Schematic	Replaced drawing.
Figure 6 1850 MHz LNA Application Schematic	Replaced drawing.
Table 14 Bill of Materials	Revised entries for the 950 MHz and 1800 MHz sections.